PLL Instability of Wind Turbines During Severe Faults

AMIR ARASTEH AND **NICOLAOS A. CUTULULIS**, (Senior Member, IEEE)
Department of Wind Energy, Technical University of Denmark, 4000 Roskilde, Denmark

Corresponding author: Amir Arasteh (amia@dtu.dk)

ABSTRACT Stringent grid codes require wind turbines (WTs) to remain connected even during severe faults. This can result in PLL instability and Loss of Synchronisation (LoS), which is the main subject of this paper. For a better understanding, the phenomenon is analysed in the dq equivalence. The presented analysis enlightens the root cause of the associated instability and clarifies the key role of PLL in that. Based on this analysis, a hybrid solution combining an Adaptive-PLL with impedance estimation is proposed. In this regard, the PLL-gains during the fault are selected in accordance with accuracy of the impedance estimation: the higher the accuracy of the estimation, the lesser the required changes in the gains of PLL. The work also proposes a logical circuit for a more reliable detection of LoS, allowing the controller to only act when necessary. Simulation results and discussions support the proposals.

INDEX TERMS Adaptive-PLL, estimated impedance value, grid following wind turbines, loss of synchronisation, PLL instability, severe faults.

I. INTRODUCTION

Grid codes today require generators, including Wind Power Plants (WPPs), to remain connected and inject (usually reactive) fault currents during grid short-circuit faults. This requirement is commonly known as Fault Ride-Through (FRT) or Low Voltage Ride-Through requirement (LVRT). In most of the grid codes, the voltage profile at the Point of Connection (PoC) is defined for grid voltage of down to 0%, i.e. Zero Voltage Ride-Through (ZVRT) [1].

As a result of advancements in WT technology over the last decade, WTs have proven to be mature and capable of meeting the FRT requirements for moderate voltage drops, e.g. below 50% of the rated voltage [2]. However, short-circuit faults occurring nearby the PoC of a WPP, which would cause the voltage drop down to 0% at the PoC are shown to cause instability of WTs, namely an inability of maintaining synchronisation with the main grid, known as Loss of Synchronisation (LoS) [3]–[5]. Accordingly, if the WTs are required to remain connected during voltage drops down to 0%, implementing an appropriate control solution for the aforementioned instability becomes a necessity.

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Fault response of the grid-connected converters is well studied in the literature. Despite this, few publications have discussed severe symmetrical faults where voltage drops to zero. Through these works, various methods for assessing the phenomenon are presented followed with different control solutions to deal with the associated PLL instability.

In [3] and [5], LoS is explained by steady state equations and the current injection limits resulting in LOS are derived. However, the key role of PLL is not illuminated because the analysis is performed in phasor domain and do not include PLL parameters. The proposed assessment method in [6] does include the effect that the PLL has on the injected current by describing the mechanism of grid-synchronisation through nonlinear differential equations. It does not give, however, an intuitive insight about the phenomenon for requiring the numerical methods. An alternative assessment tool is investigated in [7] using the Equal Area Criterion and based on the presented results in [8], [9]. The PLL synchronisation mechanism is described as analogous to that of a synchronous machine which enables a definition of PLL damping. However, for a line impedance consisting of both a resistive and an inductive part, the mathematical derivation becomes extremely complicated, hindering any applicable insight. A comprehensive review and

comparison of the proposed methods for assessing the stability of WTs during severe faults is also presented in [7]. Overall, the assessment methods in the literature do not provide an intuitive insight on the key role of PLL in LoS. In this work the LoS is assessed by considering the equivalence dq-model of the system. The presented analysis has the advantage of providing an easy to understand and intuitive insight about LoS.

In addition to the aforementioned methods for predicting LoS, there are several solutions for counteracting LoS. These solutions include modifying the active current reference according to frequency deviation [3]–[5], adapting the current references based on the estimation of the impedance [6], [10], freezing the PLL [11], coordinating controller of WTs with STATCOM [12], or modifying the control of the WTs from grid following to grid forming [7].

Modifying the current references according to the frequency deviation is an effective way to prevent the frequency drift and keep the frequency in the allowed range. It does, however, introduce new blocks in the wind turbine's control loop (current limiter, PI controller, etc), adding to its complexity. In addition, this approach relies on detecting frequency changes that the current controller responds to, resulting in additional delays. Alternately, adjusting the reference values according to the estimated impedance reduces some of the complexity and delays of the previous solution. Despite this, precise measurement of the impedance has practical challenges owing to the unknown location of the fault and the uncertainties associated with real-time measurement methods. Another solution is freezing the PLL that acts immediately after detection of LoS without any delay in between. Freezing a controller, however, is not a desirable approach in a highly dynamic system such as power systems. Although very good at maintaining the frozen variable to a desired value (the nominal frequency of the system), the de-freezing of the PLL may alter the recovery after a fault and introduce additional transients, especially if the system's frequency has not yet stabilised. It is therefore recommended to avoid freezing the PLL as possible. The other solution which contains coordinating control of WTs and STAT-COM for avoiding LoS is a potentially good approach, but it implies the existence of an expensive component such as STAT-COMs. Finally, grid forming schemes are not yet mature enough to be considered as a reliable solution for counteracting LoS. As discussed in [13], some of the grid forming control schemes still need to switch to conventional PLL to maintain the synchronisation during faults.

In this paper, LoS of WTs is analysed in *dq* domain, which corresponds to the domain where the WT is controlled. This new perspective, based on the system's *dq* equivalence, provides deeper insight into the phenomenon. On the basis of the insight acquired, a hybrid solution is proposed which combines the flexibility of Adaptive-PLLs with the estimated angle of the equivalent impedance between WT and the fault location. In the rest of the paper, the estimated angle of the equivalent impedance is referred to by $\hat{X}/\hat{R}$-ratio as it is equal

to tangent of the impedance angle. The "^" sign in $\hat{X}/\hat{R}$ indicates it is an estimation.

In the proposed solution, the current references are adjusted based on the $\hat{X}/\hat{R}$-ratio, and the PLL gains are adapted according to the accuracy of $\hat{X}/\hat{R}$-ratio. As mentioned before, relying solely on the estimated impedance values has practical challenges. The hybrid solution which uses both Adaptive-PLL and $\hat{X}/\hat{R}$-ratio, removes the necessity of having a precise value of the impedance. By doing so, it is possible to avoid freezing the PLL (or introducing smaller changes in the PLL gains) when the margin of error in $\hat{X}/\hat{R}$-ratio is small.

The concept of Adaptive-PLL is known and [14] examines the performance of the grid when PLL gains are varied. PLL freezing which is proposed in [11] for severe faults can be considered as a specific case of Adaptive-PLL. Evidently, setting gains of an adaptive-PLL to zero, when a severe fault is detected, emulates PLL freezing. As stated before, freezing the PLL with the large changes that it introduces is not desirable in a highly dynamic system. In this context, an Adaptive-PLL that minimises changes in the gains is beneficial.

In a recent work, an Adaptive-PLL is proposed to maintain transient stability at the instant of fault occurrence/clearance [15]. The integrator gain of the PLL is set to zero when a rapid change in the frequency is detected, resulting in a first-order PLL at the instant of the fault. During the fault, though, the PLL returns to its default gains and works as a second order PLL. It is an effective way to avoid instabilities caused by transients that occur during large disturbances. Nevertheless, it requires an equilibrium point after the transient [15]. If there is no equilibrium point after the transient, the solution proposed in [15] is not effective. During the fault with very small impedance, the frequency deviates and does not reach to any equilibrium point [7]. As a result, a non-zero integrator gain can still cause LoS even with guaranteed stability at the fault instance. Unlike [15], the proposed solution in this work which combines Adaptive-PLL with $\hat{X}/\hat{R}$-ratio, is applicable to faults without any equilibrium point.

In addition to the illustration of LoS in dq domain and the presented hybrid solution for counteracting LoS, the paper proposes a logical circuit for a more reliable detection of LoS. For this purpose, the circuit observes both frequency and voltage of the system. As a result, the detection circuit is able to discern and respond only when a risk of LoS is anticipated, preventing unnecessary reaction of the controls. In summary, the main contributions of this work are:

- analysing LoS phenomenon during severe faults in *dq* domain
- proposing a hybrid solution which combines flexibility of Adaptive-PLL with $\hat{X}/\hat{R}$-ratio
- proposing a logical circuit for a more reliable detection of LoS

The rest of the paper is structured as follows. Section II presents the LVRT requirements for generators, specifically for WT/WPPs. Then, instability of PLL during severe fault is
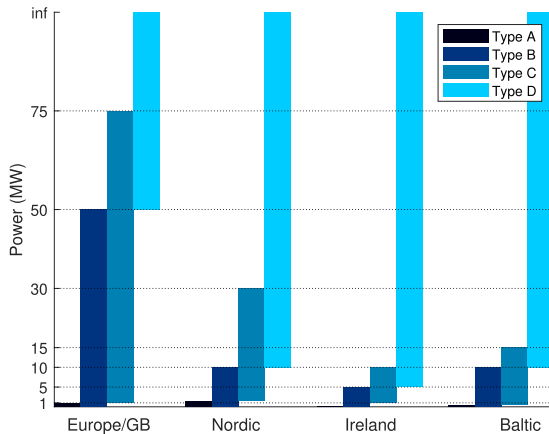
FIGURE 1. Power range of different types of PPMs (A, B, C, and D) with a connection point below 110*kV* and based on their definition in [1].

FIGURE 2. The envelope of LVRT requirement for all types of PPMs together [1].

analysed and explained from a *dq* perspective in Section III. Section IV introduces the proposed solution to the problem. The simulation results along with the discussion on the result can be found in Section V. Lastly, in Section VI, the conclusions are listed.

II. LVRT REQUIREMENTS FOR GENERATORS

The required dynamic performance of any generation unit connected to a specific power system will depend on the characteristics of that system and the generating unit's classification. Typically, those requirements are defined in so called grid codes. In Europe, each transmission system operator (TSO) issues its own grid code. This has led to significantly different requirements across Europe, which in turn involves large efforts from the manufacturers to certify their generators against all grid codes. In this direction, at the request of the European Commission, the European Network of Transmission System Operators for Electricity (ENTSO-E) has developed an European code with requirements for generators (RfG), aiming at harmonising the requirements across Europe [1].

In the RfG report of ENTSO-E published in 2016, generation units ('power park modules' or 'PPMs') are divided into four types called A, B, C, D [1]. Every PPM with a connection point at 110*kV* or above is categorised as type D. PPMs with connection points below 110*kV* are categorised in different types based on their rated power, as is illustrated in Fig. 1.

Figure 2, depicts the envelop of LVRT requirements of PPMs which is derived based on the associated requirements defined in [1]. As can be seen, even for very severe faults, the system operators have the right of requiring the WTs to remain connected for a short period of time. Consequently, investigating ZVRT of WTs is necessary to make sure that WTs are capable of maintaining their stability during severe faults and regain their synchronisation with the grid after fault clearance.
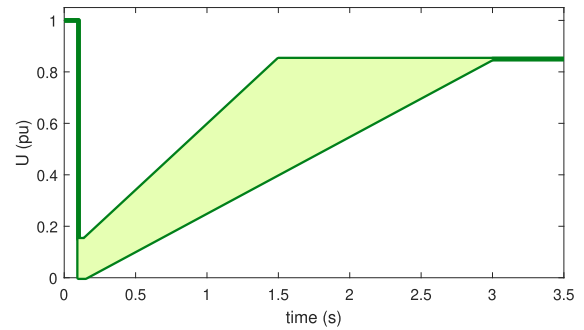
III. PLL INSTABILITY DURING SEVERE FAULTS

In the literature, the PLL instability of WTs during severe faults is analysed in phasor domain through linear equations [3], [4], nonlinear differential equations [6], and Equal Area Criterion [7].

In this work, a similar analysis is done by considering the equivalent *dq* circuit diagram of the system. In contrast to phasor domain which is compatible with the physical system, *dq* domain cannot be directly mapped on the system (it gives a virtual representation of the system). However, since most of WTs controllers are synthesised in *dq* domain, this new perspective has the advantage of enlightening the root cause of the problem and clarifies the key role of PLL in LoS. To date, there is not any non-linear stability analysis method for predicting the LoS. The available methods in the literature are either steady-state or quasi-static methods [3]–[7]. Some research works have shown that a large transient can cause LoS even if there is a stable point during the fault [15]. However, a system that does not have a steady state operating point, cannot return to a stable state after an initial transient. During a severe fault, LoS will occur regardless of the initial transient. Accordingly, for analysing LoS, the initial dynamic and transient response of the system (when the fault occurs) is not considered. Yet, the full dynamic performance of the system can be observed in the presented results in Section V.

A simple system consisting of a converter connected to an AC-grid which is used for illustration of the problem is shown in Fig. 3. In the event of a symmetrical three phase fault with negligible impedance between the converter and the ac source, the system is divided into two decoupled sections.
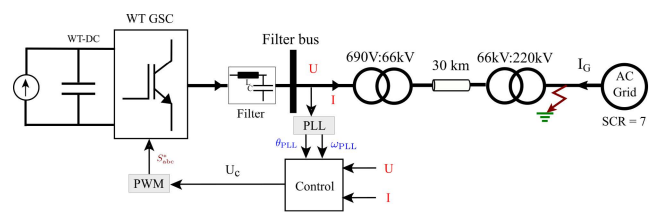

FIGURE 3. A simple system consisting of a WT connected to an AC grid.
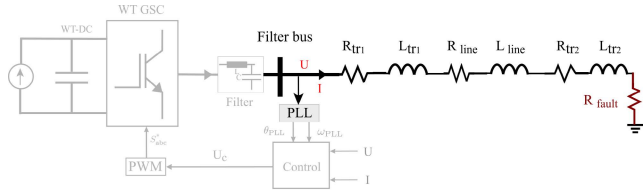
FIGURE 4. The converter side section of the system during a severe fault.
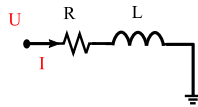

FIGURE 5. Equivalence of the converter side section of the system during a severe fault.

Note that only symmetrical faults are considered in this work since they are the only fault type that could result in LoS [7].

The converter side section of the system during severe faults is depicted in Fig. 4. For the analysis introduced in this work, the equivalent model behind the filter bus of WTs (shown in Fig.4) is not important (reasoning introduced further down). Consequently, the equivalent model of the converter-side section can be simplified as Fig. 5, where R and L represent the equivalent resistance and inductance between the filter bus and the fault location. With this, voltage at the filter bus of WT as a function of the current flowing at this point would be:

$$U = R \cdot I + L\frac{dI}{dt} \qquad (1)$$

assuming that the angular frequency is equal to ωt, the equivalence of Eq. (1) in the associated dq frame would be:

$$U_d = R \cdot I_d - L\omega I_q$$
$$U_q = R \cdot I_q + L\omega I_d \qquad (2)$$

The interested readers can find the full derivation of Eq. (2) in Appendix A. For simplicity, X is used instead of $L\omega$ which gives:

$$U_d = R \cdot I_d - X \cdot I_q$$
$$U_q = R \cdot I_q + X \cdot I_d \qquad (3)$$

Graphical representation of Eq. (3) is given in Fig. 6 which is also equivalence of Fig. 5 in dq domain. The equation and the figure clarify contribution of dq currents on dq voltages. The dq currents induce voltage on the same axis through resistive part of the equivalent impedance, while a voltage is induced on the perpendicular axis through the inductive part of the equivalent impedance.

Earlier, it was mentioned that anything behind the filter bus is not important for the presented analysis. The reason is that the voltage measured at the filter bus is used as the input to the PLL. The PLL is trying to lock to the angle of the measured voltage by setting the U_q measured at this point to zero. Therefore, U_q would be zero during steady
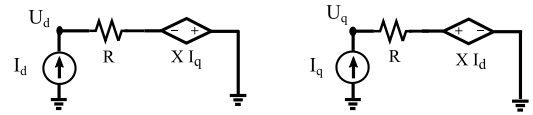

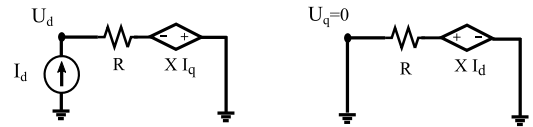**FIGURE 6.** Graphical representation of Eq. (3).

FIGURE 7. Graphical representation of Eq. (4).

state ($U_q = 0$). Rewriting Eq. (3) with $U_q = 0$ gives:

$$U_d = R \cdot I_d - X \cdot I_q$$
$$0 = R \cdot I_q + X \cdot I_d \qquad (4)$$

Solving the lower equation in Eq. (4) for I_q gives:

$$I_q = -\frac{X}{R} \cdot I_d \qquad (5)$$

which means during severe faults (with negligible impedance), I_q and I_d are proportionally coupled. The result derived based on dq equivalent circuit is compatible with the one derived by other assessment methods [7]. Fig. 7 shows the graphical representation of Eq. (4) in which both sides of q-axis equivalent circuit are grounded.

Based on the above, the root-cause behind the associated instability problem can be explained: at one end of the circuit, the PLL is trying to set U_q of the filter bus to zero in its own frame and, at the other end, the circuit is grounded with a zero voltage (which will have $U_q = 0$ in all rotating frames). In other words, the filter bus of the WT should have a q-axis voltage potential equal to that of the fault location.

It is evident that the aforementioned requirement for equal voltage potential on q-axis is merely challenged when there is a flow of current. A nonzero I_d induces a voltage on q-axis (which based on Eq. (3) is equal to $X \cdot I_d$). To compensate this induced voltage, a specific amount of I_q needs to be injected. Similarly, when I_q is injected, a voltage drop across the resistor appears. To compensate for this voltage drop, a specific amount of I_d should be injected to have a zero equivalent voltage on q axis. In case either I_d or I_q, required for this compensation, can not be injected, U_q at the filter bus would have a non-zero value, as formulated below:

if I_d reaches the limit: $U_q = R \cdot I_q + X \cdot I_{d_{max}}$
if I_q reaches the limit: $U_q = R \cdot I_{q_{max}} + X \cdot I_d \qquad (6)$

The integrator of the PLL will accumulate this non-zero value and will cause LoS. The structure of PLL is depicted in Fig. 8. As can be seen, U_q is the input to the PI controller, with the frequency deviation as an output. Equivalently, the formula for frequency deviation is:

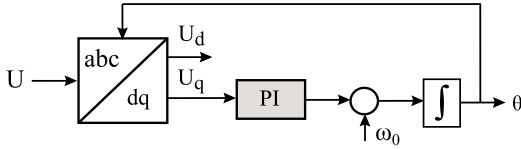$$\Delta\omega = k_p \cdot U_q + \int k_i \cdot U_q \cdot dt \qquad (7)$$
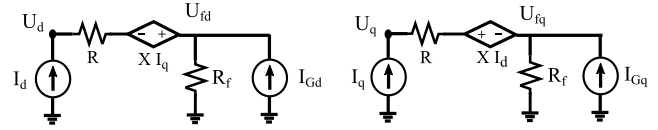
FIGURE 8. Overview of PLL structure.

FIGURE 9. dq equivalent model of the network during severe fault including fault impedance.
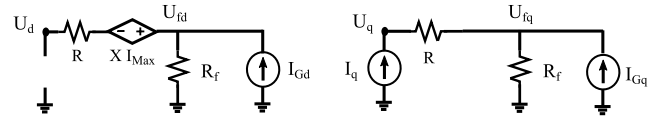

FIGURE 10. dq equivalent model of the network during severe fault including fault impedance and taking into account the grid code requirements.

which shows how a non-zero U_q makes $\Delta\omega$ non-zero and will increase/decrease it (depending on the U_q sign), leading to frequency drift and LoS. Additionally, it indicates that, with a non-zero U_q, the frequency deviation does not reach an equilibrium point as it increases over time, which means the proposed solution in [15] is not applicable in this condition.

Based on this observation, the potential solutions to the problem would be either based on reducing the value of U_q or reducing the impact of a non-zero U_q on frequency drift. The proposed solution in this work combines both of the possibilities. In that sense, the value of U_q is minimised by adjusting the current references according to $\hat{X}/\hat{R}$-ratio, and the impact of a non-zero U_q on the frequency is reduces by scaling down the PLL gains. The proposed solution is further clarified in Section IV.

In addition to illustrating the root cause of LoS, the presented method in this work is helpful for investigating the impact of grid-SCR (strength/weakness of the grid) on LoS during severe faults. In the case that the fault impedance is not negligible, the network cannot be considered as two independent sections. The fault impedance is normally resistive, so the *dq* equivalent model of the network during severe fault can be approximated as Fig. 9 depicts. Most of the grid codes prioritise reactive current during severe faults. Accordingly:

$$I_d^* = 0$$
$$I_q^* = I_{MaxWT} \tag{8}$$

Hence, taking into account the grid code requirements for reactive current injection, the *dq* equivalent model of the network during severe fault can be drawn as Fig. 10. Based on KVL-KCL and superposition principles, the following equations can be derived for the q-axis equivalent model depicted in Fig. 10.

$$U_q = U_{fq} + R \cdot I_{MaxWT}$$
$$U_{fq} = R_f \cdot I_{MaxWT} + R_f \cdot I_{Gq} \tag{9}$$

combining the terms in Eq. (9) gives:

$$U_q - R \cdot I_{MaxWT} = R_f \cdot I_{MaxWT} + R_f \cdot I_{Gq} \tag{10}$$

as mentioned before, $U_q = 0$ due to PLL settings, hence:

$$(R + R_f) \cdot I_{MaxWT} = -R_f \cdot I_{Gq} \tag{11}$$

or:

$$I_{Gq} = \frac{-(R + R_f)}{R_f} \cdot I_{MaxWT} \tag{12}$$

which means, to be able to maintain the synchronisation, the lower the fault impedance, the higher the required reactive-current injection from the grid (higher SCR or stronger grid). Specifically, when $R_f = 0$:

$$I_{Gq} = \frac{-(R + 0)}{0} \cdot I_{MaxWT} \to \infty \tag{13}$$

in the other words, for a negligible fault impedance, an infinite bus is needed for avoiding LoS (without any countermeasure and relying merely on the conventional PLL).

On the other side, when $R_f = \infty$ (no fault), R is negligible respect to R_f. Hence:

$$I_{Gq} = \frac{-R_f}{R_f} \cdot I_{MaxWT} = -I_{MaxWT} \tag{14}$$

which means for keeping the synchronisation during normal operation, the grid should be capable of absorbing the reactive-current injected by WTs. A point which is trivial but verifies the performed analysis.

IV. THE HYBRID ADAPTIVE-PLL
Based on the observation in Section III, the LoS occurs when it is physically not possible to reach $U_q = 0$ at the PLL measurement point. This work proposes a hybrid solution for counteracting LoS by combining both possibilities for counteracting LoS. The proposed solution adjusts the current references in accordance with $\hat{X}/\hat{R}$-ratio (to reduce U_q); and, assigns appropriate gains for PLL depending on the expected estimation error (to minimise the effect of a non-zero U_q on the frequency).

For the ease of illustration, this section is divided into four subsections. First, the reduction in U_q by current adjustment is analysed. Then, the effect of PLL gains on the frequency deviation is discussed. Afterwards, the proposed logical circuit for detecting LoS is explained. Lastly, the operation principle of the proposed solution is compared with that of the solution based on frequency dependant active current injection (FDACI).

A. ADJUSTING THE CURRENT REFERENCES

According to Eq. (7), reducing U_q helps to ameliorate the problem. U_q, itself, can be minimised by appropriate selection of current references as indicated in Eq. (3). In this context, one option is the dynamic change of current-references based on the measured frequency as is proposed in [3]. It does, however, require an additional PI controller which increases complexity of the system. Alternatively, the X/R ratio of the system can be used to determine the current references and make $U_q = 0$ [6], [10]. Nonetheless, it requires the precise value of X/R ratio which faces practical challenges. If the WT is capable of remaining stable with a non-zero U_q, an error in the estimation of X/R ratio would be acceptable. In this case, instead of the precise values, the estimated value of the impedance can be used for reducing U_q and improving the performance of WT during severe faults. Adaptive-PLL realises it and could prevent the instability even with a non zero U_q. Thus, combining Adaptive-PLL with $\hat{X}/\hat{R}$-ratio is promising for minimising the frequency deviation as well as keeping the WT stable.

In order to inject a maximum amount of current during a fault while still meeting the X/R ratio requirement, the references should be chosen as follows.

$$I_d^* = \frac{-1}{\sqrt{\frac{\hat{X}}{\hat{R}}^2 + 1}} \cdot I_{max}$$

$$I_q^* = \frac{1}{\sqrt{1 + \frac{\hat{R}}{\hat{X}}^2}} \cdot I_{max} \qquad (15)$$

Eq. (15) indicates that only $\hat{X}/\hat{R}$-ratio is required for defining the current references and the estimated value of X and R are not needed. Taking into account the situation in which LoS occurs eases the estimation of $\hat{X}/\hat{R}$-ratio.

Normally, the WTs are interconnected by array cables, then connected to the grid via the export cable. Additionally, as stated in Section I, the faults with a risk of LoS are the ones occurring near PoC of the WPPs. That means the considered faults in this study would be the one occurring between the WTs and PoC of the WPPs. Therefore, the impedance between WTs and the fault can be estimated as the equivalent impedance of the cables and transformers. By using only the $\hat{X}/\hat{R}$-ratio without considering X or R values, one can estimate the ratio using cable and transformer characteristics, and hence avoid the need for real-time estimation of the impedance. Real-time estimation of the impedance is very challenging in the considered condition, due to the fast dynamics of the fault and the noticeable difference between the equivalent impedance before and during the fault.

B. SELECTING GAINS OF THE PLL DURING FAULT

With the defined current-references in the previous subsection, the expected value of U_q can be estimated. Rewriting Eq. (3) with the current-references gives:

$$U_q = R \cdot I_q^* + X \cdot I_d^* \qquad (16)$$

combining Eq. (15) and (16), and after some maths:

$$U_q = \frac{R \cdot \hat{X} - X \cdot \hat{R}}{\sqrt{\hat{X}^2 + \hat{R}^2}} \cdot I_{max} \qquad (17)$$

In which $\hat{R}$ and $\hat{X}$ stand for the estimated value of the equivalent impedance, while R and X are the real values of this impedance. Normally, the precise value of the estimation error is not known. Instead, an expected error range is available. Due to this uncertainty, the worst case must be taken into account, which is the maximum U_q. In the following, an intuitive approach is provided to determine the maximum U_q for various estimation error.

A fraction is maximal when the nominator is at maximum and the denominator is at minimum. In the derived equation for U_q, the nominator is at max when the difference between two expressions ($R \cdot \hat{X}$ and $X \cdot \hat{R}$) is highest, while the denominator is minimum when both $\hat{R}$ and $\hat{X}$ have their minimum values. Since during the considered faults $R \ll X$, the denominator is dominated by $\hat{X}$, and the minimum value of $\hat{X}$ becomes very close to the minimum of the denominator. On the other side, for the minimum value of $\hat{X}$, the nominator of U_q becomes maximum when $\hat{R}$ has it's maximum value. Hence, U_q reaches it's maximum value when $\hat{R}$ is maximum and $\hat{X}$ has it's minimum value as is indicated in the following equation.

$$|U_q|_{max} = |\frac{R \cdot \hat{X}_{min} - X \cdot \hat{R}_{max}}{\sqrt{\hat{X}_{min}^2 + \hat{R}_{max}^2}}| \cdot I_{max} \qquad (18)$$

Note that the sign of U_q is not important as, in LoS, only the slope of frequency deviation is of interest. The presented reasoning for finding $|U_q|_{max}$ is further demonstrated in the simulation results graphically and with numerical examples.

Knowing $|U_q|_{max}$ for an expected estimation error of $\hat{X}/\hat{R}$-ratio, appropriate gains can be chosen for the PLL during severe faults. Rewriting Eq. (7) for $|U_q|_{max}$ gives:

$$|\Delta\omega| = k_p \cdot |U_q|_{max} + \int k_i \cdot |U_q|_{max} \cdot dt \qquad (19)$$

In this context, if $|U_q|_{max}$ is negligible, changing the PLL gains will not have a noticeable impact on the WT's performance. While, if $|U_q|_{max}$ is large, slowing down the PLL will reduce the frequency deviation significantly. The value of $|U_q|_{max}$ is defined by the accuracy of $\hat{X}/\hat{R}$-ratio. If the estimation is precise, $|U_q|_{max}$ is small, and, consequently, smaller variations in PLL gains are required. On the other side, if the estimation of $\hat{X}/\hat{R}$-ratio is not accurate, $|U_q|_{max}$ is not negligible, and, consequently, higher variations in the PLL-gains are required for preventing LoS. For instance, with a relatively large $|U_q|_{max}$, setting the integrator gain to zero gives:

$$|\Delta\omega| = k_p \cdot |U_q|_{max} \qquad (20)$$

which means, even with a none-zero U_q, the frequency will not reduce/increase through time but will stabilise to a steady state frequency determined by the value of k_p and $|U_q|_{max}$.
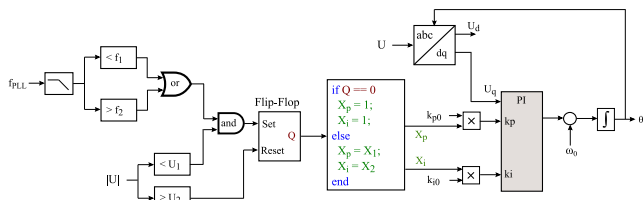
FIGURE 11. PLL with Adaptive-gains and including an embedded logical circuit for detection of severe faults.

FIGURE 12. *dq* vector diagram of voltages and currents during severe fault with different PLL implementation.
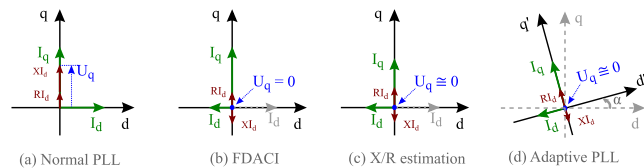
The steady state frequency deviation can be further reduced through decreasing the value of k_p. The presented results in Section V demonstrates the effect of PLL-gains on LoS with different values of $|U_q|_{max}$.

C. LOGICAL CIRCUIT FOR DETECTING LoS

To avoid unnecessary reaction of the controller, a method for a more reliable detection of LoS is required. In general, there are two indicators that can foresee LoS: voltage and frequency. During severe faults, voltage drops to small values, hence observing the voltage amplitude and checking if it goes below a threshold value can be a good indicator of severe faults. However, there is a challenge: knowing the voltage value below which PLL causes LoS is not straight forward and may vary case to case [7]. On the other hand, merely observing frequency has some drawbacks. For example, frequency may change due to other events in the system rather than the severe fault. Accordingly, a logical circuit which takes into account both voltage and frequency is implemented in this work.

The logical circuit proposed for detection of LoS is shown in Fig. 11 which contains a flip-flop. When the output of the flip-flop is zero (reset), predefined values of the PLL gains are given to the PI controller. In case the output of the flip-flop is one (set), the gains of the PLL are multiplied by X_p and X_i which are selected based on the expected error in $\hat{X}/\hat{R}$-ratio as discussed before.

By designing a logical circuit for setting and resetting the flip-flop, the circuit is completed. As previously discussed, using a combination of frequency and voltage for detection of severe faults is more reliable. Hence, the flip-flop is set when frequency goes beyond the specified limits and, at the same time, voltage drops below a threshold value. This is realised by comparing the measured frequency with the selected limits (f_1 and f_2 in which $f_1 < f_n < f_2$ and f_n is the nominal frequency of the system). If the frequency is below f_1 or above f_2, and voltage is below U_1, the flip-flop receives the set signal and, subsequently, the PLL gains are updated. For resetting the flip-flop and re-updating the PLL gains, only voltage magnitude is taken into account, since it is enough for detection of fault clearance. Besides preventing the unnecessary reaction of the control block when there is no risk of LoS, the threshold values of voltage and frequency filter out small oscillations that may occur due to measurement noise or other reasons during normal operation.

To date, there is not any analytical way for calculating threshold voltage below which LoS occurs [7]. However, considering that the faults leading to LoS are the ones occurring between the WT and PoC, a proper choice for the voltage threshold could be taking into account the maximum impedance between the WT and PoC that covers all the faults in the range. Then, the threshold voltage can be defined by the product of the rated current of the WT and the equivalent impedance between WT and the fault location as Eq. (21) indicates.

$$U_{WTT} = Z_{eq} \cdot I_{MaxWT} \tag{21}$$

Since, the frequency is also taken into account for detection of LoS, the considered margin in voltage level is acceptable. In the other words, a non-severe fault close to WT which may drop the voltage abruptly does not activate the logical circuit as long as the frequency is in the range. As for the frequency thresholds, the limits should be chosen depending on the grid code requirements not to violate the connectivity of the WTs [16].

Overall, the proposed logical circuit adds up an additional advantage to the proposed solution by avoiding unnecessary reactions of the controller.

D. OPERATION PRINCIPLE OF THE SOLUTIONS

The working principle of the proposed solution along with that of FDACI are illustrated in this part, with the aim of clarifying how each method is ameliorating the problem.

Basically, the LoS happens because, with the current-references defined in the grid codes, it is not physically possible to have $U_q = 0$, at the PLL measurement point. The FDACI solution changes I_d^* to make $U_q = 0$ in the PLL *dq* frame. On the other hand, the solution proposed in this work, adjusts the reference values of I_d and I_q based on the estimated $\hat{X}/\hat{R}$-ratio (to reduce U_q) and, at the same time, adapts the PLL's gains to minimise the frequency drift even with a non-zero U_q.

An illustrative diagram of *dq* currents and voltages during severe faults for (a) normal PLL, (b) FDACI, (c) *X/R* estimation and (d) Adaptive-PLL is shown in Fig. 12. In the case of normal PLL (no countermeasures), the voltages on *q*-axis caused by the injected I_d and I_q add up and lead to a none-zero U_q. FDACI modifies the *dq* currents, such that the induced voltage from I_d on *q* axis compensates for $R \cdot I_q$ leading to a zero U_q. Defining the current references based on the $\hat{X}/\hat{R}$-ratio does the same, except that it may lead to a non-zero U_q due to the expected estimation errors.

The Adaptive-PLL reduces the impact of U_q on frequency and allows for a non-zero U_q. A non-zero value of U_q can be interpreted as rotation of the dq axis (depicted in Fig. 12.d). The proposed solution in this work, combines Fig.12.c and Fig.12 d, as the current references are set based on $\hat{X}/\hat{R}$-ratio (reducing U_q), and the PLL gains are adapted to minimise frequency deviation even with a non-zero U_q.

One can derive that projection of the dq currents and voltage in the dq frame of Adaptive-PLL on the dq frame of normal PLL (drawn in dashed gray in Fig. 12.d) results in similar voltages and currents to those of X/R estimation (Fig. 12.c).

V. SIMULATION RESULTS

In this section, the performance of the proposed solution is verified via simulations with a WT connected to the AC grid, as shown in Fig. 3. The additional values used in the simulation are provided in Table 2 of the appendix. It is worth re-emphasising that only three phase symmetrical faults are considered in this study, since LoS and frequency drift is a stability problem which occurs merely during symmetrical faults [7]. Asymmetrical faults with very small impedance have their own challenges, but two side of the faults will not be fully decoupled since at least one phase of the system does not loose the connection with the main ac grid.

To ease the presentation and discussions, the results are presented in three subsections. First, U_q for various estimation errors is plotted to visualise $|U_q|_{max}$. Afterwards, different solutions for LoS are compared. Finally, in subsection C, response of the WT with the hybrid Adaptive-PLL solution for various estimation errors is investigated.

### A. $|U_q|$ FOR VARIOUS ESTIMATION ERRORS

U_q for various errors in the estimation of X and R are demonstrated in Fig. 13. As can be seen in this figure, $|U_q|$ is maximal when X reaches it's minimum value in each range and, at the same time, R has it's maximum value in that range. Graphically, U_q reaches it's maximum, magnitude-wise, at the right-bottom corner of the top-figure and left-bottom corner of the second-figure. For example, for an estimation error of 50%, the aforementioned points on the sub-figures are associated to -50% error in X and 50% error in R. This conclusion is valid for other values of the estimation errors, as can be deducted by looking at the intermediate plots between the plots for -50% and 50% (with a step of 10% between the plots).

B. COMPARISON OF THE SOLUTIONS

Fig. 14 depicts fault response of the WT with 25% impedance-estimation-error for different solutions; namely: FDACI, PLL Freezing, X/R-estimation and the hybrid Adaptive-PLL. For a better visualisation, a frequency deviation of 1 Hz is considered for activation of all solutions. However, as mentioned before, it needs to be chosen such that it does not violate the grid code requirements.
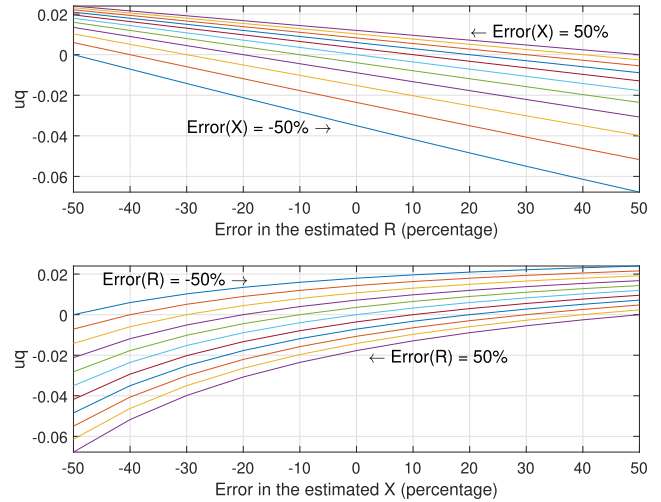
FIGURE 13. U_q value for different estimation errors in X and R ($\pm 50\%$, $\pm 40\%$, $\pm 30\%$, $\pm 20\%$, $\pm 10\%$, 0%).
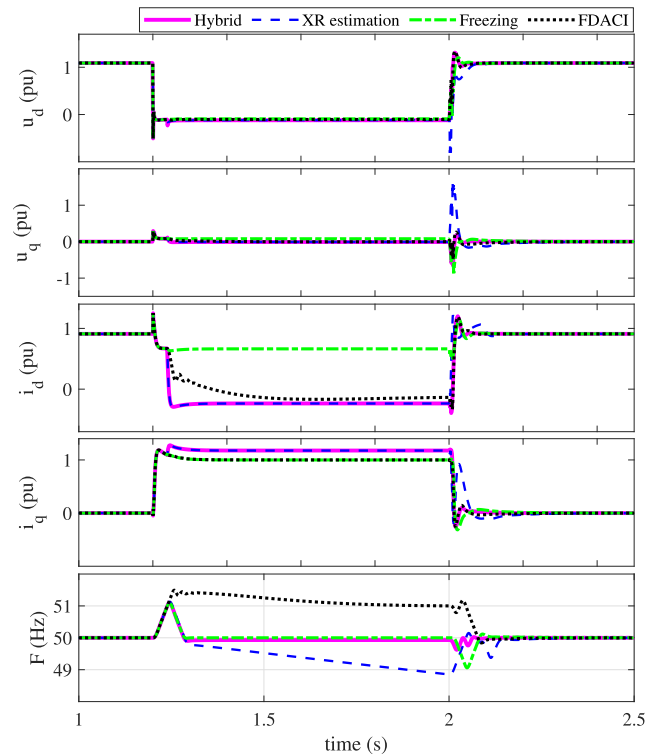
FIGURE 14. Response of WT to a severe fault with approximately 25% estimation error for different solutions.

FDACI experiences 1 Hz steady-state frequency deviation due to its embedded dead-zone [3]. Also, it has the slowest response due to the fact that it uses a PI controller which needs to be tuned in accordance with the other controllers of the WT. The method based on X/R estimation experiences a frequency drift due the considered estimation error. PLL freezing and the hybrid solution show a negligible frequency deviation as can be observed in Fig. 14.

Regarding the currents, PLL freezing keeps the defaulted current references. It, however, does not mean that it is meeting the grid code requirements as the PLL is frozen.

TABLE 1. The ranges of X and R for the considered estimation errors.

Estimation error (%)	Rang of X (pu)	Range of R (pu)
0 %	0.25	0.03
10 %	[0.225 , 0.275]	[0.027, 0.033]
25 %	[0.1875 , 0.3125]	[0.0225, 0.0375]
50 %	[0.125 , 0.375]	[0.015, 0.045]
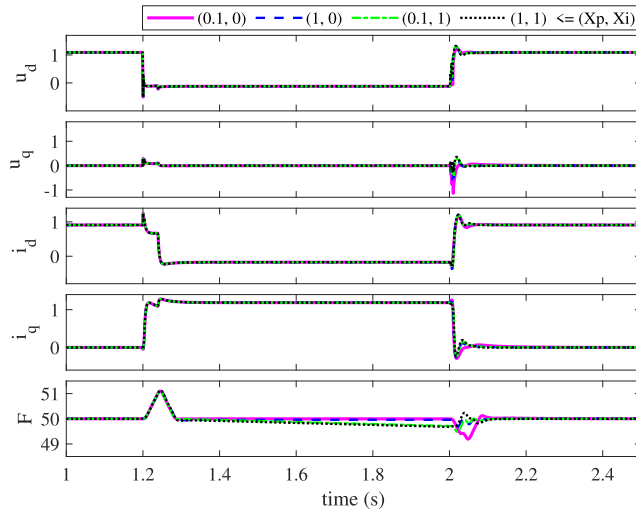
FIGURE 15. The result for an estimation error of 10%.

FIGURE 16. The result for an estimation error of 25%.

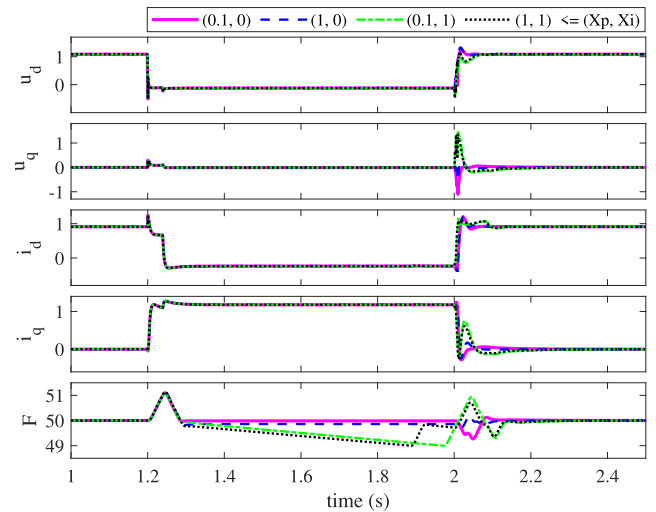**FIGURE 17.** The result for an estimation error of 50%.

FDACI modifies I_d^* to maintain the stability. Finally, X/R estimation and the hybrid solution set the current references based on $\hat{X}/\hat{R}$-ratio.

The hybrid Adaptive-PLL shows the best post fault transient if voltages, current, and frequency are considered all together. FDACI experiences the post fault transient mainly due to its steady state frequency deviation during the fault. For X/R estimation, the post fault transient is significant as a result of the frequency drift. PLL freezing also experiences a noticeable post fault transient due to the de-freezing after fault. The hybrid solution has neither frequency deviation/drift during fault nor de-freezing after fault. Minimising the frequency deviation, without freezing the PLL, results in improved transient response of the system with the proposed solution, as shown in Fig. 14 for the voltages, currents, and frequency. Besides that, the proposed solution has the advantage of avoiding unnecessary reaction of the controllers thanks to the implemented logical circuit.
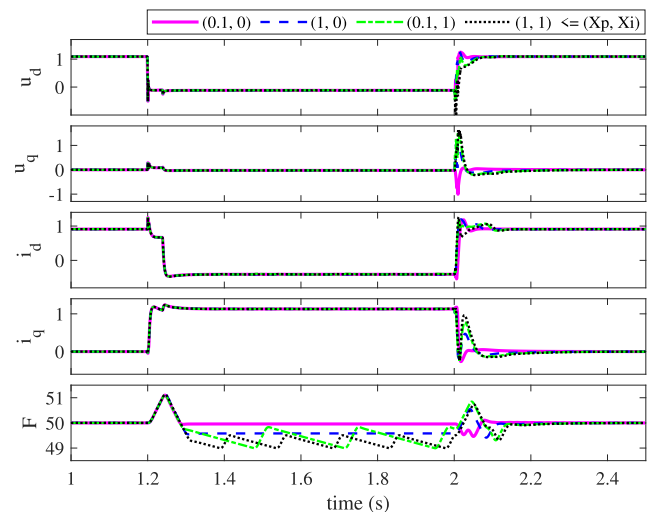
In the following subsection, results for the hybrid solution with different estimation errors of the impedance are presented.

C. THE HYBRID ADAPTIVE-PLL WITH DIFFERENT ESTIMATION ERRORS

The result for estimation errors of 10%, 25%, and 50% are presented in Fig. 15-17. Table 1 indicates the range of X and R for the considered estimation errors. The ranges are computed using the following equation in which $Error(X)$ and $Error(R)$ stand for the estimation error while R and X are real value of the impedance (taken from Table 2).

$$\text{Range of } X = [X - Error(X), X + Error(X)]$$
$$\text{Range of } R = [R - Error(R), R + Error(R)] \quad (22)$$

Based on the previous discussions, the simulations are performed with minimum value of X and maximum value of R in each case. The selected values of X and R for the simulations are Gray-highlighted in Table 1.

The result for 10% estimation error and with different scaling factors (X_p, X_i) for adapting the PLL gains are shown in Fig. 15. As it can be observed, a good estimation of the impedance removes the need for adapting the PLL gains. Interestingly, high changes in the PLL gains introduces higher transient after fault clearance due to the experienced jump in the PLL gain (see the plots for $(X_p, X_i) = (0.1, 0)$ in Fig. 15).

The result for an estimation error of 25% are presented in Fig. 16. As it can be seen in this figure, without

adapting the integrator gain, the WT experiences larger post-fault transients due to the frequency drift which happens during the fault (see the plots for $(X_p, X_i) = (1, 1)$ and $(X_p, X_i) = (0.1, 1)$ in Fig. 16). Reducing the proportional gain, however, deteriorates the post fault transient of the system and is not recommended (compare the plots for $(X_p, X_i) = (1, 0)$ with $(X_p, X_i) = (0.1, 0)$ in Fig. 16).

Finally, the results for an estimation error of 50% are shown in Fig. 17. Apparently, adapting the PLL gains in this case highly improves performance of the WT during sever faults. In contrast to the case with 25% estimation error, when the estimation error is 50%, reducing the proportional gain of PLL (k_p) decreases the steady state frequency deviation during fault and improves the post-fault transient response (compare the plots for $(X_p, X_i) = (1, 0)$ with those of $(X_p, X_i) = (0.1, 0)$ in Fig. 17)). Worth nothing that thanks to the implemented logical circuit, the frequency has tooth-wave behaviour and deos not experience a continues drift. Otherwise, the frequency would continue going down and down which would lead to an edgier post fault transient for $(X_p, X_i) = (1, 1)$ and $(X_p, X_i) = (0.1, 1)$.

Conclusively, selecting the PLL gains during severe faults turns out to be more likely a case to case practice. In the other words, the optimum PLL-gains depends on the accuracy of the available knowledge about the system parameters.

VI. CONCLUSION

For a better and intuitive understanding of LoS, a *dq* domain analysis is introduced in this paper. The main advantage of the presented analysis is its simplicity in grasping the key role of the PLL in frequency drift and LoS.

Based on the presented *dq* domain analysis, it can be easily observed that the grid code requirements for injecting reactive current, along with the current limitations of the converter, leads to a non zero U_q. Subsequently, this non-zero value is integrated by the PLL's PI controller and ultimately causes frequency drift and LoS. A hybrid solution which combines $\hat{X}/\hat{R}$-ratio with the flexibility of an Adaptive-PLL is proposed to counteract the LoS. Depending on the accuracy of $\hat{X}/\hat{R}$-ratio, the Adaptive-PLL updates its gains in case of severe fault to ameliorate the problem: the higher the accuracy of $\hat{X}/\hat{R}$-ratio, the lower the required changes in the PLL gains. Based on this criteria, the scaling factors for the Adaptive-PLL (X_p and X_i) can be selected. In this way, if $\hat{X}/\hat{R}$-ratio can be estimated accurately, it is recommended to use the default values so as to avoid the jumps in the PLL gains (for improving post-fault response of the WT). When the knowledge about the system is limited to 25% of estimation error, reducing the integrator gain ($X_i < 1$) will help in avoiding the frequency drift during severe faults. Additionally, when the estimation error is around 50%, reducing the proportional gain ($X_p < 1$), in addition to ($X_i < 1$), decreases the expected steady state frequency deviation during the fault and improves the post fault transient; as is verified with the simulation results.

Besides that, the paper proposes a logical circuit which takes into account the measured voltage and frequency for a more reliable detection of LoS. That reduces the uncertainty related to occurrence of LoS and prevents unnecessary reaction of the controllers.

As stated in the introduction, if the WTs are expected to ride through zero voltage faults, the hybrid Adaptive-PLL is a strong and feasible candidate for avoiding instability problems and guaranteeing the WTs to stay connected, which would help towards system stability.

APPENDIX
A. abc TO dq
In this part, the detailed derivation of mapping Eq. (1) into dq-frame is presented. Eq. (1) is re-written in the following.

$$U = R \cdot I + L\frac{dI}{dt} \tag{23}$$

assuming that ωt is the displacement angle between abc-frame and PLL-dq-frame, then:

$$U = U_{dq} \cdot e^{j\omega t}$$
$$I = I_{dq} \cdot e^{j\omega t} \tag{24}$$

Substituting Eq. (24) in Eq. (23) gives:

$$U_{dq}e^{j\omega t} = RI_{dq}e^{j\omega t} + \frac{dI_{dq}e^{j\omega t}}{dt} \tag{25}$$

expansion of the derivation term in Eq. (25) is written below:

$$\frac{dI_{dq}e^{j\omega t}}{dt} = I_{dq} \cdot \frac{de^{j\omega t}}{dt} + e^{j\omega t}\frac{dI_{dq}}{dt}$$
$$= j\omega e^{j\omega t}I_{dq} + e^{j\omega t}\frac{dI_{dq}}{dt} \tag{26}$$

substituting Eq. (26) in Eq. (25) leads to:

$$U_{dq}e^{j\omega t} = RI_{dq}e^{j\omega t} + j\omega e^{j\omega t}I_{dq} + e^{j\omega t}\frac{dI_{dq}}{dt} \tag{27}$$

Multiplying both sides of Eq. (27) by $e^{-j\omega t}$ leads to:

$$U_{dq} = RI_{dq} + j\omega I_{dq} + \frac{dI_{dq}}{dt} \tag{28}$$

during steady state:

$$\frac{dI_{dq}}{dt} = 0 \tag{29}$$

consequently:

$$U_{dq} = RI_{dq} + j\omega I_{dq} \tag{30}$$

and:

$$U_{dq} = U_d + jU_q$$
$$I_{dq} = I_d + jI_q \tag{31}$$

Substituting Eq. (31) in Eq. (30) results in:

$$U_d + jU_q = R \cdot (I_d + jI_q) + jL\omega(I_d + jI_q) \tag{32}$$

and separating real and imaginary part of Eq. (32) gives:

$$U_d = R \cdot I_d - L\omega I_q$$
$$U_q = R \cdot I_q + L\omega I_d \tag{33}$$

which is the equivalence of Eq. (23) in *dq* domain.

B. PARAMETER VALUES
See Table 2.

TABLE 2. Parameter values of the case study.

Parameter	Value	Unit
P_{rated}	10	MW
(X_{tr1}, R_{tr1})	(0.1, 0.01)	pu
(X_{line}, R_{line})	(0.05, 0.01)	pu
(X_{tr2}, R_{tr2})	(0.1, 0.01)	pu
(Kp_{PLL}, Ki_{PLL})	(100, 1000)	pu

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AMIR ARASTEH received the B.Sc. degree in electrical engineering and the B.Sc. degree in control-automation engineering from the Polytechnic University of Tehran, in 2012 and 2013, respectively, and the M.Sc. degree (Hons.) in electrical engineering from the Politecnico di Milano, in 2016. After a two years of research work at RWTH-Aachen, in 2018, he joined the DTU Wind Energy for his Ph.D. studies.

NICOLAOS A. CUTULULIS (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in automatic control, in 1998 and 2005, respectively. He is currently a Professor with the Department of Wind Energy, Technical University of Denmark. His main research interests include integration of wind power, with a special focus on offshore wind power, and grids, involving a variety of technical disciplines including modeling, optimisation, control of wind turbines, and farms, wind power variability, and ancillary services from wind power.

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