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Design and Implementation of Asymmetrical Multilevel Inverter With Reduced Components and Low Voltage Stress

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ABSTRACT Multilevel inverters with a high device count, low boosting and DC voltage imbalance are all common problems exists in the traditional topologies. In this article, a new single-phase asymmetrical multilevel inverter (MLI) that can generate 33 levels at the output with fewer components and lower total standing voltage (TSV) at the switches is presented. The multiple input sources of the proposed inverter make it suited for the use in renewable energy generating systems which have a variety of DC sources. The stress distribution among the switches is investigated that reduces the use of high rated devices with which overall cost of the inverter gets reduced. The topology can be extended by adding the circuits in series for higher levels. The performance of the inverter is calculated considering a variety of critical parameters such as TSV, cost function (CF), power loss, and efficiency calculations. The MLI is tested under dynamic load conditions with sudden load disturbances with a range of combinational loads and it has been determined to be stable throughout its operation. A detailed comparison is made based on stress across the switches, stress distribution, switches count, DC sources count, gate driver circuits, component count factor, TSV, CF, and other existing topologies using graphical representations and shown to be cost-effective and superior in all aspects. The total harmonic distortion (THD) derived from simulation and experiment complies with IEEE standards. The proposed framework has been developed in MATLAB/Simulink and tested in a laboratory environment with hardware.

INDEX TERMS Multilevel inverter, maximum blocking voltage (MBV), total standing voltage (TSV), normalised voltage stress (NVS), stress distribution, cost function (CF), total harmonic distortion (THD).

I. INTRODUCTION

The academic and industrial sectors are very interested in multilevel inverters. Multilevel strategies improve the inverter's output power quality while also allowing for higher voltage levels in power electronic circuits. [1]. Low–medium rated semiconductor switches are available on the market and can be used to achieve higher power levels. A sequential connection of switches is required to create a high rated converter with standard two-level operation. Because of their benefits, multilevel inverters are used in a variety of applications, including uninterruptible power supply systems (UPS) [2], hybrid photovoltaic UPS systems [3], traction [4], ships [5], renewable systems [6], electric vehicles [7], and power quality [8]. Multilevel converters, despite their differences, frequently need a large number of switches consists of greater losses and costs, and use significant modulation techniques. Many research studies are being undertaken to solve these issues.

Neutral point clamped (NPC) MLIs, flying capacitor (FC) MLIs, and cascaded H-bridge (CHB) MLIs are the three primary types of MLIs [9]. Over the last two decades, the benefits and drawbacks of the three types of MLIs outlined above have been thoroughly researched. In summary, the major disadvantages of these MLIs include altering the voltage in NPC, the control complexity for making a balance in

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voltages in the FC, and the more switches count and independent excitations in CHB. Cascaded MLIs may provide more voltage levels, and dependability than other MLI topologies due to their modular architecture. [10]. Asymmetric MLIs are topologies with uneven dc-link voltages, whereas symmetric cascaded inverters have equal dc sources. Asymmetric topologies may give a wider range of output voltage values than symmetric topologies. These are not possible to implement practically and difficult to balance the supplied power across every source of the circuit with the load with the existence of two or more excitations with same magnitudes [11]. Many techniques for opting the size of input sources are described to get a larger output levels asymmetric type of design. Reference [12] Describes a single-sourced MLI that employs various types of configurations such as equal and unequal sources, series and parallel voltage balancing methods in capacitor in order to double the magnitude of the input voltage. The inverter TSV is relatively low because there is no extra H-bridge circuit. Utilizing two unequal sources and dual capacitors, the inverter [13] can able to produce 13 levels at its output. Because of the connection type as cascade with the other modules offers greater levels at the output without the use of an extra H-bridge, reducing stress across the switches in this type of configuration. MLI [15] covers the usage of T-type architecture and cross sectional-connected units to product the output. Due to the extra power switches in this configuration in order to facilitate charging and discharging behaviour of the capacitor, stress across the switches is high.

In recent years, scholars have proposed a slew of new architectures. A couple of them are examined thoroughly. An H-bridge was proposed as part of a framework consisting of cascading basic components in [13] due to the high conduction losses, large number of switches are enhanced in this arrangement. The topology in [14] finds a second-order connection between the peak inverse voltages of the circuit (PIV) with levels count. As a result, the inverter is expensive and unsuitable for applications requiring high voltage. Each basic unit consists of a unique construction comprised of many bidirectional switches. A new cascaded MLI topology is presented in [15], which is aimed to reduce the number of switches and dc sources by utilizing three algorithms. The selective harmonic elimination modulation is used to produce the pulses to the switches for getting the desired output. In [16] and [17], a switched capacitor based MLI is proposed, which consist of high gain and energized with a single DC source. The proposed MLI has reduced switch count and has superior performance and cost-effective. In [18], a novel 21-level MLI is designed with reduced switch count having less TSV and cost function, the MLI is fed to solar PV applications. The topology in [19] introduced a novel framework that includes two algorithms for selecting dc sources. However, the symmetric operation has a high number of switches. An alternative topology is shown in [20].

The cascaded structure is addressed in [21] with a switched capacitor based single phase MLI is designed with superior performance compared with the respective MLI topologies. A reduced switch count single phase MLI is presented in [22] where the performance evaluation of the parameters is calculated and holds superior aimed to design MLI with less components count and to minimize the standing voltage. The architecture, as illustrated in [23], uses additive and subtractive techniques to generate nine level output from two unequal dc excitations. Reference [23] Offers a series-connected linear dc-source value development. In contrast, this architecture requires higher switch voltage ratings and high stress across the switches on the inverter. In [24], the authors suggested a novel architecture with reduced switch count MLI, where the MLI has outstanding performance in reducing the TSV value. The topology presented in [25] proposed a new MLI with a redesigned H-bridge and numerous dc-sources.

Although these topologies require fewer gate driver circuits, bidirectional type of power electronic switches tends to have a gradual increase of switches and size of the inverter. Another approach is to use modular-based topologies with an integrated polarity switcher to reduce the inverter's standing voltage. The ST-type architecture employs 12 power electronic switches to provide a seventeen levels of output voltage, with input excitation magnitudes to be opted using the trinary progression technique. Even though these topologies offer an output levels count with a limited sources count, they have a more switches count [26]. Each module in [27] delivers 9 level and 17 level voltage outputs in symmetric and asymmetric ways with 10 power switches and 4 input sources. Another system proposed by [28] uses 10 switches to generate seventeen levels. Despite the use of asymmetric dc-sources in this system, the maximum stress across the power electronic switches holds significant. Another reduced switch count topology presented in [29] with a less switching frequency and less TSV.

A 33-level asymmetric MLI architecture is proposed and implemented in this work, with minimal voltage stress on switches and lower THD. Along with the power loss estimates, the influence of voltage stress on the topology is addressed in depth. The number of switches, voltage levels, DC source count, the voltage stress on switches, power loss, efficiency, THD, and circuit complexity are used to determine MLI performance. The developed MLI is built using simulations in environment of MATLAB/Simulink and implemented with a experimental prototype in a laboratory, where it is evaluated under various loaded circumstances such as Resistive load, inductive load, combination of both resistive and inductive loads as well as dynamic loading conditions. The MLI performance is compared to that of different current topologies, both traditional and modern. Where a separate DC source excitation is available, the designed MLI is applied for grid integrated renewable energy systems and electric vehicles.

The remainder of the paper is formulated as: analysis and implementation of the developed 33-level MLI configuration and the extended topology are presented in section-2. Performance evaluation of the MLI with various parameters like TSV, cost function, power loss and efficiency

TABLE 1. Switching sequence for the developed 33-level MLI structure.

Positive Levels												V_O	Negative Levels											
S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	0	0	1	0	1	1	0	0	1	1	0	$16V_{dc}$	1	0	0	1	1	0	0	1	0	1	1	0
0	1	0	1	0	1	1	0	0	1	1	0	$15V_{dc}$	1	0	0	1	1	0	0	1	0	1	0	1
1	0	0	1	1	0	1	0	0	1	1	0	$14V_{dc}$	1	0	0	1	1	0	1	0	0	1	1	0
1	0	1	0	0	1	1	0	0	1	1	0	$13V_{dc}$	1	0	0	1	0	0	0	1	1	0	1	0
1	0	0	1	0	1	1	0	1	0	1	0	$12V_{dc}$	1	0	1	0	1	0	0	1	0	1	0	0
0	1	0	1	0	1	1	0	1	0	1	0	$11V_{dc}$	1	0	1	0	1	0	0	1	0	1	0	1
1	0	0	1	1	0	1	0	1	0	1	0	$10V_{dc}$	1	0	1	0	1	0	1	0	0	1	1	0
0	1	0	1	1	0	1	0	1	0	1	0	$9V_{dc}$	1	0	1	0	1	0	1	0	0	1	0	1
0	1	1	0	0	1	1	0	1	0	1	0	$8V_{dc}$	1	0	1	0	1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0	1	0	1	0	$7V_{dc}$	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	1	0	$6V_{dc}$	1	0	0	1	0	1	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1	1	0	$5V_{dc}$	1	0	0	1	0	1	1	0	0	1	1	0
1	0	1	0	0	1	0	1	0	1	1	0	$4V_{dc}$	0	1	1	0	1	0	1	0	0	1	0	1
1	0	0	1	0	1	1	0	0	1	0	1	$3V_{dc}$	0	1	0	1	1	0	0	1	0	1	1	0
0	1	0	1	0	1	1	0	0	1	0	1	$2V_{dc}$	1	0	1	0	0	1	1	0	1	0	1	0
1	0	0	1	1	0	0	1	1	0	1	0	V_{dc}	0	1	0	1	1	0	0	1	1	0	0	1
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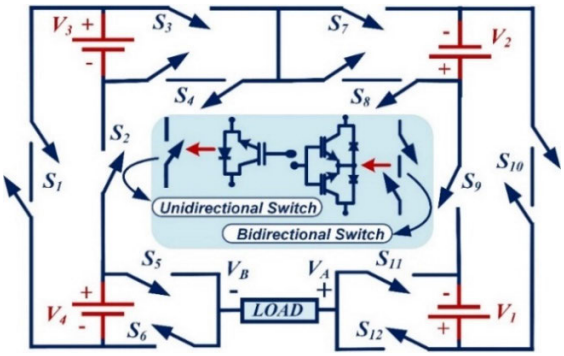

FIGURE 1. Proposed 33-level MLI topology.

calculations are presented in section-3. The comparisons and application is presented in section-4. The both simulation and experimental results with discussions are presented in section-5. Section-6 is followed by the conclusions and future scope.

II. PROPOSED INVERTER TOPOLOGY

In this section, a fundamental unit and the generalized extended structure of the proposed 33-level MLI architectures are implemented. Several parameters of the MLI are designed based on the design equations, switching states, load current paths, maximum blocking voltage (MBV), total standing voltage (TSV) calculations with a reference output voltage waveform. Several MLI parameters are calculated which are intended to estimate the performance of MLI.

The circuit configuration of the developed 33-level MLI topology is represented in FIGURE 1. It has eight unidirectional and four bidirectional semiconductor switches with four input DC voltage sources. The basic unit of the proposed architecture can able to generate thirty-three levels of voltage at the output. The magnitudes of the input DC sources V_1, V_2, V_3, and V_4 are selected in the ratio of 1:2:4:9 [31] with a V_{dc} value of 25V.

The multiple inputs with unequal sources make the inverter suited for the use in renewable energy generating systems which have a variety of DC sources. In practical applications like photovoltaic generation systems, the PV panels are integrated using DC-DC converters to optimize the output voltage waveform.

The required DC sources N_{dc} are mathematically related to the number of levels N_L used by the equation

$$N_{dc} = \frac{(N_L - 9)}{6} \tag{1}$$

The number of switches N_{SW} required are may be mathematically related to the number of levels N_L used by the equation

$$N_S = \frac{(N_L - 9)}{2} \tag{2}$$

The required gate driver circuits N_{gd} are given by

$$N_{gd} = \frac{(N_L + 3)}{3} \tag{3}$$

The maximum voltage output produced $V_{0,max}$ is given by

$$V_0 = \frac{(N_L - 1)}{2} \tag{4}$$

A. OPERATION OF THE PROPOSED TOPOLOGY

The basic unit generates 33 number of voltage levels, including 0V, $\pm 1V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, $\pm 7V_{dc}$, $\pm 8V_{dc}$, $\pm 9V_{dc}$, $\pm 10V_{dc}$, $\pm 11V_{dc}$, $\pm 12V_{dc}$, $\pm 13V_{dc}$, $\pm 14V_{dc}$, $\pm 15V_{dc}$ and $\pm 16V_{dc}$ at its output with a step size of V_{dc} with the DC voltage sources of $V_1 = 1V_{DC}$, $V_2 = 2V_{DC}$, $V_3 = 4V_{dc}$, $V_4 = 9V_{dc}$. The proposed configuration generates 16 positive output voltage steps from $+V_{dc}$ to $+16V_{dc}$, zero output voltage step, and 16 negative output voltage steps from $-V_{dc}$ to $-16V_{dc}$. The switching states for the proposed 33-level MLI during both levels of operation (positive and negative) is represented in TABLE 1. The current paths to the load along with the voltage stress

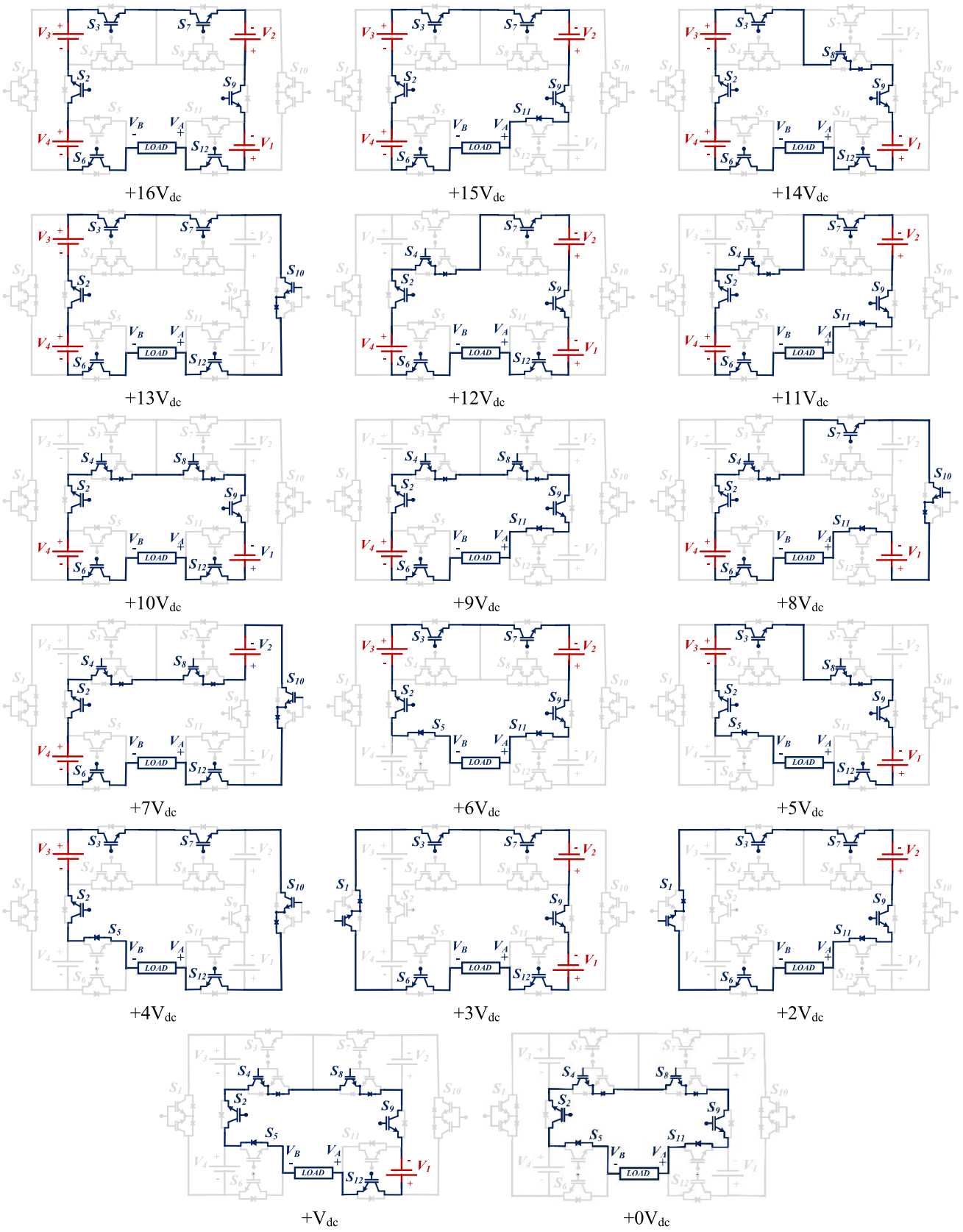

FIGURE 2. Operating modes of the developed MLI structure during the positive half cycle.

TABLE 2. Load current paths and MBV across switches for the developed 33-level MLI.

Mode	*Load current path*	*Active Sources*	*Stress on switches*	*MBV*		*Output Voltage (V_0)*
				Maximum stress across switch		
Mode-1	V_B–S_6–V_4–S_2–V_3–S_3–S_7–V_2–S_9–V_1–S_{12}–V_A	V_4+V_3+V_2+V_1	S_1, S_4, S_5, S_8, S_{10}, S_{11}	S_1	$13V_{dc}$	$16V_{dc}$
Mode-2	V_B–S_6–V_4–S_2–V_3–S_3–S_7–V_2–S_9–S_{11}–V_A	V_4+V_3+V_2	S_1, S_4, S_5, S_8	S_1	$13V_{dc}$	$15V_{dc}$
Mode-3	V_B–S_6–V_4–S_2–V_3–S_3–S_8–S_9–V_1–S_{12}–V_A	V_4+V_3+V_1	S_1, S_4, S_5, S_{11}	S_1	$13V_{dc}$	$14V_{dc}$
Mode-4	V_B–S_6–V_4–S_2–V_3–S_3–S_7–S_{10}–S_{12}–V_A	V_3+V_4	S_1, S_4, S_5	S_1	$13V_{dc}$	$13V_{dc}$
Mode-5	V_B–S_6–V_4–S_2–S_4–S_7–V_2–S_9–V_1–S_{12}–V_A	V_4+V_2+V_1	S_1, S_5, S_8, S_{10}, S_{11}	S_1=S_5	$9V_{dc}$	$12V_{dc}$
Mode-6	V_B–S_6–V_4–S_2–S_4–S_7–V_2–S_9–S_{11}–V_A	V_2+V_4	S_1, S_5, S_8, S_{10}, S_{12}	S_1=S_5	$9V_{dc}$	$11V_{dc}$
Mode-7	V_B–S_6–V_4–S_2–S_4–S_8–S_9–V_1–S_{12}–V_A	V_4+V_1	S_1, S_5, S_7, S_{10}, S_{11}	S_1=S_5	$9V_{dc}$	$10V_{dc}$
Mode-8	V_B–S_6–V_4–S_2–S_4–S_8–S_9–S_{11}–V_A	V_4	S_1, S_5	S_1=S_5	$9V_{dc}$	$9V_{dc}$
Mode-9	V_B–S_6–V_4–S_2–S_4–S_7–S_{10}–V_1–S_{11}–V_A	V_4-V_1	S_1, S_5, S_9, S_{12}	S_1=S_5	$9V_{dc}$	$8V_{dc}$
Mode-10	V_B–S_6–V_4–S_2–S_4–S_8–V_2–S_{10}–S_{12}–V_A	V_4-V_2	S_1, S_5, S_7, S_9	S_1=S_5	$9V_{dc}$	$7V_{dc}$
Mode-11	V_B–S_5–S_2–V_3–S_3–S_7–V_2–S_9–S_{11}–V_A	V_2+V_3	S_1, S_4, S_8, S_{10}	S_1=S_4	$4V_{dc}$	$6V_{dc}$
Mode-12	V_B–S_5–S_2–V_3–S_3–S_8–S_9–V_1–S_{12}–V_A	V_1+V_3	S_1, S_4, S_{10}, S_{11}	S_1=S_4	$4V_{dc}$	$5V_{dc}$
Mode-13	V_B–S_5–S_2–V_3–S_3–S_7–S_{10}–S_{12}–V_A	V_3	S_1, S_4	S_1=S_4	$4V_{dc}$	$4V_{dc}$
Mode-14	V_B–S_6–S_1–S_3–S_7–V_2–S_9–V_1–S_{12}–V_A	V_1+V_2	S_8, S_{10}, S_{11}	S_{10}	$3V_{dc}$	$3V_{dc}$
Mode-15	V_B–S_6–S_1–S_3–S_7–V_2–S_9–S_{11}–V_A	V_2	S_8, S_{10}	S_8=S_{10}	$2V_{dc}$	$2V_{dc}$
Mode-16	V_B–S_5–S_2–S_4–S_8–S_9–V_1–S_{12}–V_A	V_1	S_{10}, S_{11}	S_{10}=S_{11}	V_{dc}	V_{dc}
Mode-17	V_B–S_5–S_2–S_4–S_8–S_9–S_{11}–V_A	0	-	-	-	0
Mode-18	V_A–S_{12}–V_1–S_9–S_8–S_4–S_2–S_5–V_B	-V_1	S_{10}, S_{11}	S_{10}=S_{11}	V_{dc}	-V_{dc}
Mode-19	V_A–S_{11}–S_9–V_2–S_7–S_3–S_1–S_6–V_B	-V_2	S_8, S_{10}	S_8=S_{10}	$2V_{dc}$	-$2V_{dc}$
Mode-20	V_A–S_{11}–V_1–S_{10}–V_2–S_8–S_4–S_2–S_5–V_B	-(V_1+V_2)	S_7, S_9, S_{12}	S_9	$3V_{dc}$	-$3V_{dc}$
Mode-21	V_A–S_{12}–S_{10}–S_7–S_3–V_3–S_2–S_5–V_B	-(V_3)	S_1, S_4	S_1=S_4	$4V_{dc}$	-$4V_{dc}$
Mode-22	V_A–S_{11}–V_1–S_{10}–S_7–S_4–V_3–S_1–S_6–V_B	-(V_1+V_3)	S_2, S_3, S_9, S_{12}	S_2=S_3	$4V_{dc}$	-$5V_{dc}$
Mode-23	V_A–S_{12}–S_{10}–V_2–S_8–S_4–V_3–S_1–S_6–V_B	-(V_2+V_3)	S_2, S_3, S_7, S_9, S_{10}	S_2=S_3	$4V_{dc}$	-$6V_{dc}$
Mode-24	V_A–S_{11}–S_9–V_2–S_7–S_3–S_1–V_4–S_5–V_B	-(V_4-V_2)	S_2, S_6, S_8, S_{10}	S_2=S_6	$9V_{dc}$	-$7V_{dc}$
Mode-25	V_A–S_{12}–V_1–S_9–S_8–S_3–S_1–V_4–S_5–V_B	-(V_4-V_1)	S_2, S_6, S_{10}, S_{11}	S_2=S_6	$9V_{dc}$	-$8V_{dc}$
Mode-26	V_A–S_{12}–S_{10}–S_7–S_3–S_1–V_4–S_5–V_B	-V_4	S_2, S_6	S_2=S_6	$9V_{dc}$	-$9V_{dc}$
Mode-27	V_A–S_{11}–V_1–S_{10}–S_7–S_3–S_1–V_4–S_5–V_B	-(V_4+V_1)	S_2, S_6, S_9, S_{12}	S_2=S_6	$9V_{dc}$	-$10V_{dc}$
Mode-28	V_A–S_{12}–S_{10}–V_2–S_8–S_3–S_1–V_4–S_5–V_B	-(V_2+V_4)	S_2, S_6, S_7, S_9	S_2=S_6	$9V_{dc}$	-$11V_{dc}$
Mode-29	V_A–S_{11}–V_1–S_{10}–V_2–S_8–S_3–S_1–V_4–S_5–V_B	-(V_4+V_2+V_1)	S_2, S_6, S_7, S_9, S_{11}, S_{12}	S_2=S_6	$9V_{dc}$	-$12V_{dc}$
Mode-30	V_A–S_{11}–S_9–S_8–S_4–V_3–S_1–V_4–S_5–V_B	-(V_3+V_4)	S_2, S_3, S_5, S_6	S_2	$13V_{dc}$	-$13V_{dc}$
Mode-31	V_A–S_{11}–V_1–S_{10}–S_7–S_4–V_3–S_1–V_4–S_5–V_B	-(V_4+V_3+V_1)	S_2, S_3, S_6, S_9, S_{12}	S_2	$13V_{dc}$	-$14V_{dc}$
Mode-32	V_A–S_{12}–S_{10}–V_2–S_8–S_4–V_3–S_1–V_4–S_5–V_B	-(V_4+V_3+V_2)	S_2, S_3, S_6, S_7, S_9, S_{11}	S_2	$13V_{dc}$	-$15V_{dc}$
Mode-33	V_A–S_{11}–V_1–S_{10}–V_2–S_8–S_4–V_3–S_1–V_4–S_5–V_B	-(V_4+V_3+V_2+V_1)	S_2, S_3, S_6, S_7, S_9, S_{12}	S_2	$13V_{dc}$	-$16V_{dc}$

on the switches and maximum blocking voltage (MBV) is provided in TABLE 2. The various operating modes of the MLI during the positive cycle are represented in FIGURE 2. The highlighted lines indicate the current flowing through the active elements during each level of operation. The maximum stress on the switches and the respective blocking voltage is given in TABLE 2. It is found that there exist redundant switches for some levels of operating voltages. The developed 33-level topology is designed based on the parameters given in TABLE 3. Therefore, for one basic unit of MLI, n = 1, the switches count N_{SW} is 12, the input DC sources count N_{dc} is 4 and the total number of the level N_L is 33 with a load voltage of V_0 = 400V. The maximum output voltage levels for the implemented 33-level inverter configuration are $\pm 16V_{dc}$, which can be accessed from equation (4). The simulation results of output voltage, current waveform and THD are shown in FIGURE 12, FIGURE 13 and FIGURE 14 respectively.

The functioning of the switches in Mode-1 of the circuit are S_2, S_3, S_6, S_7, S_9, and S_{12} are in conduction in producing a load voltage of 16 V_{dc} and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_4, S_5, S_8, S_{10}, S_{11}. Out of these switches, the maximum stress occurs on a switch S_1 with $13V_{dc}$ stress. The operating of the switches in Mode-2 are S_2, S_3, S_6, S_7, S_9 and S_{11} are in conduction in producing a load voltage of 15 V_{dc} and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_4, S_5, S_8. Out of these switches, the maximum stress occurs on a switch S_1 with $13V_{dc}$ voltage stress. The operating of the switches in Mode-3 of the circuit are S_2, S_3, S_6, S_8, S_9 and S_{12} are in conduction in producing a load voltage of $14V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_4, S_5, S_{11}. Out of these switches, the maximum stress occurs on a switch S_1 with $13V_{dc}$ voltage stress. The operating of the switches in Mode-4 of the circuit are S_2,

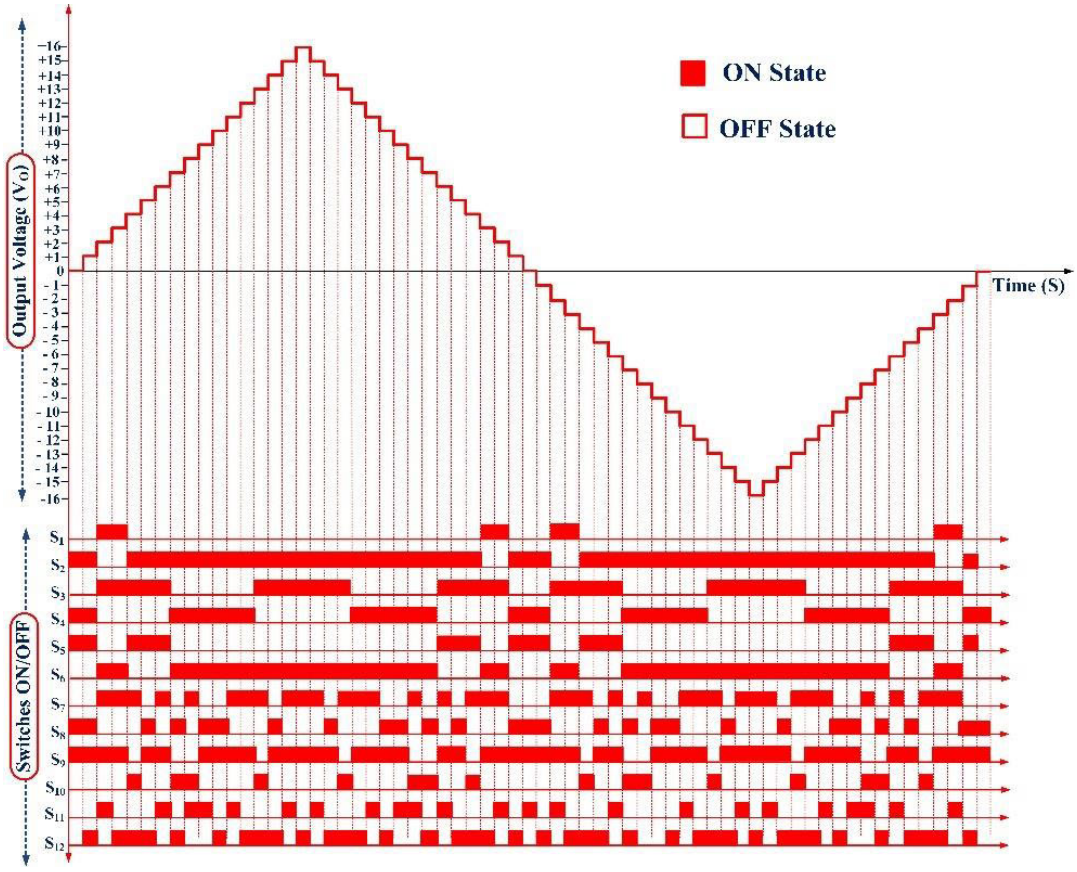

FIGURE 3. 33-level staircase typical output waveform.

S_3, S_6, S_7, S_{10} and S_{12} are in conduction and generates a load voltage of $13V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_4, S_5. Out of these switches, the maximum stress occurs on a switch S_1 with $13V_{dc}$ voltage stress. The operating of the switches in Mode-5 of the circuit are S_2, S_4, S_6, S_7, S_9 and S_{12} are in conduction and generates a load voltage of $12V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_5, S_8, S_{10}, S_{11}. Out of these switches, the maximum stress occurs on the switches S_1 and S_5 with $9V_{dc}$ voltage stress. The operating of the switches in Mode-6 of the circuit are S_2, S_4, S_6, S_7, S_9 and S_{11} are in conduction and generates a load voltage of $11V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_5, S_8, S_{10}, S_{12}. Out of these switches, the maximum stress occurs on the switches S_1 and S_5 with $9V_{dc}$ voltage stress. The operating of the switches in Mode-7 of the circuit are S_2, S_4, S_6, S_8, S_9 and S_{12} are in conduction and generates a load voltage of $10V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_5, S_7, S_{10}, S_{11}. Out of these switches, the maximum stress occurs on the switches S_1 and S_5 with $9V_{dc}$ voltage stress. The operating of the switches in Mode-8 of the circuit are S_2, S_4, S_6, S_8, S_9 and S_{11} are in conduction and generates a load voltage of $9V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1 and S_5. Out of these switches, the maximum stress occurs on the switches S_1 and S_5 with $9V_{dc}$ voltage stress. The operating of the switches in Mode-9 of the circuit are S_2, S_4, S_6, S_7, S_{10} and S_{11} are in conduction and generates a load voltage of $8V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_5, S_9, S_{12}. Out of these switches, the maximum stress occurs on the switches S_1 and S_5 with $9V_{dc}$ voltage stress. The operating of the switches in Mode-10 of the circuit are S_2, S_4, S_6, S_8, S_{10} and S_{12} are in conduction and generates a load voltage of $7V_{dc}$ and the rest of the switches are inoperative, where the voltage stress occurs across the switches on S_1, S_5, S_7, S_9. Out of these switches, the maximum stress occurs on the switches S_1 and S_5 with $9V_{dc}$ voltage stress. Similarly, the remaining levels along with negative voltage levels are obtained as per the switching sequences represented in TABLE 2. Some applications such as solar PV systems and energy storage systems are suitable for the proposed inverter. The typical 33-level expected reference voltage waveform at the output and respective gate pulses are represented in FIGURE 3. The gate pulses are produced in MATLAB/Simulink using the round-robin condition (staircase modulation approach).

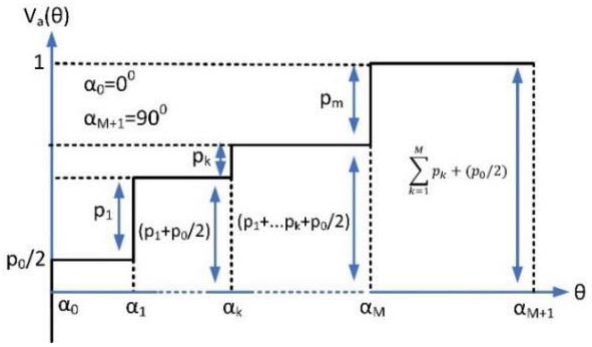

FIGURE 4. Generalized representation of a quarter-wave staircase waveform.

The staircase Modulation technique is considered than the traditional PWM technique because of its major benefits such as less complexity and lesser switching losses. This is applied for both high rated MLIs, with higher voltage levels (N) and low rated MLIs. Here forth, this technique is the most common and famous strategy for specifically multilevel inverters. Also, this technique is the best alternative for the Sine PWM switching technique with its reduced losses for the MLIs with higher ratings (N). While the symmetric type MLIs are common in general, utilizing the asymmetric type MLIs with a cascaded H-Bridge further reduces the total harmonic distortion (THD) value.

The waveform generated by staircase modulation technique, its generalized quarter-wave representation is given in FIGURE 4, which consists of M desired steps per quarter-wave, and one optional extra half-step appearing at the origin. For every kth step appearing at the phase switching angle αk, consists of a normalized width and height concerning DC supply voltage ratio of pk. The phase switching angle is α is given as $\alpha = \{\alpha 1, \alpha 2, \ldots \alpha, \ldots \alpha M\}$ and the DC supply voltage ratio is given as p = {p1, p2, ... pk, ... pM}, which are in degrees and per unit values respectively. To provide even values of N, an extra half-step with a value of p0/2, appearing at 0th phase angle, which is $\alpha 0 = 0$. The total number of phase switching angles per quarter-wave M is given as M = (N-1)/2 excluding $\alpha 0$, is related to N [30].

B. EXTENDED CASCADED STRUCTURE OF THE PROPOSED MLI

The fundamental unit of the developed MLI configuration can be connected in cascade typed of connection in order to increase the number of levels at the output. The extendable generalized MLI architecture for higher levels of output is shown in FIGURE 5. An efficient opting of DC sources in asymmetric type of operation, the cascaded structure can able to produce a larger levels of voltage at the output. Equations for determining the switches count, TSV and driver boards and the variance of selection is provided in TABLE 3, where 'n' indicates the fundamental unit count.

The parameters for the cascaded connection of the fundamental units are as follows:

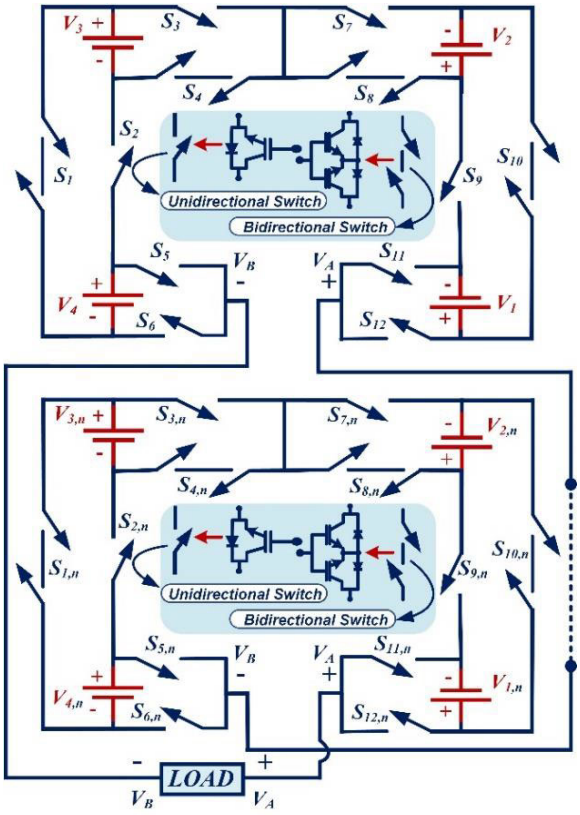

FIGURE 5. Extended architecture of the proposed MLI.

TABLE 3. Design Equations of the developed MLI structure.

S.no	Parameters	Based on basic units	Based on desired voltage levels
1	Voltage levels	32n+1	N_L
2	Power switches	12n	$6\left(\frac{N_L-1}{16}\right)$
3	Gate driver circuits	12k	$6\left(\frac{N_L-1}{16}\right)$
4	Diodes	-	-
5	TSV	53n	$5\left(\frac{N_L-1}{3}\right)$
6	TSV_{PU}	3.3n	$2\left(\frac{N_L-1}{19}\right)$

The number of fundamental units is "n".

Thus, for n basic units of MLI, the total number of switches are needed for the extended structure

$$N_s = 12n \tag{5}$$

The DC sources N_{dc} required for the extended topology is assessed as

$$N_{dc} = 4n \tag{6}$$

The extended topology produces a higher number of levels N_L, which are calculated as

$$N_L = 2\,(17n) - 1. \tag{7}$$

The voltage at the load terminals of an extended topology is calculated as

$$V_0 = 16n \times V_{dc} \tag{8}$$

The maximum output voltage for the developed extended MLI structure is be accessed using equation (9)

$$V_{0,max} = \pm\left(\frac{N_L - 1}{2}\right) \tag{9}$$

The total number of DC sources,

$$V_{1,n} = V_1 = V_{dc}, V_{2,n} = V_2 = 2V_{dc}, V_{3,n} = V_3 = 4V_{dc}, V_{4,n} = V_4 = 9V_{dc}, \tag{10}$$

where the DC sources count is $N_{dc} = 4n$.

The TSV of the extended MLI is given by

$$\sum_{i=1}^{n} MBV_{S,n} = \sum_{i=1}^{n} V_{S,n} \tag{11}$$

The sum of all maximum blocking voltages across the switches is used to compute the TSV.

$$TSV = MBVs_{1,n} + MBVs_{2,n} + \cdots\cdots\cdots .. + MBVs_n \tag{12}$$

Hence, the TSV for the extended MLI topology is calculated as

$$TSV = 2\sum_{i=1}^{n} MBV_{S,2n+1} \tag{13}$$

III. PERFORMANCE EVALUATION

The proposed 33-level MLI performance can be evaluated by considering the parameters of TSV, cost function (CF), impact of TSV on the circuit, total harmonic distortion (THD), power losses and efficiency calculations. Less TSV across the switches has numerous advantages, including lower losses and the ability to use a low-rated switch, which makes the inverter cost-effective. The following parameters are used to compute the performance parameters:

A. TSV CALCULATION

The total standing voltage of the switches plays a major role in determining the cost effectiveness and efficiency of the MLI. By lowering the stress across the semiconductor switches, the cost of the inverter architecture gets decreased [26]. The maximum voltage stress on a power device during the off state is described as the standing voltage. The sum of all maximum blocking voltages across the switches is the total standing voltage.

The TSV can be evaluated based on the operating modes shown in FIGURE 2. The maximum voltage blocking capacity of S_1 is determined using the blocking voltage of S_1 as an example at $V_0 = \pm 16V_{dc}$ or $\pm 15V_{dc}$ or $\pm 14V_{dc}$ or $\pm 13V_{dc}$. S_1 is turned off at all of these voltage levels. V_3 and V_4 apply a blocking voltage to S_1. The voltage stress across the bidirectional switches are $Vs_{bi} = V_i/2$, where $i = 1, 2, 3 \ldots .n$. The stress across each individual bidirectional switch is represented as follows:

$$MBVs_1 = V_{S1} = (V_3 + V_4)/2 = 6.5V_{dc}$$

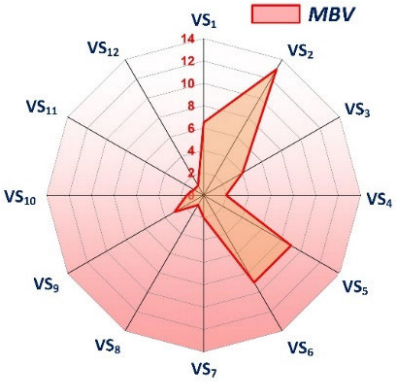

FIGURE 6. Maximum voltage stress across switches.

$$MBVs_4 = V_{S4} = V_3/2 = 2V_{dc}$$
$$MBVs_8 = V_{S8} = V_2/2 = 1V_{dc}$$
$$MBVs_{10} = V_{S10} = (V_1 + V_2)/2 = 1.5V_{dc}$$

The voltage stress across the unidirectional switches are $V_{Suni} = V_i$, where $i = 1, 2, 3 \ldots .n$. The stress across each individual unidirectional switch is represented as follows:

$$MBVs_2 = V_{S2} = V_3 + V_4 = 13V_{dc}$$
$$MBVs_3 = V_{S3} = V_3 = 4V_{dc}$$
$$MBVs_5 = V_{S5} = V_4 = 9V_{dc}$$
$$MBVs_6 = V_{S6} = V_4 = 9V_{dc}$$
$$MBVs_7 = V_{S7} = V_2 = 2V_{dc}$$
$$MBVs_9 = V_{S9} = V_1 + V_2 = 3V_{dc}$$
$$MBVs_{11} = V_{S11} = V_1 = 1V_{dc}$$
$$MBVs_{12} = V_{S12} = V_1 = 1V_{dc}$$

FIGURE 6 shows a graphical representation of MBV across all switches. The total maximum blocking voltages across all switches is used to compute the TSV. Hence TSV is calculated from the equation (14)

$$\begin{aligned} TSV &= \sum_{i=1}^{n} MBV_{Si} \\ TSV &= MBVs_1 + MBVs_2 + \cdots\cdots\cdots .. + MBVs_{12} \\ TSV &= 6.5V_{dc} + 13V_{dc} + 4V_{dc} + 2V_{dc} + 9V_{dc} + 9V_{dc} \\ &\quad + 2V_{dc} + 1V_{dc} + 3V_{dc} + 1.5V_{dc} + 1V_{dc} + 1V_{dc} \\ &= 53V_{dc} \end{aligned} \tag{14}$$

The TSV per unit (TSV_{pu}) is the ratio of the total TSV to the maximum voltage levels of the proposed MLI, can be obtained mathematically from the following equation (15)

$$TSV_{PU} = \frac{V_{TSV}}{V_{OMAX}} \tag{15}$$

where $TSV_{PU} = 3.31$.

The impact of stress distribution on the switches is represented in FIGURE 7 and is calculated based on the TSV and MBV values of the power switches, which is known as normalized voltage stress. This represents the amount of

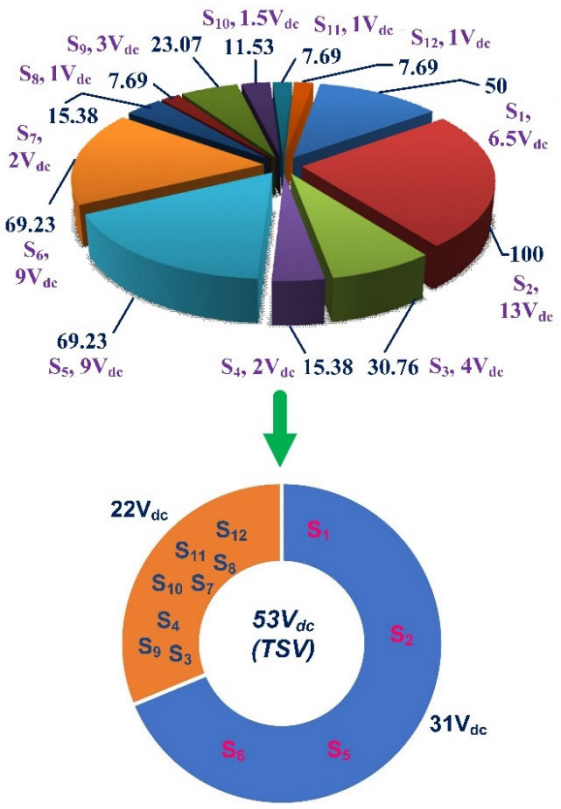

FIGURE 7. Impact of voltage stress distribution on the proposed 33-level MLI.

TABLE 4. Normalised voltage stress on power switches.

Power switches	MBV	Normalized voltage stress (NVS)	Impact of stress on switches (NVS)
S_1	$6.5V_{dc}$	$6.5V_{dc}/13V_{dc}$	50%
S_2	$13V_{dc}$	$13V_{dc}/13V_{dc}$	100%
S_3	$4V_{dc}$	$4V_{dc}/13V_{dc}$	30.76%
S_4	$2V_{dc}$	$2V_{dc}/13V_{dc}$	15.38%
S_5	$9V_{dc}$	$9V_{dc}/13V_{dc}$	69.23%
S_6	$9V_{dc}$	$9V_{dc}/13V_{dc}$	69.23%
S_7	$2V_{dc}$	$2V_{dc}/13V_{dc}$	15.38%
S_8	$1V_{dc}$	$1V_{dc}/13V_{dc}$	7.69%
S_9	$3V_{dc}$	$3V_{dc}/13V_{dc}$	23.07%
S_{10}	$1.5V_{dc}$	$1.5V_{dc}/13V_{dc}$	11.53%
S_{11}	$1V_{dc}$	$1V_{dc}/13V_{dc}$	7.69%
S_{12}	$1V_{dc}$	$1V_{dc}/13V_{dc}$	7.69%

stress distribution among the switches. It is the ratio of voltage stress over a single switch to circuit's maximum stress [27], which is calculated from equation (16).

$$\text{NVS} = \frac{\text{Actual voltage stress across switch}}{\text{Maximum voltage stress in the circuit}} \quad (16)$$

The voltage stress across each power switch along with the maximum stress for 33-level MLI is represented in TABLE 4. The switches S_8, S_{11} and S_{12} are subjected to the lowest stress and lowest NVS which is V_{dc} and 7.69 %. Power switches S_4 and S_7 have double the lowest stress and NVS, which are $2V_{dc}$ and 15.38 %. But the power switches S_2, S_5 and S_6 have maximum stress of voltage with $13V_{dc}$ and $9V_{dc}$ with a NVS of 100 % and 69.23% respectively. Power switch S_9 have stress of $3V_{dc}$ and NVS of 23.07 %, which is greater than the minimal NVS. The stress on the switch S_3 is $4V_{dc}$ with a NVS of 30.76 %, which is less than the maximum NVS. The stress on switch S_{10} is $1.5V_{dc}$ with a NVS of 11.53%, which is under minimum NVS. The stress on the switch S_1 is $6.5V_{dc}$ with a NVS of 50%, which is half of the maximum NVS. The overall stress distribution of the circuit is represented in TABLE 5.

TABLE 5. Stress distribution of the proposed topology across power switches.

Stress distribution	Switches (N_{St})	Switches under stress % (N_{St}/N_S)	MBV (V_{dc})	MBV % (MBV/TSV)
Maximum Stress	S_2, S_5, S_6	25%	31	58.5%
Intermediate Stress	S_1, S_3, S_9	25%	13.5	25.47%
Minimum Stress	S_4, S_7, S_8, S_{10}, S_{11}, S_{12}	50%	8.5	16.03%

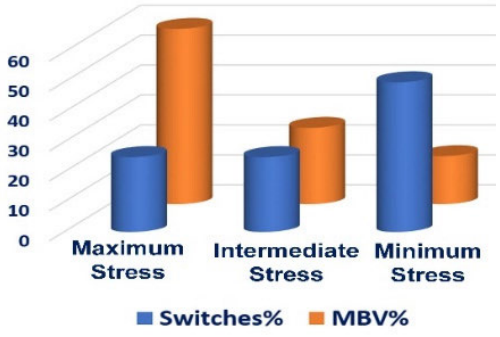

FIGURE 8. Overall stress distribution across the switches.

The four switches S_1, S_2, S_5, S_6 experience a stress of $31V_{dc}$, which is 58 % of the total stress distribution, while the remaining eight switches S_3, S_4, S_7, S_8, S_9, S_{10}, S_{11}, S_{12} experience a stress of $22V_{dc}$, which is 42 % of the total stress distribution in the proposed 33-level MLI structure. Although switch stress is unequally distributed in the developed structure, 50% of the switches experience minimum stress with an MBV of 16.03%, 25% of the switches experience maximum stress with an MBV of 58.5%, and the remaining 25% of the switches experience intermediate stress with an MBV of 25.47%. As a result, the suggested 33-level MLI provides effective sharing of stress among the power switches. Also the topology makes effective use of as many DC sources and switches as possible with lowering the TSV and cost of MLI. The graphical representation of stress distribution is shown in FIGURE 8.

Based on the stress distribution across the switches, it is found that eight switches experience less stress and hence these are selected with low voltage rating, the cost of the switches gets reduced. The remaining four switches experiences high stress, high rated switches are selected, the cost gets increased. Therefore variable rated switches are

operating in the circuit reduces the size, complexity and overall cost of the inverter.

B. COST FUNCTION

The cost function (CF) plays an important role in determining the best suited MLI based on the application. Several factors may be used to calculate the cost function, including the switches count N_S, the DC sources count N_{dc}, the diodes count N_D, the capacitors count N_C, gate drivers count N_{gd} and TSV. As a result, the cost factor is determined using the following equation (17) [28].

$$CF = (N_S + +N_{gd} + N_D + N_C + \alpha TSV_{PU}) \times N_{DC} \quad (17)$$

The weight coefficient α is always larger than 1 and less than unity. The cost factor is estimated in the developed 33-level MLI with the value of 0.5 (1) and 1.5 (>1) for the usual operating state. The following is the component level count (CF/L):

For $\alpha = 0.5$, CF/level $= (25.65 \times 4)/33 = 3.11$

For $\alpha = 1.5$, CF/level $= (28.96 \times 4)/33 = 3.51$

The cost function per level factor is compared with other modern existing topologies and found to be less compared with all topologies. Hence the proposed MLI is found to be cost-effective.

C. POWER LOSS CALCULATION

The power loss of the power electronic switches is the combination of conduction and switching losses. These are calculated based on the approach provided in [17] may be assessed for the developed topology. Conduction losses occurs when semiconductor devices conduct at the on-states owing to voltage drop. Conduction losses are calculated by multiplying the semiconductor device's $V_{on}(t)$ and I(t) during on-state. The calculations are calculated and represented in TABLE 6. The variation of efficiency with respect to the load is represented in FIGURE 9.

The total losses are made up of conduction and switching losses related to switches. Equation (18) may be used to determine the conduction losses for the switches.

$$P_{Cl} = \left[V_S + R_S i^{\beta}(t)\right] i(t) \quad (18)$$

The IGBT switch has a voltage drop of V_S, whereas diodes have a voltage drop of V_d. The equivalent resistance of a diode is R_d and R_S is the switch resistance. The following is a generalized relationship for estimating conduction power losses (P_{cl}) using the switces N_{IGBT} and diodes N_d at a specific time are calculated from equation (19).

$$P_{Cl} = \frac{1}{2\pi} \int_0^{2\pi} \left[N_{IGBT}(t)\, P_{cl,IGBT}(t)\, dt\right] \quad (19)$$

The switching losses are calculated from the equation (20).

$$P_{Sl} = f \sum_{K=1}^{N_{switch}} \left[\sum_{j=1}^{N_{on,k}} En_{on,kj} + \sum_{j=1}^{N_{off,k}} En_{off,kj}\right] \quad (20)$$

TABLE 6. Power loss and efficiency calculations.

Parameters	R-Load (100Ω)	R-Load (150Ω)	L-Load (187mH)
V_{rms} (V)	282.84	282.84	282.84
I_{rms} (A)	2.82	1.88	4.8
Conduction losses P_{cl} (W)	58.47	30.5	145.15
Switches turn on loss E_{on} (W)	0.21	0.14	0.37
Switches turn off loss E_{off} (W)	0.31	0.21	0.52
Switching losses P_{sl} (W)	0.52	0.35	0.89
Total losses P_{loss} (W)	58.9	30.85	146.04
Output power P_{out} (W)	797.6	531.7	1357.63
Input power P_{in} (W)	856.5	562.55	1503.67
Efficiency η (%)	94.1	95.2	90.3

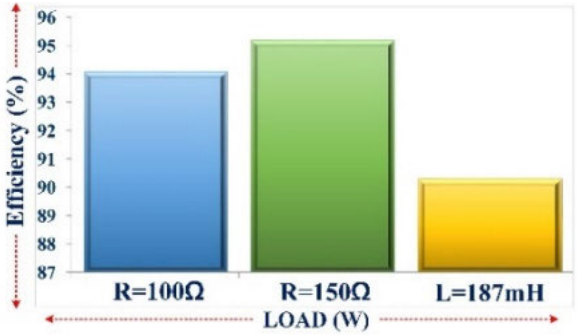

FIGURE 9. Efficiency of the proposed MLI for various loads.

The energy utilized by the switches is E_{on} and E_{off} during conduction and isolation of the switches respectively.

The following formula is used to calculate total power losses (P_{loss}):

$$P_{loss} = P_{cl} + P_{sl} \quad (21)$$

The following equation is used to compute the efficiency (η).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (22)$$

where the output and input powers are denoted by P_{out} and P_{in} respectively.

The following equation can be used to calculate power:

$$P_{out} = V_{rms} \times I_{rms} \quad (23)$$

IV. COMPARISON ANALYSIS AND APPLICATION

The proposed MLI is validated by comparing with other structures based on several key parameters such as the switches count (N_S), gate drivers (N_{gd}), DC sources (N_{dc}), diodes (N_D), capacitors (N_C), total standing voltage (TSV_{pu}), components count per level factor (CC/L), cost function per level count (CF/L), and the number of levels to switches ratio (N_L/N_S). Table 7 summarises the relevant comparisons, while FIGURE 11 represents the graphical representations of the respective comparisons. The proposed 33-level MLI is found to be efficient in all parameters and cost-effective when compared to other topologies. The following are the detailed comparisons. The DC sources count has a major impact on the

TABLE 7. Comparative analysis with existing topologies.

Topologies	N_L	N_S	N_L/N_S	N_{gd}	N_D	N_C	N_{dc}	CC/L	THD%	TSV_{PU}	C.F	
											α=0.5	α=1.5
[26]	33	18	1.83	18	-	-	8	1.33	-	5	9.33	10.54
[32]	33	21	1.57	21	32	16	1	2.75	-	-	-	-
[33]	33	18	1.83	18	18	6	1	1.84	-	-	-	-
[34]	33	14	2.35	14	8	-	5	1.24	6.17	4.37	5.78	6.44
[35]	33	14	2.35	14	2	-	7	1.12	2.06	5.87	6.9	8.23
[36]	33	16	2.06	16	-	-	7	1.18	5.9	6	7.42	8.69
[37]	33	24	1.37	15	-	-	9	1.45	4.54	9.62	11.94	14.57
[38]	33	22	1.5	15	-	-	9	1.39	-	9.5	11.38	13.97
[39]	33	18	1.83	18	18	-	8	1.87	-	5	13.69	14.9
[40]	35	12	2.9	12	2	2	5	0.94	2.2	5.52	4.39	5.18
[41]	31	16	1.93	12	-	-	6	1.2	-	6.33	6.03	7.25
[42]	31	20	1.65	20	-	-	8	2.06	3.26	7	15.39	17.09
[43]	31	14	2.21	14	-	-	4	1.03	3.35	5.86	4.0	4.74
[44]	33	15	2.2	15	-	-	7	1.12	-	3.76	6.76	7.56
[45]	33	14	2.35	12	-	-	5	0.93	-	4.70	4.29	5.00
[46]	33	14	2.35	14	6	-	7	1.24	-	4.14	7.65	8.52
Proposed	33	12	2.8	12	-	-	4	0.84	2.03	3.31	3.11	3.51

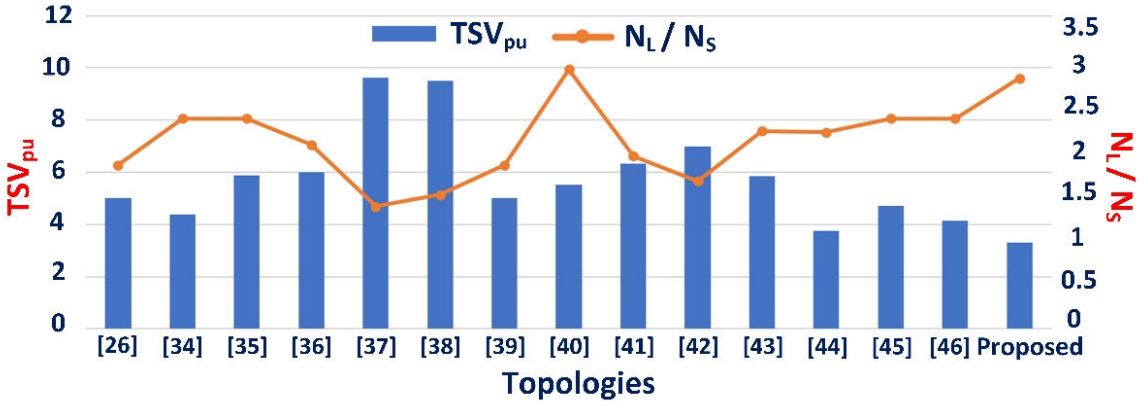

FIGURE 10. Comparison of TSV_{pu} Vs N_L/N_S.

topology application towards practical implementation. With higher DC sources, the cost of the circuit and voltage stress gets increased. TABLE 7 shows that topologies [31]–[33] have a single input source, but the overall component count is quite high due to the utilization of more number of capacitors as well as diode. The proposed architecture is shown to have fewer DC sources and total components, making it a viable choice for improved power quality. Table 7 shows the number of levels to switches (N_L/N_S) ratio, which is compared to all other topologies [27] and the graphical representation is shown in FIGURE 10. This ratio determines the topology's overall cost and efficiency. The higher the N_L/N_S ratio, the fewer switches are used, and the potential of generating greater voltage levels increases. As a result, higher output levels may be achieved with fewer switches. The proposed topology has a rating of 2.8, greater than other existing topologies. The developed topology is highly suited for renewable energy applications, based on the previous explanation.

TSV_{pu} plays a crucial role in calculating the inverter's total cost by estimating the rating of the IGBT switches concerning the stress across the switches. The higher the load on the switches, the higher the rating switches must be used, which increases the switches cost. Hence, the overall cost of the circuit gets increased. In the proposed topology, TSV is $53V_{dc}$ and TSV_{pu} is 3.31, which is less compared with all other existing topologies and hence the stress across the switches is less. The relative stress distributions among the switches are represented in FIGURE 7 and FIGURE 8. FIGURE 10 shows the graphical representation of the TSV_{pu} vs N_L/N_S ratio comparison. Based on the stress across switches, it can be inferred that the proposed topology provides high performance and is cost-effective.

The cost function of the MLI plays a vital role in obtaining the cost-effectiveness of the topology with a variation of weight coefficient α, the variation of the value of α is from 0.5 (<1) and 1.5 (>1). In the developed 33-level MLI, the cost function is 3.11 for $\alpha = 0.5$ and 3.51 for $\alpha = 1.5$, which

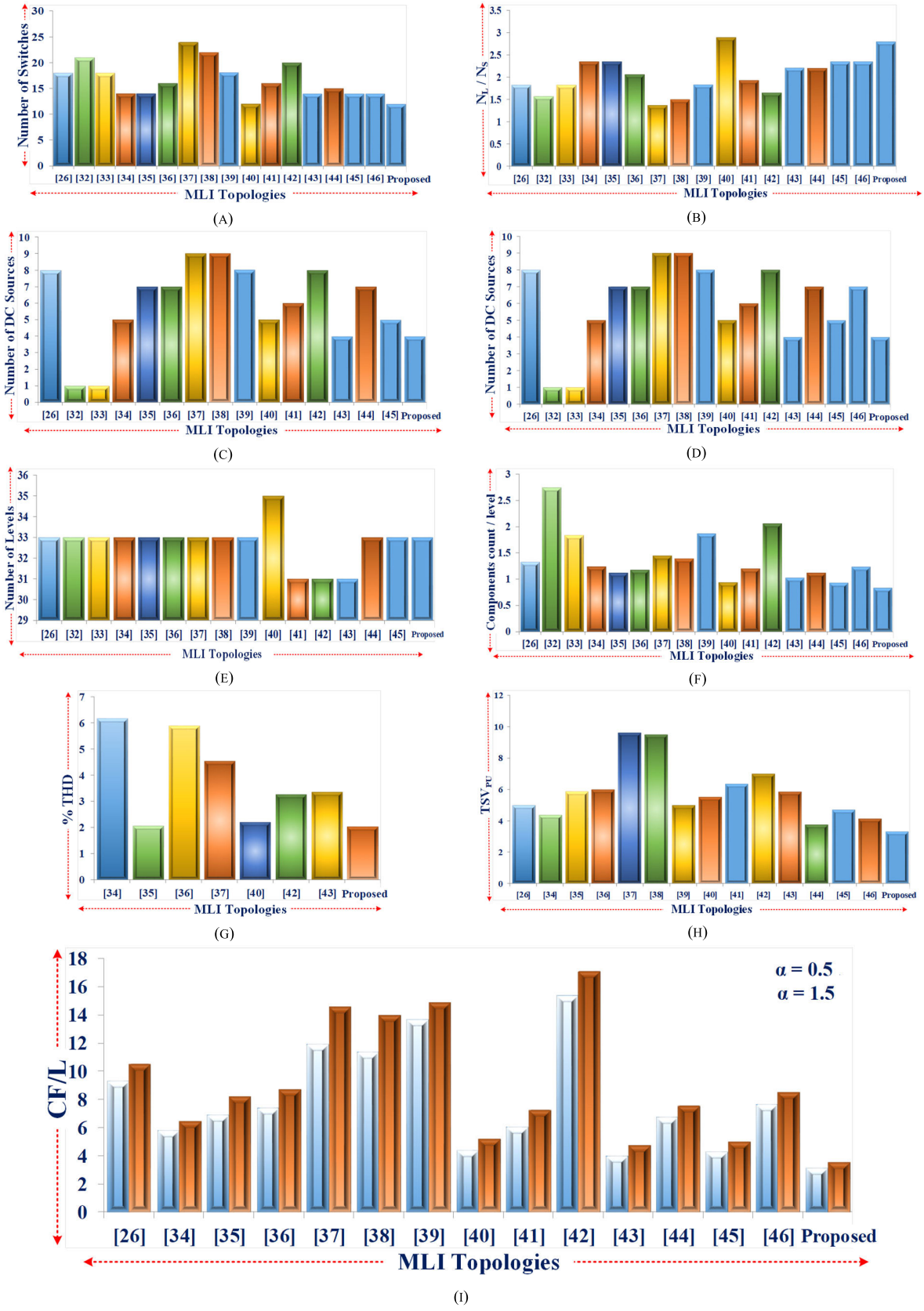

FIGURE 11. Comparison of various existing topologies with the proposed 33-level MLI. (a) N_S, (b) N_L/N_S, (c) N_{dc}, (d) N_{gd}, (e) N_L, (f) CC/L, (g) THD% (h) TSV_{PU}, (i) CF/.

is lesser compared with the other topologies and found to be cost-effective.

The topology in [40] has a competitive performance with the proposed MLI in several parameters like components count per level, THD, TSV and cost function. Even though the N_L/N_S value is higher than the proposed MLI, the overall components count factor is high, which is inferior to the proposed MLI and holds better results in all the parameters shown in Table 7. The topology in [43] has the cost function, which is nearer to the proposed MLI parameter with a TSV_{PU} of 5.86. The components count factor is having a nearer value but the THD and all other parameters hold inferior compared with the proposed MLI. The topology represented in [44] has very closer TSV_{PU} value but the overall performance parameters of the proposed MLI hold superior with less cost function. The topology represented in [45] has nearer components count factor but the overall performance of the proposed MLI holds superior. Hence the above mentioned topologies provides a competitive performance with the proposed MLI in some parameters but the overall performance parameters holds superior to that of the all topologies represented in TABLE 7. The graphical representation of the respective comparisons are represented in FIGURE 10 and FIGURE 11 for the easy identification of the performance of the proposed MLI.

According to the parametric comparisons above, the suggested MLI outperforms the modern existing topologies. Following comparisons show how the proposed inverter architecture reduces the number of required switches, TSV of the switches and driver circuits. These significant benefits might lead to the MLI topology's overall cost and installation area being reduced, making it cost-effective. FIGURE 11 represents the results of the various comparisons.

A. APPLICATION OF THE PROPOSED MLI

The proposed reduced switch count MLI is an alternative for the traditional MLIs in industrial requirements due to the wide range of operation with the modulation index. Individual PV panels with varied ratings are supplied into all four input sources of the proposed MLI, which correspond to the ratings of the DC sources [22]. In order to achieve this, some control objectives should be achieved such as the inverter must maintain optimum power quality in accordance with grid constraints, reduce harmonic distortions at the output ac voltage waveform, and extract maximum power from solar panels under various irradiance conditions in order to provide an efficient and stable output throughout its operation. Furthermore, the extracted power has been transferred to the output with a unity power factor in order to maintain reliability.

Because different solar panel ratings are used for different DC sources, an efficient maximum power extraction is used to harvest power under varying irradiance situations. In this aspect, the power factor control of the system plays a major role in transferring power from the solar panels to the grid, which is closer to a high power factor of 0.95. Reactive power consideration is not required in these systems because the inverter rating is low as per IEC 929-2000 and IEC 62109-2 standards. Furthermore, because the suggested MLI has a greater number of redundant switching states, it is more suitable for solar PV applications in terms of fault ride-through capability and power balance.

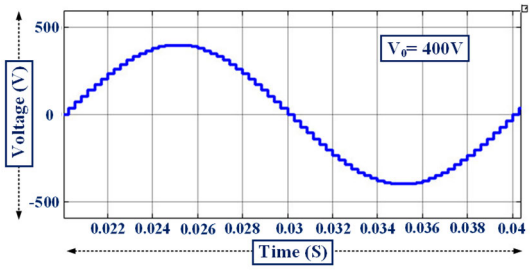

FIGURE 12. Simulation output voltage waveform of 33-level MLI.

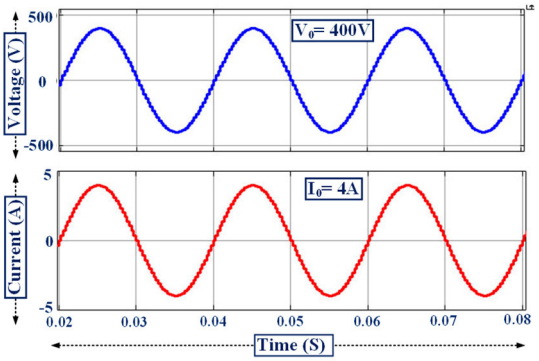

FIGURE 13. Simulation output voltage and current waveforms of 33-level MLI.

V. RESULTS AND DISCUSSION

The developed 33-level MLI is designed and implemented in a laboratory illustrated in FIGURE 22, is used to test the inverter's performance. For the developed MLI configuration, the input dc sources utilized are $V_1 = 25V$, $V_2 = 50V$, $V_3 = 100V$, $V_4 = 225V$. The results of the simulations are acquired utilizing MATLAB/Simulink, with the levels count and is achieved for the developed 33-level MLI along with the voltage and current output waveforms are represented in FIGURE 12 and FIGURE 13 respectively. The output voltage value and current values obtained are $V_0 = 400V$, and $I_0 = 4A$ respectively. The simulation THD accessed is 2.03% represented in FIGURE 14, which is less than IEEE standards. The parameters showing the simulation and experimental constraints of the MLI are given in TABLE 9. The variation of modulation index (M) with respect to the number of levels (N_L) is shown in TABLE 8 and the simulation output waveform of the modulation index for $M = 0.6$ consists of 21 levels, $M = 0.8$ with 27 levels and $M = 1$ with 33 levels are represented in FIGURE 15.

For the developed 33-level MLI, the simulation results are tested using a hardware prototype for verifying the results

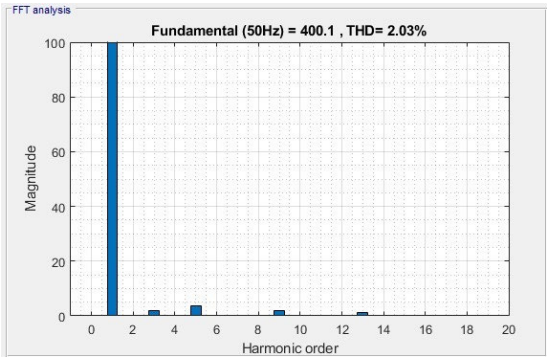

FIGURE 14. Simulation THD for the proposed 33-level MLI.

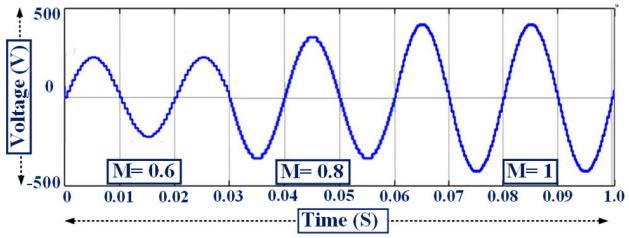

FIGURE 15. Simulation output of modulation index variation.

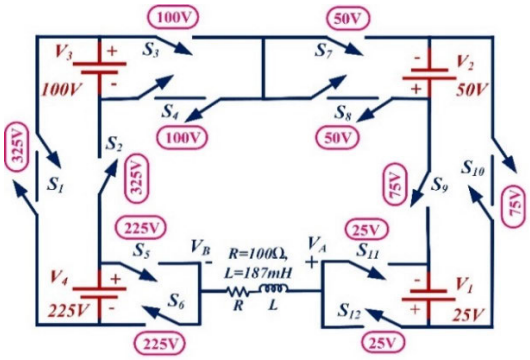

FIGURE 16. Experimental circuit of the proposed 33-level MLI.

TABLE 8. Variation of modulation index with levels of proposed MLI.

M	N_L	M	N_L
0.06	3	0.56	19
0.13	5	0.63	21
0.19	7	0.69	23
0.25	9	0.75	25
0.31	11	0.81	27
0.38	13	0.88	29
0.44	15	0.94	31
0.5	17	1.00	33

experimentally. The hardware prototype of the designed experimental circuit is illustrated in FIGURE 16 along with the entire setup is represented in FIGURE 22. The system consists of four CM75DU-12, 600V, 75A IGBTs with four input DC sources V_1, V_2, V_3, and V_4 that generates 33 levels and a 400V output voltage at 50Hz. Utilizing dSPACE

TABLE 9. Simulation and experimental parameters of the proposed MLI.

Programmable DC Sources	0-500V
IGBT	CM75DU-12H 600V, 75A
Load Resistance	100Ω, 150Ω
Switching frequency	5 kHz
Fundamental frequency	50Hz
Controller	dSPACE RTI 1104
Driver board	TLP-250
R-Load	100Ω & 150Ω
L-Load	187 mH
Motor Load	Single-phase, 230V, 0.5 HP

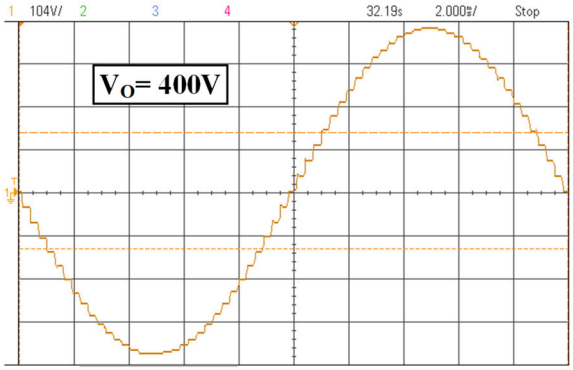

FIGURE 17. Experimental output voltage for proposed 33-level MLI.

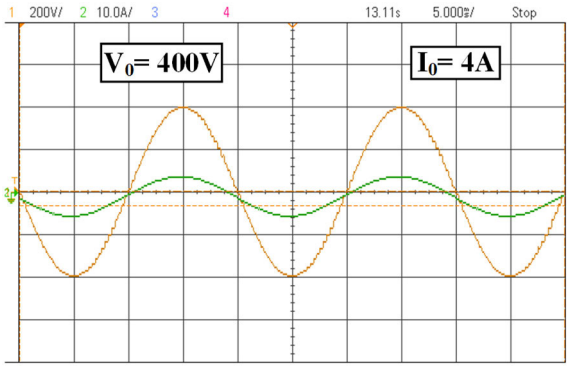

FIGURE 18. Experimental output voltage and current for R-Load.

RTI1104 board, the pulses are generated from the digital input and output ports to operate the IGBT switches. The gate driver in the range of 4 to 16V adds to the pulse width modulation design. The 15V pulse activates the power semiconductor switches. The experimental result of an output voltage is shown in FIGURE 17, which is $V_0 = 400$V, and FIGURE 18 represents the hardware results with the combination of output voltage $V_0 = 400$V and current $I_0 = 4$A for the resistive load with a load resistance of 100Ω. Experimental THD obtained is shown in FIGURE 23, which is 2.03%, similar to that of the simulation THD. The MLI is tested using a single phase motor load with an inductance L = 187mH produces the output voltage and current V_0 and I_0 of 400V and 6.8A respectively are shown in FIGURE 19.

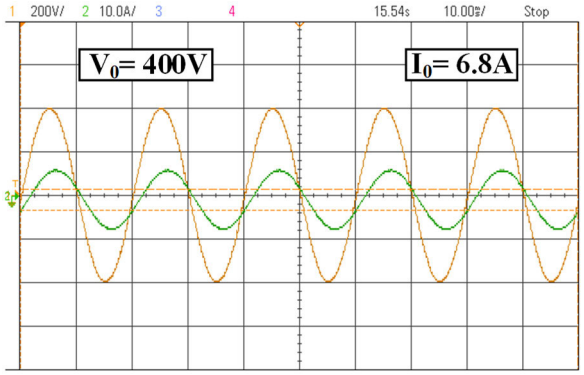

FIGURE 19. Experimental output voltage and current for L-load.

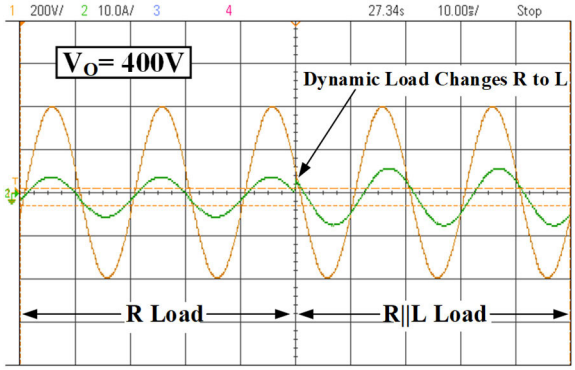

FIGURE 20. Experimental output voltage and current under dynamic load variations for R||L-load.

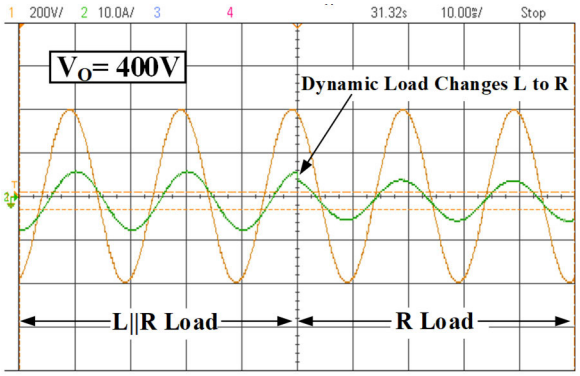

FIGURE 21. Experimental output voltage and current under dynamic load variations for L||R-load.

The proposed MLI is tested for dynamic loaded conditions with various combinations like R||L with L-load variation of R-load, the respective experimental results are obtained and represented below. The case when the inverter is loaded with R-load and suddenly an inductor is added in parallel to the existing R-load, the variation is represented in FIGURE 20 and it is found that the proposed MLI is stable with the load disturbances in throughout its operation. Also the case when the inverter is loaded with L||R load and suddenly the inductive load is removed, the respective variation is represented

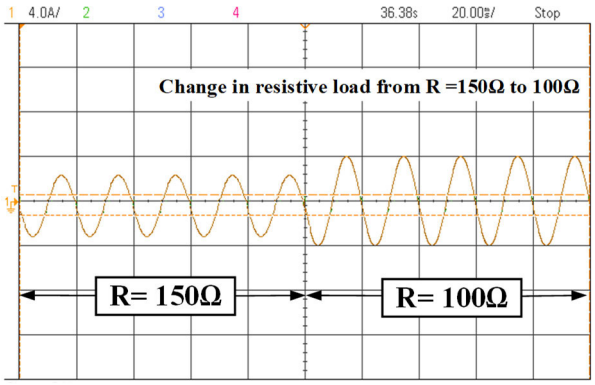

FIGURE 22. Experimental output current under variation of resistive load.

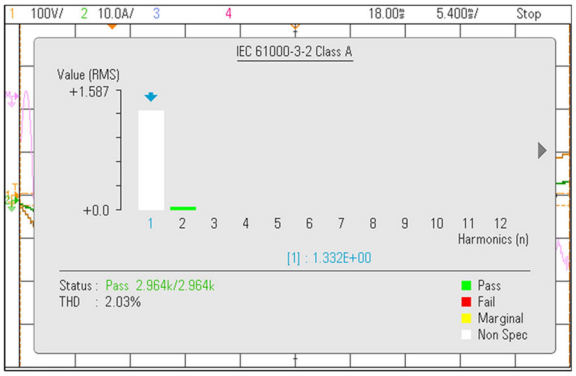

FIGURE 23. Experimental THD of the proposed 33-level MLI.

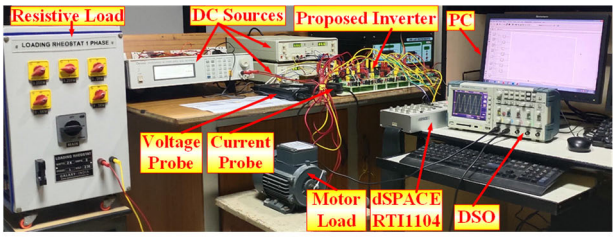

FIGURE 24. Experimental set up of the proposed 33-level MLI.

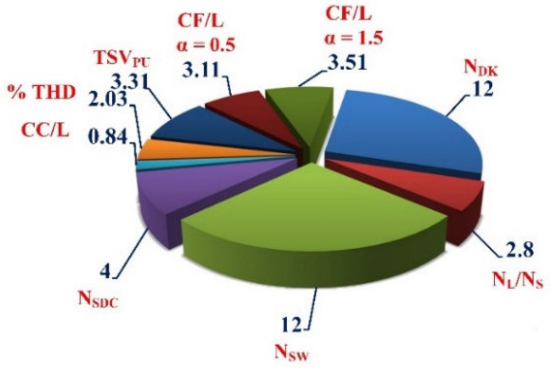

FIGURE 25. Outstanding features of the proposed 33-level MLI topology.

in FIGURE 21 and it is found that the proposed MLI is stable in the load disturbance for throughout its operation.

Also when the inverter is loaded with a resistive load of 150Ω and suddenly the load has been changed from 150Ω to 100Ω, the respective variation in the current is shown in FIGURE 22 experimentally. Hence based on the above observations, it is found that the load voltage remains constant under all loading conditions. The simulation and experimental specifications of the proposed MLI are given in TABLE 9. The outstanding features of the proposed MLI are represented in FIGURE 25.

VI. CONCLUSION

The proposed new asymmetrical MLI topology that can able to generate 33 voltage levels is implemented with reduced components and less TSV. A detailed stress distribution across the switches is analyzed with which the low voltage rated switches are selected, which decreases the cost and size of the inverter. An extended circuit is designed for higher output voltage levels. The developed MLI is compared with other existing MLI architectures considering several parameters for estimation of its performance and found to be superior. The MLI requires fewer power switches with less DC sources count for the generation of higher output levels. TSV_{PU} of the MLI is 3.31, only 25% of the switches are under maximum stress. Hence the cost of the inverter gets reduced. The comparisons represents that the proposed MLI has low TSV, cost-effective and efficient. As the unequal DC sources and low-rated switches are utilized in this topology, it is feasible for various hybrid energy storage and electric vehicle applications. For evaluating the performance of the MLI, it is tested for dynamically loaded conditions and found to be stable throughout its operation. Both simulation and experimental THD obtained is 2.03% with an efficiency of 95.2%, cost function α is 3.11 and 3.51 respectively, which is less when compared with other existing topologies. The proposed topology can be extended for the solar PV applications with various ratings of PV panels for the multiple inputs.

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