

Received December 14, 2021, accepted December 27, 2021, date of publication December 31, 2021, date of current version January 12, 2022.

Digital Object Identifier 10.1109/ACCESS.2021.3139948

Optimization of Impedance-Source Galvanically Isolated DC–DC Converters With Reduced Number of Switches

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This work was supported by the Development of Modular Green Substation and Operation Technology of Korea Electric Power Corporation (KEPCO).

ABSTRACT In this study, a new type of Z-source converter comprising galvanic isolation transformers is introduced based on classical non-isolated Z-source converters, which are promising devices for renewable applications. Compared to the typology of conventional converters with isolation transformers, the proposed converter topology has a simpler structure with fewer power switches and lower costs. Considering the lower number of switching devices required in the proposed typology, these efficiency and reliability of the presented converters are higher than those of the conventional ones. As only one switch is used in the developed structure, voltage stresses on the Z-source converter decreases in each period, which maintains voltage stress low and steady across the switch. Another desirable feature of the proposed topology is reduced converter size and volume with a maximum theoretical and practical efficiency of 97 to 94.05%, respectively. Moreover, these converters need low input voltage and provide the required amount of output voltage in small duty cycles. The theoretical and operational analysis of the designed converter and its comparison with other counterpart converters (e.g., isolated Z-source converters) is presented. The simulation and experimental results confirm the applicability of the proposed system.

INDEX TERMS Galvanic isolation transformer, DC-DC power converter, Z-source network, simulation analysis, reduced switches.

I. INTRODUCTION

Because of the ever-growing demand for renewable energy resources, such as photovoltaic systems, wind turbines, and fuel cells, considerable attention has been directed to such resources. Therefore, the need for high voltage (HV) DC-DC power supplies is now highly tangible. In general, conventional DC-DC topologies are categorized into with and without transformer topologies. Although the technology of these typologies has been widely investigated and recognized, they have a fairly large size, impose high costs, and yield low efficiency owing to their single structure in complex

applications [1], [2]. To eliminate these problems and boost their efficiency, DC-DC converters with HV gains should be utilized [3]; therefore, Z-source (ZS) networks have been considered.

The concept of ZS networks was first introduced by Peng in 2003 [4]. This network refers to a one-stage increment/decrement converter that has the potential to augment voltage through a capacitive inductive impedance network located between the source and the inverter. In this converter, no additional DC-DC solvents are required. In addition, as voltage sources are not allowed for use in this type of inverter, short-circuit intervals are placed in the legs of the inverter for voltage increment. Because short circuit intervals are permitted to be used in the legs of the converter as part of the

The associate editor coordinating the review of this manuscript and approving it for publication was Vitor Monteiro.

power conversion process, this converter is not sensitive to noise switching. Furthermore, among the advantages of ZS networks are one-step conversion, low number of components, high efficiency, low energy loss, high reliability, and low costs [5]. Provided the characteristics of ZS networks, it has widely been simulated in converters with transformers in modern power systems, such as HVDC networks, smart networks, photovoltaic power plants, wind power plants, and electric vehicle batteries. In these simulations, transformers may be integrated into isolated DC-DC power converters [6]. Therefore, an appropriate power converter is required to connect DC microgrid systems with loads [7] so that a relatively high voltage can be generated using the DC-DC converter [8], as illustrated in Fig. 1.

By locating ZS networks in converters with isolation transformers, achieving higher performance is feasible in approximately all types of energy conversion, including AC-AC, DC-DC, AC-DC, and DC-AC. Among them, DC-AC energy conversion, and thus the topology of DC-AC converters has garnered a considerable attention. Moreover, ZS-based converters have several drawbacks, such as discontinuous input current, limited boost factor $1/(1-2D)$, where D represents the duty cycle in a short circuit [9]. In addition, D must be increased to achieve an HV gain; however, it causes HV tensions in network components [10]. Therefore, a variety of topologies for ZS-based DC-DC converters have been proposed using magnetic connection methods (e.g., methods that use transformers) to eliminate this problem, optimize voltage gain, and reduce voltage stress [11].

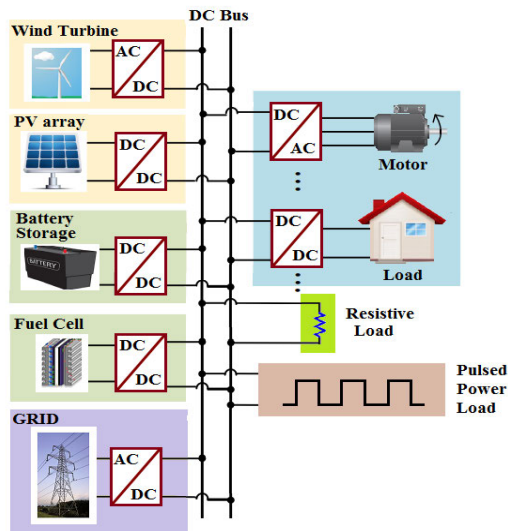


FIGURE 1. Typical architecture of independent and integrated DC microgrids.

The current study primarily concentrates on ZS-based DC-DC converters with isolation transformers. These converters are capable of enhancing voltage gain by adjusting the turn ratio of transformers [12], and have higher reliability and safety compared to non-isolated converters [13].

However, the switches in these converters might undergo intense voltage pressures owing to the leakage inductance of transformers [14]. To overcome this problem, a resistive capacitive diode is required [15]; nonetheless, it boosts power loss and declines efficiency. Another solution is to utilize active-clamp circuits [16], which eliminates voltage spike without increasing power loss. However, another power switch is required, which imposes higher costs and enhances control complexity. Moreover, the use of high-frequency transformers with complicated configurations in isolated DC-DC converters increases the costs, size, and weight of the converters [14], [15], [17], [18].

Another less-recognized method to solve the problems associated with the use of converters with isolation transformers is to reduce the number of active and inactive components of these converters. Hence, the size, weight, and related costs decrease. It is also possible to highly benefit from the desirable characteristics of isolation transformers. Furthermore, unnecessary active elements, such as insulated gate bipolar transistor (IGBT) or metal-oxide-semiconductor field-effect transistor (MOSFET) with high power and frequency require the addition of heat-sink and drive circuits, which promotes the control complexity of these converters [19].

This study introduces an optimized structure for Z-source DC-DC converters based on galvanically isolation transformers with a reduced number of switches and diodes as an alternative to conventional isolated Z-source DC-DC converters. In the proposed topology, by reducing voltage stress on the elements of the Z-source network, a fewer number of constituents (e.g., switches and diodes) are needed, voltage tension on active elements decreases, and using double-winding isolation transformers becomes feasible. Therefore, the proposed converter exhibits a high efficiency concerning its expenses, size, and weight. The simulation analysis is conducted using the MATLAB software and several experiments are performed to evaluate the characteristics of the proposed converter.

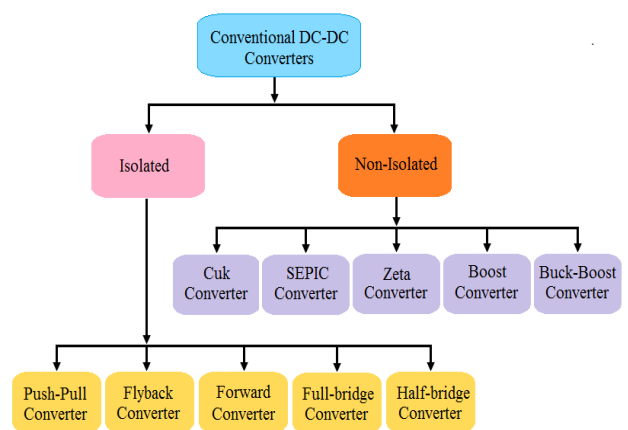


FIGURE 2. Classification of conventional isolated and non-isolated DC-DC converters.

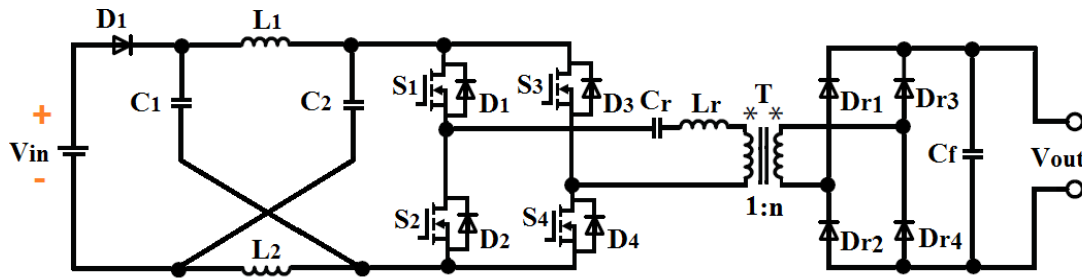


FIGURE 3. Conventional isolated DC-DC converter based on Z-source.

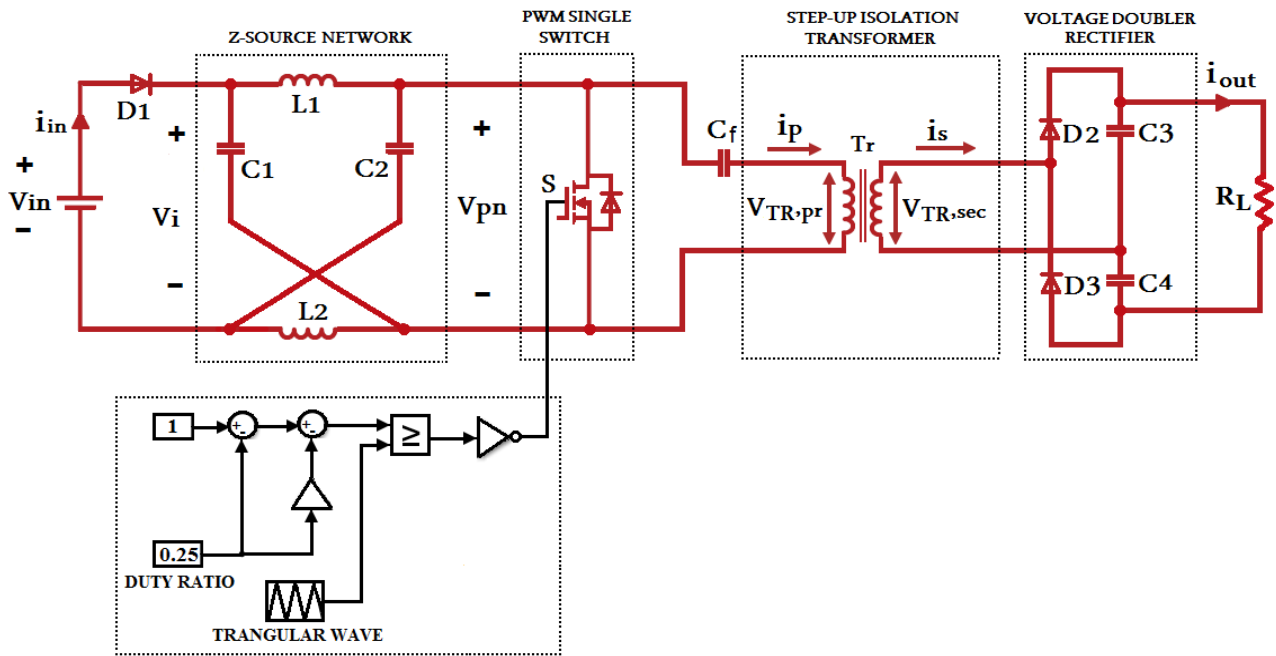


FIGURE 4. Proposed isolated DC-DC converter based on the Z-source network.

Photovoltaic panels, fuel cells, and wind turbines on a small scale (20 to 150 V) should be adjusted by dc-dc converters in order for their low voltage to reach higher dc-link voltage (between 200 and 600 V) [20]. The proposed impedance-source isolated dc-dc converter with an output voltage of 206 V is located in the range of 200 to 600 V before being connected to the network of 110, 230, and 400 V AC [21], [22]. Therefore, the proposed converter is a promising device for photovoltaic panels, fuel cells, and wind turbines.

II. CONVENTIONAL DC-DC CONVERTERS WITH ISOLATION TRANSFORMERS

Conventional DC-DC converters are mainly divided into non-isolated and isolated types, as illustrated in Fig. 2. Non-isolated typologies include Boost-Buck, Boost, Cuk, Zeta, and SEPIC types. Among isolated typologies are forward, flyback, push-pull, full-bridge, and half-bridge circuits. To connect renewable systems to the power grid with a low

input voltage, one of the most promising options is to use DC-DC converters with isolation transformers and a DC bus at the high voltage side [23]–[26]. However, owing to their single, they have large sizes, impose elevated costs, and reduce efficiency structure in complex applications.

III. PROPOSED TOPOLOGY AND ITS OPERATING PRINCIPLES

Wang et al, presented isolated DC-DC converters based on Z-source networks for use in renewable energy systems [19]. Fig. 3 illustrates that the structure of these converters is comprised of four main parts: 1) z-source impedance network, 2) single-phase full-bridge inverter, 3) step-up isolation transformer, and 4) single-phase voltage doubler rectifier (VDR). These converters consist of many switches in their structure, which occupy a large system space, increase converter weight, and consequently boost costs. In addition, the switches undergo an intense pressure of HV because of the leakage inductance of transformers. Therefore, all switches

exhibit significant energy losses, and thus the quality of output power decreases on the primary side of the transformer. Using many switches at high power and frequency also necessitates the addition of heat-sink and drive circuits, which increases the control complexity of these converters. Consequently, some measures have been offered in the present study to eliminate these problems.

The proposed Z-source converter consists of a unique impedance network and a galvanically isolation transformer, as depicted in Fig. 4. It contains a Z-source network comprising inductors (L_1, L_2), capacitors (C_1, C_2), and diodes (D_1), a power switch (S), a galvanically isolation transformer (T), VDRs consisting of diodes D_2 and D_3 , capacitors C_3, C_4 , and C_f , and a blocking capacitor in series with the primary winding of the transformer. The blocking capacitor is required to isolate the DC component from the input voltage of the transformer so as to hinder its saturation.

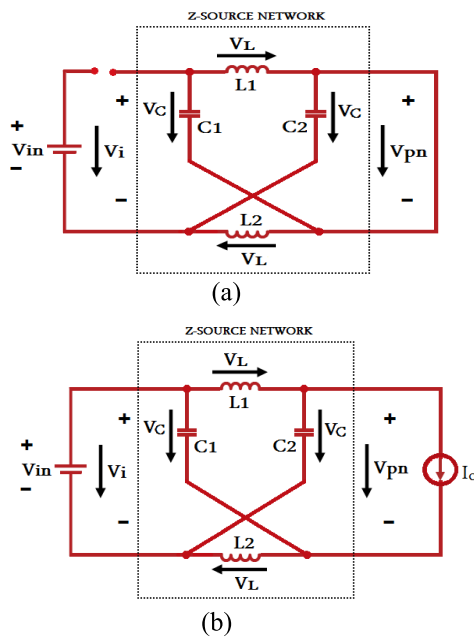


FIGURE 5. Equivalent circuits of the Z-source DC-DC converter in the (a) shoot-through transfer mode, and (b) non-shoot-through transfer mode.

The Z-source converter alters voltage by switching the power switch (S). To change voltage, the converter directs it toward the isolation transformer, and ultimately, the required DC voltage is obtained via VDR modifications. Moreover, D_1 is used to prevent the discharge of the capacitor onto the DC source. Therefore, the presence of this diode in series with the DC source causes discontinuities in the source current.

A. OPERATING PRINCIPLES OF THE PROPOSED CIRCUIT

In terms of the structure of the proposed converter, if the impedance network is symmetrical, we can write:

$$L1 = L2 = L, C1 = C2 = C, \quad (1)$$

$$v_{L1} = v_{L2} = v_L, v_{C1} = v_{C2} = V_C, \quad (2)$$

where V_C and V_L represent the average voltage value at both ends of capacitors and instantaneous voltage value on both sides of inductors, respectively.

Siwakoti et al. discussed that the impedance source converter has the shoot-through transfer and non-shoot-through transfer operating modes [10]. Fig. 5 indicates the equivalent circuits of the Z-source converter.

Considering Equations (1) and (2) and Fig. 5(a), the following relationships are obtained:

$$v_{L,sh} = V_C. \quad (3)$$

$$v_{i,sh} = 2V_C. \quad (4)$$

$$v_{pn,sh} = 0, \quad (5)$$

where v_i and v_{pn} represent the input and output voltages of impedance sources, respectively.

According to Equations (1) and (2) and Fig. 5(b), the relationships can be expressed as follows:

$$v_{L,nsh} = V_{in} - V_C, \quad (6)$$

$$v_{i,nsh} = V_{in}, \quad (7)$$

$$v_{pn,nsh} = V_C - V_L = 2V_C - V_{in}. \quad (8)$$

In a stable system, the average voltage of the two ends of an inductor in one switching period ($T_{sw} = T_{sh} + T_{nsh}$) is equal to zero based on the principle of voltage balance, the following equation is formed:

$$v_{L,av} = \int_0^{T_{sh}} v_L dt + \int_0^{T_{nsh}} v_L dt = 0, \quad (9)$$

where $v_{L,av}$ represents the average voltage value at both ends of the inductor. To calculate the second integral in Equation (9), a new time origin is considered. By substituting the values of v_L from Equations (4) and (7) into Equation (9), the result can be expressed as follows

$$v_L = \bar{v}_L = \frac{T_{sh}(V_C) + T_{nsh}(V_{in} - V_C)}{T_{sw}} = 0. \quad (10)$$

Based on Equations (5) and (8), the average value of the DC-link voltage between the power switches (S) (i.e., $v_{pn,av}$) can be computed a

$$\begin{aligned} v_{pn,av} &= \frac{(T_{sh} \times 0) + T_{nsh}(2V_C - V_{in})}{T} \\ &= \frac{T_{nsh}}{T_{nsh} - T_{sh}} V_{in} = \frac{1 - D}{1 - 2D} V_{in}. \end{aligned} \quad (11)$$

Using Equation (11), the peak output voltage of the Z-source impedance can be expressed as follows

$$\begin{aligned} v_{pn,max} &= V_C - v_L = 2V_C - V_{in} \\ &= \frac{T_{sw}}{T_{nsh} - T_{sh}} V_{in} = BV_{in}. \end{aligned} \quad (12)$$

where, B is the boost factor induced by the shoot-through mode and is greater than or equal to 1 ($B \geq 1$), therefore

$$B = \frac{T_{sw}}{T_{nsh} - T_{sh}} = \frac{1}{1 - 2(\frac{T_{sh}}{T_{sw}})} = \frac{1}{1 - 2D} \geq 1, \quad (13)$$

where D represents the shoot-through duty cycle, which satisfies $0 \leq D \leq 0.5$. The shoot-through duty cycle is equal to $\frac{T_{sh}}{T_{sw}}$.

From Equation (13), shoot-through duty cycle can be measured as follows:

$$D = (B - 1)/2B, \tag{14}$$

The converter performance highly depends on the voltage of the capacitor in the Z-source network. From Equations (2) and (13), the average voltage at both ends of the capacitor (VC) is obtained as follows:

$$V_{C1} = V_{C2} = V_C = \left(\frac{1 - \frac{T_{sh}}{T_{sw}}}{1 - \frac{2T_{sh}}{T_{sw}}} \right) V_{in} = \frac{1 - D}{1 - 2D} V_{in}. \tag{15}$$

By substituting Equations (13) and (14) into Equation (15), the voltage of the capacitor in the Z-source network is computed as follows:

$$V_C = \frac{B + 1}{2B} B V_{in} = \frac{B + 1}{2} V_{in}. \tag{16}$$

As illustrated in Fig. 7, the boost factor can be controlled by straight lines as follows:

$$\tan a_1 = \frac{V_{Ca} - V_p}{\frac{T_{sh}}{4}}, \tag{17}$$

$$\tan a_2 = \frac{V_{Ca}}{\frac{T_{sw}}{4}}, \tag{18}$$

where V_{Ca} is the peak value of the triangular carrier signal.

Therefore, as angles a_1 and a_2 are equal, D can be estimated as follows

$$\frac{T_{sh}}{T_{sw}} = \frac{V_{Ca} - V_p}{V_{Ca}} = D. \tag{19}$$

By substituting Equation (19) into Equation (13), the boost factor can be calculated as follows

$$B = \frac{1}{1 - 2 \left(\frac{V_{Ca} - V_p}{V_{Ca}} \right)} = \frac{V_{Ca}}{2V_p - V_{Ca}}. \tag{20}$$

Based on Equations (19) and (20), if V_{Ca} is constant and V_p increases, D and B reduce. According to Equation (15), V_C decreases under these conditions.

Capacitor voltage functions as a voltage stress on the capacitor and can be estimated using Equations (16) and (20) using.

$$S_C = V_C = \frac{V_p}{2V_p - V_{Ca}} V_{in}. \tag{21}$$

Therefore, V_p cannot be less than $\frac{V_{Ca}}{2}$. If $V_p = \frac{V_{Ca}}{2}$, V_C approaches infinity, which indicates the HV stress on the capacitors of the impedance network

Ellabban et al, proved that the DC voltage is a discontinuous unipolar pulse [27]. Hence, the DC voltage, as the input voltage on the primary side of the transformer, can alter the input voltage because $n = N_{tp}/N_{ts}$. In addition, the output

voltage of VDR can gain the required DC voltage on the secondary side of the transformer:

$$V_{C3} = V_{C4} = nV_C = \frac{n(1 - D)}{1 - 2D} V_{in}. \tag{22}$$

From Equations (11) and (22), we can write

$$V_{out} = \frac{n}{1 - 2D} V_{in}. \tag{23}$$

Therefore, the DC voltage gain is calculated as follows

$$G = \frac{n}{1 - 2D}. \tag{24}$$

If the capacitors and inductors of the impedance network are appropriately determined, the proposed converter can function effectively in a wide range of voltages and loads despite discontinuous input voltage [28]. Compared to conventional Z-source DC-DC converters, the proposed converter elevates output DC voltage as the number of active elements are reduced. Furthermore, the secondary winding of the isolation transformer should have two more rotations to maintain the DC voltage gain. Therefore, the introduced converter achieves higher efficiency, simpler operation, and lower cost than those of the conventional Z-source converters.

Operating principle of the proposed structure described in Fig. 6 contains two switch modes that occur during the switching period (T)

First mode [$t_1; t_2$]: S is on and D_1 is off. Capacitors (C_1, C_2) are discharged and inductors (L_1, L_2) start being charged. Therefore, D_3 conducts the current, and D_2 is reverse biased. In addition, C_4 is charged, whereas C_3 discharges load current.

Second mode [$t_2; t_3$]: S is off and D_1 is on. Under this condition, capacitors (C_1, C_2) are charged, and inductors (L_1, L_2) start being discharged. Thus, D_2 conducts the current and D_3 is reverse biased. In addition, C_3 is charged, whereas C_4 discharges load current.

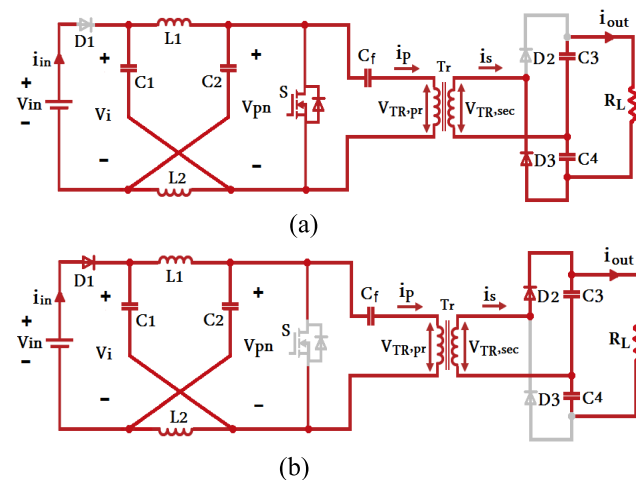


FIGURE 6. Equivalent circuits of the proposed topology for its main operation modes: (a) shoot-through, and (b) non-shoot-through.

B. CONTROL STRATEGY OF THE PULSE WIDTH MODULATION (PWM)

The performance of isolated Z-source converters can be controlled using various schemes of PWM, including simple boost, maximum boost, and constant boost controls [4], [5]. In this study, the simple control boost scheme is employed as a control strategy. The simple boost control scheme for the proposed converter involves the comparison of a triangular wave signal with an adjustable DC reference, called V_p . Consequently, duty cycle of the switching pulse can be changed to fabricate the required and desirable converter. Fig. 7 shows the control strategy of the proposed structure. These results show that despite the discontinuous input current, I_{L1} and I_{L2} operate in the continuous conduction mode (CCM).

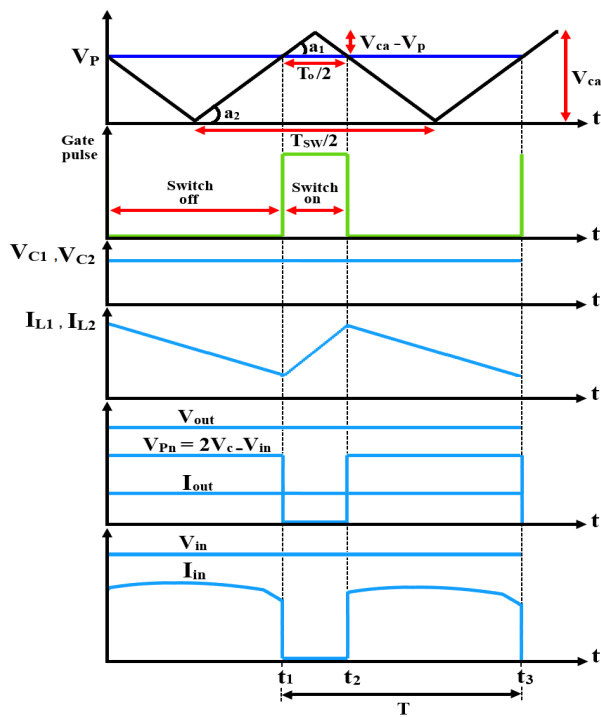


FIGURE 7. PWM switching scheme for simple boost control of the proposed converter.

IV. DESIGN OF IMPEDANCE NETWORK CAPACITORS AND INDUCTORS

A. INDUCTOR

To determine the values of inductances, induction capacity should be relatively small. If induction capacity is large, power and system losses increase, which leads to the discontinuity of alternating current and increases the complexity of the control system. Furthermore, a moderately small induction capacity prevents inductor current ripple [14].

During the short circuit, the inductors are charged by the capacitor; thus, inductor current ripple can be determined as follows:

$$\Delta i_L = \frac{T_{sh} V_C}{L} = \frac{DT_{sw} V_C}{L} \tag{25}$$

From Equations (14), (16), and (25), the following equation is achieved:

$$\Delta i_L = \frac{B^2 - 1}{4B} \frac{T_{sw} V_{in}}{L} \tag{26}$$

Therefore, Δi_L increases with an increasing T_{sw} or V_{in} ; however, it decreases with an increasing L . If $B = 1$ or $D = 0$, then $\Delta i_L = 0$. By substituting Equation (20) into Equation (26), inductor current ripple is calculated as follows:

$$\Delta i_L = \frac{V_{Ca} V_p - V_p^2}{V_{Ca}(2V_p - V_{Ca})} \frac{T_{sw} V_{in}}{L} \tag{27}$$

Equation (27) indicates that variations in V_p have a significant effect on Δi_L . Therefore, if $V_p = \frac{V_{Ca}}{2}$ or $D = 0.5$, Δi_L approaches infinity.

B. CAPACITOR

During the short circuit mode, capacitors are discharged. Thus, capacitor voltage ripple can be computed as follows

$$\Delta V_C = \frac{T_{sh} I_L}{C} = \frac{DT_{sw} I_L}{C} \tag{28}$$

$$I_L = \frac{1 - D}{1 - 2D} I_l \tag{29}$$

$$I_l = \frac{V_C}{R_l} \tag{30}$$

where I_L and I_l are the average inductor and load currents, respectively.

Considering equations (28), (29), and (30), the following equation can be established:

$$\Delta V_C = \frac{D(1 - D)}{1 - 2D} \frac{T_{sw} I_L}{C} = \frac{D(1 - D)}{1 - 2D} \frac{T_{sw} V_C}{CR_l} \tag{31}$$

Substituting Equation (15) into Equation (31) results in the following relationship

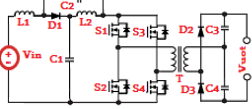
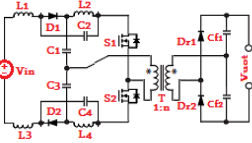
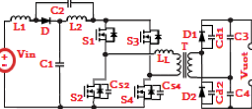
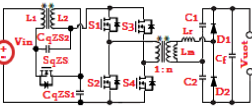
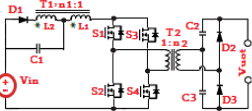
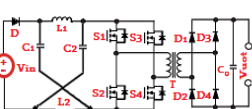
$$\begin{aligned} \Delta V_C &= D \left(\frac{1 - D}{1 - 2D} \right)^2 \frac{T_{sw} V_{in}}{CR_l} \\ &= \frac{(B + 1)(B^2 - 1)}{8B} \frac{T_{sw} V_{in}}{CR_l} \end{aligned} \tag{32}$$

Equation (32) suggests that ΔV_C increases by an increase in T_{sw} or V_{in} . Additionally, if $B = 1$ or $D = 0$, $\Delta V_C = 0$. By substituting Equation (20) into Equation (32), capacitor voltage ripple can be estimated as follows:

$$\Delta V_C = \frac{V_p(V_{Ca} V_p - V_p^2)}{V_{Ca}(2V_p - V_{Ca})^2} \frac{T_{sw} V_{in}}{CR_l} \tag{33}$$

Based on Equation (33), changes in V_p substantially influence ΔV_C ; thus, if $V_p = \frac{V_{Ca}}{2}$ or $D = 0.5$, ΔV_C approaches infinity.

TABLE 1. Comparison of the proposed galvanically isolated Z-source DC-DC converter with other similar converters.

Ref	Circuit structure	DC voltage gain	Duty cycle range	No. of SC*		No. of MC*			No. of C*	NP*, W	FLE*, (%)	Advantages(+)and disadvantages(-)
				D*	S*	L*	CL*	TR*				
[29]		$\frac{2 \cdot n}{(1-2 \cdot D)}$	$0 < D < 0.75$	3	4	2	0	1	4	250	95	+ continuous input current - relatively high number of PCs*
[30]		$\frac{n}{(1-2 \cdot D)}$	$0 < D < 0.75$	4	2	4	0	1	6	300	92	+ double input possibility + low number of switches + continuous input current - high number of passive components - high voltage stress of switches
[31]		$\frac{2 \cdot n}{(1-2 \cdot D)}$	$0 < D < 0.5$	3	4	2	0	1	8	100	95	+ continuous input current - high number of passive components - high voltage stress of switches
[32]		$\frac{1}{(1-2 \cdot D)}$	$0 < D < 0.5$	2	5	4	0	1	5	300	97.4	+ magnetically integrated ISN + continuous input current - high voltage stress of switches - high number of components
[33]		$\frac{2 \cdot n}{(1-(1+m) \cdot D)}$	$0 < D < 0.5 + \frac{1}{2 \cdot (1+m)}$	3	4	0	1	1	3	500	93	+ high voltage step-up at the input stage + low number of passive components - high voltage stress of switches - discontinuous input current
[34]		$\frac{n \cdot (1-d)}{(1-2 \cdot D)}$	$0 < D < 0.5$	5	4	2	0	1	3	500	96	- discontinuous input current - limited performance due to LC filter
Proposed topology	Fig. 4	$\frac{n}{(1-2 \cdot D)}$	$0 < D < 0.5$	3	1	2	0	1	4	206	94.05	+ single switch + high power density - discontinuous input current

SC*: semiconductor component, MC*: magnetic component, D*: diode, S*: switch, L*: inductor, LC*: coupled inductor, TR*: transformer, C*: capacitor, PC*: passive component, NP*: Nominal Power, FLE*: Full Load Efficiency.

V. A COMPARISON BETWEEN THE PERFORMANCE AND STRUCTURE OF THE PROPOSED AND SIMILAR CONVERTERS

Table. 1 summarizes the main topologies of the galvanically isolated Z-source DC-DC converters. In addition to the converter introduced in [19], six other converters with improved structures are compared with the introduced converter in terms of the number of passive and semi-conductive components and maximum duty cycle of switches. The advantages and disadvantages of each converter is listed in Table.1. Many studies have focused on increasing DC voltage in the boost mode and neglected reducing passive and active elements. Therefore, the proposed topology has not only high output DC voltage but also the least number of active components in comparison with the those of the other converters.

VI. SIMULATION AND EXPERIMENTAL RESULTS

Performance of the designed converter is evaluated through simulations in MATLAB/SIMULINK and testing the built prototype. The ideal methods of non-active components (inductors, capacitors, and an isolation transformer) are utilized to simplify the analysis. The simulation parameters of the proposed device and the specifications of the semiconductor components are presented in Tables. 2 and 3, respectively.

A. SIMULATION RESULTS

Conventional isolated Z-source DC-DC converters with four MOSFET switches, require a spacious system space, have high weights, and thus impose substantial costs. On the contrary, the proposed converter with only one MOSFET switch not only has the benefits of conventional isolated Z-source DC-DC converters but also decreases costs and

TABLE 2. Simulation parameters of the proposed Z-source DC-DC converter.

Parameter	Symbol	Value
Input voltage range, V	V_{in}	50
Maximum input current, A	I_{in}	6.5
Output voltage, V	V_{out}	206
DC-Link voltage, V	I_{out}	107
Duty cycle	D	0.25
Capacitance of ZS capacitors, μF	C_1, C_2	450
Inductance of ZS inductors, μH	L_1, L_2	50
Capacitance of output capacitors, μF	C_3, C_4	51
Converter power rating, W	P	206
Switching frequency, kHz	f_{sw}	100
Transformer turns ratio	n	2
Resistive load, Ω	R	200

TABLE 3. Electrical specifications of the semiconductor components used in simulation and experiments.

Component	Type	Specifications
S	Infineon SPP20N60C3	$V_{DS} = 600 V$; $R_{DS(on)} = 190 m\Omega$ $I_D = 20.7 A$, $Q_g = 87 nC$, $R_g = 2.5 \Omega$
D_1	Vishay V60D100C	$V_{RRM} = 100 V$; $V_F = 0.66 V$ $I_{F(AV)} = 2 \times 30 A$ (common cathode)
D_2, D_3	CREE C3D02060E	$V_{RRM} = 600 V$; $V_F = 1.8 V$ $I_{F(AV)} = 4 A$

required space and weight. Furthermore, reducing the number of switching devices enhances the efficiency and reliability of the converter [29].

The simulation results in Figs. 8(a) and (b) show that the voltage and input current of the suggested Z-source DC-DC converter are $V_{in} = 50 V$ and $I_{in} = 6.5 A$, respectively, with a duty cycle of 0.25 ($D = 0.25$), which generates an output voltage of 206 V ($V_o = 206 V$) and an output current of 1 A ($I_o = 1 A$). The waveforms of output voltage and current are displayed in Figs. 8(c) and (d). The capacitors of VDR are charged asymmetrically as predicted analytically. The simulated current of inductors and voltage of capacitors in the Z-source network are $I_{L1} = I_{L2} = 6.5 A$ and $V_{C1} = V_{C2} = 73V$, which are illustrated in Figs. 9(a)–(d), respectively.

Fig. 10(a) exhibits a maximum voltage of 107 V on the DC-link (V_{pn}). A magnified view of DC-link voltage is depicted in Fig. 10(b). Moreover, the highest voltage stress (reverse-bias voltage) of diode D_1 is -107 V, as indicated in Fig. 10(c). Similarly, Figs. 10(d–e) depict the voltage waveforms of the transformer on the primary side ($V_{TR,pr} = 107 V$) and secondary side ($V_{TR,sec} = 207 V$).

Compared to the structures of conventional isolated Z-source DC-DC converters displayed in Fig. 3 and improved isolated Z-source DC-DC converters presented in Table. 1, typology of the proposed isolated Z-source converter consists of only one switch, which increases its simplicity, and yet

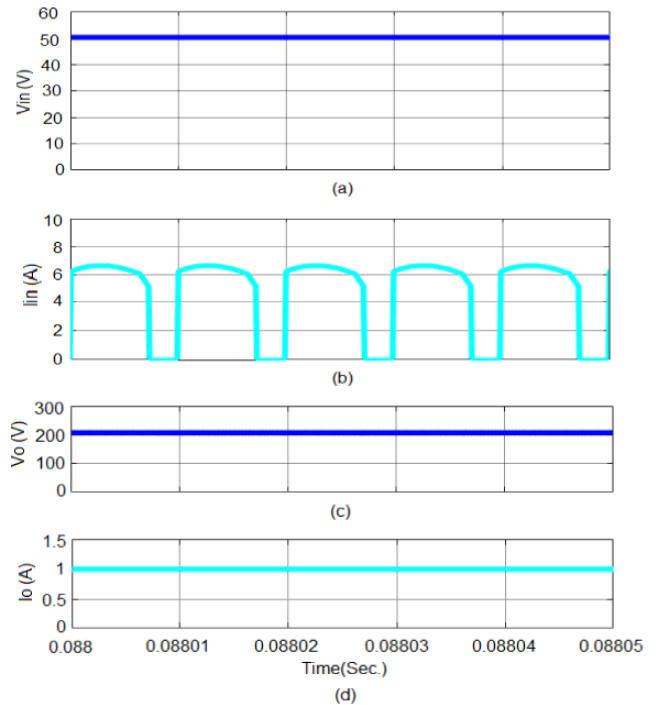


FIGURE 8. Simulation results of the proposed converter for (a) input voltage, (b) input current, (c) output voltage, and (d) output current.

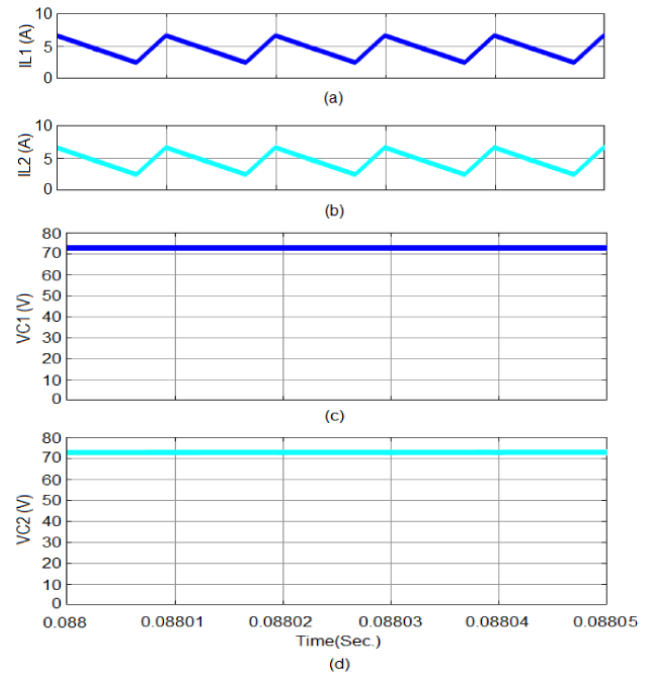


FIGURE 9. Simulation results of the proposed converter: (a) inductor current I_{L1} , (b) inductor current I_{L2} , (c) capacitor voltage V_{C1} , and (d) capacitor voltage V_{C2} .

yields a high output voltage gain. Therefore, the presented converter can be utilized in various applications.

B. EXPERIMENTAL RESULTS

A 200 W prototype converter was assembled to perform experimental tests on the proposed topology. The prototype

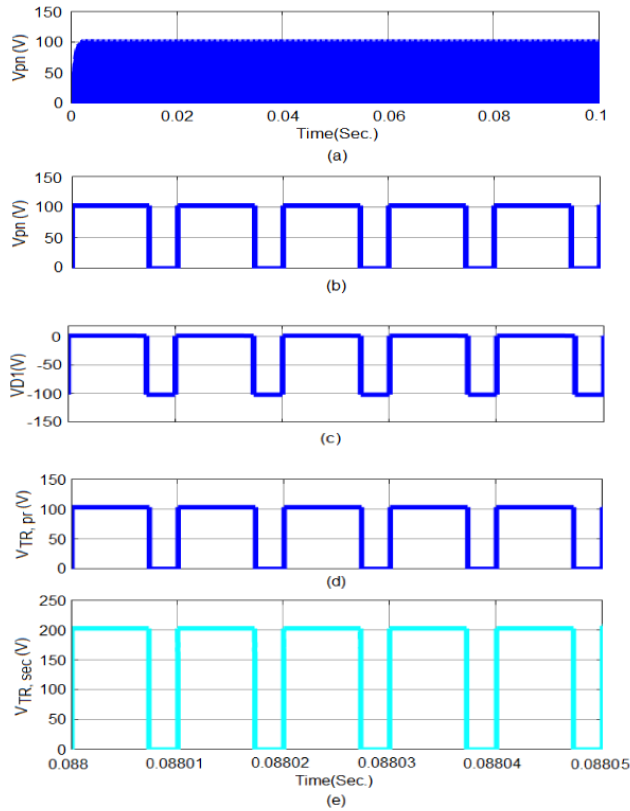
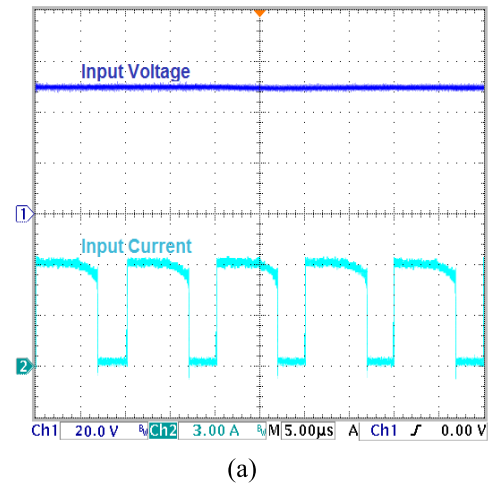


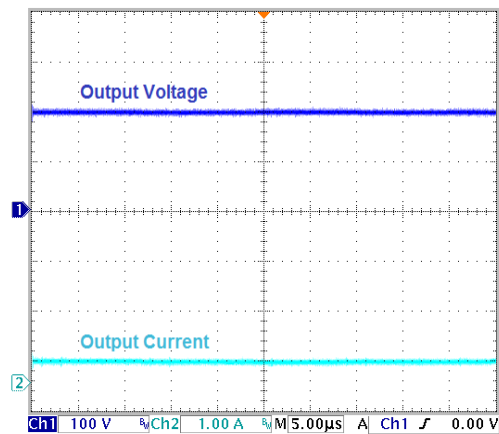
FIGURE 10. Simulation results of the proposed converter: (a) DC-link voltage V_{pn} , (b) zoomed view of DC-link voltage V_{pn} , (c) maximum voltage across D_1 , (d) primary voltage of the isolation transformer $V_{TR,pr}$, and (e) secondary voltage of the isolation transformer $V_{TR,sec}$.

and its technical specifications are displayed in Fig. 4 and Table. 2, respectively. The experimental parameters match the simulated parameters presented in Subsection VI. A.

The Z-source network comprises a coupled inductor that is made of ferrite material N87 with a magnetizing inductance of $24 \mu\text{H}$, and is wound on an EFD25 core. The isolation transformer is wound on the ETD34 core with a magnetizing and primary-side leakage inductances of 35.5 and $0.65 \mu\text{H}$, respectively. Capacitors of the Z-source network are operated with electrolytic multilayered capacitors connected in parallel. Each capacitor of the Z-source network includes 3 EKZN101ELL151MJ25S capacitors operated at 100 V with a capacity of $150 \mu\text{F}$. Moreover, two EGXF251ELL510MK25S capacitors with a capacity of $51 \mu\text{F}$ and voltage of 250 V are connected in series to form the VDR. All diodes are Silicon (Si)-based or Silicon carbide (SiC)-based Schottky diodes. Si- and SiC-based Schottky diodes are placed on the input (low voltage) and the output (HV) sides, respectively. The types and electrical specifications of semiconductors are presented in Table. 3. The prototype is constructed using SPP20N60C3 MOSFET (600 V and 20.7 A). For the half- and full-bridge methods, two and four MOSFET switches are needed, respectively, whereas the proposed typology requires only one MOSFET switch.



(a)



(b)

FIGURE 11. Experimental results: (a) input voltage and current, and (b) output voltage and current.

The experimental results with an input DC-adjusted voltage of 50 V ($V_{in} = 50 \text{ V}$) and a duty cycle of 0.25 ($D = 0.25$) are illustrated in Figs. 11–13.

Figs. 11(a) and (b) indicate that the experimentally estimated values for the input voltage (V_{in}), input current (I_{in}), output voltage (V_{out}), and output current (I_{out}) are 50 V , 6.5 A , 200 V , and 1 A , respectively. Under the same condition, the measured output voltage decreased by 6 V compared to the output voltage obtained using the voltage drop principle, as discussed in Subsection VI. A.

Currents of L_1 and L_2 (I_{L1} and I_{L2}) and the voltages of C_1 and C_2 (V_{C1} and V_{C2}) are illustrated in Figs. 12(a) and (b). The measured current for both inductors is 6.5 A ($I_{L1} = I_{L2} = 6.5 \text{ A}$), maximum inductor current ripple is 4.1 A , and capacitor voltage is 66 V ($V_{C1} = V_{C2} = 66 \text{ V}$). Although simulation and measured values of inductor currents are identical, theoretical voltages of capacitors ($V_{C1} = V_{C2} = 73 \text{ V}$) declined by 7 V in comparison with the corresponding experimental results ($V_{C1} = V_{C2} = 66 \text{ V}$), as illustrated in Figs. 9(c) and (d).

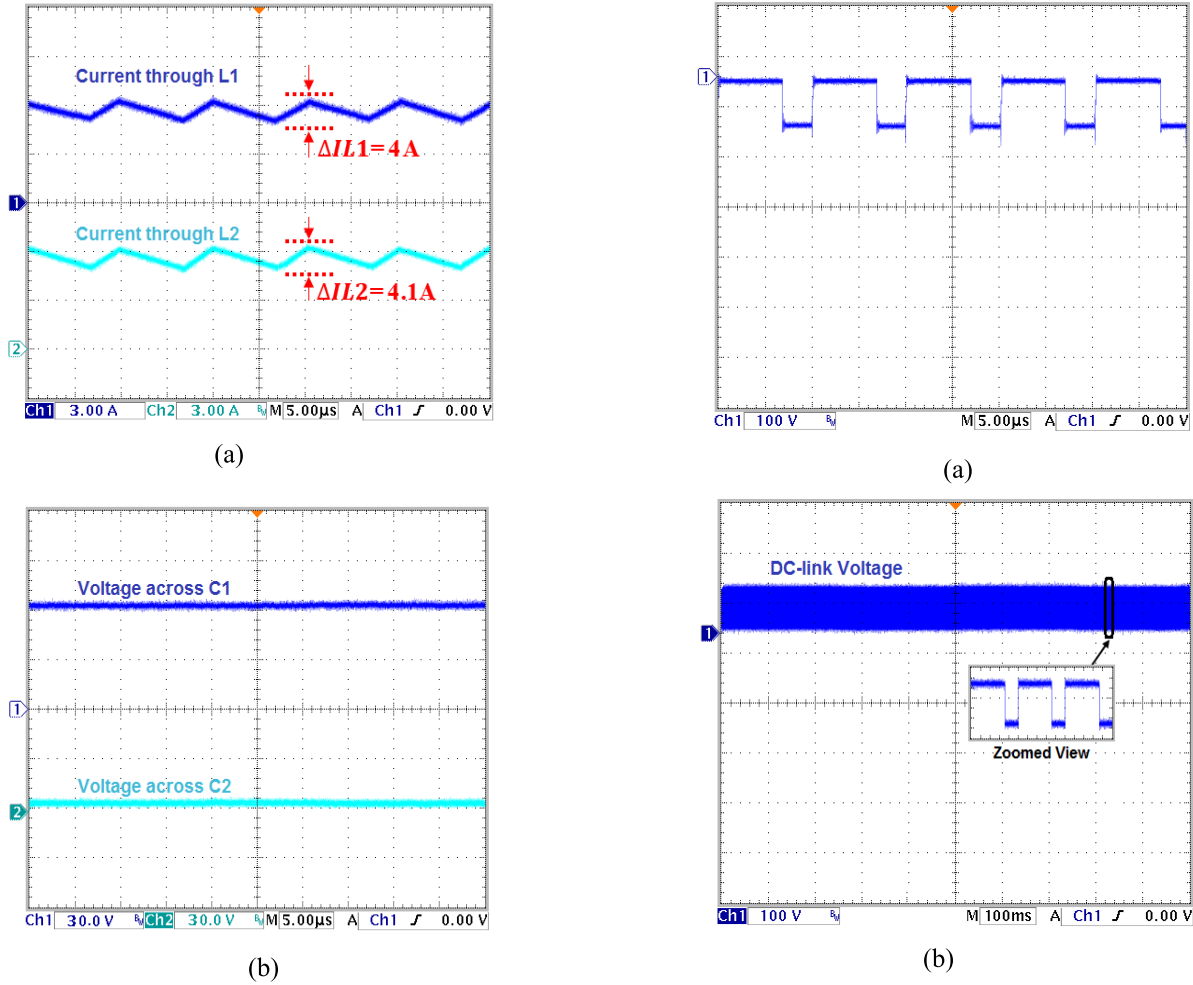


FIGURE 12. Experimental results: (a) inductor currents I_{L1} and I_{L2} , and (b) capacitor voltages V_{C1} and V_{C2} .

Fig. 13 (a) and (b) exhibits the experimental waveforms of the peak value of DC-link voltage (V_{pn}) and maximum voltage stress of D_1 , respectively. The experimentally measured value for the DC-link and diode voltages were 100 V ($V_{pn} = 100$ V) and -100 V ($V_{D1} = -100$ V), respectively. Similarly, Fig. 13(c) presents the voltage waveforms of the primary and secondary transformer sides. The measured primary and secondary voltages of the transformer were 100 V ($V_{TR,pr} = 100$ V) and 200 V ($V_{TR,sec} = 200$ V), respectively. These values partially differ from the theoretical values presented in Subsection VI. A. ($V_{pn} = 107$ V, $V_{D1} = -107$ V, $V_{TR,pr} = 107$ V, $V_{TR,sec} = 207$ V).

The experimental results slightly differ from the simulation results, which can primarily be attributed to the leakage inductance of the coupled inductors in the Z-source network, leakage inductance of the transformer, equivalent series resistance (ESR) of each component, voltage drop owing to the parasitic parameters of passive and active components (particularly VDR diodes in the proposed typology), parasitic resistance of inductance (r_L), ESR of capacitors (r_C), and equivalent resistance of the drain-source switch (r_{DS}).

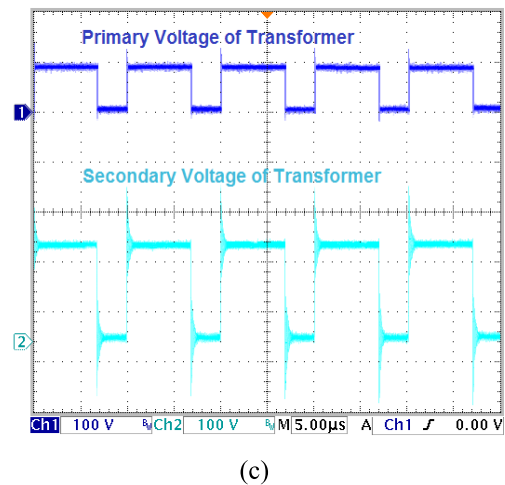


FIGURE 13. Experimental results: (a) DC-link voltage V_{pn} , (b) maximum voltage across D_1 , and (c) primary and secondary voltages of the isolation transformer.

Fig. 14 demonstrates comparisons between the theoretical and experimental results estimated for the efficiency and voltage gain. The theoretical and experimental efficiencies under various loads are shown in Fig. 14(a). The maximum theoretical efficiency of the proposed converter is 97% under

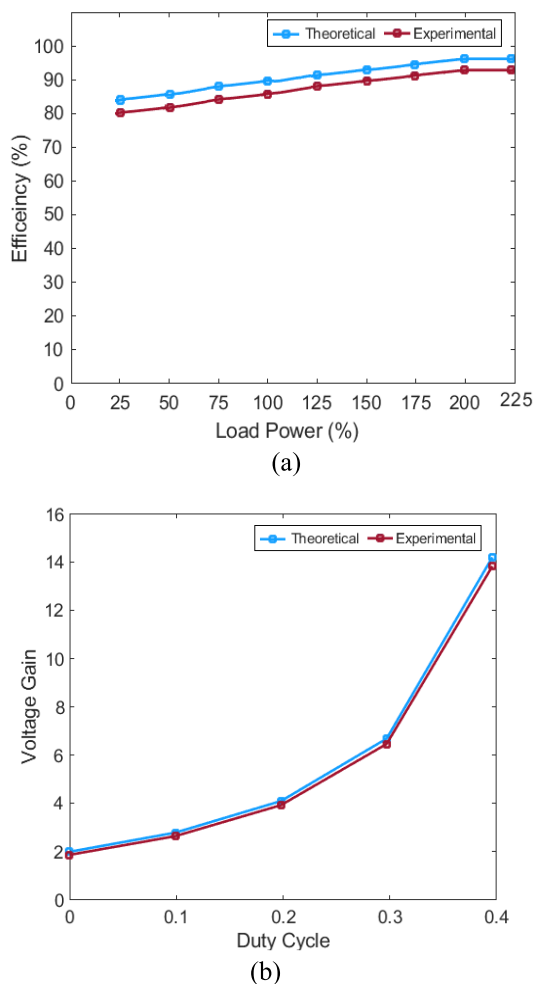


FIGURE 14. (a) Comparison between the theoretical and experimental efficiencies at various loads, and (b) comparison between the theoretical and experimental voltage gains versus duty cycle.

200% of the nominal load and is higher than 90% under 100% of the nominal load. Nonetheless, the maximum experimental efficiency is 94.05%. The efficiency is greater than 86.15% under 100% of the nominal load and decreases by 2.95% under 200% of the nominal load. This reduction can be ascribed to the leakage inductance of coupled inductors in the Z-source network, leakage inductance of the transformer, ESR, parasitic parameters of passive and active components, and diodes of VDR. Furthermore, Fig. 14(b) illustrates the voltage gain curves of the proposed converter with respect to the duty cycle. Fig. 14(b) illustrates that the theoretical and experimental voltage gain of the introduced converter is considerably high for duty cycles in the range of 0.3–0.4.

VII. CONCLUSION

The performance of the improved galvanically isolated Z-source DC-DC converter was compared with that of conventional isolated Z-source DC-DC converters. The advantages of the proposed converter are as follows: a) generates desirable output voltage just by altering the voltage ratio at the same duty cycle; b) maintains voltage stress down; thus,

the number of required switches reduces, production cost and size of the converter decreases, and efficiency and reliability increases; c) has a simple controller; hence, no disturbing signals exist; and, d) although the implementation of VDR on the secondary side of the converter reduces the voltage drop, it promotes the efficiency of the rectifier and stabilizes the performance of the converter. Consequently, the proposed converter is a promising candidate for interfacing an input DC source with a nonharmonic DC bus or a DC microgrid owing to its excellent specifications. Theoretical results were verified using the experimental tests. The measurements on the fabricated prototype proved that it can control a power of 200 W with an efficiency of 94.05%, and provide an output voltage of 200 V.

ACKNOWLEDGMENT

(Naser Fakhri and Saeid Gholami Farkoush are co-first authors.)

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