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Low-Voltage Implementation of Neuromorphic Circuits for a Spike-Based Learning Control Module

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ABSTRACT Recent brain emulation engines have been configured using thousands of neurons and billions of synapses. These components make a significant impact on the whole system in terms of power consumption and silicon area. In this work, several upgraded neuromorphic circuits are used to configure an efficient and compact spike-based learning control module that is capable of operating under ultralow-voltage supplies offering a low energy consumption per spike. In this way, a conductance-based silicon neuron is developed using the simplest highly efficient analog circuits. Moreover, an upgraded winner-take-all (WTA) circuit is used to form a low-voltage multi-threshold current comparator to determine whether to increase or decrease the synaptic weight. Other components such as low-speed amplifier, differential pair integrator (DPI)-based synapse, and weight update controller are designed such that they properly operate under a 0.5V supply voltage. Simulation results in TSMC 0.18 μm CMOS process show an energy consumption of 2.5 pJ for the upgraded learning control module, while its stop-learning mechanism improves the performance of the system by avoiding overfitting.

INDEX TERMS Neuron, WTA, spike-based, low-voltage, neuromorphic, control module.

I. INTRODUCTION

Nowadays, analog and digital neuromorphic circuits are widely used to propose brain-inspired electronic systems [1]–[3]. Spiking neural networks are a well-known case by which computational properties of the nervous system are explored [4]–[6]. To provide the capability of real-time interactions with the environment in such neural technologies, building low-power spike-based circuits with realistic temporal dynamics is still an unavoidable challenge that circuit designers are dealing with [6]–[8]. In addition, those neural networks that are supposed to process big data or classify complex patterns require a neural-inspired learning rule such as spike-timing-dependent plasticity (STDP). In fact, the STDP mechanism that operates based on the relative timing of pre-synaptic and post-synaptic spikes has efficiently been implemented using analog circuitry blocks [9]–[11]. Nonetheless, a developed spike-based learning rule with the capability of classifying complex patterns has been implemented as a neuromorphic circuit in [5], [12], [13]. Such a learning rule consists of two modules including a stop-learning control module and a synaptic weight update module, which both can be upgraded for portable applications if the simplest and highly efficient low-voltage analog circuits are used for implementation.

Among all neuromorphic circuits, neurons are considered as an effective component since thousands of them are employed in the computing units, which significantly affect power consumption [14], [15]. Although the Integrate and Fire (I&F) model was many times implemented using CMOS technologies that do not consume high power, however, non-generalized I&F models do not offer important features observed in real neurons [16], [17]. Therefore, several low-power solutions such as simple positive-feedback topology, tau-cell, tunable differential pair integrator (DPI), and low-pass filter were used to enhance the performance of the neurons and provide adequate firing patterns [18]–[22]. In this way, log-domain subthreshold circuits play

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a key role in terms of time constant, which should be in a realistic range to achieve biologically temporal dynamics. Recently, Izehikevich and Mihalas-Niebur models were frequently implemented based on the aforementioned methods achieving different firing patterns, but cannot be considered as the best low-power designs and compact cases [19], [23]. Therefore, designing a conductance-based silicon neuron with low energy consumption, small die area, biological time constant, and tunability is still an open challenge.

On the other hand, memristor and winner-take-all (WTA) circuits are other effective neuromorphic blocks, which are widely used in neural networks [24], [25]. Since the variability and nonvolatility of memristors are much similar to the characteristics of synapses in biological neural networks, many scholars have put efforts to build neural networks with memristor synapses [26]–[28]. Moreover, the WTA circuit is usually used as a current comparator or a selector block to distinguish the highest-ranked input [24]. It is worth noting that the WTA-based networks are very applicable in solving complex classifications and sorting, where the WTAs perform parallel computations [29]. Since the circuit implementation of a WTA is easier than other solutions, designers have been motivated to solve general programming problems using a new family of WTA-based neural networks [30]. Moreover, there is an intrinsic potential in WTAs under which it could be used as a non-binary current comparator that is an unremovable part of a learning module [5], [31]. Actually, a stop-learning control module needs a multi-threshold comparator to determine whether to increase or decrease the synaptic weight, which could be efficiently implemented using several WTAs [31]. Although reducing the supply voltage is a well-known method to decrease the power dissipation, the traditional WTAs are not able to adequately operate under low-voltage supplies that keep this challenge still open.

To implement a spike-based learning control module with the capability of low-voltage operation and real-time interaction for ultralow-power applications, a compact and low-energy DPI-based neuron along with a low-voltage WTA circuit are designed in this work. For this purpose, a tunable low-voltage multi-threshold comparator is also designed as the decision-making block that provides the possibility of reducing the supply voltage of the learning module to 0.5V resulting in a low energy consumption per spike. In other words, the simplest and highly efficient low-voltage analog circuits including DPI as a variable-gain low-pass filter, current mirror-based positive feedback, auxiliary level shifters, and class-AB comparator are employed to configure the sub-circuits of the learning module providing adequate firing behaviors, high adjustability, and realistic temporal dynamics with low energy consumption. In addition to the above solutions, other required circuits including a low-speed amplifier for the weight update module, and a differential pair integrator as the synapse circuit are designed such that the whole module consumes just 2.5 pJ per synaptic operation (SOP) under a supply voltage of 0.5V.

The rest of the paper is organized as follows: Section II describes the structure and operation of the low-voltage spike-based learning control module in detail. Section III presents the upgraded sub-circuits of the learning module. Simulation results in TSMC 180 μm CMOS process are reported in Section IV. Finally, the paper is concluded by Section V.

II. SPIKE-BASED LEARNING MODULE

Spike-timing-dependent plasticity (STDP) is a well-known learning mechanism that updates the synaptic weights based on the relative timing of pre-synaptic and post-synaptic spikes. It was implemented many times using analog or mixed analog-digital circuits with high efficiency. Although spatio-temporal spike patterns can efficiently be classified using STDP-based learning mechanisms, these algorithms have not shown suitable results for some cases, evaluated in [5], [14]. Therefore, an elaborate plasticity rule presented in [32] was upgraded, which its operation depends on both the timing of pre-synaptic spikes and membrane potential of the neuron calling spike-driven synaptic plasticity (SDSP). In fact, this mechanism was used to implement both supervised and unsupervised learning protocols, training the neuron to play the role of a binary classifier [33].

Fig. 1 shows the simplified block diagram of the spike-based learning control module with its waveforms [12] that is supposed to operate under low-voltage supplies by upgrading its sub-circuits and employing a low-voltage multi-threshold current comparator. In this structure, the stop-learning control module and its output signals V_{UP} and V_{DN} (dotted box on the right in Fig. 1), will be shared among an array of synaptic weight update modules to provide several input terminals. In other words, according to the SDSP learning rule implemented in [5], the synaptic weight update module (dotted box on the left in Fig. 1) is used for each synapse to separately provide the possibility of changing the values of the weights. Therefore, the input patterns are applied to the pre-synaptic synapses to steer the behavior of the post-synaptic neuron achieving the desired response. At the input part of Fig. 1, transistors ML1-ML4 receive the input signal from pre-synaptic neurons and decide whether to increase or decrease the value of the weight, depending on two global signals, V_{UP} and V_{DN}. The amplifier that has been configured as a positive-feedback topology compares a threshold voltage, V_{thw}, with the weight potential, V_w, to slowly drive V_w toward one of the high or low rails, V_{whi} or V_{wlo}, respectively. Thus, the updated weight potential will make an impact on the amplitude of I_{syn}, generated by the DPI synapse, and it affects the behavior of the neuron to re-generate two global signals, V_{UP} and V_{DN}. The synaptic weights will be updated again, and this procedure continues until the desired responses are achieved.

The stop-learning control module can be considered as the most important part of such a learning mechanism. To provide a measure of the neuron behaviors as the post-synaptic

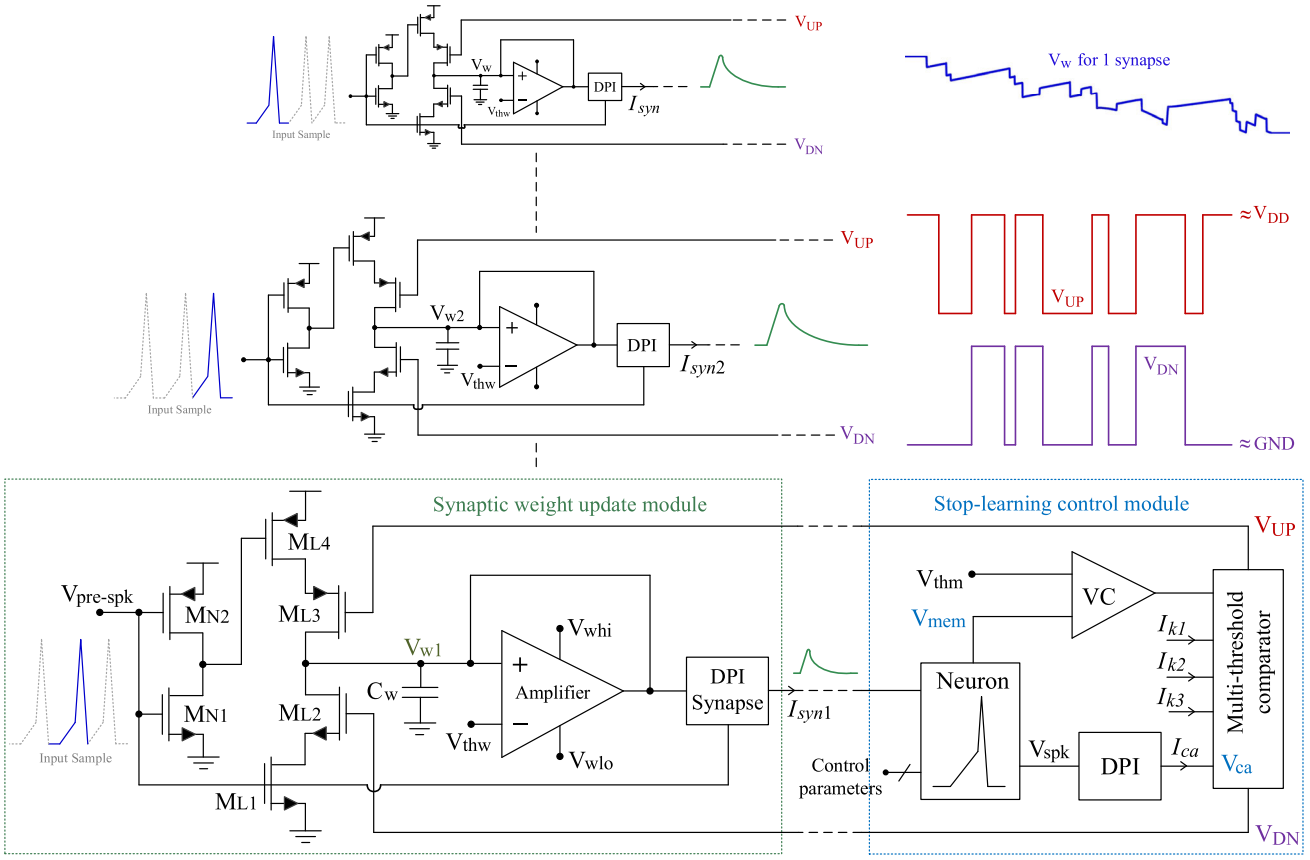


FIGURE 1. Simplified block diagram of the spike-based learning control module [12].

calcium concentration I_{ca}, the output spikes of the neuron (post-synaptic) are integrated onto a capacitance embedded in the DPI circuit. Therefore, three different threshold currents, I_{k1}, I_{k2}, and I_{k3}, are compared to I_{ca} by a multi-threshold current comparator, while the membrane voltage, V_{mem}, is parallelly compared to a fixed threshold voltage, V_{thm}, by a voltage comparator. The results of these comparisons update the weight potential as

$$V_w = V_w + \Delta w, \quad if \begin{cases} V_{mem} > V_{thm} \\ I_{k1} < I_{ca} < I_{k3} \end{cases}$$
$$V_w = V_w - \Delta w, \quad if \begin{cases} V_{mem} < V_{thm} \\ I_{k1} < I_{ca} < I_{k2} \end{cases} \quad (1)$$

where Δw is the amount of the change made at V_w. If none of the above conditions are met, the learning procedure is stopped by setting $V_{UP} = V_{DD}$ and $V_{DN} = 0$. In fact, such a stop-learning rule improves the performance of the network by avoiding overfitting if the input pattern has already been learned.

The neuron and multi-threshold comparator of the stop-learning control module usually operate under normal supplies, 1.2-1.8V in 0.18 μm CMOS process, which does not allow designers to reduce the power dissipation by applying a lower supply voltage. It means circuitry methods can still be useful to provide the capability of operating under low-voltage supplies such as $V_{DD} = 0.5$V for applications with stringent power supply conditions. Such an approach not only decreases the power dissipation but also eases achieving realistic time constants. As it is seen from Fig. 2, both traditional and upgraded multi-threshold comparators are configured using several current comparators (CC). Since the traditional one, shown in Fig. 2 (a), was configured based on a kind of cascode structure [5], and the supply voltage drops across at least two CCs, it cannot be used under low-voltage supplies and needs an upgrade. Therefore, Fig. 2 (a) is efficiently upgraded as a low-voltage case [31], shown in Fig. 2 (b).

In Fig. 2 (a), if $I_{ca} > I_{k1}$, CC1 flows its output current through transistors Mt2 or Mt3, then, a voltage comparator (VC) decides whether to turn on or off Mt2 and Mt3. Therefore, for $V_{mem} < V_{thm}$, Mt2 turns on to activate CC2 that its output current is converted to a voltage named V_{DN} by a diode-connected transistor, Mo2. In a similar way, if $V_{mem} > V_{thm}$, CC3 is activated to generate V_{UP}. It is obvious that the traditional multi-threshold comparator needs a normal supply voltage because of its cascoded structure. To remove this limitation, an upgraded low-voltage multi-threshold comparator, shown in Fig. 2 (b), is designed. The voltage comparator has been replaced with another current comparator with the capability of comparing two input

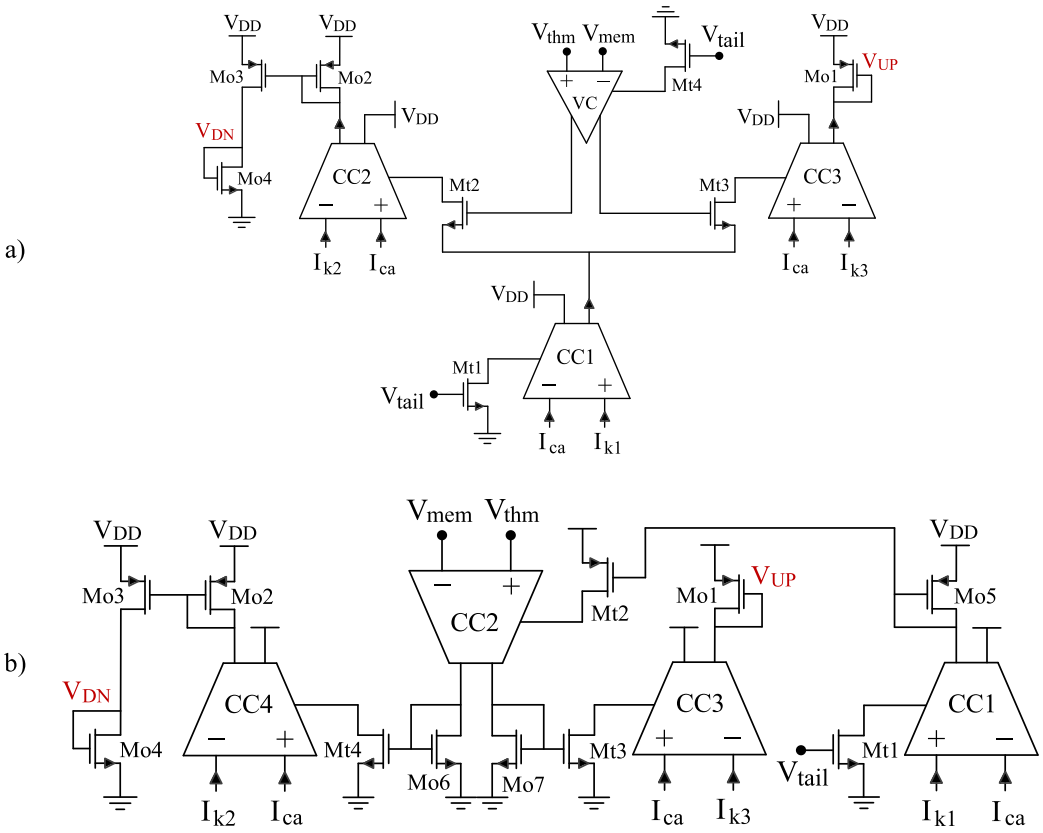


FIGURE 2. Schematic of multi-threshold comparators, a) traditional [5], and b) upgraded.

voltages. Actually, a single-MOS converter is used at the input to convert the input voltage to current. Thus, employing four CCs in the upgraded circuit, instead of three CCs and one VC, certainly improves matching properties for the fabrication process. In addition, the cascoded structure of the traditional case has been reconfigured based on a serial structure, which lets designers reduce the supply voltage as much as the sub-comparators allow. The upgraded structure not only consumes less power than the traditional one but also provides the possibility of changing the output voltage's level by adjusting a control parameter, V_{tail}. The operation of the upgraded multi-threshold comparator can mathematically be expressed as

$$
\begin{aligned}
&V_{UP}\\
&= V_{DD} - \Delta V \begin{cases} \text{if } V_{mem} > V_{thm} \Rightarrow \begin{cases} M_{t3} : on \\ M_{t4} : off \end{cases} & \Rightarrow CC3 : on \\ \text{and } I_{k1} < I_{ca} < I_{k3} \end{cases}\\
&V_{DN}\\
&= GND + \Delta V \begin{cases} \text{if } V_{mem} < V_{thm} \Rightarrow \begin{cases} M_{t3} : off \\ M_{t4} : on \end{cases} & \Rightarrow CC4 : on \\ \text{and } I_{k1} < I_{ca} < I_{k2} \end{cases}
\end{aligned}
\tag{2}
$$

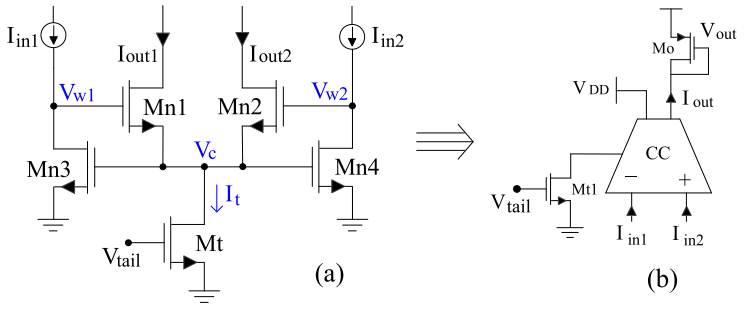
Here ΔV is a factor that depends on V_{tail}, the tail current of CC1, and determines the level of the output voltage changes. If none of the above conditions are met, V_{UP} and V_{DN} are respectively set at V_{DD} and GND to stop the learning process.

Regarding the power dissipation and silicon area, since the voltage comparator used in Fig. 2 (a) consumes approximately the same power and also occupies the same area with a CC circuit, the power dissipation and silicon area of the traditional multi-threshold current comparator can approximately be estimated by 4×CC, similar to that of the upgraded multi-threshold comparator. It still seems that Fig. 2 (b) employs 3 transistors (Mo5-Mo7) more than Fig. 2 (a), but all of them are a part of their corresponding CCs and are not considered as additional transistors. Therefore, if both structures of Fig. 2 employ the same CC, it can be expected to achieve the same power dissipation and silicon area, while the upgraded circuit offers low-voltage features.

III. SUB-CIRCUITS IMPLEMENTATION

To provide low-voltage features for the spike-based learning control module, the structure of the required sub-circuits such as the WTA circuit, and silicon neuron are upgraded in this section. In other words, the simplest and highly efficient low-voltage methods are employed to configure the sub-circuits, which result in low energy consumption and low-voltage operation. In addition, for real-time interactions with the environment, realistic temporal dynamics are achieved.

	Traditional
Device	Size
Mt	4×3.6 µm/0.5 µm
Mn1, Mn2	4 µm/0.5 µm
Mn3, Mn4	3.6 µm/0.5 µm



	Upgraded
Device	Size
Mt	4×3.6 µm/0.5 µm
Mn1, Mn2	4 µm/0.5 µm
Mn3, Mn4	3.6 µm/0.5 µm
Mn5, Mn6	4 µm/0.5 µm
Mp5, Mp6	2× 3.6 µm/0.5 µm
Mp7, Mp8	1.8 µm/0.5 µm
Mn7, Mn8	0.9 µm/0.5 µm

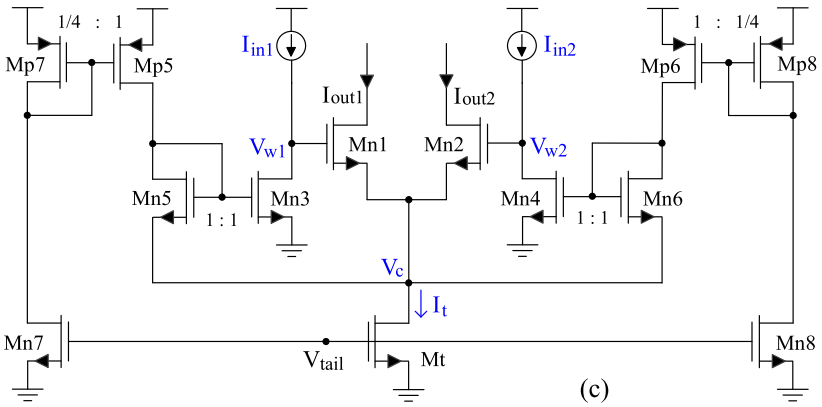


FIGURE 3. Schematic of (a) traditional WTA [24], (b) WTA-based comparator, and (c) upgraded WTA.

A. UPGRADED WTA CIRCUIT

The traditional winner-take-all (WTA) circuit is shown in Fig. 3 (a) [24], while Fig. 3 (b) configures a WTA-based current comparator by connecting one of the output terminals to the supply voltage [5]. In the structure of the traditional WTA, the gate-source voltage of transistors Mn3-Mn4 drops across the drain-source of Mt, while the tail transistor Mt does not need such a big drain-source voltage to keep working in the saturation region. This circuitry limitation does not allow designers to significantly reduce the supply voltage, thus, the traditional WTA can be upgraded as Fig. 3 (c), inspired from [31]. In other words, a minimum voltage of $(2V_{GS} + V_{DS,sat})$ is required to supply the traditional WTA that can be decreased if $V_{GS,Mn3}$ is removed across $V_{DS,Mt}$. Compared to [31], the upgraded WTA biases all transistors using just one control parameter, V_{tail}, by which a kind of self-biasing structure is configured. Actually, once V_{tail} is changed to control the output voltage level, the DC currents flowing through Mp5:Mp7 and Mp6:Mp8 proportionally change. It makes a small change at V_c by which V_{w1} and V_{w2} will be affected through Mn3:Mn5 and Mn4:Mn6, respectively. Thus, new values of V_{w1} and V_{w2} re-adjust the DC currents flowing through Mn1 and Mn2 to recover desired V_c, and keep Mt in saturation. In addition, the source terminals of Mn3 and Mn4 are connected to the ground providing a high voltage swing for winning outputs, V_{w1} and V_{w2}.

As can be seen from the upgraded structure, the drain voltage of Mt, V_c, can be reduced as low as possible, while it does not affect the operation of other transistors as long as Mt operates in saturation. Unlike the traditional WTA, the gate terminals of Mn3-Mn4 are indirectly connected to V_c through two diode-connected topologies Mn5-Mn6. In addition, two current mirrors Mp5:Mp7 and Mp6:Mp8 have been added to provide the bias currents of the circuit, while they can be tuned by the bias voltage of the tail transistor, V_{tail}. Transistors Mn1 and Mn2 configure a kind of differential pair to provide a smooth bi-stability condition between both sides of the circuit such that any change made at V_c will indirectly affect $V_{w1,2}$ through Mn5:Mn3 and Mn6:Mn4. In fact, these two current mirrors play the role of level shifters to strengthen the impact of the input currents on $V_{w1,2}$. Assuming $I_{in1} = I_{in} + \delta$ and $I_{in2} = I_{in}$, transistor Mn3 has to sink an extra current of δ causing an increase at V_c through Mn1 that will be shifted to the gate terminals of Mn3 and Mn4 making a considerable change at V_{w1} and V_{w2}. Since $I_{in2} = I_{in}$, transistor Mn4 does not sink extra current and its drain voltage V_{w2} decreases, while V_{w1} increases. Therefore, a current of $I_t/2$ is divided between Mn1 and Mn2, depending on the values of V_{w1} and V_{w2}. According to the large-signal analysis done in [31], the winning voltage of the traditional and upgraded WTAs can respectively be expressed by

$$V^{w}_{Traditional} = nU_T\left[Ln\left(\frac{I_{in}+\delta}{I_s}\frac{L_3}{W_3}\right)+Ln\left(\frac{I_t}{I_o}\frac{L_1}{W_1}\right)\right]+2V_T \tag{3}$$

$$V^{w}_{Upgraded} = nU_T\left[Ln\left(\frac{I_{in}+\delta}{I_o}\frac{L_3}{W_3}\right)+Ln\,(2)\right]+V_T \tag{4}$$

Device	Size
M1-5, M11	1.2 µm/0.4 µm
M6, M10	2.5 µm/0.4 µm
M7, M12	0.25 µm/1 µm
M8	2 µm/0.36 µm
M9	0.25 µm/0.4 µm
Mc1, Mc2	1 µm/0.36 µm
Mc3, Mc4	2 µm/0.36 µm
Mc5, Mc6	1 µm/0.36 µm

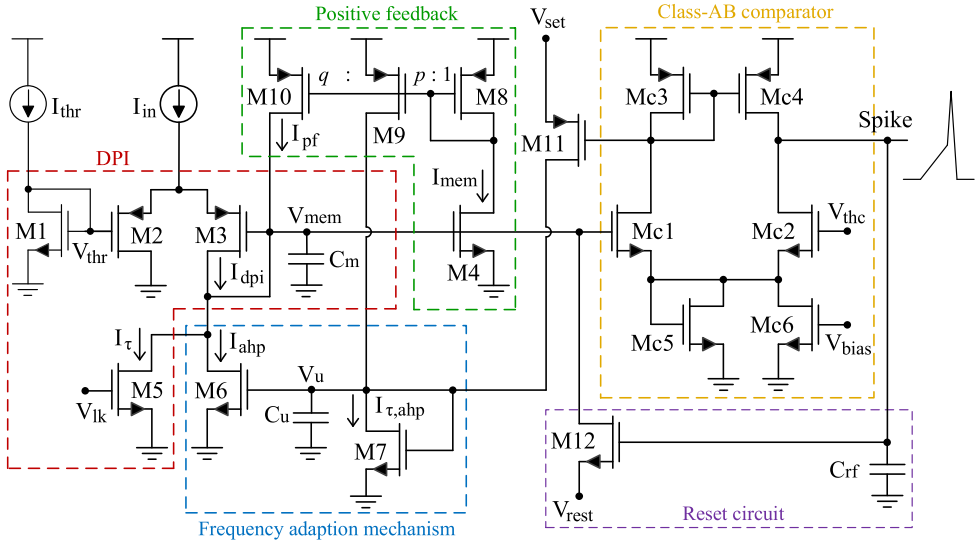


FIGURE 4. Upgraded conductance-based silicon neuron.

where U_T is the thermal voltage, n is the slope factor, V_T is the threshold voltage and $I_o = \mu C_{ox} n U_T^2$. To clarify the operation of Mt under a low-voltage supply, since all transistors are supposed to operate in the weak-inversion region, a minimum drain-source voltage of 50-75 mV could be enough to keep them in saturation [35]. Depending on the required speed of the WTA circuit (low-speed for biologically temporal dynamics), transistors Mn5-Mn6 could be sized for a gate-source voltage from 0.15V to 0.3V if $V_{\mathrm{T}} = 0.5$V (threshold voltage). Since a current of I_{t} flows always through Mt, thus, all transistors can be sized and biased such that the above-mentioned operating points are achieved. In other words, the input current variation results in a small change at V_{c} that will be shifted to the gate terminals of Mn3 and Mn4 to make a considerable change at V_{w1} and V_{w2}. Depending on the values of V_{w1} and V_{w2}, a current of $I_{\mathrm{t}}/2$ is divided between Mn1 and Mn2, still flowing through Mt. On the other side, another $I_{\mathrm{t}}/2$ always flows through Mt by Mn5 and Mn6 to keep Mt in its desired operating point. And once V_{tail} is changed to control the output voltage's level, the current of all transistors specially Mp7 and Mp8 will similarly change with transistor Mt. Therefore, V_{c} does vary too much and simulation results show that Mt remains in saturation.

In addition, the upgraded WTA seems to need more DC current than the traditional one. However, it is worth mentioning that, unlike the traditional WTA, Fig. 3 (c) is configured such that Mn3-Mn4 are driven by level shifters Mn5-Mn6, which lead to a higher speed during the transition phase because Mn5-Mn6 are biased by constant current sources, Mp5-Mp6. Therefore, as it is seen from Fig. 3, the tail transistor Mt can be biased by the same current I_{t} in both structures to keep the power dissipation and silicon area unchanged, while the speed of the upgraded WTA does not degrade. The only difference corresponds to Mn7-Mn8 and Mp7-Mp8 that flow a very small current of $I_{\mathrm{t}}/16$ to provide the biasing voltages of the circuit. According to the above discussion, it can be mentioned that the upgraded circuit provides low-voltage features, while it still does not consume higher power. Considering the non-functionality and functionality of the traditional and upgraded WTAs under low-voltage supplies, respectively, the upgraded circuit is capable of consuming less power once the supply voltage reduces. Thus, although the upgraded WTA consists of more transistors, they are not sized as large as those of the traditional WTA because both structures are designed such that consuming approximately the same power (Figs. 3 (a) and (c) occupy 504 μm^2 and 638 μm^2, respectively).

B. UPGRADED SILICON NEURON

Fig. 4 shows the upgraded conductance-based silicon neuron, inspired from [18]. In order to design an adjustable low-voltage and low-energy neuron with the capability of offering different oscillatory behaviors, the simplest highly efficient analog sub-circuits are used. Compared to [18], the implementation of the frequency adoption mechanism is eased by employing a diode-connected topology, M7, as a resistor. Another diode-connected transistor, Mc5, is used in the structure of the comparator to upgrade its class-A operation to class-AB, which improves its driving capability as a part of the spike generator circuit. In addition, C_{rf} is added to increase the refractory period that guarantees the membrane capacitance is fully discharged to V_{rest} during the reset phase.

Regarding the circuit operation, a differential pair integrator (DPI) is employed as the input block to linearly integrate the input spikes onto the membrane capacitance C_m. The DPI circuit includes two control parameters I_{thr} and V_{lk} to adjust the gain of the integrator and change the leak conductance, respectively, providing more adjustability. Therefore, any increase at V_{mem} motivates the positive feedback circuit formed by M4, M8, and M10 to boost the charging

process of C_m. It significantly reduces energy consumption by decreasing the switching time. Then, as soon as the membrane potential exceeds the threshold voltage of the comparator V_{thc}, the comparator changes its state to generate the output spike. Thanks to the use of a diode-connected transistor Mc5, the comparator provides a class-AB operation during the transition phase to decrease the duration of the spike. However, there is still a control parameter V_{bias} to change the speed of the comparator. Based on the analysis done in [18], the subthreshold behavior of the membrane circuit can be expressed as

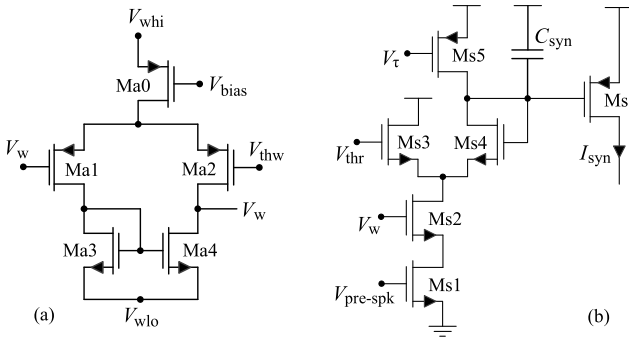
$$\tau_m \frac{d}{dt} I_{mem} + I_{mem}\left(1 + \frac{I_{ahp}}{I_\tau} - \frac{I_{pf}}{I_\tau}\right) = I_{in}\frac{I_{mem}/I_\tau}{1+\left(I_{mem}/I_g\right)} \quad (5)$$

where $\tau_m = nU_T C_m/I_\tau$, I_{mem} is the membrane current, I_{pf} is the positive feedback current, I_{ahp} is after-hyperpolarizing current, and $I_g = I_{o4}\left(W/L\right)_4 \exp\left(V_{thr}/nU_T\right)$.

Equation (5) represents a first-order non-linear differential relationship, which can be simplified to a linear case if $I_{mem} \gg I_{pf}$ and $I_{mem} \gg I_g$. Therefore, after a linear integration of the input signals onto C_m and generation of the output spike, transistor M12 turns on to discharge C_m as the reset circuit, while the refractory period is increased by allocating a small capacitance C_{rf} to make sure the membrane voltage is completely discharged to V_{rest}. On the other side, the comparator turns on M11 to add a small charge to the slow variable capacitance C_u for generation of each spike. In addition, the membrane circuit will charge C_u through the current mirror M8:M9, while a part of I_{M9} flows through M7 as the leak current $I_{\tau,ahp}$ of the frequency adaption mechanism. Therefore, this procedure controls the after-hyperpolarizing current flowing through M6 to slow down the firing rate of the neuron and decrease energy consumption. In other words, I_{ahp} does not allow C_m to be charged as fast as possible and adopts the firing rate with a realistic time constant, depending on the values of C_m, C_u, V_{set}, and the sizes of transistors. According to the analysis done in [18], the subthreshold behavior of the neuron can be expressed by

$$\tau_m \frac{d}{dt} I_{mem} + I_{mem}\left(1 + \frac{I_{ahp}}{I_\tau} - \frac{q}{p} I_{\tau,ahp}\right) = \left(\frac{q}{p}\frac{I_{mem}}{I_\tau}\right)\tau_u \frac{d}{dt} I_{ahp} + I_{in}\frac{I_{mem}/I_\tau}{1+\left(I_{mem}/I_g\right)} \quad (6)$$

where $\tau_u = nU_T C_u/I_{ahp}$, p and q are the current gains of M8:M9 and M8:M10, respectively. Equation (6) describes a conductance-based leaky I&F model that must be versatile. Actually, each part of the upgraded neuron includes a control parameter that allows designers to achieve a wide range of firing behaviors such as adaption, chattering, and slow/fast firing. Moreover, the structure of the neuron has the capability of operating under low-voltage supplies, $V_{DD} = 0.5$V. It is worth mentioning that since the upgraded silicon neuron employed the simplest and highly efficient low-voltage analog circuits such as DPI, positive feedback topology, and low-voltage comparator, not only the energy consumption is reduced but also it does not occupy a large silicon area in comparison with other works [3], [6].



Device	Size
Ma0	3 µm/3 µm
Ma1, Ma2	2 µm/3 µm
Ma3, Ma4	1 µm/3 µm

Device	Size
Ms1, Ms2	3 µm/0.5 µm
Ms3, Ms4	1 µm/0.5 µm
Ms5, Ms6	1 µm/0.5 µm

FIGURE 5. Schematic of (a) low-speed amplifier, and (b) DPI synapse [5].

C. SYNAPTIC CIRCUITS

As it is seen from Fig. 1, a low-speed amplifier and a DPI synapse are still required that can be implemented as Figs. 5 (a) and (b), respectively. The amplifier is a simple differential case, while its speed can be significantly decreased by reducing V_{bias} to slowly drive the weight potential toward one of the high or low rails, V_{whi} or V_{wlo}. Moreover, the synapse circuit has been configured based on the DPI circuit by which the pre-synaptic spikes will be integrated onto C_{syn} and it flows a synaptic current of I_{syn} through Ms6 to be applied to the post-synaptic neuron. Transistor Ms5 plays the role of a leak current controlled by V_τ, and the gain of the integrator can also be tuned by V_{thr}. It is worth noting that the weight potential affects the behavior of the DPI synapse if it is directly or indirectly applied to the gate terminal of Ms2 [5]. Both amplifier and synapse circuits can be designed in the subthreshold region under low-voltage supplies.

IV. SIMULATION RESULTS

The upgraded low-voltage spike-based learning control module (Fig. 1) along with its sub-circuits (Figs. 2-5) have been designed and simulated using TSMC 0.18μm CMOS technology under a 0.5 V supply voltage. To evaluate the performance of the sub-circuits, Fig. 6 shows the output currents (I_{out}) and winning voltages (V_{w}) of both traditional and upgraded WTAs, respectively from top to bottom, while the WTAs were configured as a current comparator. As it is seen, the conventional WTA does not provide an output current as high as that of the upgraded WTA. Unlike the upgraded WTA, the traditional one does not properly operate under low-voltage supplies (0.5V), thus, its output voltage level does not reach the final value. In addition, Fig. 6 shows that the upgraded WTA offers shorter rising and falling times at the winning voltage in comparison with the traditional one.

Fig. 7 shows the output voltages (V_{UP} and V_{DN} from top to bottom) of the upgraded multi-threshold current comparator (Fig. 2), in which the upgraded WTA was employed to provide low-voltage features. To evaluate its performance under a supply voltage of 0.5V, a step current and a step voltage were respectively applied to CC1 and CC2 such that 3nA$<$ I_{ca} $<$5nA, and 0.22V$<$ V_{mem} $<$0.28V, while I_{k1}, I_{k2}, I_{k3}, and V_{thm} were set at 2nA, 4nA, 6nA, and 0.25V, respectively. The tail current of CC1 (V_{tail}) was used as a control parameter to adjust the level of the output voltages by which the changes of the weight potential are controlled.

At the next step, the performance of the upgraded conductance-based neuron is evaluated through Fig. 8, which was obtained for a 20-80pA$_{pp}$ input current step along with V_{thc} = 0.2V, V_{set} = 0.25V, 40mV$<$ V_{rest} $<$ 60mV, 0.35V$<$ V_{thr} $<$ 0.4V, and 40mV$<$ V_{lk} $<$ 80mV. Actually, by adjusting the control parameters in the aforementioned ranges, different firing patterns including regular spiking (slew and fast), frequency adaption mechanism, and chattering behavior have been achieved, respectively from top to bottom. The adoption mechanism adds a specific amount of charge to the slow variable potential, V_u, for generation of each spike, and it slows down the firing rate to decrease the energy consumption. Some considerations such as larger C_u = 1.2pF than C_m = 0.4pF, a small size of M11, and a smaller size of M9 than M10 ensure achieving biological time constants and a proper operation of the adaption mechanism. Table 1 reports the performance summary of the upgraded sub-circuits in comparison with the traditional ones.

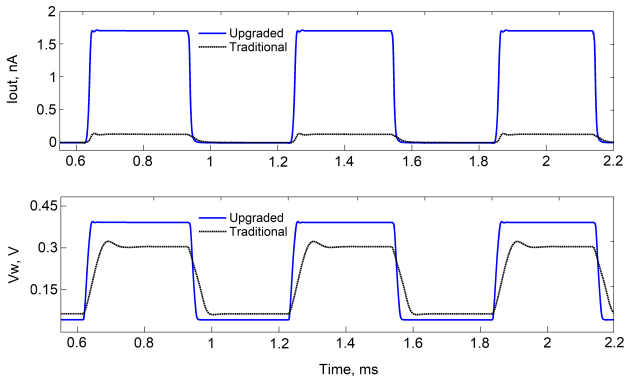


FIGURE 6. From top to bottom: output current (I_{out}), and wining voltage (V_W) of the traditional and upgraded winner-take-all circuits.

Fig. 9 shows the stop-learning control module data that is responsible for generating two global signals V_{UP} and V_{DN}, enabling weight updates. As was shown in Fig. 1, post-synaptic spikes V_{spk}, generated by the neuron, are integrated by the DPI circuit to provide the Calcium concentration current I_{ca}, which can be converted to voltage (V_{ca}) by a MOS transistor at the input of the current comparator. For this aim, an input DC-current of 80pA was applied to the neuron to fire at a regular rate, while other control parameters of the neuron were set as V_{lk} = 60mV, V_{thc} = 0.2V, V_{rest} = 60mV, V_{set} = 0.25V, and V_{thr} = 0.35V. From top to bottom, the first

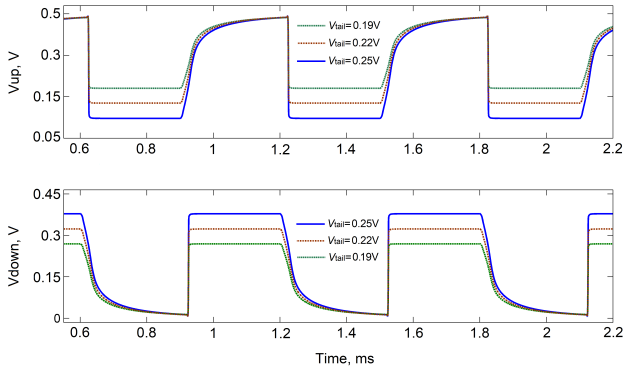


FIGURE 7. From top to bottom: down voltage (V_{DN}), and up voltage (V_{UP}) of the upgraded multi-threshold comparator for different tail voltages (V_{tail}).

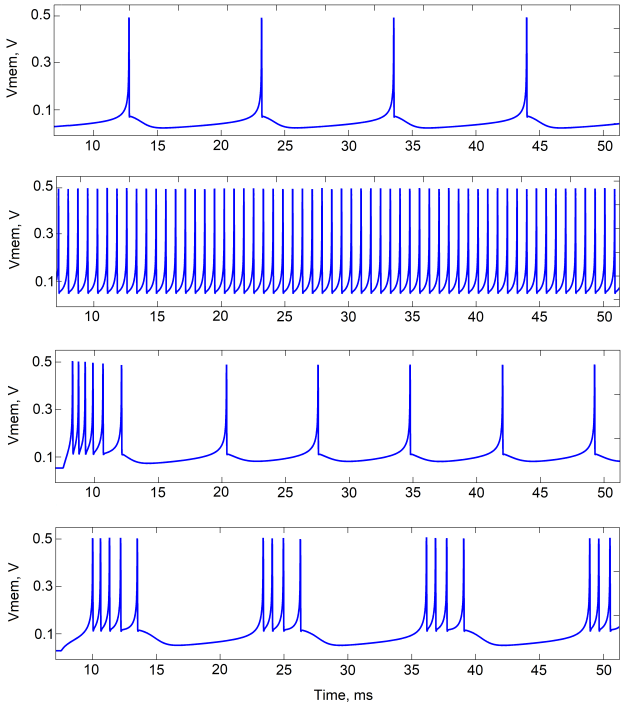


FIGURE 8. From top to bottom: slow firing, fast firing, frequency adaption behavior, and chattering pattern of the upgraded conductance-based neuron.

curve of Fig. 9 shows that V_{ca} decreases from positive rail to lower levels, flowing I_{ca} through one of the input terminals of the upgraded multi-threshold current comparator. Therefore, (V_{dd} − V_{ca}) is compared to (V_{dd} − V_{k1}) = 0.05V, (V_{dd} − V_{k2}) = 0.15V, and (V_{dd} − V_{k3}) = 0.25V (I_{ca}, I_{k1}, I_{k2}, and I_{k3} are achieved by a MOS converter), while the membrane voltage, V_{mem}, is also compared to a fixed threshold voltage, V_{thm} = 0.12V. As can be seen, the second and third curves of Fig. 9 show that the multi-threshold comparator generates V_{UP} and V_{DN} signals in the middle range of V_{ca}, where the conditions of equations (1) and (2) are met.

To have a better evaluation of the stop-learning control module, Fig. 10 shows its operation for a biologically

TABLE 1. Performance summary of the upgraded sub-circuits in comparison with traditional ones.

Winner-take-all Circuits			Multi-threshold current comparators			Silicon neuron	
PARAMETER	Traditional	Upgraded	PARAMETER	Traditional	Upgraded	PARAMETER	Upgraded
V_{DD} [V]	0.5	0.5	V_{DD} [V]	0.5	0.5	V_{DD} [V]	0.5
Technology	180nm	180nm	Technology	180nm	180nm	Technology	180nm
Min Output DC voltage, V	$V_{GS}+V_{DS,sat}$	$2V_{DS,sat}$	Min Output DC voltage, V	$V_{GS}+2V_{DS,sat}$	$2V_{DS,sat}$	Energy [J/spike]	0.38p
Min supply voltage, V	$2V_{GS}+V_{DS,sat}$	$V_{GS}+2V_{DS,sat}$	Min supply voltage, V	$2V_{GS}+2V_{DS,sat}$	$V_{GS}+2V_{DS,sat}$	C_{mem} [F]	0.4p
Power dissipation, nW	12	13	Power dissipation, nW	49	53	Time-scale	Biological
Rise time (V_w), µs	34.7	10.1	Output voltage swing, V	Limited	V_{SS} to V_{DD}	Neuron type	LIF
Fall time (V_w), µs	35.1	11.3	Adjustability	Yes	Yes	Implementation	Analog
Area, µm^2	504	638	Area, µm^2	2208	2780	Area, µm^2	3675

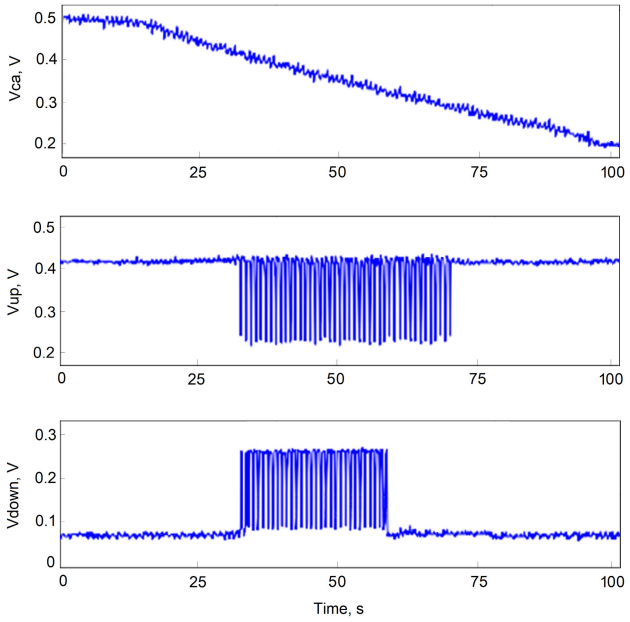


FIGURE 9. Stop-learning control module data, from top to bottom: postsynaptic calcium concentration voltage (V_{ca}), state of the V_{UP}, and V_{DN} signals.

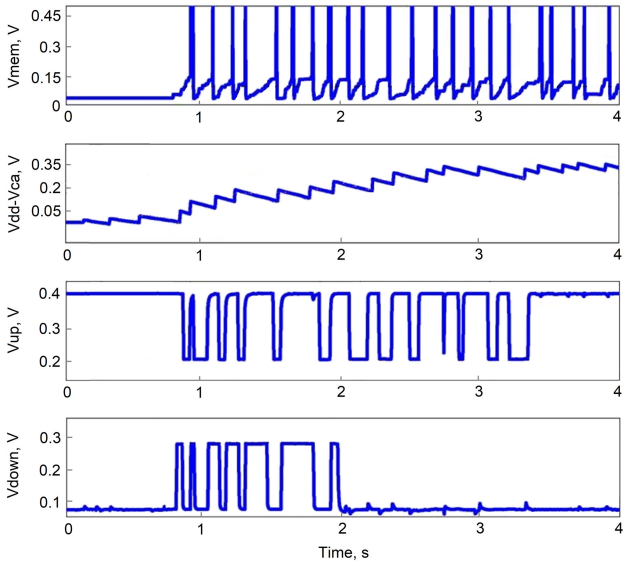


FIGURE 10. Stop-learning control module data, from top to bottom: neuron's membrane potential, postsynaptic calcium concentration voltage (V_{dd}-V_{ca}), state of the V_{UP}, and V_{DN} signals.

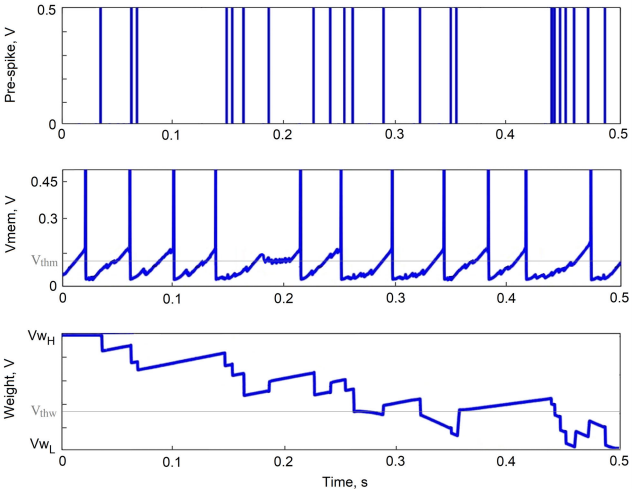


FIGURE 11. Stochastic transitions in synaptic states, from top to bottom: pre-synaptic input spike, neuron's membrane potential, and synapse's weight potential.

plausible time constant. From top to bottom, the first curve shows the membrane voltage of the neuron forcing the DPI circuit to generate V_{ca} that is shown by V_{dd}-V_{ca} as the second curve. Therefore, if $I_{k1} < I_{ca} < I_{k2}$ and $V_{mem} < V_{thm}$ then decreases in synaptic weights ($V_{DN} > 0$) are enabled. Similarly, if $I_{k1} < I_{ca} < I_{k3}$ and $V_{mem} > V_{thm}$ then increases in synaptic weights ($V_{UP} < V_{dd}$) are enabled. Otherwise, no changes in the synaptic weights are allowed ($V_{DN} = 0$, and $V_{UP} = V_{dd}$), which avoids overfitting if the input pattern has already been learned.

To test the weight update mechanism, Poisson distributed spike trains with a mean firing rate of 50Hz were used as the input signal for a period of 500ms. Fig. 11 shows, from top to bottom, the state of the input signal, the membrane potential V_{mem}, and the weight potential V_w, in which the weight made a transition from V_{w-High} to V_{w-Low} denoting long-term depression (LTP). Actually, as soon as the input signal arrives, the synaptic weight update module of Fig. 1 decides whether to increase or decrease the value of the weight, depending on V_{UP} and V_{DN} signals. The non-monotonicity of the LTP in the weight transition is considered

TABLE 2. Performance summary of the upgraded learning control module in comparison with other neuromorphic systems.

PARAMETER	This work#	[7] 2020	[1] 2019	[3] 2018	[6] 2018	[11] 2012	[17]# 2012
V_{DD} [V]	0.5	0.8	1	1.3-1.8	2.5/1.2	0.6	1
Technology	180nm	22nm	28nm	180nm	65nm	90nm	65nm
Energy [J/SOP]	2.5p	>14p	>12.7p	>17p	>200p	-	>41p
C_{mem} [pF]	0.4	0.82	-	1	2.36	0.2	0.5
Time-scale	Biological	Biological	Bio-Acce.	Biological	Accelerated	Biological	Accelerated
Neuron type	LIF	AdEx-IF	LIF	AdExp-IF	AdExp	LIF	LIF
Implementation	Analog	Mixed	Digital	Mixed	Analog	Analog	Analog
Learning rule	SDSP	-	SDSP	Hebbian	-	STDP	STDP
Neuron core area	7119 μm^2	> 900 μm^2	> 43000 μm^2 /256	> 5 mm^2 /1k	> 3372 μm^2	> 442 μm^2	> 538 μm^2
Synapse core area	998 μm^2	> 204 μm^2	> 45000 μm^2 /64k	> 5 mm^2 /64k	-	> 4823 μm^2	-

Simulation

as a feature of the implemented learning rule in the synaptic weight control module [5]. Once stop-learning occurs, the learned synaptic weights lead to correct classification, this mechanism implements a Perceptron learning rule. However, the transition probability can be tuned by changing the pre- and post-synaptic neuron's mean firing rates, by changing the value of the weight transition threshold V_{thw}(see Fig. 1), by changing the height of the synaptic weight jump (set by V_{tail} in Figs. 2-3), and by modifying the control parameters of the post-synaptic neuron (see Fig. 4).

Although the upgraded circuits are versatile and can be controlled under different situations by adjusting control parameters, however, to verify their robustness against the mismatch in the weak inversion region [34], Monte-Carlo simulation was perfumed for 500 runs. The results are shown in Fig. 12 in which the input currents of the circuits were set to obtain a regular firing rate of 100 Hz for the neuron, a rise-time of 10μs for the winning voltage of the WTA, and an output voltage level of 0.35V for the multi-threshold comparator. Since the latter was configured using four sub-comparators, its output voltage level variations are usual, and as was already described, there is a control parameter V_{tail} to adjust the output voltage level by which the changes of the weight potential are controlled. It is worth noting that, although the sensitivity to mismatch is higher in subthreshold, the upgraded sub-circuits employed the simplest well-known analog topologies such as differential pair integrator (DPI), current mirror-based positive feedback, level shifters, and a simple amplifier, which their robustness is as high as possible [5].

The aim of upgrading this spike-based learning control module was to offer an efficient and compact implementation with the capability of operating under low-voltage supplies leading to a low energy consumption system, 2.5 pJ/SOP. In this way, the sub-circuits such as silicon neuron, WTA, and multi-threshold comparator were upgraded as the key building blocks of the learning module. In addition, the aforementioned circuits were wisely designed such that realistic time constants and high adjustability were achieved. Indeed, employing a supply voltage of 0.5V pushed all transistors into the weak inversion region where exponential

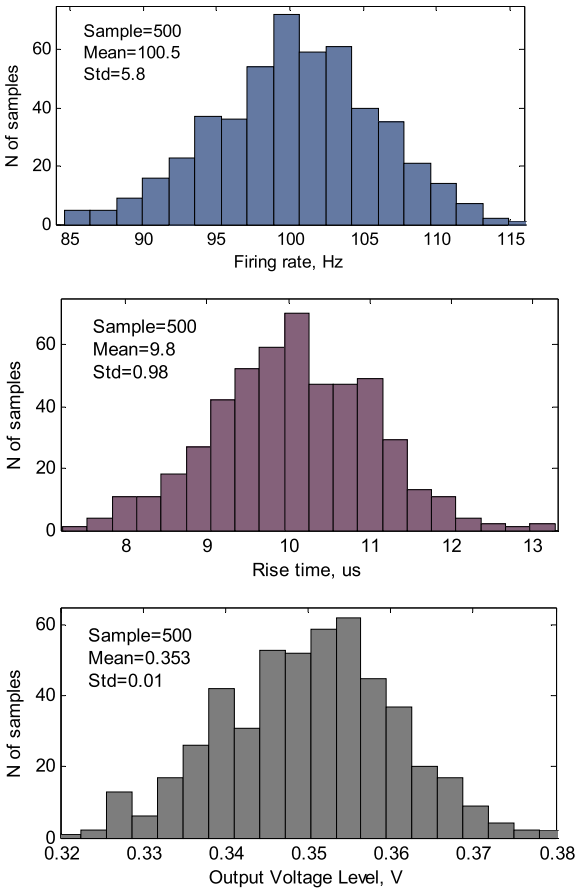


FIGURE 12. Monte-Carlo analysis results for 500 runs, from top to bottom: firing rate of the upgraded neuron, the rise time of the winning voltage of the upgraded WTA, and the output voltage level of the upgraded multi-threshold comparator.

subthreshold dynamics eased achieving a biologically plausible time constant that is essential for interacting with real environmental signals. In the near future, spiking neural networks will widely be used in medical implants, portable devices and other applications with stringent power supply conditions. In view of the above, a number of analog building blocks, powered with supply voltages (VDD) as low as 0.5V are required including silicon neuron, WTA, operational

amplifier, voltage comparator, synapse, and many others. Therefore, an interesting challenge that circuit and system designers will deal with could be implementing ultralow-power and ultralow-voltage spiking neural networks with the capability of interacting with real signals [36]–[38]. However, the designed learning module with a supply voltage of 0.5V can only be used in CMOS-based neural networks. In other words, synapses composed of emerging devices have a high degree of integration and it is almost impossible to change the weight (conductance) of most synapses under a 0.5V supply. Of course, synapses that are configured based on emerging devices can reduce energy consumption by reducing the current even when the operating voltage is somewhat high.

Table 2 reports the performance summary of the upgraded learning control module in comparison with other neuromorphic systems. It is worth mentioning that, the energy per spike of the sub-circuits (reported in Table 1) such as the neuron was calculated by (Power/Frequency) at its firing rate, described in [7]. Therefore, according to the SDSP learning rule, the energy paid for each SOP includes the contributions of reading and updating the synaptic weight, the associated neuron state, as well as the controller circuits for a biological time constant [1]. Of course, the values of the energy reported in Table 2 may not present a fair comparison because the energy consumption is dependent on several factors such as the membrane capacitance, supply voltage, silicon area, input patterns, firing rate, etc., which latter was set at a biological time constant for this work. However, it is obvious that if the traditional sub-circuits and an older LIF neuron are used instead of the upgraded ones, the supply voltage should be increased leading to a significant increase in the energy consumption.

To have a fair comparison for the occupied silicon area, the neuron core area (dotted box on the right in Fig. 1) and the synapse core area (dotted box on the left in Fig. 1) have separately been reported in Table 2, by which the silicon area can be estimated based on the count of the neurons and synapses. It is worth noting that the reported silicon areas of other works correspond to single neuron and single synapse, and do not include the controller circuits. In addition, the upgraded circuits have been designed using an old CMOS technology (TSMC 180-nm), while most of the other works were designed using newer technology nodes such as 22-nm that certainly reduces the silicon area. Indeed, a considerable part of the neuron core area was occupied by the membrane capacitance C_{mem}, the slow variable capacitance C_{u}, weight capacitance C_{w}, and the integration capacitance of the DPI circuit. Since the upgraded neuron is versatile and offers different oscillatory behaviors such as regular firing, chattering, and frequency adoption, the $C_{\text{u}} = 1.2\text{pF}$ was required to provide a slow variable parameter. In addition, the upgraded neuron used several current-mode subthreshold circuits with realistic time constants, which allow designers to reduce C_{mem} and C_{u} without losing the biological temporal dynamics. However, if C_{mem} is reduced below 0.1pF, the controllability of the firing rate will be affected by environmental noise after the fabrication, and it is way a C_{mem} of 0.4pF was allocated.

V. CONCLUSION

In this paper, several low-voltage neuromorphic circuits were designed in the subthreshold region to decrease the energy consumption of a spike-based learning control module. In the meantime, the silicon neuron was configured using the simplest adjustable circuitry blocks such as differential pair integrator, current mirror-based positive feedback, and low-voltage comparator offering different oscillatory behaviors with low energy consumption. Moreover, the structure of a traditional WTA circuit has been upgraded using an auxiliary path to improve low-voltage capabilities by which a 0.5V multi-threshold current comparator was presented. Employing the aforementioned sub-circuits in a spike-based learning control module provided low-voltage features leading to low energy consumption, while its stop-learning module and synaptic weight update module properly operate under a 0.5V supply voltage.

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