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An Interleaved High Step-Up DC-DC Converter Based on Integration of Coupled Inductor and Built-in-Transformer With Switched-Capacitor Cells for Renewable Energy Applications

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ABSTRACT This paper proposes an interleaved high step-up DC-DC converter with the coupled inductor (CI) and built-in transformer (BIT) for renewable energy applications. Two double-winding (2W) CIs and one triple-winding (3W) BIT are integrated with the switched-capacitor (SC) voltage multiplier cells (VMCs) to achieve high-voltage gains without extreme duty cycles. The CIs and BIT turns-ratios provide two other degrees of freedom—in addition to the duty cycle—to adjust the voltage gain that leads to increased design flexibility. The diodes turn off naturally under the zero-current switching (ZCS) conditions because their current falling rates are controlled by the leakage inductances of the CIs and BIT; therefore, the diodes' reverse-recovery problems are alleviated. Moreover, employing passive diode-capacitor clamp circuits, the voltage stresses of the switches are limited to a low value far less than the output voltage. Additionally, the leakage inductances energies are recycled and transferred to the output to further extend the voltage gain. Furthermore, due to the interleaved structure, the input current ripple and current stresses of the components are reduced. The proposed converter is analyzed in detail and then compared with similar converters that employed CIs and/or BIT along with passive/active clamp circuits for the MOSFETs. Finally, to verify the feasibility of the proposed converter, the experimental results of a 200 W prototype with output voltage of 400 V and voltage gain of 25 are presented.

INDEX TERMS DC-DC converter, high step-up, high-voltage gain, coupled inductor, built-in transformer, switched-capacitor (SC), voltage multiplier cell (VMS), photovoltaic, fuel cell, renewable energy.

I. INTRODUCTION

Renewable energy sources, such as photovoltaic (PV) and fuel cells have received much attention in recent years [1], [2]. A hybrid renewable energy-based system is shown in Fig. 1, where the PV and fuel cells are used as renewable energy sources; the voltage of these renewable energy sources is less than 50 V, which is relatively low compared to that of the DC link's voltage (e.g., 300-400 V) [3]. Thus, a high step-up DC-DC converter is required as an interface between the renewable energy sources and DC link, as depicted in Fig. 1.

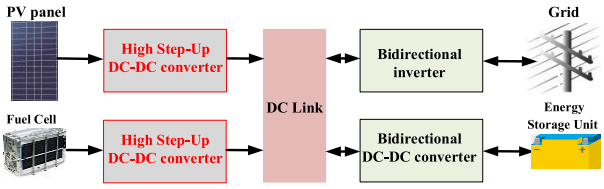

FIGURE 1. A hybrid renewable energy-based system with PV and fuel cells.

The traditional boost DC-DC converter can provide a high-voltage gain under extremely large duty cycles; however, it suffers from high voltage and current stresses in the semiconductor devices, reverse-recovery problem in the

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output, diode, large ripple on the input current and the output voltage and high power losses [4], [5]. To eliminate these effects, voltage-boosting (VB) techniques were presented to extend the voltage gain of the conventional boost converter without an extremely high duty cycle. The VB techniques are based on switch-capacitor (SC) voltage multiplier cells (VMCs) [6], switched-inductor (SL) VMCs [7], coupled-inductor (CI) [8], built-in transformer (BIT) [9], cascaded structure [10], quadratic converter [11], and Z-source/quasi Z-source converters [12]. Any potential combination of the mentioned VB techniques were considered to achieve a high step-up converter, such as those in [13]–[16]. Along with VB techniques, the interleaved structure is beneficial because a low input current ripple is obtained that reduces the size of the input filter, increases the lifetime of the renewable energy sources, reduces the current stresses on the components, and improves the efficiency [17], [18]. In [19]–[21], interleaved converters integrated with SC VMCs were introduced, and they suffered from high current transitions on the capacitors and required a large number of diodes and capacitors to achieve high-voltage gains. To eliminate the extreme instantaneous currents of the capacitors in the SC CMCs, the boost inductors can be replaced by CIs, or a BIT can be inserted into the converter topology—the energy stored in the leakage inductances of the CIs and BIT can be absorbed and recycled by either passive or active clamped techniques [22], [23]. In addition, the existence of the leakage inductances meant the current falling rates of diodes were controlled, and zero-current switching (ZCS) conditions are achieved in the turn-off instants of the diodes, thereby improving the converter efficiency. In [24], an interleaved converter was presented that integrated an asymmetric SC VMC with double-winding (2W) CIs and employed passive clamp circuits to recycle the energy of the leakage inductances and limit the voltage stresses on the main switches. Another 2W CI-based interleaved converter was introduced in [25] in which, like the topology in [24], the secondary windings of the CIs were integrated into SC VMCs to extend the voltage gain. Other 2W CI-based interleaved converters were proposed in [26]–[29]. The interleaved converters in [30]–[33] used two triple-winding (3W) CIs to further extend the voltage gains. The interleaved converters in [34] and [35] utilized the 2W and 3W BIT, respectively. In interleaved converters without CI and BIT, the voltage gain is only adjusted with the duty cycle of the main switches. By contrast, for the converters with either CI or BIT, there were two degrees of freedom—duty cycle and turns-ratio—that made the voltage gain adjustment flexible. The interleaved converters in [36], [37] took advantage of both the CI and BIT to further enhance the voltage gain; these converters utilized two 2W CIs and one 3W BIT, where the secondary windings of CIs, along with the secondary and tertiary windings of BIT, were combined with the SC VMCs to achieve a high voltage gain. Having three degrees of freedom for converters with both CI and BIT (duty cycle of the main switches, turns-ratio of the CIs, and turns-ratio of the BIT) resulted in a flexible deign that was appropriate for the high-voltage gain applications. Therefore, the usage of the CI together with BIT integrated with SC VMCs is the most effective technique used to further increase the voltage gain.

Considering the previously discussed information, in this paper, an interleaved high step-up DC-DC converter with two 2W CIs and one 3W BIT is proposed to achieve high-voltage gains without extremely high cycle cycles. Passive clamped circuits are used to absorb and recycle the leakage inductances energies and limit switches voltage stresses to a value far less than the output voltage. The leakage inductances provide the proposed converter with turn-off ZCS conditions for the diodes that improve efficiency. Also, the reverse recovery problem of the diodes is suppressed. The voltage gain and the voltage stresses for the semiconductor devices can be controlled flexibly by three parameters, including turns-ratio of the 2W CIs, turns-ratio of the 3W BIT, and duty cycle of the switches. Furthermore, low-voltage-rated semiconductor devices with low ON-state resistances are adopted for the proposed converter, thus leading to the reduction of the conduction losses. Additionally, due to the interleaved structure of the proposed converter, the input current ripple and the current stresses of the components decrease significantly.

The rest of this paper is organized as follows: Section II introduces the topology of the proposed converter and analyzes its operation modes. Section III presents a steady-state analysis of the proposed converter. The design considerations of the proposed converter are presented in Section IV. In Section V, a comparison analysis in terms of voltage gain, normalized voltage stresses, and components count is accomplished, and that proves the superior performance of the proposed converter compared to other similar existing counterparts. Section VI presents experimental results to validate the study, and the overall conclusion is presented in Section VII.

II. PROPOSED CONVERTER AND OPERATING MODES

The proposed converter is shown in Fig. 2; the power switches are denoted by Q_1 and Q_2, which are gated in interleaved manner with a 180° phase shift. There are two 2W CIs whose coupling references are denoted by "●" and"★"— each CI is modeled as the combination of a magnetizing inductance, an ideal 2W transformer, and the leakage inductance for each winding; L_{k1} and L_{k2} are the leakage inductances of primary

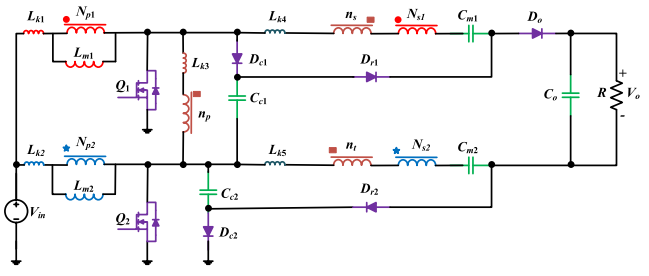

FIGURE 2. Proposed converter.

windings; L_{m1} and L_2 are the magnetizing inductances; N_{p1} and N_{p2} are the number of the primary turns; the secondary turns are shown by N_{s1} and N_{s2}. Also, there is a 3W BIT whose reference points are represented by "■"; the primary, secondary, and tertiary windings' turns of the BIT are denoted by n_p, n_s, and n_t, respectively; L_{k3} is the leakage inductance of the primary side for BIT. Each of secondary and tertiary windings of the BIT are connected in-series with the secondary winding of CI for each phase, resulting in the total leakage inductances of L_{k4} and L_{k5}. D_{c1} and D_{c2} are the clamp diodes; C_{c1} and C_{c2} are the clamp capacitors. Diode-capacitors pairs (D_{c1}, C_{c1}) and (D_{c2}, C_{c2}) make the clamp circuits, leading to limit the voltage stresses on switches Q_1 and Q_2, and they recycle the energy stored in the leakage inductances; D_{r1} and D_{r2} represent the regenerative diodes; C_{m1} and C_{m2} denote the intermediate energy storage capacitors; D_o and C_o represent the output diode and capacitor, respectively. There is a total of five diodes and five capacitors. The input voltage, output voltage, and load are represented by V_{in}, V_o, and R, respectively. The turns-ratios of the CIs represented by $N_1 = N_{s1}/N_{p1}$, $N_2 = N_{s2}/N_{p2}$; for the BIT, the turns-rations are denoted by $n_{sp} = n_s/n_p$ and $n_{tp} = n_t/n_p$. The duty cycle (D) of the power switches is more than 0.5, and during a switching period T, the proposed converter has 8 operation modes. Fig. 3 illustrates the key current waveforms of the proposed converter; it should be noted that the scales of the curves are not the same in Fig. 3. To analyze the proposed converter, the following assumptions are made: the converter operates at steady-state condition and continuous conduction mode (CCM); the capacitors are large enough such that their voltages are constant. The voltage drops on the diodes are neglected. The equivalent circuits for different operating modes are depicted in Fig. 4 and explained as follows:

Mode 1 (Fig. 4a, $t_0 \le t \le t_1$): This operating mode is too short and begins when switch Q_1 starts to conduct at $t = t_0$; switch Q_2 and output diode D_o keep their ON states from the previous operating mode (Mode 8). Leakage inductances L_{k3}, L_{k4}, and L_{k5} release their energies quickly to the output side through diode D_o. In addition, these leakage inductances control the current falling rate of D_o—accordingly, the reverse-recovery problem of D_o is alleviated by the leakage inductances. The current through magnetizing inductances L_{m1} and L_{m2} increase linearly. The relationships in this mode are as:

$$\begin{cases} V_{L_{m1}} = V_{in} - V_{L_{k1}} = L_{m1}\dfrac{di_{L_{m1}}(t)}{dt} \\ V_{L_{m2}} = V_{in} - V_{L_{k2}} = L_{m2}\dfrac{di_{L_{m2}}(t)}{dt} \end{cases} \tag{1}$$

$$\begin{cases} i_{Do}(t) = I_o + i_{Co}(t) = I_o + C_o\dfrac{dV_o(t)}{dt} \\ \qquad = i_{Lk4}(t) = -i_{Lk5}(t) \\ i_{Lk1}(t) = i_{Lm1}(t) + i_{p1}(t) = i_{Lm1}(t) - N_1 i_{Do}(t) \\ i_{Lk2}(t) = i_{Lm2}(t) + i_{p2}(t) = i_{Lm2}(t) + N_2 i_{Do}(t) \end{cases} \tag{2}$$

$$\begin{cases} (n_{sp} + n_{tp})V_{Lk3} = -V_{Lk4} + V_{Lk5} - V_o - N_1 V_{Lm1} \\ \qquad\qquad +N_2 V_{Lm2} + V_{Cm1} + V_{Cm2} \end{cases} \tag{3}$$

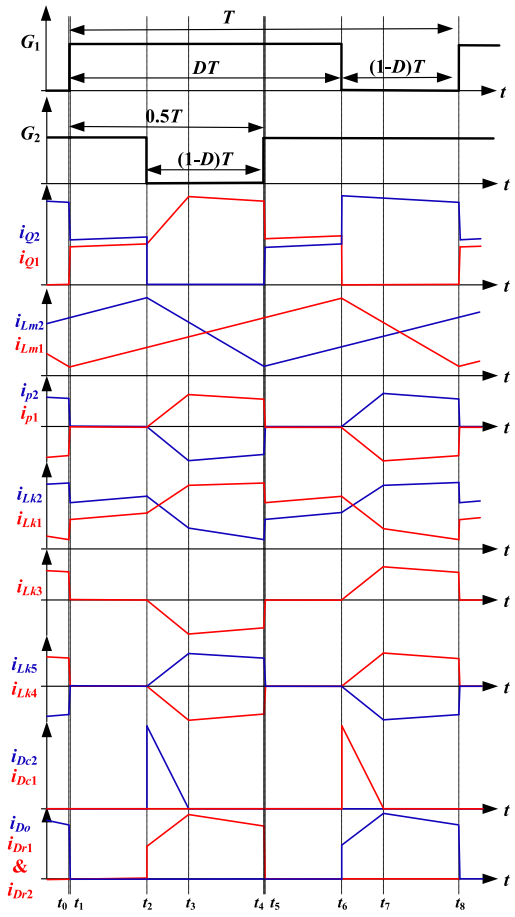

FIGURE 3. Key waveforms of the proposed converter.

$$\begin{cases} (n_{sp} + n_{tp})L_{k3}\dfrac{di_{L_{k3}}(t)}{dt} \\ \qquad = -L_{k4}\dfrac{di_{L_{k4}}(t)}{dt} + L_{k5}\dfrac{di_{L_{k5}}(t)}{dt} - V_o \\ \qquad\qquad -N_1 V_{L_{m1}} + N_2 V_{L_{m2}} + V_{C_{m1}} + V_{C_{m2}} \end{cases} \tag{4}$$

Mode 2 (Fig. 4b, $t_1 \le t \le t_2$): This operation mode begins when D_o turns off with ZCS condition at $t = t_1$; both switches Q_1 and Q_2 remain in ON state. Inductances L_{m1}, L_{m2}, L_{k1}, and L_{k2} are charged by the input voltage, and the load is supplied solely by the output capacitor. The key relationships are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ i_{L_{m1}}(t) = i_{L_{k1}}(t) = i_{L_{m1}}(t_1) + \dfrac{V_{in}}{L_{m1} + L_{k1}}(t - t_1) \\ i_{L_{m2}}(t) = i_{L_{k2}}(t) = i_{L_{m2}}(t_1) + \dfrac{V_{in}}{L_{m2} + L_{k2}}(t - t_1) \end{cases} \tag{5}$$

Mode 3 (Fig. 4c, $t_2 \le t \le t_3$): At $t = t_2$, the gate signal becomes zero for Q_2, and clamp diode D_{c2} turns on to clamp the voltage across Q_2 to V_{Cc2}; simultaneously, regenerative diodes D_{r1} and D_{r2} start to conduct because the reverse voltages across them becomes zero. As the currents through diodes D_{r1} and D_{r2} increase, the current through diode D_{c2} decreases. By means of the conducting current through the

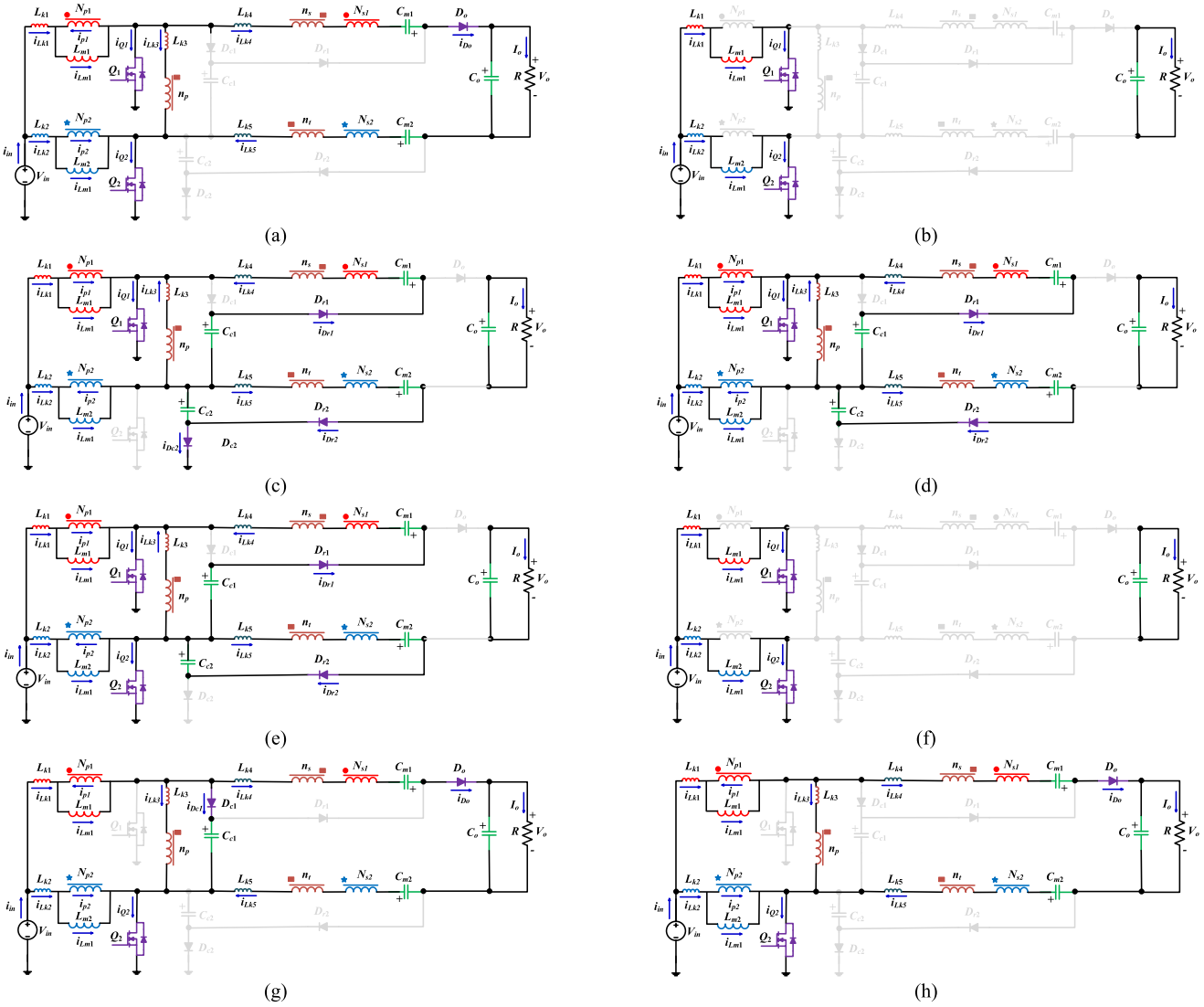

FIGURE 4. Operation modes in one switching period: (a) Mode 1 [t_0-t_1], (b) Mode 2 [t_1-t_2], (c) Mode 3 [t_2-t_3], (d) Mode 4 [t_3-t_4], (e) Mode 5 [t_4-t_5], (f) Mode 6 [t_5-t_6], (g) Mode 7 [t_6-t_7], (h) Mode 8 [t_7-t_8].

secondary windings of the CIs and secondary and tertiary windings of the BIT, clamp capacitor C_{c1} is discharged and intermediate capacitors C_{m1} and C_{m2} are charged. The magnetizing inductance L_{m1} is charged, while L_{m2} transfers the energy to the secondary side. When the energy of leakage inductance L_{k2} is completely absorbed by C_{c2}, diode D_{c2} is reverse-biased and turns off with ZCS condition at the end of this mode. The relationships for this mode are as (6)-(8).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} - V_{C_{c2}} \\ V_{p_{BIT}} + V_{L_{k3}} = -V_{C_{c2}} \end{cases} \tag{6}$$

$$\begin{cases} N_1 V_{L_{m1}} + V_{L_{k4}} + n_{sp} V_{L_{k3}} \\ \qquad = V_{C_{m1}} - V_{C_{c1}} - (n_{sp}+1) V_{C_{c2}} \\ N_2 V_{L_{m2}} + V_{L_{k5}} - n_{tp} V_{L_{k3}} = (n_{tp}+1) V_{C_{c2}} - V_{C_{m2}} \end{cases} \tag{7}$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_{r1}}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_{r2}}(t) \\ i_{L_{k3}}(t) = -n_{sp} i_{D_{r1}}(t) - n_{tp} i_{D_{r2}}(t) \\ i_{L_{k4}}(t) = -i_{D_{r1}}(t) \\ i_{L_{k5}}(t) = i_{D_{r2}}(t) \end{cases} \tag{8}$$

Mode 4 (Fig. 4d, $t_3 \le t \le t_4$): At $t = t_3$, clamp diode D_{c2} turns off with ZCS condition because its current decreases to zero after the leakage energy of L_{k2} is fully transferred. The diode current rate is controlled by the leakage inductance, thus there is no turn-off reverse-recovery problem. The currents of both diodes D_{r1} and D_{r2} start to decrease. The mechanism of the energy transferring is the same as the previous operation mode. In this mode, the relationships are

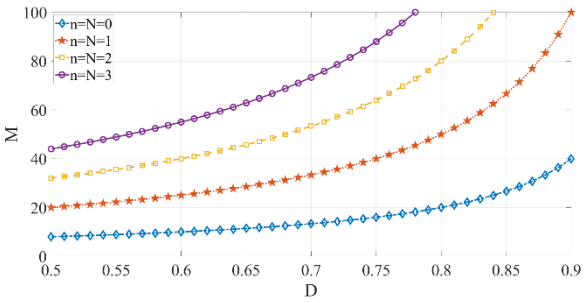

FIGURE 5. Voltage gain versus duty cycle for different values of *N* and *n*.

obtained as (9)-(12).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} - V_{p_{BIT}} - V_{L_{k3}} = V_{in} \\ V_{p_{BIT}} + V_{L_{k3}} = V_{L_{m2}} + V_{L_{m1}} + V_{L_{k2}} - V_{L_{k1}} \end{cases} \tag{9}$$

$$\begin{cases} (N_1 + n_{sp} + 1)V_{L_{m1}} - (n_{sp} + 1)(V_{L_{m2}} + V_{L_{k2}} - V_{L_{k1}}) \\ +V_{L_{k4}} + n_{sp}V_{L_{k3}} = V_{C_{m1}} - V_{C_{c1}} \end{cases} \tag{10}$$

$$\begin{cases} n_{tp}(V_{L_{m1}} + V_{L_{k1}} + V_{L_{k3}} - V_{L_{k2}}) \\ -(N_2 + n_{tp})V_{L_{m2}} - V_{L_{k5}} = V_{C_{m2}} - V_{C_{c2}} \end{cases} \tag{11}$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_{r1}}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_{r2}}(t) \\ i_{L_{k3}}(t) = -n_{sp} i_{D_{r1}}(t) - n_{tp} i_{D_{r2}}(t) \\ i_{L_{k4}}(t) = -i_{D_{r1}}(t) \\ i_{L_{k5}}(t) = i_{D_{r2}}(t) \end{cases} \tag{12}$$

Mode 5 (Fig. 5e, $t_4 \le t \le t_5$): At $t = t_4$, this mode begins when switch Q_2 turns on. This operation mode ends when the currents through regenerative diodes D_{r1} and D_{r2} decrease to zero, and accordingly, the energy at the secondary/tertiary windings of the CIs and BIT reaches zero. D_{r1} and D_{r2} turn off with ZCS condition at $t = t_5$. The circuit relationships of this mode are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{p_{BIT}} = -V_{L_{k3}} \end{cases} \tag{13}$$

$$\begin{cases} N_1 V_{L_{m1}} + V_{L_{k4}} + n_{sp} V_{L_{k3}} = V_{C_{m1}} - V_{C_{c1}} \\ -N_2 V_{L_{m2}} - V_{L_{k5}} + n_{tp} V_{L_{k3}} = V_{C_{m2}} - V_{C_{c2}} \end{cases} \tag{14}$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_{r1}}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_{r2}}(t) \\ i_{L_{k3}}(t) = -n_{sp} i_{D_{r1}}(t) - n_{tp} i_{D_{r2}}(t) \\ i_{L_{k4}}(t) = -i_{D_{r1}}(t) \\ i_{L_{k5}}(t) = i_{D_{r2}}(t) \end{cases} \tag{15}$$

Mode 6 (Fig. 4f, $t_5 \le t \le t_6$): Diodes D_{r1} and D_{r2} turn off at $t = t_5$, while switches Q_1 and Q_2 remain in ON state. Magnetizing inductances L_{m1} and L_{m2} are charged by the input voltage, which is the same as Mode 2. The relationships are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{p_{BIT}} = 0 \end{cases} \tag{16}$$

$$\begin{cases} i_{L_{m1}}(t) = i_{L_{k1}}(t) = i_{L_{m1}}(t_6) + \dfrac{V_{in}}{L_{m1} + L_{k1}}(t - t_6) \\ i_{L_{m2}}(t) = i_{L_{k2}}(t) = i_{L_{m2}}(t_6) + \dfrac{V_{in}}{L_{m2} + L_{k2}}(t - t_6) \\ i_{p1}(t) = i_{p2}(t) = i_{L_{k3}}(t) = i_{L_{k4}}(t) = i_{L_{k5}}(t) = 0 \end{cases} \tag{17}$$

Mode 7 (Fig. 4g, $t_6 \le t \le t_7$): This mode is similar to Mode 3. At $t = t_6$, clamp diode D_{c1} is forward-biased, then the voltage across Q_1 is clamped to V_{Cc1}; the voltage across output diode D_o reaches zero, and it is forward-biased. The stored energy in magnetizing inductance L_{m1} is transferred to the secondary side. As the current through D_o increases, the current through D_{c1} decreases. Intermediate capacitors C_{m1} and C_{m2} are discharged. The relationships for this mode aren as (18)-(20).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{p_{BIT}} + V_{L_{k3}} = V_{C_{c1}} \end{cases} \tag{18}$$

$$\begin{cases} N_2 V_{L_{m2}} - N_1 V_{L_{m1}} - V_{L_{k4}} + V_{L_{k5}} \\ -(n_{sp} + n_{tp})V_{L_{k3}} \\ \quad = V_o - (n_{sp} + n_{tp} + 1)V_{C_{c1}} - V_{C_{m1}} - V_{C_{m2}} \end{cases} \tag{19}$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = (n_{sp} + n_{tp}) i_{D_o}(t) \\ i_{L_{k4}}(t) = i_{D_o}(t) \\ i_{L_{k5}}(t) = -i_{D_o}(t) \end{cases} \tag{20}$$

Mode 8 (Fig. 4h, $t_7 \le t \le t_8$): At $t = t_7$, the current through clamp diode D_{c1} decreases to zero, and it turns off with ZCS condition due to leakage inductance L_{k1}. The current of D_o starts to decrease, and its decreasing rate is controlled by the leakage inductances. The energy stored in the magnetizing inductor L_{m1} is continuously transferred to output. The relationships for this mode are as:

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} + V_{p_{BIT}} + V_{L_{k3}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ V_{p_{BIT}} + V_{L_{k3}} = V_{L_{m2}} - V_{L_{m1}} + V_{L_{k2}} - V_{L_{k1}} \end{cases} \tag{21}$$

$$\begin{cases} -(N_1 + n_{sp} + n_{tp} + 1)V_{L_{m1}} \\ \quad +(N_2 + n_{sp} + n_{tp} + 1)V_{L_{m2}} \\ -(n_{sp} + n_{tp})V_{L_{k3}} + (n_{sp} + n_{tp} + 1)(V_{L_{k2}} - V_{L_{k1}}) \\ -V_{L_{k4}} + V_{L_{k5}} = V_o - V_{C_{m1}} - V_{C_{m2}} \end{cases} \tag{22}$$

$$\begin{cases} i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = (n_{sp} + n_{tp}) i_{D_o}(t) \\ i_{L_{k4}}(t) = i_{D_o}(t) \\ i_{L_{k5}}(t) = -i_{D_o}(t) \end{cases} \tag{23}$$

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

To simplify the steady-state analysis of the proposed converter, Modes 1 and 5 with the short durations were ignored.

A. VOLTAGE GAIN

Ignoring the leakage inductances, Modes 3 and 4 are the same; similarly, Modes 7 and 8 are assumed to be the same. The, by applying the voltage–second balance law to magnetizing inductances L_{m1} and L_{m2}, the following equations are written:

$$2(D-\frac{1}{2})V_{in}+2(1-D)V_{in}+(1-D)V_{C_{c1}}=0 \quad (24)$$

$$2(D-\frac{1}{2})V_{in}+2(1-D)V_{in}+(1-D)V_{C_{c2}}=0 \quad (25)$$

From (24) and (25), the voltages on capacitors C_{c1} and C_{c2} are obtained as:

$$V_{C_{c1}}=V_{C_{c2}}=\frac{1}{1-D}V_{in} \quad (26)$$

Considering Mode 3, the following relationship is written:

$$\begin{cases} V_{C_{m1}}=V_{C_{c1}}+(n_{sp}+1)V_{C_{c2}}+N_1V_{in} \\ V_{C_{m2}}=(n_{tp}+1)V_{C_{c2}}-N_2(V_{in}-V_{C_{c2}}) \end{cases} \quad (27)$$

Substituting (26) in (27), the voltages across capacitors C_{m1} and C_{m2} are obtained as:

$$\begin{cases} V_{C_{m1}}=\dfrac{2+n_{sp}+(1-D)N_1}{1-D}V_{in} \\ V_{C_{m2}}=\dfrac{1+n_{tp}+DN_2}{1-D}V_{in} \end{cases} \quad (28)$$

Considering Mode 7, the following equation is obtained:

$$V_o=(n_{sp}+n_{tp}+1)V_{C_{c1}}+V_{C_{m1}}+V_{C_{m2}} \quad (29)$$

Substituting (26) and (28) in (29), the voltage of the output capacitor is extracted as:

$$V_{C_o}=V_o=\frac{4+2(n_{sp}+n_{tp})+N_1+N_2}{1-D}V_{in} \quad (30)$$

Accordingly, the ideal voltage gain is obtained as:

$$M=\frac{V_o}{V_{in}}=\frac{4+2(n_{sp}+n_{tp})+N_1+N_2}{1-D} \quad (31)$$

If the turns-ratios of the CIs are equal to N (i.e., $N_1=N_2=N$) and the turns-ratios of the BIT are equal to n (i.e., $n_{sp}=n_{tp}=n$), the capacitors' voltages and voltage gain are simplified as:

$$\begin{aligned} V_{C_{c1}}&=V_{C_{c2}}=\frac{1}{1-D}V_{in} \\ V_{C_{m1}}&=\frac{2+n+(1-D)N}{1-D}V_{in} \\ V_{C_{m2}}&=\frac{1+n+DN}{1-D}V_{in} \\ V_{C_o}&=V_o=\frac{4+4n+2N}{1-D}V_{in} \end{aligned} \quad (32)$$

$$M=\frac{V_o}{V_{in}}=\frac{4+4n+2N}{1-D}=\frac{4(1+n+\frac{N}{2})}{1-D} \quad (33)$$

As explored in the above analysis, the voltage gain of the proposed converter is controlled by three parameters: the turns-ratio of the CIs (N), the turns-ratio of the BIT (n), and the duty cycle of the switches (D); thus, there are three degrees of freedom to extend the voltage gain without an extreme duty cycle at high voltage gains. The plot of the voltage gain is sketched in Fig. 5 for different values of N, n, and D. As observed, the voltage gain increases significantly as the duty cycle and the turns-ratios increase, which makes the proposed converter reach high voltage gains without extreme duty cycles in high step-up applications.

B. EFFECT OF LEAKAGE INDUCTANCES ON VOLTAGE GAIN

In fact, the leakage inductances of the CIs and BIT are not zero. By analyzing the current of the output diode, the effect of leakage inductances on the voltage gain is clarified. The current of D_o flows through the circuits during Modes 7 and 8; the duration of the Mode 7 ($\Delta t_7 = t_7$-t_6) is supposed to be $0.6\times(1-D)T$ for the designed converter in this paper. Additionally, the current-falling rate of diode D_o ($\mathrm{d}i_{Do}/\mathrm{d}t$) is nearly zero during Mode 8. Additionally, the average current of D_o is equal to the output current (I_o). Thus, the peak current of the output diode can be obtained as:

$$\begin{cases} \dfrac{1}{T}\displaystyle\int_0^T i_{Do}(t)=I_o \\ \rightarrow \dfrac{1}{T}\left(\begin{matrix}\frac{1}{2}\times 0.6\times(1-D)T\times I_{D_o,peak} \\ +0.4\times(1-D)T\times I_{D_o,peak}\end{matrix}\right)=I_o \\ \rightarrow I_{D_o,peak}=\dfrac{10I_o}{7(1-D)} \end{cases} \quad (34)$$

Knowing the peak current of D_o, the voltage gain is obtained in (35), as shown at the bottom of the next page.

As obvious, the voltage gain reduces slightly as the leakage inductances increase.

C. SEMICONDUCTOR DEVICES VOLTAGE STRESSES

The voltage stresses of the semiconductor devices are given by (36)-(41).

$$V_{Q_1}=V_{Q_2}=\frac{1}{1-D}V_{in}=\frac{1}{4(1+n+\frac{N}{2})}V_o \quad (36)$$

$$V_{D_{c1}}=\frac{2}{1-D}V_{in}=\frac{1}{2(1+n+\frac{N}{2})}V_o \quad (37)$$

$$V_{D_{c2}}=\frac{1}{1-D}V_{in}=\frac{1}{4(1+n+\frac{N}{2})}V_o \quad (38)$$

$$V_{D_{r1}}=\frac{2(1+n+\frac{N}{2})}{1-D}V_{in}=\frac{1}{2}V_o \quad (39)$$

$$V_{D_{r2}}=\frac{2n+N}{1-D}V_{in}=\frac{n+\frac{N}{2}}{2(1+n+\frac{N}{2})}V_o \quad (40)$$

$$V_{D_o}=\frac{2(1+2n+N)}{1-D}V_{in}=\frac{1+2n+N}{2(1+n+\frac{N}{2})}V_o \quad (41)$$

As the turns-ratio of either CIs or BIT increases, the voltage stresses of semiconductors D_{c1}, D_{c2}, Q_1, and Q_2 decrease significantly when compared to the output voltage; thus, low-voltage-rated switches with a low $R_{DS(on)}$ are employed, which reduces the conduction losses. Also, the voltage stress of the regenerative diode D_{r1} is equal to half the output voltage, and V_{Dr2} is less than the output voltage.

D. COMPONENTS AVERAGE CURRENT

The average currents of the leakage and magnetizing inductances are calculated as:

$$\begin{cases} I_{Lm1} = I_{Lm2} = I_{Lm} = \dfrac{2+2n+N}{1-D} I_o \\ I_{L_{k1}} = I_{L_{k2}} = I_{Lm} \\ I_{L_{k3}} = I_{L_{k4}} = I_{L_{k5}} = 0 \end{cases} \tag{42}$$

The average root mean square (rms) currents of the semiconductor devices are as:

$$\begin{cases} I_{D_{c1_{avg}}} = I_{D_{c2_{avg}}} = I_{D_{r1_{avg}}} = I_{D_{r2_{avg}}} = I_{D_{o_{avg}}} = I_o \\ I_{Q_{1_{avg}}} = I_{Q_{2_{avg}}} = \dfrac{2+2n+N}{1-D} I_o \end{cases}$$

$$\begin{cases} I_{D_{c1_{rms}}} = I_{D_{c2_{rms}}} = \dfrac{10}{3\sqrt{2(1-D)}} I_o \\ I_{D_{r1_{rms}}} = I_{D_{r2_{rms}}} = I_{D_{o_{rms}}} \\ \quad = \dfrac{2+2n+N}{(1+2n+N)\sqrt{1-D}} I_o \\ I_{Q_{1_{rms}}} = I_{Q_{2_{rms}}} = \dfrac{(4+4n+2N)\sqrt{D}}{1-D} I_o \end{cases} \tag{43}$$

IV. DESIGN CONSIDERATIONS

A. COUPLED INDUCTORS AND BUILT-IN TRANSFORMER DESIGN

1) LIMITATION OF TURNS-RATIOS

Given that the duty cycle of the switches is higher than 0.5, it can be written as:

$$D = 1 - \frac{4(1+n+\frac{N}{2})}{M} \geq 0.5 \rightarrow n + \frac{N}{2} \leq \frac{M-8}{8} \tag{44}$$

2) MAGNETIZING INDUCTANCES OF CIS

For any arbitrary ripple current, $L_{m1} = L_{m2} = L_m$ is obtained from:

$$L_m = \frac{V_{in} D}{f_{sw} \Delta i_L} \tag{45}$$

To operate in CCM, the magnetizing inductance of CIs must be higher than the critical inductance that is obtained from (46).

$$\begin{cases} \Delta i_{Lm} = \dfrac{V_{in} D}{f_{sw} L_m} = \dfrac{V_o D}{f_{sw} L_m M} \\ \mathrm{I}_{Lm} = I_{Lm1} = I_{Lm2} = \dfrac{2+2n+N}{1-D} I_o = \dfrac{M}{2} I_o \\ R = \dfrac{V_o}{I_o} \end{cases}$$

$$\Delta i_{Lm} = 2 I_{Lm} \rightarrow L_m = L_{crit} \rightarrow L_{crit} = \frac{DR}{M^2 f_{sw}} \tag{46}$$

3) NUMBER OF TURNS OF CIS' WINDINGS

Having the flux density variation (ΔB_{CI}) and the cross-sectional area of the core ($A_{c,\mathrm{CI}}$) for the CIs, the number of turns for the primary winding (N_p) is determined from (47); then, the number of the secondary winding' turns (N_s) is obtained by having the CIs turns-ratio (N).

$$N_p = \frac{V_{in} D}{\Delta B_{CI} A_{c,CI} f_{sw}} \tag{47}$$

4) NUMBER OF TURNS OF BIT'S WINDINGS

Using ΔB_{BIT} and $A_{c,\mathrm{BIT}}$ for the BIT mean the number of turns for the primary winding (n_p) is calculated from (48), and the numbers of turns for the secondary and tertiary windings (n_s, n_t) are obtained from the obtained BIT turns-ratio (n).

$$n_p = \frac{V_{C_{c1}} D}{\Delta B_{BIT} A_{c,BIT} f_{sw}} = \frac{V_{in} D}{(1-D) \Delta B_{BIT} A_{c,BIT} f_{sw}} \tag{48}$$

B. CAPACITORS DESIGN

The voltages of the capacitors are determined from (32). By knowing the maximum ripple voltages ($\Delta V_{C\max}$) of the capacitors, the capacitances can be determined as:

$$\begin{cases} C_{c1}, C_{c1}, C_{m1}, C_{m2} \geq \dfrac{4+4n+2N}{5 f_{sw}(1+2n+N) \Delta V_{C\max}} I_o \\ C_o \geq \dfrac{D I_o}{f_{sw} \Delta V_{C\max}} \end{cases} \tag{49}$$

V. CIRCUIT PERFORMANCE COMPARISON

In this section, comparisons are made between the proposed converter and other interleaved high step-up converters in terms of the component's numbers, voltage gains, normalized voltage stress on power switches, and normalized total voltage stress on all diodes, as listed in Table 1; the voltages are normalized to the input voltage. The high step-up converters in [16], [34], [35] are based on the integration the normal inductor and BIT with the SC VMCs, and the converters in [27], [30], [32], [33] extend the voltage gain through integration the CIs with the SC VMCs. To adjust the voltage gain, there are two degrees of freedom for the converters in [16], [27], [30], [32]–[35], one of which is the duty cycle of the switches and the other is the turns-ratio of the

$$M = \frac{4(1+n+\frac{N}{2})}{1-D+\frac{50 f_{sw}}{21(1-D)R}\left(N^2(L_{k1}+L_{k2}) + 4n^2 L_{k3} + L_{k4} + L_{k5}\right)} \tag{35}$$

TABLE 1. Comparison of proposed converter with other interleaved high step-up converters.

Converter	Number of		Voltage gain (M)	Normalized voltage stress on switches	Normalized total voltage stress on all diodes
	Switches/ Diodes/ Capacitors	Inductors/CIs/ BIT/ Total magnetic cores			
Ref. [16]	2/6/5	2/0/1/3	$\frac{2(1+n)}{1-D}$	$\frac{1}{2+2n}M$	$\frac{3+4n}{1+n}M$
Ref. [27]	2/6/5	0/2/0/2	$\frac{2(1+N)}{1-D}$	$\frac{1}{2+2N}M$	$\frac{3+2N}{1+N}M$
Ref. [30]	2/2/1	0/2/0/2	$\frac{1+N}{1-D}$	$\frac{1}{1+N}M$	$\frac{2+3N}{1+N}M$
Ref. [32]	2/6/5	0/2/0/2	$\frac{2(1+N)}{1-D}$	$\frac{1}{2+2N}M$	$\frac{3+4N}{1+N}M$
Ref. [33]	2/6/5	0/2/0/2	$\frac{2(1+N)}{1-D}$	$\frac{1}{2+2N}M$	$\frac{3+4N}{1+N}M$
Ref. [34]	4/4/3	2/0/1/3	$\frac{1+n}{1-D}$	$\frac{1}{1+n}M$	$4M$
Ref. [35]	4/4/5	2/0/1/3	$\frac{2(1+n)}{1-D}$	$\frac{1}{2+2n}M$	$4M$
Ref. [36]	2/6/5	0/2/1/2	$\frac{2(1+n+\frac{N}{2})}{1-D}$	$\frac{1}{2+2n+N}M$	$\frac{6+8n+4N}{2+2n+N}M$
Ref. [37]	2/8/7	0/2/1/2	$\frac{2(1+n+N)}{1-D}$	$\frac{1}{2+2n+2N}M$	$\frac{3+4n+2N}{1+n+N}M$
Proposed converter	2/5/5	0/2/1/2	$\frac{4(1+n+\frac{N}{2})}{1-D}$	$\frac{1}{4+4n+2N}M$	$\frac{7+8n+4N}{4+4n+2N}M$

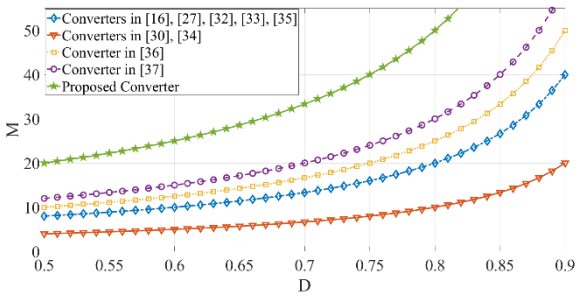

FIGURE 6. The voltage gain comparison for $N = n = 1$.

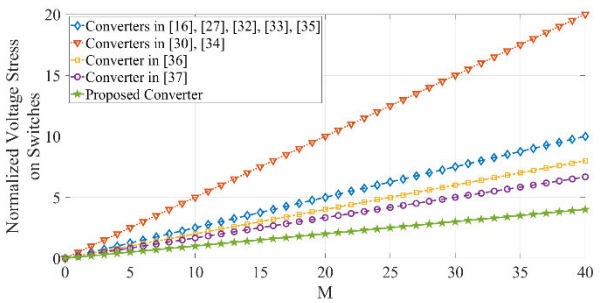

FIGURE 7. The comparison of the normalized voltage stress on switches for $N = n = 1$.

CIs or BIT. However, the proposed converter and converters in [36], [37] offer three degrees of freedom (i.e., D, n, N) for adjusting the voltage gain because they are developed based on the combination of BIT and CIs into the SC VMCs, which results in a flexible deign that is appropriate for high-voltage gain applications. The converters in [16], [34], [35] have three magnetic cores, while other converters and proposed converter have two magnetic cores.

In the comparison of the voltage gain, as seen from Fig. 6, the proposed converter has the highest voltage gain for the whole duty cycle range. According to Fig. 7, illustrating the normalized voltage stress on the switches, the proposed converter offers the lowest voltage stress on the switches under the same turns-ratios and voltage gain. As for the voltage stresses on the diodes, it is fair to compare the total voltage stress on all the diodes, which is performed in the last cilium of Table 1 and depicted in Fig. 8. As obvious, under the voltage gain and input voltage, the proposed converter provides the lowest total voltage stress on the diodes compared to other converters. Thus, semiconductor devices with low ON-state resistances and low-forward-voltage drops could be employed, which reduces the conduction losses and converter cost.

Among all the converters, the two converters in [36], [37] are the most similar ones to the proposed converter. Like the proposed converter, the converters in [36], [37] took advantage of an interleaved structure with two 2W CIs and one 3W BIT to achieve high voltage gains. Also, all three converters

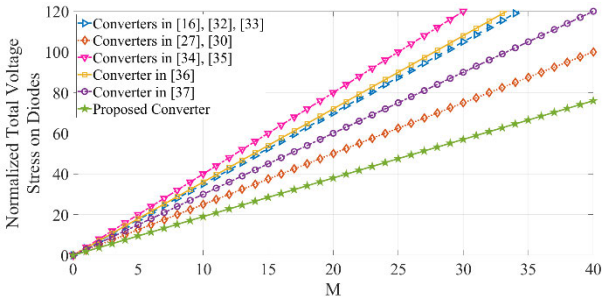

FIGURE 8. The comparison of the normalized total voltage stress on diodes for $N = n = 1$.

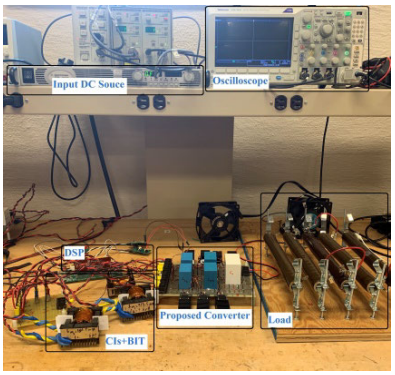

FIGURE 9. The experimental prototype.

employ passive diode-capacitor clamp circuits to absorb the leakage energy of the circuit and pass it to the output to further extend the voltage gain. However, the proposed converter approximately doubles the voltage gain under the same turns- ratios and duty cycle conditions and with lower number of components compared with the converters in [36], [37]. Furthermore, for a given voltage gain with the same turns-ratios for the magnetically coupled devices, the proposed converter has a smaller duty cycle compared to the converters in [16], [27], [30], [32]–[37]; thus, according to (49), the proposed converter has the smallest output voltage ripple.

VI. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed converter, an experimental setup was developed, as shown in Fig. 9, with the specifications listed in Table 2. Ferrite cores ETD59/31/22-3C97 and ETD54/28/19-3C90 were used to implement the 2W CIs and 3W BIT, respectively. The DC resistances of the windings for 2W CIs are as $R_{p1} = R_{s1} = R_{p2} = R_{s2} = 0.01\ \Omega$, and for the 3W BIT, the windings' DC resistances are as $R_p = R_s = R_t = 0.06\ \Omega$, where R_p, R_s, and R_t represent the DC resistances of the primary, secondary, and tertiary windings, respectively.

Figs. 10(a)-(h) show the experimental current and voltage waveforms for in the input voltage of 16 V and duty cycle of 0.6. According to Fig. 10(a), the measured output voltage and current are 391 V and 0.5 A, respectively. As exemplified, the proposed converter achieves a high voltage of 391 V from

TABLE 2. Specifications of experimental setup.

Parameters/Components	Values/Part Number
Output voltage V_o	400 V
Rated power	200 W
Switching frequency f_{sw}	50 kHz
Capacitors C_{c1} and C_{c2}	B32776G4506K000 50 µF, ESR=0.004 Ω
Capacitors C_{cm1} and C_{cm2}	B32678G4206K000 20 µF, ESR=0.0033 Ω
Capacitor C_o	C4AEOBW5200A3LJ 20 µF, R_C=0.0039 Ω
Turns-ratios N and n	1
Magnetizing inductances L_{m1} and L_{m2}	190 µH
Leakage inductances L_{k1} and L_{k2}	1.5 µH
Leakage inductances L_{k3}	3 µH
Leakage inductances L_{k4} and L_{k5}	4.5 µH
Switches Q_1 and Q_2	PSMN016-100PS $R_{DS(on)}$=0.0288 Ω, C_{oss}=189 pF
Diodes D_{c1}, D_{c2}, D_{r1}, and D_{r2}	LQA06T300 R_D=0.1 Ω, V_F=0.45 V
Output diode D_o	C3D10060A R_D=0.17 Ω, V_F=0.75 V

a low input voltage of 16 V with the duty cycle of 0.6 that is not an extreme duty cycle. There is a deviation of 9 V from the ideally calculated 400 V in (32), which is due to the parasitic elements of the circuit. Fig. 10(b) illustrates the voltages across capacitors C_{c1}, C_{c2}, C_{m1}, and C_{m2}, which are relatively in agreement with the values calculated from (32), namely are $V_{Cc1} = V_{Cc2} = 40$ V, $V_{Cm1} = 136$ V, and $V_{Cm2} = 104$ V. The semiconductors' voltages and currents are shown in Figs. 10(c)-(f). As presented, the measured voltage stresses match theoretically calculated values from (36) and (39)-(41) as $V_{Q1} = V_{Q2} = 40$ V, $V_{Dr1} = 200$ V, $V_{Dr2} = 120$ V, and $V_{Do} = 320$ V. As seen, the voltage stresses across the switches are far less than the high output voltage, thus leading to adopting low-voltage-rated MOSFETs with low ON-state resistances. In addition, there is no reverse-recovery problem for the diodes because they turn off naturally with ZCS conditions. Fig. 10(g) shows the input current and currents of leakage inductances L_{k1} and L_{k2}. The input current ripple is small, and that is beneficial for the input renewable energy source. The average currents of L_{k1} and L_{k2} are about 6.25 A, showing a proper current sharing between CIs in the interleaved structures, thereby resulting in the reduction of the components' current stresses. The currents of leakage inductances L_{k3}, L_{k4}, and L_{k5} are shown in Fig. 10(h), and they agree with Fig. 3.

In addition, the dynamic response of the output voltage for a 40% step change in the output load is depicted in Fig. 10(i). The output power is changed from 200 W to 120 W and vice versa. This dynamic response illustrates the inherent stability of the proposed converter; there is a little voltage change that can be eliminated if a closed-loop control with a proper bandwidth is employed to manipulate the duty cycle of the switches for compensating the voltage change.

Fig. 11 shows the measured efficiency curve of the proposed converter for the various load powers—with the input

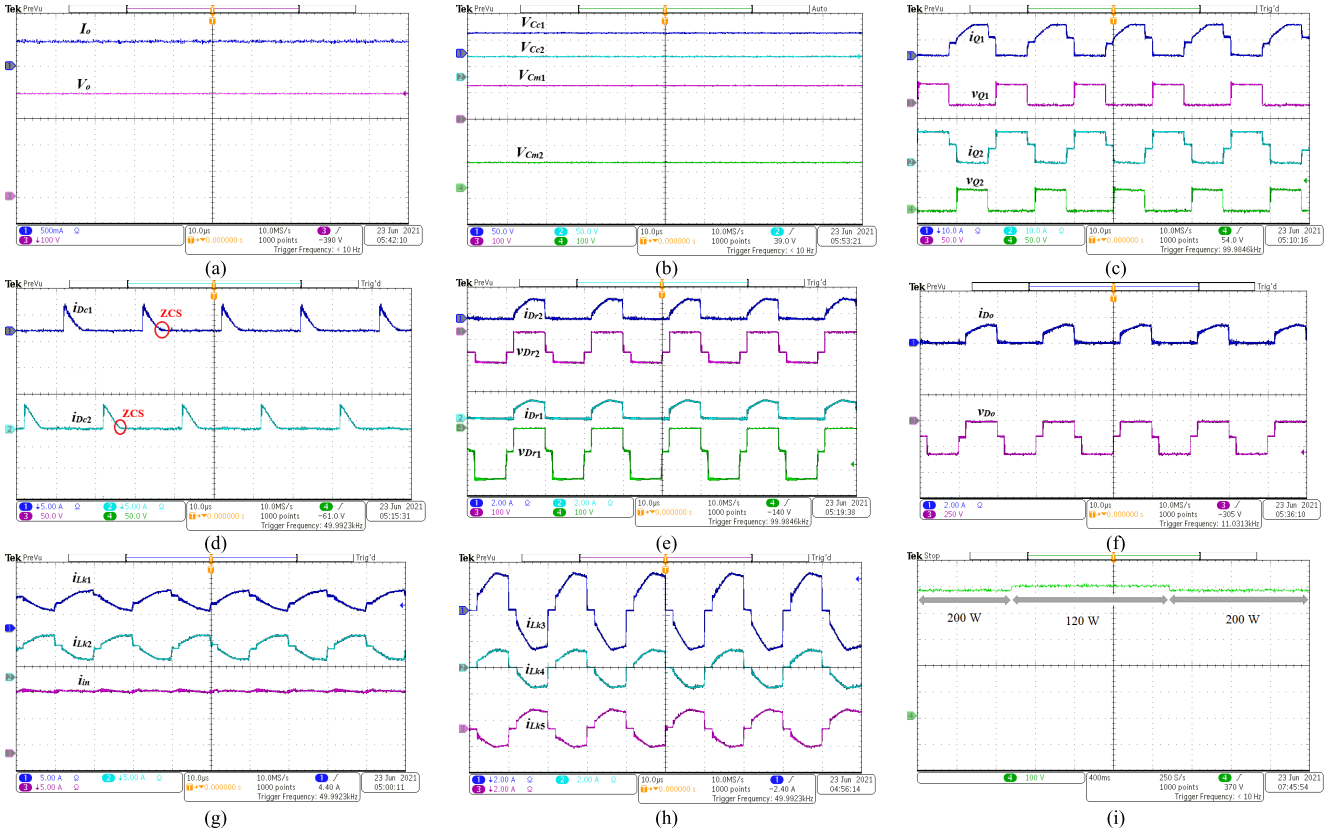

FIGURE 10. The experimental results under full load for $V_{in} = 16$ V: (a)-(h) current and voltage waveforms; (i) dynamic response of the output voltage for the 40 % step change in the load.

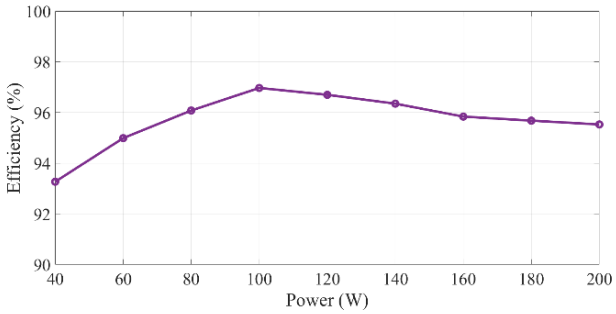

FIGURE 11. The measured efficiency versus the output power for the proposed converter.

voltage of 16 V and duty cycle of 0.6. The maximum efficiency is 96.97 % at the load of 100 W, and the full-load efficiency is 95.53 %. As seem from Fig. 11, the efficiency of the proposed converter rises first and then reduces as the output power increase. The reason is that for the output power less than 100 W, the converter operates in discontinuous conduction mode (DCM); however, for output power higher than 100 W, the converter operates in CCM. In the DCM, the components' ripple currents are higher compared to the CCM, which leads to lower efficiency in comparison with CCM.

To evaluate analytical loss distribution in the components of the proposed converters, the parasitic elements of the components are considered to calculate the losses of the components, which are described below.

The losses of the switches consist of the conduction loss and switching loss, which are expressed as (50).

$$\begin{cases} P_{Q_1} = P_{Q_1,\,cond} + P_{Q_1,\,sw} \\ \qquad = R_{DS\,(on)} I^2_{Q_{1rms}} + V^2_{Q_1} C_{oss} f_{sw} \\ P_{Q_2} = P_{Q_2,\,cond} + P_{Q_2,\,sw} \\ \qquad = R_{DS\,(on)} I^2_{Q_{2rms}} + V^2_{Q_2} C_{oss} f_{sw} \\ P_Q = P_{Q_1} + P_{Q_2} \end{cases} \tag{50}$$

Due to the turn-off ZCS conditions, the revere-recovery losses of the diodes are ignored in the loss and only their conduction losses are considered; thus, the diodes losses are expressed as (51).

$$\begin{cases} P_{D_{c1}} = R_{D_{c1}} I^2_{D_{c1_{rms}}} + V_{F_{D_{c1}}} I_{D_{c1avg}} \\ P_{D_{c2}} = R_{D_{c2}} I^2_{D_{c2_{rms}}} + V_{F_{D_{c2}}} I_{D_{c2avg}} \\ P_{D_{r1}} = R_{D_{r1}} I^2_{D_{r1_{rms}}} + V_{F_{D_{r1}}} I_{D_{r1avg}} \\ P_{D_{r2}} = R_{D_{r2}} I^2_{D_{r2_{rms}}} + V_{F_{D_{r2}}} I_{D_{r2avg}} \\ P_{D_o} = R_{D_o} I^2_{D_{o_{rms}}} + V_{F_{D_o}} I_{D_{oavg}} \\ P_D = P_{D_{c1}} + P_{D_{c2}} + P_{D_{r1}} + P_{D_{r2}} + P_{D_o} \end{cases} \tag{51}$$

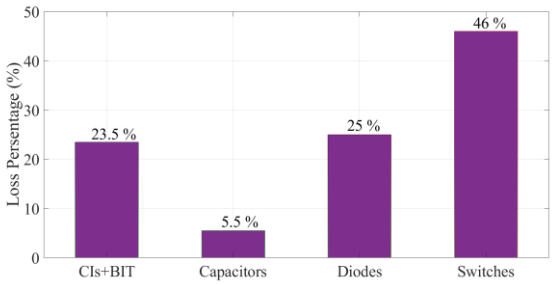

FIGURE 12. The analytical loss distribution of the proposed converter at full load.

The losses of the capacitors are given by (52).

$$\begin{cases} P_{C_{c1}} = R_{C_{c1}} I^2_{C_{c1_{rms}}} \\ P_{C_{c2}} = R_{C_{c2}} I^2_{C_{c2_{rms}}} \\ P_{C_{m1}} = R_{C_{m1}} I^2_{C_{m1_{rms}}} \\ P_{C_{m2}} = R_{C_{m2}} I^2_{C_{m1_{rms}}} \\ P_{C_o} = R_{C_o} I^2_{C_{o_{rms}}} \\ P_C = P_{C_{c1}} + P_{C_{c2}} + P_{C_{m1}} + P_{C_{m2}} + P_{C_o} \end{cases} \tag{52}$$

The losses of the 2W CIs and 3W BIT are extracted by (53), where $P_{\text{core,CI1}}$, $P_{\text{core,CI2}}$, $P_{\text{core,BIT}}$ are the core losses of the 2W CIs and 3W BIT, which are extracted from the datasheets of the selected magnetic cores.

$$\begin{cases} P_{CI1} = R_{p_1} I^2_{L_{k1},\,rms} + R_{s_1} I^2_{L_{k4},\,rms} + P_{core,\,CI1} \\ P_{CI2} = R_{p_2} I^2_{L_{k2},\,rms} + R_{s_2} I^2_{L_{k5},\,rms} + P_{core,\,CI2} \\ P_{BIT} = R_p I^2_{L_{k3},\,rms} + R_s I^2_{L_{k4},\,rms} \\ \qquad + R_t I^2_{L_{k5},\,rms} + P_{core,\,BIT} \\ P_{CIs+BIT} = P_{CI1} + P_{CI2} + P_{BIT} \end{cases} \tag{53}$$

The total loss of the proposed converter is given by (54).

$$P_{Loss} = P_Q + P_D + P_C + P_{CIs+BIT} \tag{54}$$

Considering (50)-(54), the analytical loss distribution in the components at full load is obtained, which shown in Fig. 12; as observed, the largest losses occur in the power switches.

VII. CONCLUSION

In this paper, an interleaved high step-up DC-DC converter was introduced for renewable energy applications, including the PV and fuel cells. Double 2W CIs and one 3W BIT are combined with the SC VMCs to offer increased design flexibility to adjust the voltage gain. Compared to competitors presented in literature, the proposed converter yields the highest voltage gain and lowest voltage stresses on the switches with a low number of magnetic cores. Due to the low voltage stresses on the switches, which are provided by the passive diode-capacitor clamps, low-voltage-rated MOSFETs with low ON-state resistances are selected, which contributes to the reduction in conduction losses. Due to the interleaved structure, the input current ripple and current stresses for the components are reduced. The diodes' reverse-recovery problem is suppressed because leakage inductances of the CIs and BIT provide the diodes with turn-off ZCS conditions. The feasibility and performance of the proposed converter were validated through a 200 W experimental setup with a voltage gain of 25 and full-load efficiency of 95.53 %. The proposed converter could be utilized for the integration of PV and fuel cells onto a 400 V DC bus in the renewable energy applications.

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