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Microwave Synthesizer and Self-Adaption System for High Performance Coherent Population Trapping Atomic Clocks

MINGHAO YAO^{1,2}, JUNYI DUAN¹, XUEYING WANG², QINA HAN¹, YANG SHI¹, KUNLI ZHOU¹, NING RU¹, PETER YUN³, AND XIAOCHI LIU¹

¹Center for Advanced Measurement Science, National Institute of Metrology, Beijing 100029, China

²College of Metrology and Measurement Engineering, China Jiliang University, Hangzhou 314423, China

³National Time Service Center, Chinese Academy of Sciences, Xi'an 710600, China

Corresponding author: Xiaochi Liu (liuxch@nim.ac.cn)

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ABSTRACT A microwave (MW) synthesizer is a key component of high-performance coherent population trapping (CPT) atomic clocks, which are competitive candidates as miniature, low-power-consumption atomic clocks. In this work, we demonstrated a microwave synthesizer and a self-adaption system to satisfy the requirement of short term and mid-long term frequency stability of CPT clocks. From the experimental results, the absolute phase noise of the microwave synthesizer was measured as -110 dBc/Hz at 200 Hz. The off-resonant light shift limitation for CPT clock can achieve better than 2×10^{-14} based on our microwave synthesizer and self-adaption system. The proposed low-phase-noise microwave synthesizer and self-adaption system presented can also be used in other high-performance microwave atomic sensors and standards.

INDEX TERMS Microwave synthesizer, phase noise, light shift, atomic clock.

I. INTRODUCTION

High-performance miniature microwave (MW) atomic clocks are widely used in navigation systems, telecommunications, and other compact systems. Among the various kinds of MW atomic clocks based, the ones based on coherent population trapping (CPT) can potentially develop high-performance miniature atomic clocks. Considering MW interrogation is optically carried out by a phase-coherent bichromatic light field in the CPT clocks, an MW resonant cavity is not required, which significantly reduces the system volume. Therefore, CPT clocks are competitive candidates as miniature, low-power-consumption atomic clocks [1]–[3].

Various studies have demonstrated the outstanding performance of CPT clocks [4]–[8]. CPT clocks based on vapor cell and Ramsey interrogation exhibited a short-term frequency of $10^{-13} \tau^{-1/2}$ [4]–[6]. However, the collisional shift of the buffer gas in vapor cell-based CPT clocks limited the mid-to-long-term frequency stability. Therefore, efforts have been made to mitigate the collisional shift and increase the

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Ramsey interrogation period using the laser-cooling atom technique [7], [8]. As a result, the cold atoms CPT clock exhibited long-term frequency stability of 10^{-13} with an integration time of 40000 s. The MW signal from the local oscillator (LO) is one of the main factors to limit the short-term and mid-to-long-term frequency stability of CPT clocks.

First, the phase noise of the MW signal limits the short-term frequency stability of the CPT clocks via the Dick effect [9]–[12]. The frequency stability limitation $\sigma_y(\tau)$ is given as:

$$\sigma_y(\tau) \sim \frac{f_m}{f_c} \sqrt{S_\varphi(2f_m)} \quad (1)$$

where f_m is the LO modulation frequency and $S_\varphi(2f_m)$ is the LO phase noise at a Fourier frequency of $2f_m$.

Eq. 1 indicates that a low-noise MW synthesizer with a phase noise lower than approximately -106 dBc/Hz at 200 Hz is required to develop a CPT clock operating at an LO modulation frequency of 100 Hz and having a relative frequency stability of 10^{-13} at 1s.

Besides the phase noise, the output power of MW synthesizer also affects the CPT clock performance.

In Ramsey-based CPT clocks, [4], [7], [8], [13]–[18], the mid-to long-term frequency stability is mainly limited by light shifts comprising resonant and off-resonant components. Given that the resonant light shift vanishes with the high intensity and duration of the Ramsey pulse [8], the off-resonant light shift is the dominant systematic shift. In CPT physics, the optical single sideband (SSB) Ω_1 and Ω_2 couple the hyperfine splitting of the ground state (Fig. 1). However, based on the theoretical model [19]–[21], the off-resonant light shift depends strongly on the ratio of the optical SSB of CPT bichromatic light fields and not variations in the total optical intensity.

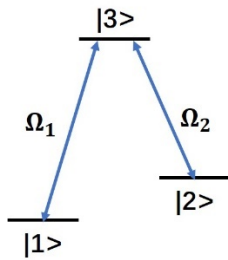


FIGURE 1. CPT coupling scheme with two single sidebands.

Generally, the sidebands are generated from a MW-modulated monochromatic light field. The modulation depth or amplitude of each SSB depends on the MW signal power. Therefore, to mitigate the off-resonant light shift, the MW synthesizer used in a general CPT clock system should exhibit high power stability.

Moreover, the pigtailed electro-optical modulator (EOM) is frequently used in several high-performance CPT clock to maintain high phase coherence of SSB [4]–[8]. However, the transfer function of the EOM may drift owing to temperature variations, photorefractive effects, and aging [22], [23]. Therefore, only a power-stabilized MW signal cannot guarantee that the stability of the ratio of the SSB in the EOM-based system unless the transfer function of the EOM is also stabilized.

A stabilization system of intensity Mach-Zehnder (MZ) EOM has been developed in [4]. The beatnote signal of SSB is detected and compared with a reference. The error signal is used to adjust the bias voltage signal applied on the MZ EOM. However, this approach is particularly for MZ-type EOM, and an additional feedback system increase the complexity of the clock system. Thus, here we demonstrate a simple MW self-adaption system for EOM stabilization. The MW signal power is adjusted to compensate the drift of the EOM.

In this study, we demonstrate a simple MW synthesizer exhibiting low phase noise to mitigate the Dick effect. Furthermore, given the instability caused by the EOM transfer function in the SSB ratio, we developed a self-adaption feedback system that stabilizes the SSB ratio. Section II describes a basic low-phase-noise MW synthesizer system with a simple architecture and presents the phase noise measurement

results. Section III reports the proposed power stability-improved MW synthesizer and the self-adaption feedback system. Section IV presents the conclusions of this study, which provides a summary of the setup scheme and experimental results that can be applied to other high-performance atomic clocks and atomic sensors.

II. LOW PHASE NOISE MW SYNTHESIZER

Previous studies have demonstrated generation of MW signals using oven-controlled crystal oscillator (OCXO) [25]–[27]. In this study, we generated a high-purity and low-phase-noise MW signal spectrum by combining the phase-locked dielectric resonant oscillator (PDRO) and direct digital synthesis (DDS). Fig. 2 shows a schematic representation of the MW synthesizer architecture.

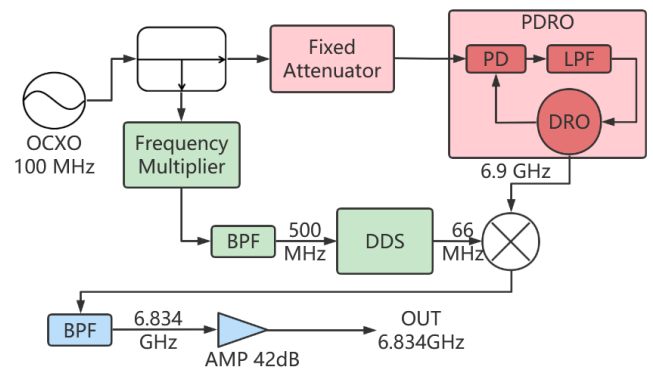


FIGURE 2. Basic scheme of the MW synthesizer. OCXO: oven-controlled crystal oscillator, PDRO: phase-locked dielectric resonant oscillator, PD: photodiode, LPF: low pass filter, DRO: dielectric resonant oscillator, DDS: direct digital synthesis, BPF: band pass filter, AMP: amplifier.

A 100 MHz OCXO was used as the MW synthesizer, which generates a 6.834 GHz signal, a combination of 6.9 GHz and 66 MHz signals from a PDRO and a DDS, respectively. A 100 MHz high spectral purity (ZF550) was used as the LO for the MW synthesizer. The output signal of the OCXO was divided using a frequency distributor (STMFP4-1-120). The 100 MHz signal of the first arm was sent to a sampling phase detector to phase lock the DRO. A sub-sampling PLL was used to directly phase-lock the 6.9 GHz signal of the DRO to the 100 MHz OCXO. The 100 MHz of the second arm was sent to a frequency multiplier (RMK-5-52+), and after bandpass filtering, the 500 MHz multiplied signal was used as the low-phase-noise reference signal for the DDS (AD9912). A 6.834 GHz MW signal was produced by mixing a 6.9 GHz signal with the 66 MHz of the DDS. The resulting 6.834 GHz signal was bandpass filtered and amplified, which enables the subsequent measurement of CPT atomic clock.

Fig. 3 shows the key signal absolute phase noise performance, inclusive of the theoretical phase noise of the 6.834 GHz signal, of the low phase noise MW synthesizer. The results are measured with Anapico APPH6040. The MW synthesizer output 6.834 GHz phase noise and PDRO output exhibit similar offset frequencies ranging from 1 Hz–100 kHz. The measured and theoretical phase noise

values of the MW signal were in well agreement at 200 Hz, which is the second harmonic of the clock modulation frequency. However, the measured phase noise of the 6.834 GHz signal deteriorated compared to the theoretical value owing to the phase noise of the PDRO. Additionally, the locking bandwidth of PLL was approximately 300 kHz. Therefore, the phase noise of the MW synthesizer at 300 kHz cannot be suppressed completely, and is not degraded by the phase noise of the DDS. The measurement results indicate that this system achieved similar performance as compared to that in [24], using fewer components.

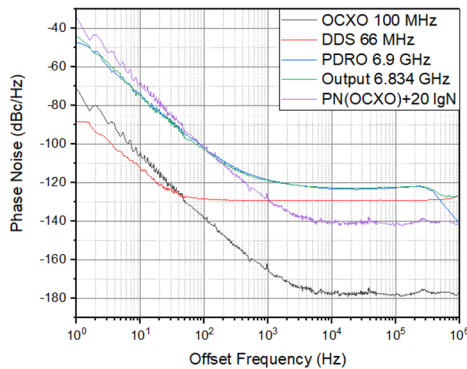


FIGURE 3. Absolute phase noises of the key signals and components of the MW synthesizer.

As seen in Fig. 3, the absolute phase noise of the 6.834 GHz MW signal at an offset frequency of 200 Hz is -110 dBc/Hz. Using Eq. 1, the limitation of the frequency stability of CPT clock was calculated as 6.5×10^{-14} with 1 s integration time, indicating improved frequency stability as compared to the state-of-the-art frequency stability of the CPT clock [4]–[6].

III. MW SELF-ADAPTION SYSTEM

The off-resonant light shifts due to the instable SSB ratio of the bichromatic light fields limits the mid-to-long-term frequency stability of CPT clocks [21]. A 0.1% variation in the SSB ratio resulted in a variation of 0.35 mHz in the frequency of the CPT clock, thus limiting the frequency stability to 5×10^{-14} [7], [8], [21].

The SSB ratio is generated when the monochromatic light field is modulated by a 6.834 GHz MW signal, and also depends on MW signal power. Fig. 4 shows the SSB ratio as a function of the MW power in our experimental setup. A 0.1% variation in the SSB ratio requires MW power fluctuations over 1.1×10^{-3} . Therefore, the output power of the MW synthesizer must be stabilized in a high-performance CPT clock system.

A. POWER-STABILIZED LOOP

The self-adaption system is developed based on a power-stabilized MW synthesizer. Thus, a power-stabilized loop for MW synthesizer is firstly developed.

The MW power stabilization loop system aims at detecting the 6.834 GHz MW power using a Schottky diode detector,

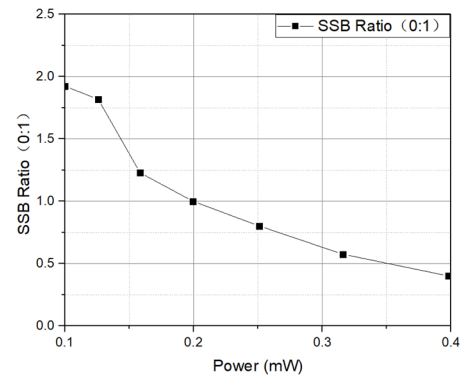


FIGURE 4. MW signal power versus the SSB ratio.

and compare it with an ultra-stable voltage reference to generate an error signal. A PI controller generates a correction signal that is sent to a voltage-controlled attenuator (V-A) placed at the output of the MW synthesizer.

Fig. 5 shows the architecture of the stabilization loop. The output MW signal is sent to the V-A (CLVA-2G18G-50) and divides into two arms. The signal in the first arm is sent to the clock system, and the MW signal in the second arm is attenuated and converted into a DC voltage using a Schottky diode (LTC5532ES6). An error signal was generated by comparing the resultant output voltage with a voltage reference (LTZ 1000). The PI controller comprises an ADC, a DAC, and a microprocessor (STM32). A PI control program was written to STM32.

The MW power is measured in the free-running (red) and locked regimes (black), as shown in Fig. 6. The MW power is decreased with the environmental temperature in free-running regime. The measured results indicated a significant improvement in the stability of the MW power with the feedback loop.

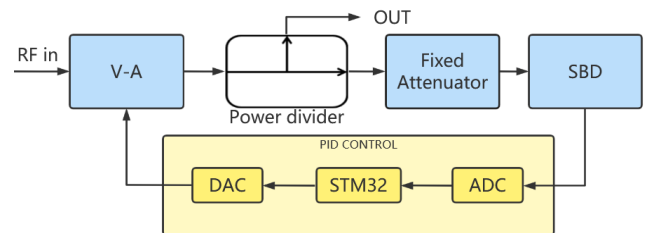


FIGURE 5. Power stabilization loop. V-A: voltage-controlled attenuator, SBD: Schottky barrier diode, DAC: digital to analog converter, ADC: analog to digital converter.

B. SELF-ADAPTION SYSTEM

The scheme of the self-adaption system with an EOM is shown in Fig. 7. The MW signal from the synthesizer drives the phase EOM to generate an SSB. A fast photodiode (FPD) was used to detect the 6.834 GHz beatnote signal of the SSB. Fig. 8 shows the SSB ratio versus the 6.834 GHz beatnote signal, which indicates that the MW beat note signal represents the SSB ratio and can be used to feedback the EOM.

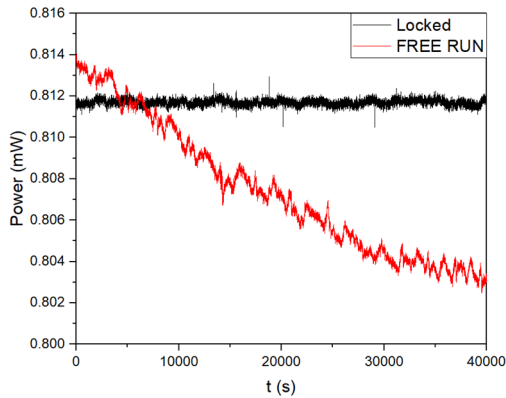


FIGURE 6. MW power fluctuations in the free-running (black) and locked regimes (red).

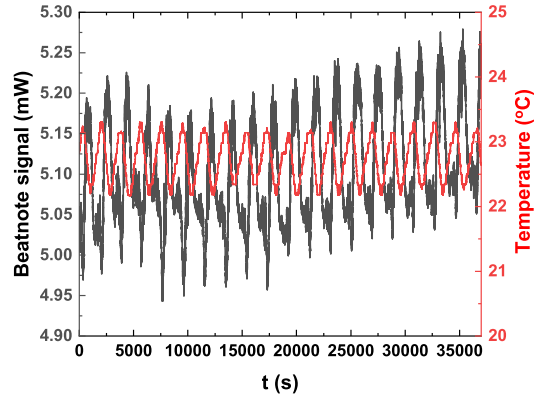


FIGURE 9. 6.834 GHz SSB beatnote fluctuations in free-running regime (black) and the temperature fluctuations during the measurement (red).

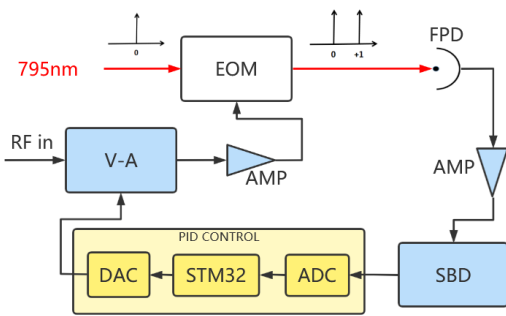


FIGURE 7. Architecture of the self-adaption system with an EOM. EOM: electro-optical modulator, FPD: fast photodiode, V-A: voltage-controlled attenuator, SBD: Schottky barrier diode, DAC: digital to analog converter, ADC: analog to digital converter, AMP: amplifier.

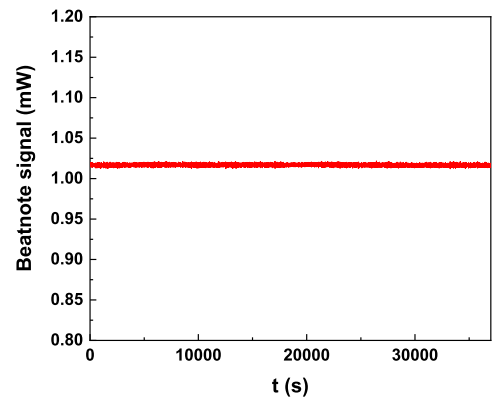


FIGURE 10. 6.834 GHz SSB beatnote fluctuations in the locked regime.

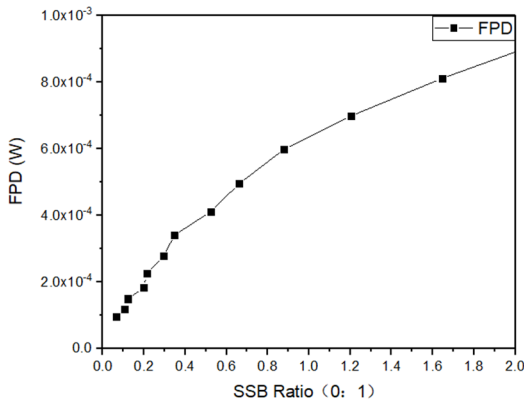


FIGURE 8. SSB ratio versus the 6.834 GHz beatnote signal.

The beat note signal was then converted to a voltage signal using a Schottky diode and compared to a voltage reference. The error signal was sent to a PI controller. The SSB ratio can be varied using the measurement results of the MW signal. Consequently, we can stabilize the SSB ratio and transfer function of the EOM using the correction signal from the PI controller.

The black data plotted in Fig. 9 is the beatnote signal of the two SSB measured with the FPD in the free-running regime, while the red curve is the temperature variations

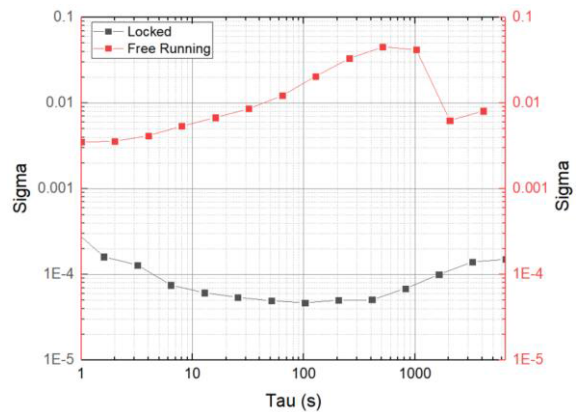


FIGURE 11. Fractional fluctuations in the 6.834 GHz SSB beatnote in free-running (black) and locked regimes (red).

during the measurement. The SSB varied periodically owing of the temperature dependence of the EOM. Fig. 10 plots the SSB beatnote fluctuations (the same scale as Fig. 9) in the locked regime with the self-adaption system, which indicated that the fluctuations due to the EOM is significantly corrected. Furthermore, the self-adaption system measured the fluctuations for the mid-long term as 3×10^{-4} at 1 s and 2×10^{-4} at 6000 s integration time in Fig. 11. The corresponding

frequency fluctuation was measured as 0.136 mHz, which limited the frequency stability of CPT clock to 2×10^{-14} .

IV. CONCLUSION

In conclusion, we demonstrated a simple architecture of a low-phase noise and high-power stability MW synthesizer for high-performance CPT clocks. We also developed a self-adaption system to compensate for the EOM drift in the CPT clock system. The experimental results showed that the absolute phase noise of the 6.834 GHz MW signal was -110 dBc/Hz at an offset frequency of 200 Hz. The theoretically calculated MW synthesizer phase noise for the frequency stability was 6.5×10^{-14} , which was significantly improved compared to the state-of-the-art short term frequency stability performance of the CPT clock [4], [5]. The SSB ratio stability was further improved using the self-adaption system, with a ratio stability of 3×10^{-4} at 1 s and 2×10^{-4} at 6000 s integration time, which is nearly two orders of magnitude compared to the free-running regime. The proposed high-performance MW synthesizer and self-adaption system can also be used in MW atomic sensors and standards, such as atomic magnetometers, atomic interferometers, and atomic gyroscopes. In particular, the simple architecture and low power consumption can also enable the development of compact alkali atom-based systems.

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