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A Nanosized-Metal-Grain Pattern-Dependent Threshold Voltage Model for the Work Function Fluctuation of GAA Si NW MOSFETs

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ABSTRACT To estimate characteristic fluctuation of emerging devices, three-dimensional device simulation has been performed intensively for various random cases; however, it strongly relies on huge computational resources. In this paper, we report a nanosized-metal-grain pattern-dependent model by using the method of multi-variable non-linear regression (MVNLR) for the threshold voltage fluctuation (σV_{th}) of gate-all-around silicon nanowire metal-oxide-semiconductor field-effect transistors. The model is developed by perturbing the local metal grains of specific patterns and summing up each metal grain of various grain patterns. The method of MVNLR is applied to build equations for nominal devices, and devices with high work-function (WK) and low WK with respect to process parameters (radius of channel, gate length, channel doping, and oxide thickness), which are generated by the design of experiments. The proposed model can estimate the magnitude of σV_{th} accurately (error rate $< 1\%$) for all parameters, where an error-correction process is further adopted by using a simplified one-perceptron method.

INDEX TERMS Work function fluctuation, gate-all-around, nanowire, MOSFETs, threshold voltage, variability, metal grain, multi-variable non-linear regression, one-perceptron.

I. INTRODUCTION

Three-dimensional (3D) gate-all-around (GAA) silicon (Si) nanowire (NW) metal-oxide-semiconductor field-effect transistors (MOSFETs) with high-κ/metal-gate technology are potential devices to replace the fin-type-field effect transistor (FinFET) due to improved electrostatic performance and transistor scaling in sub-5-nm nodes [1]–[5]. However, in nano-scaled devices, process variations will impact the yield of chips due to fluctuations of key device parameters, such as threshold voltage (V_{th}). The fluctuation sources include the random dopant fluctuation, work function fluctuation (WKF), random interface trap, random telegraph noise and process variation effect (PVE) [6]–[13]. Notably, the WKF has been considered to be a key fluctuation source due to large grain size or small metal grain number (MGN) by a 3D device simulation (3D-DS) for the GAA Si NW MOSFETs [13]–[15]. Moreover, the PVE of in-line critical-dimension (CD) variation affects the device characteristics significantly in the nanometer regime, for example, radius (R) of a cylindrical channel [13]. Different CDs may influence the results of the WKF-induced threshold-voltage variability (σV_{th}) because the area of metal grains is different in the assumption of the same MGN. Moreover, the GAA devices with multi-channels have been considered to increase the drive current [5]. Estimating the variability of the GAA devices requires huge computational resources based on the 3D-DS [14].

Previously, different models for the WKF-induced σV_{th} had been proposed by various research groups.

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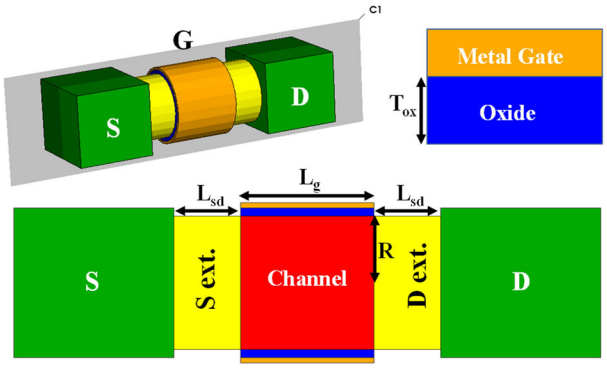


FIGURE 1. Schematic of the nominal GAA Si NW MOSFET, where the L_g is 10 nm, the R is 5 nm, the L_{sd} is optimized at 5 nm, and the T_{ox} is 0.6 nm, respectively. The C1 is the cutting plane.

TABLE 1. The process parameters for the nominal GAA Si NW MOSFET.

Parameter	Value
L_g (nm)	10
T_{ox} (nm)	0.6
R (nm)	5
L_{sd} (nm)	5
Channel Doping (Ch_dop) (cm^{-3})	5×10^{17}
S/D Doping (SD_dop) (cm^{-3})	1×10^{20}
S/D Extension Doping (SDE_dop) (cm^{-3})	5×10^{18}
LWK (eV)	4.432
HWK (eV)	4.632
Nominal EWK (eV)	4.552

In 2008 and 2010, H. F. Dadgour *et al.* had proposed an effective work-function (EWK) model to calculate the magnitude of σV_{th} immediately and circuit performance for various MGN (MGN $= (L_g/G_L) \times (W_{eff}/G_W)$, where L_g is the gate length, G_L and G_W are the length and width of grain size, and W_{eff} is the effective width of the metal gate) [16]–[18]. However, the EWK model cannot create accurate results for emerging devices due to the location effect of a large metal grain size or few MGN (for example, MGN < 20) in the nano-scaled gate area [19]. Thus, in 2011, S. H. Rasouli *et al.* had proposed an accurately physical-based model for planar-MOSFET [19]. This model is modified from the net-work transistors model [20], which considers the location effect of the work-function (WK) of adjacent metal grains. In 2017, P. H. Vardhan *et al.* had commented that the modified net-work transistors model [19] only works well for large-scale devices with relatively small grain sizes. Thus, by that time, they had proposed a new model from Laplace's potential solution and percolation resistance net-work models to estimate the WKF-induced σV_{th} for FinFET devices [21]. In the same year, G. Indalecio *et al.* had proposed a novel fluctuation sensitivity map technique to capture fluctuation sensitivity and estimate the WKF-induced σV_{th} for FinFET devices, which considers the location of fluctuations [22]. However, it still has a high error rate (ER). In 2018, P. H. Vardhan *et al.* extended the FinFET-based model to GAA NW MOSFETs with cylindrical geometry and constraint boundary conditions [23]. Moreover, in 2019, a Fourier-Bessel model had been proposed due to more accurate expression for GAA NW MOSFETs [24], but, the Fourier-Bessel model also has a large ER for large grain size. In the same year, K. Ko *et al.* proposed a compact model strategy to reduce the ER by adding a percentage to capture the interactions between the grains for the case of large grain size [15]. Nevertheless, they have highlighted their approach still has a high ER due to many preconditions. Thus, they had proposed an artificial-neural-network-based machine learning (ML) approach with more accurate results for process variations [25]. Recently, various deep learning (DL) techniques had been studied for the WKF on the GAA Si NW devices with high efficiency and accuracy [26]. The advantage of these ML/DL models is data-oriented, not model-oriented. They do not need a fixed relationship or physical model between the input and output parameters. However, one of disadvantages of these ML/DL models is hard to decide the best-hidden layers to ensure the global convergence for the WKF-induced variability of the GAA devices with multi-channels with respect to various process conditions and MGNs.

In this work, we propose the nanosized-metal-grain pattern-dependent model by using the method of multi-variable non-linear regression (MVNLR) to overcome the aforementioned issues. The advantages of the proposed model are fast, simple and easy to calculate the WKF-induced σV_{th} for various process conditions. To minimize the ER, an one-perceptron method [27] is simplified and applied to conduct the error correction (EC).

This paper is structured as follows: Section II presents the device structure, statistical device simulation and model for the GAA Si NW MOSFETs. Section III reports the results and the detailed discussion for different MGNs, process conditions and the GAA devices with multi-channels. In addition, we also discuss the main error source and their physical mechanisms. Finally, we conclude and offer directions for future research.

II. DEVICE, WKF, AND STATISTICAL MODEL

A. THE SIMULATED DEVICE

Fig. 1 shows the schematic of the nominal GAA Si NW MOSFET, where the L_g is 10 nm, the R of a cylindrical channel is 5 nm, the S/D extension (L_{sd}) is optimized at 5 nm, and the oxide thickness (T_{ox}) is 0.6 nm, respectively. To simulate the low-power devices with higher V_{th}, the nominal EWK of the TiN metal is set to 4.552 eV [13], [17] for the nominal device, where the low WK (LWK) is 4.432 eV, the high WK (HWK) is 4.632 eV, and the nominal EWK is calculated by LWK $\times$ 0.4 + HWK $\times$ 0.6. Table 1 summarizes the process parameters for the nominal GAA Si NW MOSFET. Notably, a 3D quantum-mechanically corrected transport model was calibrated against the experimental I_D–V_G curve for the nominal GAA Si NW MOSFET [8].

B. THE WKF SIMULATION

According to grain orientations of TiN [28]–[31], we set TiN<111> (probability (p) = 0.4, LWK = 4.432 eV),

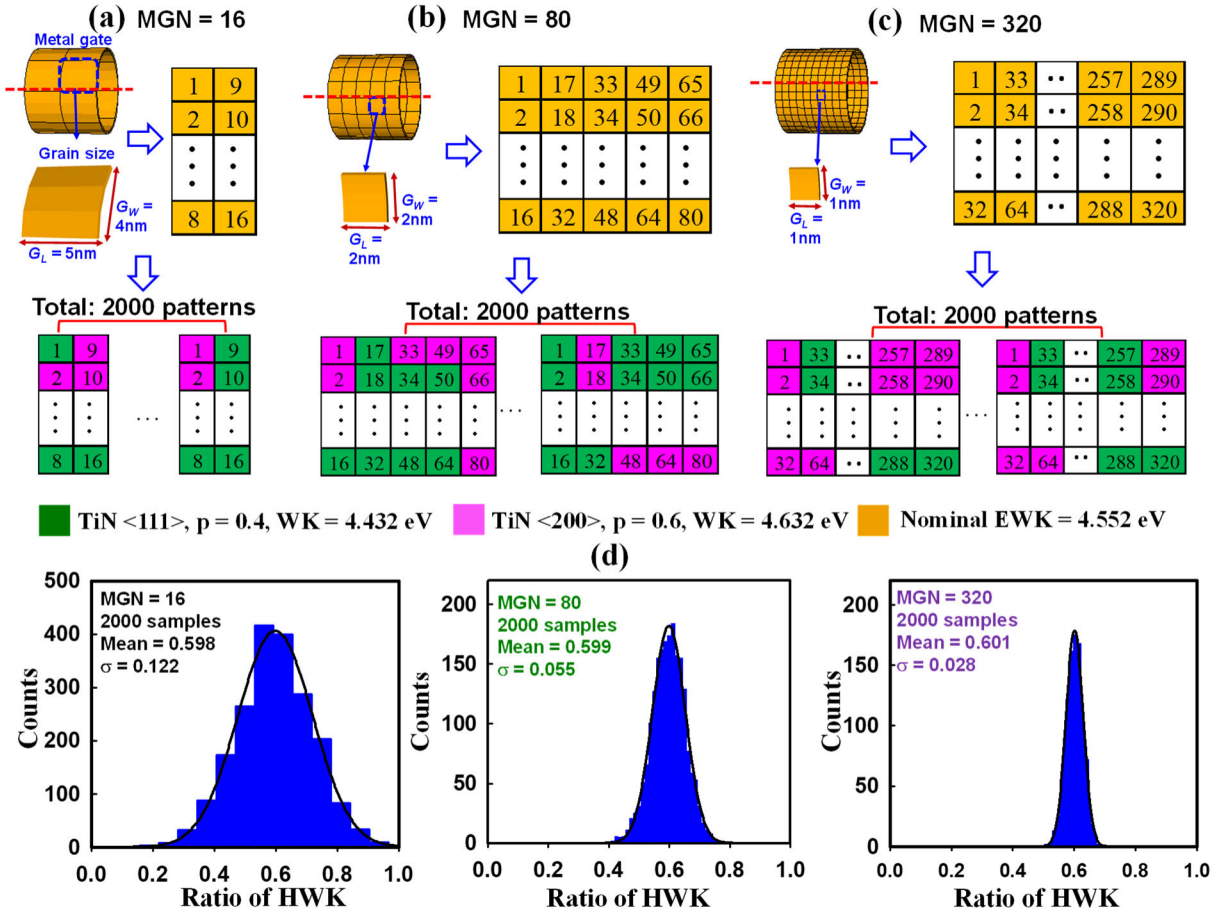


FIGURE 2. The cuboid method for the WKF simulations for three different MGNs and the transformation of 3D metal gate to 2D plane, where the metal gate is partitioned into three grain sizes and 2000 different grain patterns are generated by the MC program. (a) MGN = 16. (b) MGN = 80. (c) MGN = 320. (d) The distributions of the ratio of HWK are normal distributions for different MGNs, where the ratio of HWK is the number of HWK divided by MGN.

TiN<200> (p = 0.6, HWK = 4.632 eV), MGNs and 2000 simulated samples in Monte Carlo (MC) program, respectively. To label the index number of metal grains in different locations, we transfer the 3D metal gate to 2D plane. As shown in Figs. 2(a)-(c), the 2000 random patterns (samples) with the label number can be generated by our MC program for the WKF simulations. The probabilistic distribution of the ratio of HWK (i.e., the number of HWK divided by MGN) follow the "binomial distribution" and will be approached to the normal distribution in large enough MGN and samples by the central limit theory [17], as shown in Fig. 2(d). Because the probability density function of the "binomial distribution" is related to the MGN [17], we can obviously observe that the distributions become widen as the MGN decreases due to the increase of the standard deviation. Additionally, the mean of the ratio of HWK is close to the probability of HWK. It means that the MC program generates the similar distributions to the experimental data [17]. Fig. 3 illustrates the schematics of the patterns of the devices affected by HWK or LWK from S to D for different metal ring sizes (RS) [11]: (a) $L_g/2$, (b) $L_g/5$, and (c) $L_g/10$ nm, where all simulated cases are in the inset of plots. The simulated results of the devices affected by HWK or LWK will be fed into the nanosized-metal-grain pattern-dependent model to calculate the perturbations of local metal grains for various patterns. The starting positions of Sh_L are set to 0 for the devices affected by HWK or LWK, where the metal grain in golden color has a nominal EWK (4.552 eV). The other positions can be shifted by adding the equal RS sequentially for the Sh_L. Then, the devices affected by HWK or LWK are generated in different locations.

C. THE PROPOSED MODEL

The proposed model contains the equations of the nominal devices and the devices affected by HWK and LWK with respect to various process parameters.

1) THE NOMINAL AND PERTURBED EQUATIONS

To build the equations of the nominal devices and the devices affected by HWK and LWK, the design of experiments (DOEs) is created by process parameters of R (range: 4∼6 nm, step: 0.5 nm), Lg (range: 9∼11 nm, step: 0.5 nm), Norm_Ch_dop (range: 3∼7, step: 1), and T_{ox} (range: 0.6∼0.8 nm, step: 0.1 nm), where the Norm_Ch_dop is given

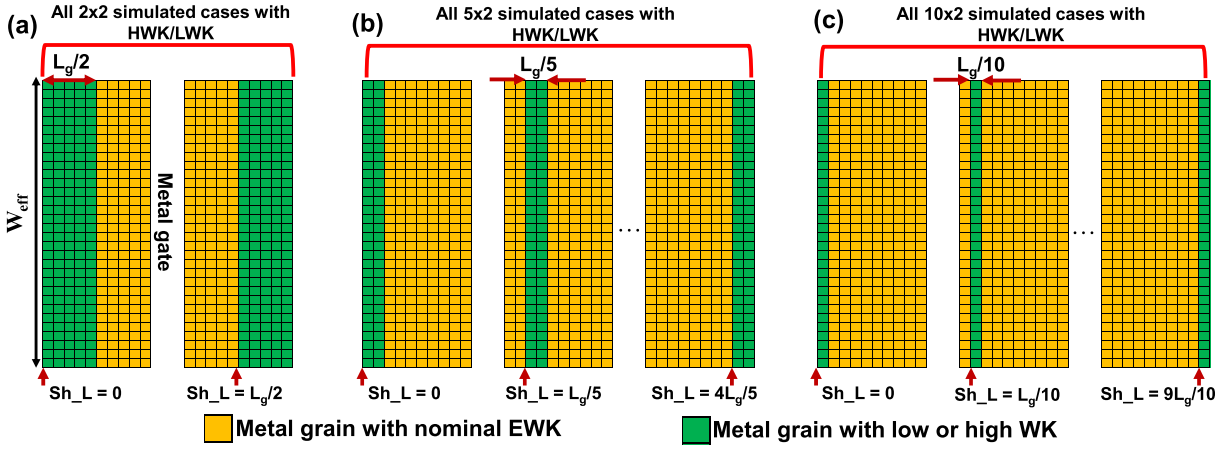


FIGURE 3. Schematics of the patterns of the devices affected by HWK or LWK from S to D for different metal ring sizes: (a) *Lg*/2, (b) *Lg*/5, and (c) *Lg*/10 nm. According to the different grain sizes of Figs. 2(a)-(c), the *Lg* is divided by 2, 5, and 10. In addition, the number of location grains of the RS is set to W_{eff}/G_W. Our program will generate the devices affected by HWK or LWK in different locations. The total simulated cases with HWK and LWK are in the inset of Fig. 3. The simulated results of the devices affected by HWK or LWK will be fed into the nanosized-metal-grain pattern-dependent model (See (9) and (10)) to calculate the perturbations of local metal grains for various patterns.

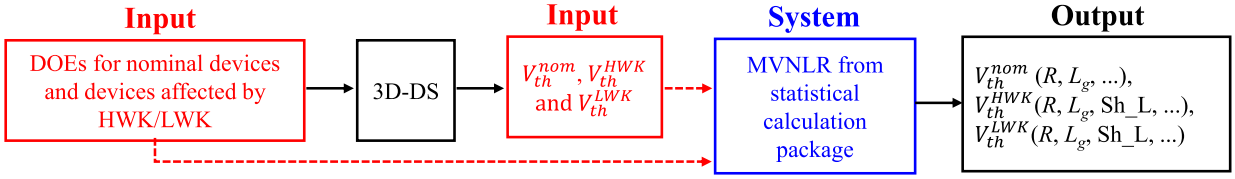


FIGURE 4. A flow to build the equations of nominal devices, and devices affected by HWK/LWK from the MVNLR, where V_{th}^{nom} is the V_{th} of nominal device, V_{th}^{HWK} is the V_{th} of device affected by HWK and V_{th}^{LWK} is the V_{th} of device affected by LWK. The red dash lines are inputs of statistical calculation package.

by the Ch_dop divided by 10^{17} cm^{-3}. Fig. 4 shows a flow to build the equations of the nominal devices and the devices affected by HWK and LWK. First, we input the DOEs into the nominal devices and the devices affected by HWK and LWK for the 3D-DS. Second, we input the DOEs and the V_{th} of the nominal devices, and the devices affected by HWK and LWK into the statistics calculation package. By using the method of the MVNLR, the equations of the nominal devices and the devices affected by HWK and LWK can be obtained for various process conditions. As shown in Fig. 5, for the nominal devices and devices with HWK and LWK, their V_{th} depends on R, L_g, Norm_Ch_dop, and T_{ox} nonlinearly. Thus, we can apply the MVNLR directly at all data points to obtain the equations of the devices affected by HWK and LWK and the nominal devices for each process parameter, where the values of the regression coefficient are over 99.5%. The equations of the devices affected by HWK and LWK and the nominal devices are listed as follows, where the process parameters, "R, Lg, Norm_Ch_dop, T_{ox}", denoted as "pr", Num is the number of location grains of the RS and k is the index number of metal grain:

$$\begin{aligned} &V_{th}^{nom}(pr) \\ &= 675.0 - 89.66 \times R - 19.193 \times Lg - 83.6 \times T_{ox} \\ &\quad + 0.655 \times \text{Norm\_Ch\_dop} + 5.211 \times R \times Lg - 21.64 \\ &\quad \times R \times T_{ox} \\ &\quad + 0.6059 \times R \times \text{Norm\_Ch\_dop} + 12.6 \times Lg \times T_{ox} \\ &\quad + 0.0621 \times Lg \times \text{Norm\_Ch\_dop} \end{aligned} \tag{1}$$

We denote $V_{th}^{nom}(pr) = V_{th}^{nom}$ hereafter.

$$\text{Sh\_L}(k) = G_L \times \text{Quotient}((k-1)/Num) \tag{2}$$

For the case of MGN = 16, we have

$$\begin{aligned} &V_{th}^{HWK}(pr, \text{Sh\_L}(k)) \\ &= 652.5 - 86.9 \times R - 11.48 \times Lg \\ &\quad - 18.31 \times \text{Sh\_L}(k) - 83.6 \times T_{ox} + 1.52 \\ &\quad \times \text{Norm\_Ch\_dop} \\ &\quad + 4.2 \times \text{Sh\_L}(k)^2 + 4.643 \times R \times Lg + 0.4613 \\ &\quad \times R \times \text{Sh\_L}(k) \\ &\quad - 21.98 \times R \times T_{ox} + 0.675 \times R \times \text{Norm\_Ch\_dop} \\ &\quad + 7.54 \times Lg \times T_{ox} \\ &\quad - 0.092 \times Lg \times \text{Norm\_Ch\_dop} - 1.106 \times \text{Sh\_L}(k) \\ &\quad \times T_{ox} \\ &\quad - 0.0158 \times \text{Sh\_L}(k) \times \text{Norm\_Ch\_dop} - 0.347 \times \text{Sh\_L}(k)^3 \end{aligned} \tag{3}$$

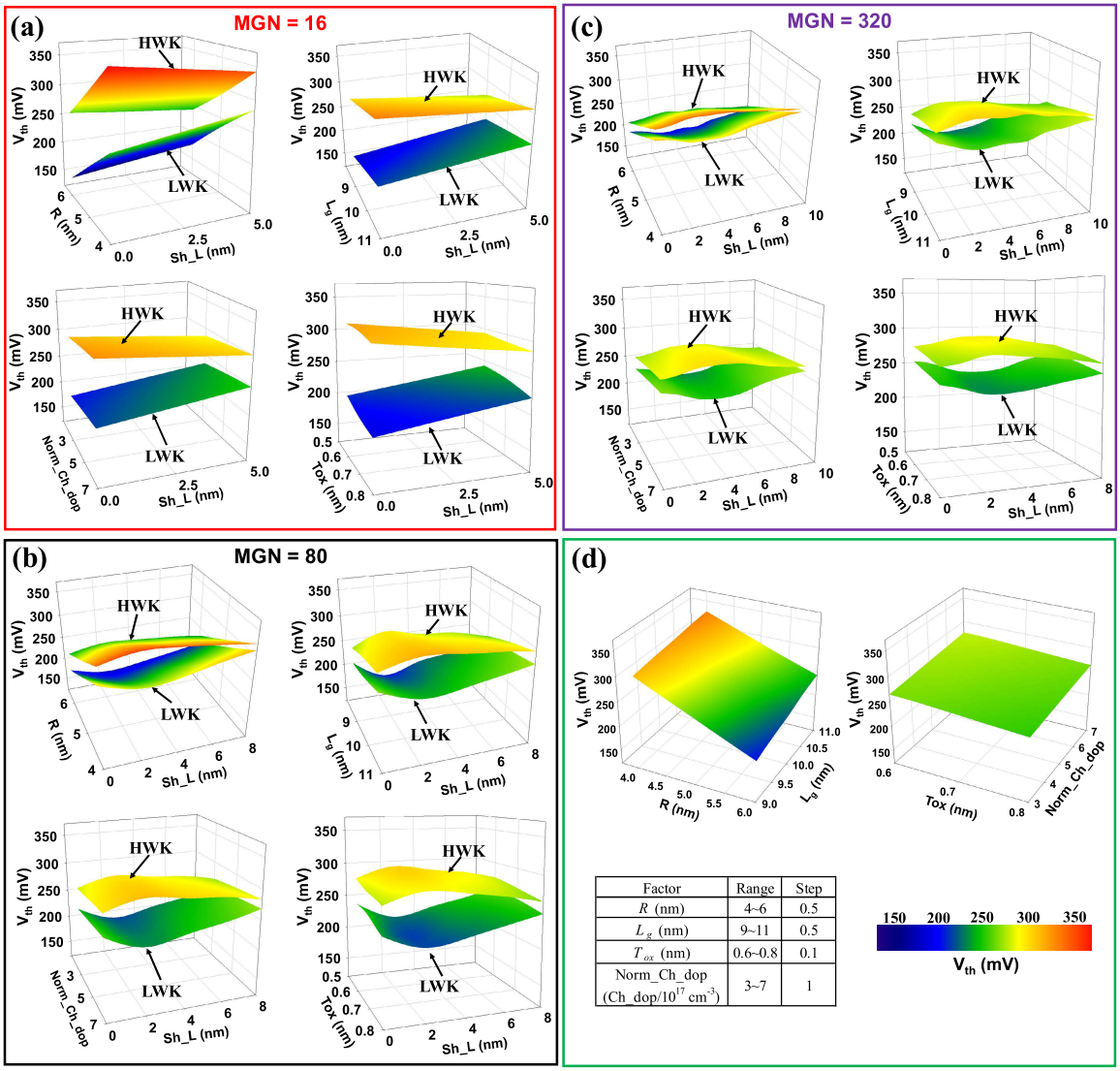


FIGURE 5. For the nominal devices and devices with HWK and LWK, their V_{th} depends on R, L_g, Norm_Ch_dop, and T_{ox} nonlinearly. (a) MGN = 16. (b) MGN = 80. (c) MGN = 320. (d) Nominal devices.

and

$$\begin{aligned}
&V_{th}^{LWK}(pr, \mathrm{Sh_L}(k)) \\
&= 632.3 - 87.84 \times R - 20.44 \times Lg \\
&\quad +15.34 \times \mathrm{Sh_L}(k) - 126.7 \times T_{ox} + 1.56 \\
&\quad \times \mathrm{Norm_Ch_dop} \\
&\quad -2.32 \times \mathrm{Sh_L}(k)^2 + 5.113 \times R \times Lg - 0.4964 \\
&\quad \times R \times \mathrm{Sh_L}(k) \\
&\quad -24.75 \times R \times T_{ox} + 0.677 \times R \times \mathrm{Norm_Ch_dop} \\
&\quad +15.97 \times Lg \times T_{ox} \\
&\quad -0.107 \times Lg \times \mathrm{Norm_Ch_dop} + 2.488 \times \mathrm{Sh_L}(k) \times T_{ox} \\
&\quad +0.0256 \times \mathrm{Sh_L}(k) \times \mathrm{Norm_Ch_dop} + 0.125 \times \mathrm{Sh_L}(k)^3. \qquad (4)
\end{aligned}$$

For the case of MGN = 80, we have

$$\begin{aligned}
&V_{th}^{HWK}(pr, \mathrm{Sh_L}(k)) \\
&= 655.6 - 86.48 \times R - 15.84 \times Lg \\
&\quad +10.996 \times \mathrm{Sh_L}(k) - 71.1 \times T_{ox} + 1.56 \\
&\quad \times \mathrm{Norm_Ch_dop} \\
&\quad -3.1031 \times \mathrm{Sh_L}(k)^2 + 4.87 \times R \times Lg + 0.2163 \\
&\quad \times R \times \mathrm{Sh_L}(k) \\
&\quad -23.62 \times R \times \mathrm{T_{ox}} + 0.6675 \times R \times \mathrm{Norm_Ch_dop} \\
&\quad +12.07 \times Lg \times T_{ox} - 0.0933 \times Lg \times \mathrm{Norm_Ch_dop} \\
&\quad +0.065 \times \mathrm{Sh_L}(k) \times T_{ox} - 0.0099 \times \mathrm{Sh_L}(k) \\
&\quad \times \mathrm{Norm_Ch_dop} + 0.18067 \times \mathrm{Sh_L}(k)^3 \qquad (5)
\end{aligned}$$

and

$$\begin{aligned}
&V_{th}^{LWK}(pr, \mathrm{Sh_L}(k)) \\
&= 645.3 - 87.94 \times R - 19.61 \times Lg
\end{aligned}$$

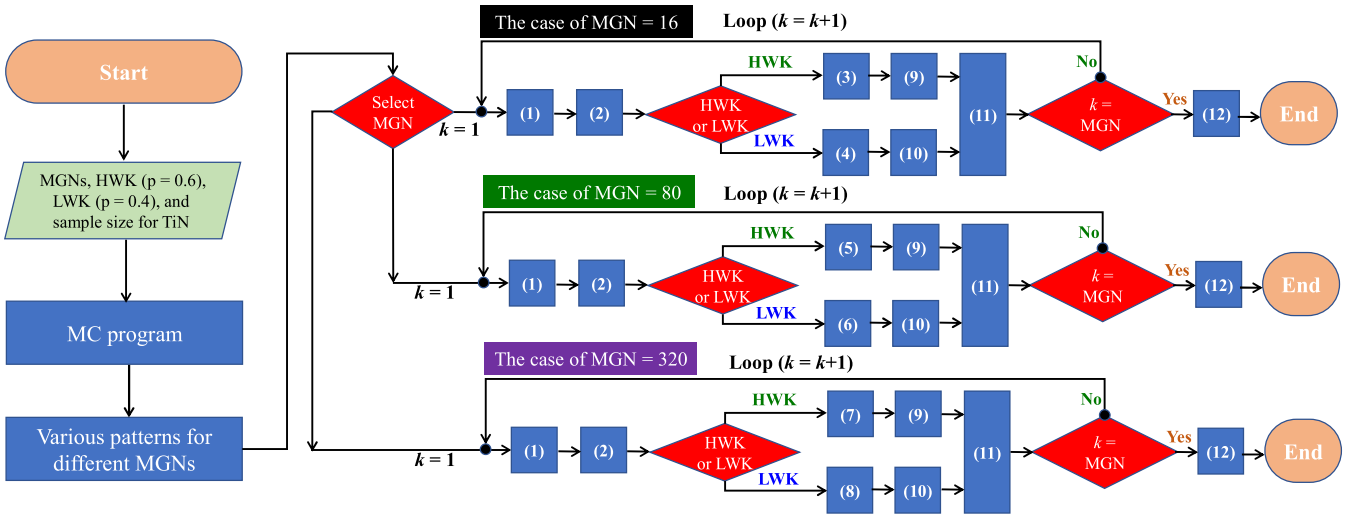


FIGURE 6. The computational flow of the nanosized-metal-grain pattern-dependent model for various MGNs and process parameters, where the W_nom, W_HWK and W_LWK are the weights for the nominal device and devices affected by HWK and LWK, respectively. The k represents the index number of the metal grains.

$$
\begin{aligned}
&-17.773 \times \mathrm{Sh\_L}(k) - 58.2 \times T_{ox} + 1.6 \\
&\times \mathrm{Norm\_Ch\_dop} \\
&+4.887 \times \mathrm{Sh\_L}(k)^2 + 5.234 \times R \times Lg - 0.1579 \\
&\times R \times \mathrm{Sh\_L}(k) \\
&-25.46 \times R \times T_{ox} + 0.674 \times R \times \mathrm{Norm\_Ch\_dop} \\
&+11.85 \times Lg \times T_{ox} - 0.107 \times Lg \times \mathrm{Norm\_Ch\_dop} \\
&-0.353 \times \mathrm{Sh\_L}(k) \times T_{ox} + 0.0114 \times \mathrm{Sh\_L}(k) \\
&\times \mathrm{Norm\_Ch\_dop} - 0.29459 \times \mathrm{Sh\_L}(k)^3. \qquad (6)
\end{aligned}
$$

For the case of MGN = 320, we have

$$
\begin{aligned}
&V_{th}^{HWK}(pr, \mathrm{Sh\_L}(k)) \\
&= 662.11 - 87.5 \times R - 17.921 \times Lg \\
&+8.018 \times \mathrm{Sh\_L}(k) - 72.43 \times T_{ox} + 1.621 \\
&\times \mathrm{Norm\_Ch\_dop} \\
&-1.9136 \times \mathrm{Sh\_L}(k)^2 + 5.1035 \times R \times Lg + 0.1049 \\
&\times R \times \mathrm{Sh\_L}(k) \\
&-24.478 \times R \times T_{ox} + 0.6663 \times R \times \mathrm{Norm\_Ch\_dop} \\
&+12.533 \times Lg \times T_{ox} \\
&-0.1002 \times Lg \times \mathrm{Norm\_Ch\_dop} + 0.027 \times \mathrm{Sh\_L}(k) \times T_{ox} \\
&-0.0044 \times \mathrm{Sh\_L}(k) \times \mathrm{Norm\_Ch\_dop} + 0.1011 \\
&\times \mathrm{Sh\_L}(k)^3 \qquad (7)
\end{aligned}
$$

and

$$
\begin{aligned}
&V_{th}^{LWK}(pr, \mathrm{Sh\_L}(k)) \\
&= 643.7 - 87.54 \times R - 18.35 \times Lg \\
&-11.888 \times \mathrm{Sh\_L}(k) - 55.4 \times T_{ox} + 1.598 \\
&\times \mathrm{Norm\_Ch\_dop} \\
&+2.8391 \times \mathrm{Sh\_L}(k)^2 + 5.131 \times R \times Lg - 0.0876 \\
&\times R \times \mathrm{Sh\_L}(k) \\
&-24.56 \times R \times T_{ox} + 0.6745 \times R \times \mathrm{Norm\_Ch\_dop} \\
&+11.44 \times Lg \times T_{ox} - 0.1048 \times Lg \times \mathrm{Norm\_Ch\_dop} \\
&-0.376 \times \mathrm{Sh\_L}(k) \times T_{ox} + 0.0045 \times \mathrm{Sh\_L}(k) \\
&\times \mathrm{Norm\_Ch\_dop} - 0.1529 \times \mathrm{Sh\_L}(k)^3. \qquad (8)
\end{aligned}
$$

We denote $V_{th}^{HWK}(pr, \mathrm{Sh\_L}(k)) = V_{th}^{HWK}(k)$ and $V_{th}^{LWK}(pr, \mathrm{Sh\_L}(k)) = V_{th}^{LWK}(k)$ hereafter.

2) THE OVERALL EQUATIONS AND THEIR COMPUTATIONAL FLOW

The nanosized-metal-grain pattern-dependent model is developed by perturbations of metal grains for various patterns with the EC process from evaluating the one-perceptron method. The equations of model are given by

$$\delta V_{th}^{HWK}(k) = (V_{th}^{nom} - V_{th}^{HWK}(k))/Num \qquad (9)$$

$$\delta V_{th}^{LWK}(k) = (V_{th}^{nom} - V_{th}^{LWK}(k))/Num \qquad (10)$$

$$\delta V_{th} = \sum_{k=1}^{MGN} (\delta V_{th}^{HWK}(k) \times \mathrm{W\_HWK} + \delta V_{th}^{LWK}(k) \times \mathrm{W\_LWK}) \qquad (11)$$

and

$$V_{th} = W_{nom} \times V_{th}^{nom} + \delta V_{th}, \qquad (12)$$

where the V_{th}^{nom} is the V_{th} of the nominal device, the V_{th}^{HWK} is the V_{th} of the devices affected by HWK, the V_{th}^{LWK} is the V_{th} of the devices affected by LWK, Num is the number of location grains of the RS, k is the index number of metal grain, the W_nom, W_HWK and W_LWK are the weights for the nominal device and the devices affected by HWK and LWK, respectively. The perturbation of each metal grain is calculated by (9) and (10) with respect to various grain patterns. Based on the assumption of the superposition principle, the total perturbation of all grains is calculated by (11), where the weights of (11) are used to execute the EC process.

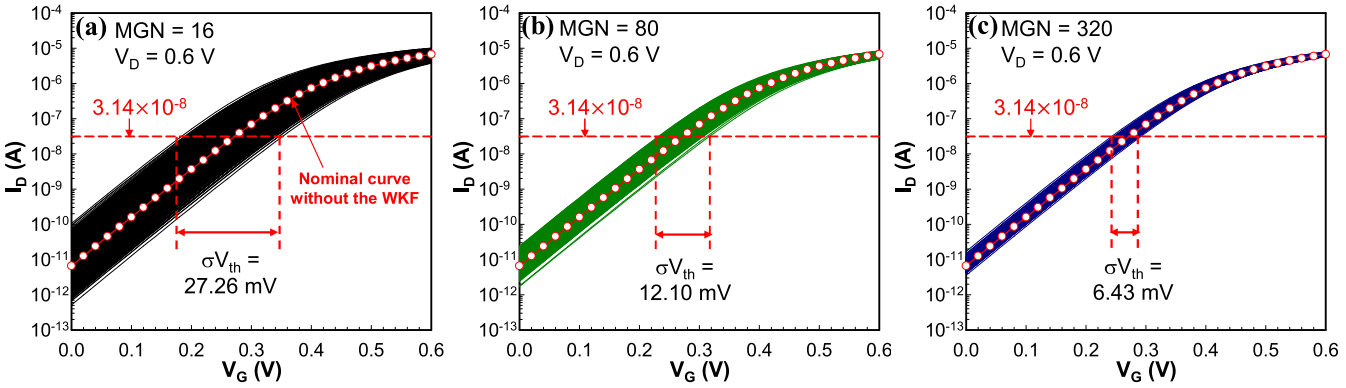


FIGURE 7. The fluctuated I_D-V_G of 2000 studied devices with random patterns induced by the WKF from the 3D-DS, where the red dot line is the nominal curve without the WKF. (a) MGN = 16. (b) MGN = 80. (c) MGN = 320.

Without the EC process, the W_nom, W_HWK and W_LWK are set to one. After calculating (11), the V_{th} can be obtained by (12). Fig. 6 illustrates the computational flow of the nanosized-metal-grain pattern-dependent model for various MGNs and process parameters. First, we set various MGNs, sample size, HWK with p = 0.6, and LWK with p = 0.4 as inputs of the MC program. The MC program will generate various patterns. Second, depending on the MGNs, the different computational flow will be selected. For example, if the case of MGN = 16 is selected, the nominal V_{th} will be calculated by (1). Because (2) will be fed into (3) and (4), we must calculate (2) before the separation of HWK and LWK. After the separation, (3) and (4) will be calculated. Then, the perturbation of each metal grain with HWK and LWK can be obtained by (9) and (10), respectively. After executing the loop of k from 1 to MGN, the sum of all perturbations will be obtained by (11). Finally, the program will output the value of V_{th} by (12). After repeating various patterns, we can obtain each V_{th} for each pattern; and, then the WKF-induced σV_{th}. For other cases of MGNs, the same flow of the case of MGN = 16 can be followed. To minimize the computational errors, a simplified one-perceptron method is adopted to guarantee the high accuracy of the proposed model by adjusting the weights. For the simplified one-perceptron method, we do not consider the activation function as used in the conventional methods [27]. Moreover, in the conventional one-perceptron method, the number of weights depends on different MGN and the initial weights are randomly generated by a random number generator. This may not ensure the global convergence in the learning process for various MGNs and process parameters. Instead, the simplified one-perceptron method only has the W_LWK and W_HWK for various MGNs and process parameters because of the separation of the HWK and LWK. The weight can vary from 0.5 to 1.5 to ensure the global convergence because the perturbations of metal grains are computed by (9) and (10). In this work, we vary the W_LWK to find an optimal W_LWK so that the computational errors can be minimized, where W_HWK = 1 is assumed. 2000 samples are randomly generated and simulated by the 3D-DS for the model validation, where the metric definitions of ER and relative ER (RER) are $[(\sigma V_{th}^{\text{Model}} - \sigma V_{th}^{\text{3D-DS}})/\text{Mean}] \times 100\%$ and $[(\sigma V_{th}^{\text{Model}} - \sigma V_{th}^{\text{3D-DS}})/\sigma V_{th}^{\text{3D-DS}}] \times 100\%$, respectively.

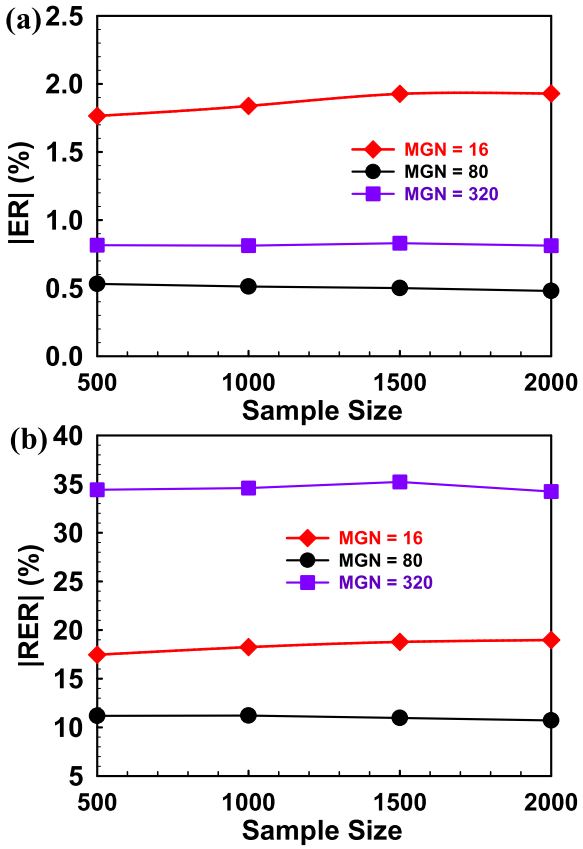
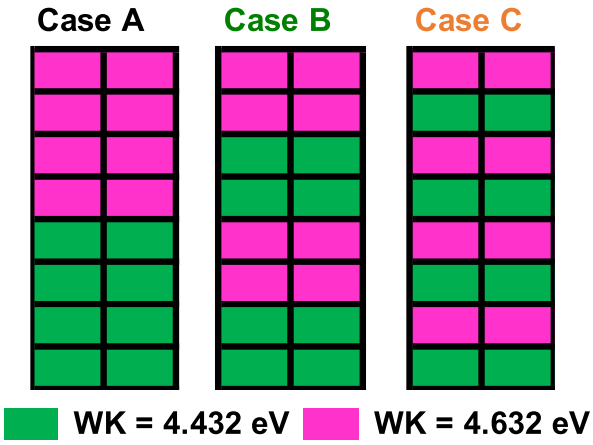


FIGURE 8. The ER and RER of σV_{th} versus sample size for various MGNs without the EC process. (a) ER. (b) RER.

III. RESULTS AND DISCUSSIONS

To validate the model accuracy, 2000 samples are randomly generated and simulated by the 3D-DS for the GAA Si



Item	$V_{th}^{3D\text{-}DS}$ (mV)	V_{th}^{Model} (mV)	Error (mV)
Case A	233.683	250.638	16.955
Case B	246.064	250.638	4.574
Case C	253.000	250.638	-2.361

FIGURE 9. The cases of different cluster metal grains with the same grains of LWK and the corresponding V_{th} from the 3D-DS and model for the GAA Si NW MOSFETs.

NW MOSFETs with respect to various MGNs, as shown in Fig. 7. The magnitude of V_{th} is extracted by a constant current method from the fluctuated I_D-V_G curves, where the current criterion of V_{th} is $(W_{ch}/L_g) \times 10^{-8}$ A, and W_{ch} is the circumference of a cylindrical channel. Fig. 8 illustrates the ER and RER of σV_{th} versus sample size for various MGNs without the EC process. As shown in Fig. 8(a), the ER of σV_{th} is slightly affected by sample size for the case of MGN = 16. This is because the case of MGN = 16 has a comparatively larger grain size, therefore, it has more location effect as compared to the case of MGN = 80, etc. As shown in Fig. 8(b), the RER becomes large than the ER because of the lower value of σV_{th}, it is prominent especially for the case of MGN = 320. The error sources may be attributed to the clusters of metal grains. It is because of the difference between HWK and LWK. Thus, the input values from (9) and (10) will be biased. Then, the errors will be generated from the proposed model. To analyze the clusters of metal grains, as shown in Fig. 9, the V_{th} of Case A from the 3D-DS has a much lower value than that from the model because of the clusters of metal grains. It also can be seen that it causes a large error if the patterns have the clusters of metal grains. Fig. 10 shows the conduction band of Case A, Case B and Case C in the on-state ($V_G = V_D = 0.6$ V) along the channel position from S to D, respectively. Fig. 10(a)–(c) and 10(a')–(c') show that the cluster of metal grains with the low WK in the channel of Case A alters the conduction band distributions of the 3D and 2D views in the channel. Moreover, Fig. 10(d) shows the plot of the 1D conduction band from S to D along the channel. This plot shows that the conduction band of Case A is relatively lower than that of Case B and Case C in the channel, thus generating a lower

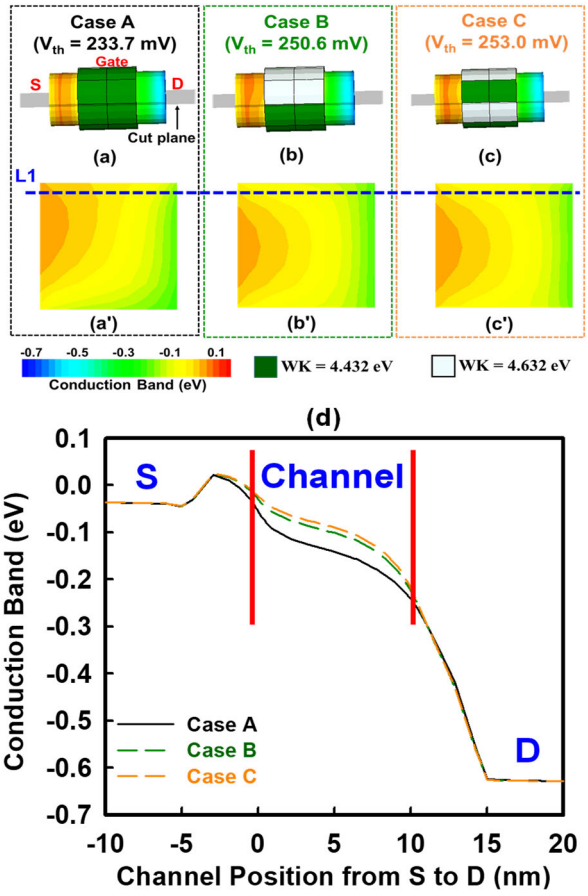


FIGURE 10. The conduction band of Case A, Case B and Case C in the on-state ($V_G = V_D = 0.6$ V) along the channel position from S to D, where the L1 cut-line is along the channel from S to D: (a)-(c) 3D view, (a')-(c') 2D view, and (d) 1D plot in the channel region.

V_{th} in Case A than that in Case B and Case C. To further reduce the computational errors, the EC process will be necessary for the proposed model. Using (11), we can adjust the W_LWK to fine tune the value of fluctuation and calculate the updated σV_{th}. Therefore, by varying the W_LWK (where W_HWK = 1 is assumed), the RER plots are obtained, as shown in Fig. 11.

It can be observed that the plots are showing linear behavior. Thus, the optimized value of the W_LWK can be obtained by the linear RER plot at RER = 0. By using the optimized value of the W_LWK from (11), the updated σV_{th} can be obtained. Notably, the optimized value of the W_LWK also can be achieved by minimizing the value of root-mean-square error. Fig. 12 illustrates the ER and RER versus sample size for various MGNs after the EC process. We find that the ER and RER have significant reductions after the EC process as compared to Fig. 8. In addition, both ER and RER are stable as the sample size increases. It indicates that the proposed model with the EC process can significantly reduce the errors and predict the accurate value of σV_{th} in a large enough sample size. Table 2 summarizes the computational cost and error rate for various major methods [17], [25], [32]. To estimate the results of the WKF-induced σV_{th} with respect

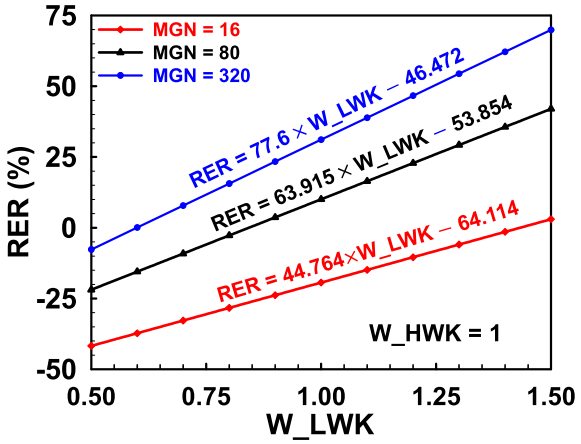


FIGURE 11. The RER versus W_LWK of the V_{th} on the GAA Si NW MOSFET for various MGNs, where 100 samples are used for the EC.

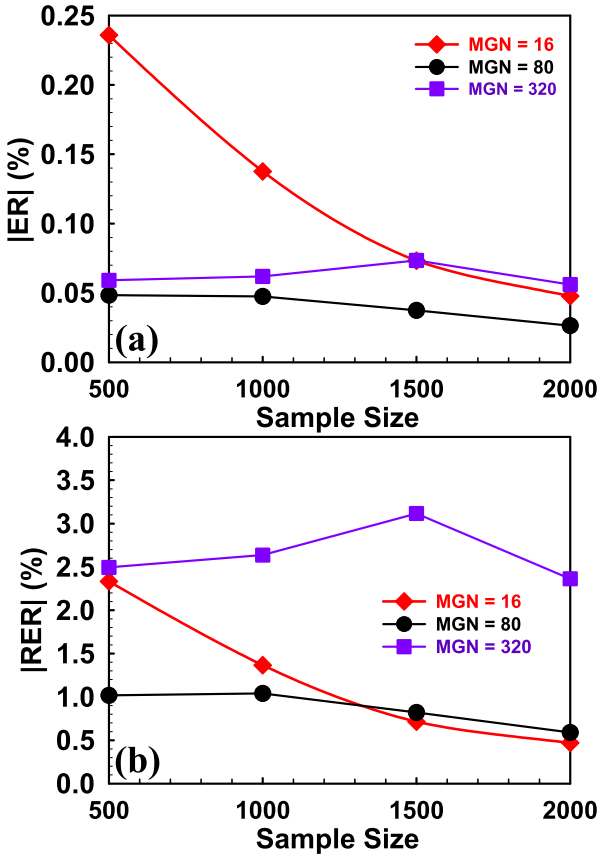


FIGURE 12. The (a) ER and (b) RER versus sample size for various MGNs after the EC process.

to various process parameters, we proceed with the 3D-DS simulation for the DOEs of the concerned process parameters (R, L_g, T_{ox}, and Ch_dop). As shown in Fig. 13(a), in the same range of the process parameters, the variation of R plays a key factor to affect the variation of V_{th}. Thus, we vary different R to estimate the WKF-induced σV_{th}. For different MGNs, as shown in Fig. 13(b), the variations of σV_{th} are insignificant (< 2%). However, the improvement of σV_{th} is large for relatively larger MGN. It can be observed that the grain size is a key factor affecting the results of the WKF. Additionally, the proposed model can be applied not only with the results of the 3D-DS, but also directly from measured data. By applying a similar procedure, we can model and analyze the WKF-induced σV_{th} of 3D vertically stacked GAA NW MOSFETs with multi-channels. As shown in Fig. 14, the WKF-induced σV_{th} decreases exponentially by increasing the number of channels (or MGN) for the 3D-DS and the proposed model.

TABLE 2. List of the computational cost and error rate for various major methods.

Method	ER (%)	Computational Cost	Reference
3D-DS	0	High	This work
EWK Model	< 30%*	Low	[17], [32]
ML	< 1%	Medium	[25]
Proposed Model	< 1%	Low	This work

* The value of ER was depending on different grain sizes and devices.

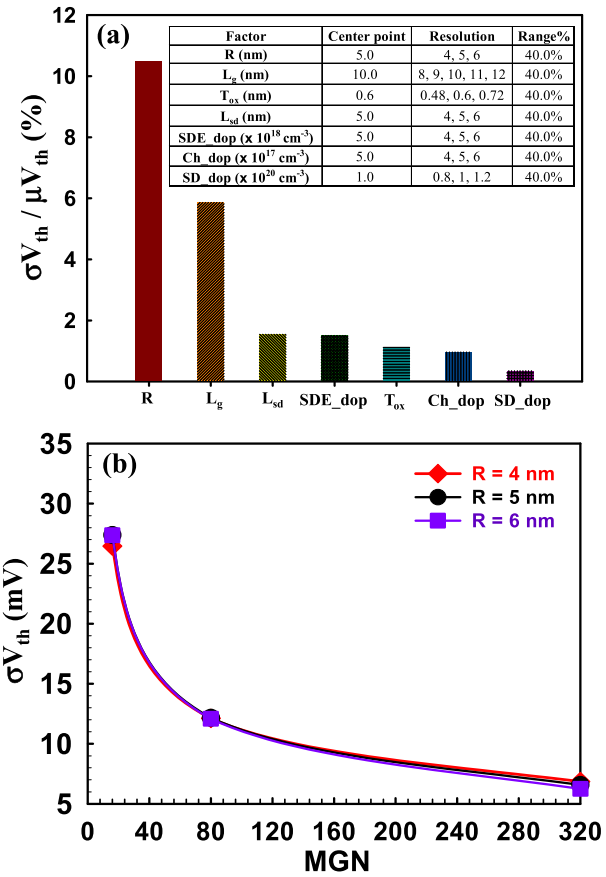


FIGURE 13. (a) The Pareto chart of process variations for different process parameters. (b) A plot of the σV_{th} versus MGN for various R.

Furthermore, the absolute value of ER is lower than 0.4%. Thus, we can fit the data by using (13) for the GAA devices

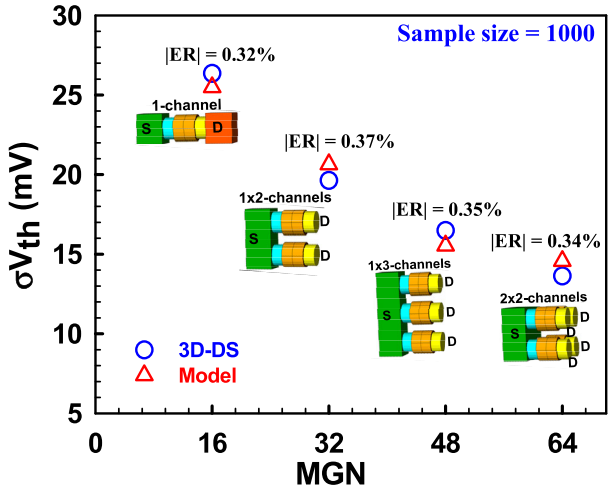


FIGURE 14. Plot of the σV_{th} versus MGN for the 3D-DS and model.

TABLE 3. The extracted parameters of the statistical model [14] for the 3d-ds and the proposed model.

Method	α (mV)	β	γ	R^2
3D-DS	4.325	15.58	70.25	0.998
Proposed Model	3.306	23.93	10.09	0.980

with multi-channels [14].

$$\sigma V_{th}(MGN) = \alpha \times exp[\beta/(MGN + \gamma)], \qquad (13)$$

where the best regression coefficients: α (mV), β (unit-less), and γ (unit-less) are listed in Table 3. The value of the R^2 is close to 1. Therefore, based on the low ER and high efficiency, we believe that the proposed model with the EC process is a good predictive approach for the WKF-induced σV_{th}. Furthermore, in the process viewpoint, if the distributions of grain sizes can be measured by transmission electron microscopy from the foundries in advance, the proposed model can estimate the σV_{th} affected by the WKF immediately. And, it can be plugged into circuit simulation for estimating the performance of CMOS circuits by circuit simulator and feedback the results for the yield improvement before the test results of chip-probe yield.

IV. CONCLUSION

In this paper, we have presented the nanosized-metal-grain pattern-dependent model to calculate the WKF-induced σV_{th}. Moreover, the MVNLR has been explored with and without the EC process on the GAA Si NW MOSFETs for various process conditions (R (range: 4∼6 nm), Lg (range: 9∼11 nm), Ch_dop (range: 3∼7 × 10^{17} cm^{-3}), and T_{ox} (range: 0.6∼0.8 nm) and MGNs (16∼320)). It has been proved that by using the proposed model, the high computational cost can be reduced significantly and the explored model outperforms in terms of accuracy using the EC process having fewer simulated sample sizes. Notably, the proposed model is only suitable for the GAA Si NW MOSFETs with cylindrical channels. Currently, we are investigating the variability of vertically stacked GAA nanosheet. The approach reported in this work can also be advanced to model the variability of complementary FETs (CFETs) for circuit applications of CFETs.

REFERENCES

[1] R. Chau, "Process and packaging innovations for Moore's law continuation and beyond," in *IEDM Tech. Dig.*, Dec. 2019, pp. 1–6.
[2] J. Appenzeller, J. Knoch, M. T. Björk, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2827–2845, Nov. 2008, doi: 10.1109/TED.2008.2008011.
[3] H. Mertens *et al.*, "Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 158–159.
[4] S. Barraud, V. Lapras, B. Previtali, M. P. Samson, J. Lacord, S. Martinie, M.-A. Jaud, S. Athanasiou, F. Triozon, O. Rozeau, J. M. Hartmann, C. Vizioz, C. Comboroure, F. Andrieu, J. C. Barbe, M. Vinet, and T. Ernst, "Performance and design considerations for gate-all-around stacked-NanoWires FETs," in *IEDM Tech. Dig.*, Dec. 2017, pp. 677–680.
[5] T. Al-Ameri, V. P. Georgiev, F. Adamu-Lema, and A. Asenov, "Simulation study of vertically stacked lateral Si nanowires transistors for 5-nm CMOS applications," *IEEE J. Electron Devices Soc.*, vol. 5, no. 6, pp. 466–472, Nov. 2017, doi: 10.1109/JEDS.2017.2752465.
[6] G. Espineira, D. Nagy, G. Indalecio, A. J. Garcia-Loureiro, K. Kalna, and N. Seoane, "Impact of gate edge roughness variability on FinFET and gate-all-around nanowire FET," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 510–513, Apr. 2019, doi: 10.1109/LED.2019.2900494.
[7] C. Millar, D. Reid, G. Roy, S. Roy, and A. Asenov, "Accurate statistical description of random dopant-induced threshold voltage variability," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 946–948, Aug. 2008, doi: 10.1109/LED.2008.2001030.
[8] W.-L. Sung and Y. Li, "DC/AC/RF characteristic fluctuations induced by various random discrete dopants of gate-all-around silicon nanowire n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2638–2646, Jun. 2018, doi: 10.1109/TED.2018.2822484.
[9] M.-L. Fan, V. P.-H. Hu, Y.-N. Chen, P. Su, and C.-T. Chuang, "Analysis of single-trap-induced random telegraph noise on FinFET devices, 6T SRAM cell, and logic circuits," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2227–2234, Aug. 2012, doi: 10.1109/TED.2012.2200686.
[10] W.-L. Sung, Y.-S. Yang, and Y. Li, "Work-function fluctuation of gate-all-around silicon nanowire n-MOSFETs: A unified comparison between cuboid and Voronoi methods," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 151–159, 2021, doi: 10.1109/JEDS.2020.3046608.
[11] W.-L. Sung and Y. Li, "Effects of random number and location of the nanosized metal grains on the threshold voltage variability of silicon gate-all-around nanowire n-type metal-oxide-semiconductor field-effect transistors," *J. Comput. Electron.*, vol. 19, no. 4, pp. 1478–1484, Dec. 2020, doi: 10.1007/s10825-020-01572-9.
[12] H. Nam, Y. Lee, J.-D. Park, and C. Shin, "Study of work-function variation in high-k/metal-gate gate-all-around nanowire MOSFET," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3338–3341, Aug. 2016.
[13] Y. Li, H.-T. Chang, C.-N. Lai, P.-J. Chao, and C.-Y. Chen, "Process variation effect, metal-gate work-function fluctuation and random dopant fluctuation of 10-nm gate-all-around silicon nanowire MOSFET devices," in *IEDM Tech. Dig.*, Dec. 2015, pp. 887–890.
[14] W.-L. Sung and Y. Li, "Statistical prediction of nanosized-metal-grain-induced threshold-voltage variability for 3D vertically stacked silicon gate-all-around nanowire n-MOSFETs," *J. Electron. Mater.*, vol. 49, no. 11, pp. 6865–6871, Nov. 2020, doi: 10.1007/s11664-020-08332-2.
[15] K. Ko, M. Kang, J. Jeon, and H. Shin, "Compact model strategy of metal-gate work-function variation for ultrascaled FinFET and vertical GAA FETs," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1613–1616, Mar. 2019, doi: 10.1109/TED.2019.2891677.
[16] H. Dadgour, V. De, and K. Banerjee, "Statistical modeling of metal-gate work-function variability in emerging device technologies and implications for circuit design," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, Nov. 2008, pp. 270–277.

[17] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—Part I: Modeling, analysis, and experimental validation," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504–2514, Oct. 2010, doi: 10.1109/ted.2010.2063191.

[18] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—Part II: Implications for process, device, and circuit design," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2515–2525, Oct. 2010, doi: 10.1109/TED.2010.2063270.

[19] S. H. Rasouli, C. Xu, N. Singh, and K. Banerjee, "A physical model for work-function variation in ultra-short channel metal-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1507–1509, Nov. 2011, doi: 10.1109/LED.2011.2166531.

[20] X. Zhang, J. Li, M. Grubbs, M. Deal, B. Magyari-Köpe, B. M. Clemens, and Y. Nishi, "Physical model of the impact of metal grain work function variability on emerging dual metal gate MOSFETs and its implication for SRAM reliability," in *IEDM Tech. Dig.*, Dec. 2009, pp. 57–60.

[21] P. H. Vardhan, S. Mittal, S. Ganguly, and U. Ganguly, "Analytical estimation of threshold voltage variability by metal gate granularity in finfet," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3071–3076, Aug. 2017, doi: 10.1109/TED.2017.2712763.

[22] G. Indalecio, N. Seoane, K. Kalna, and A. J. García-Loureiro, "Fluctuation sensitivity map: A novel technique to characterise and predict device behaviour under metal grain work-function variability effects," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1695–1701, Apr. 2017, doi: 10.1109/TED.2017.2670060.

[23] P. H. Vardhan, S. Mittal, S. Ganguly, and U. Ganguly, "Analytical modeling of metal gate granularity based threshold voltage variability in NWFET," *Solid-State Electron.*, vol. 147, pp. 26–34, Sep. 2018, doi: 10.1016/j.sse.2018.05.007.

[24] P. H. Vardhan, S. Ganguly, and U. Ganguly, "An accurate expression to estimate the metal gate granularity induced threshold voltage variability in NWFETs," *Solid-State Electron.*, vol. 152, pp. 65–71, Feb. 2019, doi: 10.1016/j.sse.2018.12.003.

[25] K. Ko, J. K. Lee, M. Kang, J. Jeon, and H. Shin, "Prediction of process variation effect for ultrascaled GAA vertical FET devices using a machine learning approach," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4474–4477, Oct. 2019, doi: 10.1109/TED.2019.2937786.

[26] C. Akbar, Y. Li, and W.-L. Sung, "Deep learning algorithms for the work function fluctuation of random nanosized metal grains on gate-all-around silicon nanowire MOSFETs," *IEEE Access*, vol. 9, pp. 73467–73481, 2021, doi: 10.1109/ACCESS.2021.3079981.

[27] F. Chollet, *Deep Learning With Python*. New York, NY, USA: Manning Publications Co., 2021.

[28] M. M. Hussain, M. A. Quevedo-Lopez, H. N. Alshareef, H. C. Wen, D. Larison, B. Gnade, and M. El-Bouanani, "Thermal annealing effects on a representative high-*k*/metal film stack," *Semicond. Sci. Technol.*, vol. 21, no. 10, pp. 1437–1440, Oct. 2006, doi: 10.1088/0268-1242/21/10/012.

[29] A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, K. Matsuo, T. Shibata, Y. Tsunashima, K. Suguro, and T. Arikado, "Improvement of threshold voltage deviation in damascene metal gate transistors," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1604–1611, Aug. 2001, doi: 10.1109/16.936569.

[30] G. Indalecio, A. J. García-Loureiro, N. S. Iglesias, and K. Kalna, "Study of metal-gate work-function variation using Voronoi cells: Comparison of Rayleigh and gamma distributions," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2625–2628, Jun. 2016, doi: 10.1109/TED.2016.2556749.

[31] H. Nam and C. Shina, "Comparative study in work-function variation: Gaussian vs. Rayleigh distribution for grain size," *IEICE Electron. Exp.*, vol. 10, no. 9, pp. 1–5, 2013, doi: 10.1587/elex.10.20130109.

[32] S.-H. Chou, M.-L. Fan, and P. Su, "Investigation and comparison of work function variation for FinFET and UTB SOI devices using a Voronoi approach," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1485–1489, Apr. 2013, doi: 10.1109/TED.2013.2248087.

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