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Expandable Non-Isolated Multi-Input Single-Output DC-DC Converter With High Voltage Gain and Zero-Ripple Input Currents

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ABSTRACT In this paper, an expandable non-isolated multi-input single-output DC-DC high voltage gain converter with the capability of cancelling input current ripples is proposed, which can be applied in photovoltaic (PV) systems. The proposed converter has several advantages including: 1) it provides a single voltage gain for the whole range of duty cycles; 2) the duty cycle's operating range is not decreased when increasing the number of input stages; 3) it has a simple switching pattern, and all switches go on and off, simultaneously; 4) the current ripple of each input stage is eliminated for the whole range of duty cycles; 5) the output load has a common ground with all input voltage sources; and 6) the voltage stress on switches is low. In this paper, the proposed converter in a dual-input single-output (DISO) form is introduced at first, and its general form with multi-input single-output (MISO) is then analyzed. Following that, the voltage gain, voltage and current stresses on switches, diodes and capacitors, and input current ripple cancelling condition are calculated. Finally, experimental results are used to validate the calculated theoretical results.

INDEX TERMS DC-DC power converters, high-voltage gain, input current ripple cancellation, dual input single output (DISO), multi input single output (MISO).

NOMENCLATURE

V_{i1}, V_{i2}	Low input DC voltages.
V_o	High output DC voltage.
T_s	A complete switching period.
f_s	Switching frequency.
D_1, D_2	Diodes.
S_1, S_2	Switches.
D	Duty cycle of Switches S_1 and S_2.
C_1, C_2, C_{i1}, C_{i2}	Capacitors.
T_1	Transformer of the first coupling inductor.
L_{m1}	Magnetizing inductance of the first coupled inductor.
L_{k1}	Leakage inductance of the first coupled inductor.
T_2	Transformer of the second coupling inductor.
L_{m2}	Magnetizing inductance of the second coupling inductor.
L_{k2}	Leakage inductance of the second coupled inductor.
n_{p1}	The number of turns of the first winding for the first coupled inductor.
n_{s1}	The number of turns of the second winding for the first coupled inductor.
n_{t1}	The number of turns of the third winding of the first coupled inductor.
n_{p2}	The number of turns of the first winding for the second coupled inductor.

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n_{s2}	The number of turns of the second winding for the second coupled inductor.
n_{t2}	The number of turns of the third windings for the second coupled inductor.
N_{S1}	Turn ratio of the second winding over the first winding for the first coupled inductor.
N_{S2}	Turn ratio of the second winding over the first winding for the first coupled inductor.
V_{C1}	The voltage across capacitor, C_1.
I_{h1}	The maximum value of the current of L_{m1} at t_1.
I_{h2}	The maximum value of the current of L_{m2} at t_1.
$I_{\ell 1}$	The minimum value of the current of L_{m1} at t_0 and t_2.
$I_{\ell 2}$	The minimum value of the current of L_{m2} at t_0 and t_2.
i_{Lm1}	The current of the magnetizing inductance in the first coupling inductor.
i_{Lm2}	The current of the magnetizing inductance in the second coupling inductor.
v_{Lm1}	The voltage across the magnetizing inductance in the first coupling inductor.
v_{Lm2}	The voltage across the magnetizing inductance in the second coupling inductor.
v_{Lk1}	The voltage across the leakage inductance in the first coupling inductor.
v_{Lk2}	The voltage across the leakage inductance in the second coupling inductor.
$\tilde{v}_{Lm1}$	The average voltage across the magnetizing inductance in the first coupling inductor.
$\tilde{v}_{Lm2}$	The average voltage across the magnetizing inductance in the second coupling inductor.
G_T	The total voltage gain of the proposed converter.
V_{S1}	The voltage stress on the switch S_1.
V_{S2}	The voltage stress on the switch S_2.
V_{D1}	The voltage stress on the diode D_1.
V_{D2}	The voltage stress on the diode D_2.
i_{S1}, i_{S2}	Currents passing through the switches at each moment.
i_{D1}, i_{D2}	Currents passing through the diodes at each moment.
I_{S1}	Average current passing through the switch S_1 during a switching period under steady state.
I_{S2}	Average current passing through the switch S_2 during a switching period under steady state.
I_{D1}	Average current passing through the diode D_1 during a switching period under steady state.
I_{D2}	Average current passing through the diode D_2 during a switching period under steady state.
I_{Lm1}	Average magnetizing inductance current of magnetizing inductance of the first coupled inductor.
I_{Lm2}	Average magnetizing inductance current of magnetizing inductance of the second coupled inductor.
$\tilde{i}_{C1}$	Average current passing through the capacitor C_1.
I_{i1}	Average input current passing through the input DC voltage source, V_{i1}.
I_{i2}	Average current passing through the DC voltage source, V_{i2}.
I_o	Output current crossing through the output load R_o.
P_{i1}	Input power from the first input DC voltage source V_{i1}.
P_{i2}	Input power from the first input DC voltage source V_{i2}.
P_o	Output power through the output load R_o.
Δi_{Lm1}	Current ripples of the magnetizing inductance L_{m1}.
Δi_{Lm2}	Current ripples of the magnetizing inductance L_{m2}.
ΔV_{Co}	Voltage ripples across the output capacitor.
ΔV_C	Voltage ripples across the capacitors.
ΔV_{C-ESR}	Voltage ripples across the capacitors caused by the Equivalent Series Resistance (ESR) of capacitors.
ΔI_C	Current ripples of the capacitor.
V_{Ci1}, V_{Ci2}	Average voltage across the input capacitors, C_{i1}, C_{i2}.
$C_{1\_\min}$, $C_{2\_\min}$	The minimum designed capacitance value for the capacitors, C_1, C_2.
$C_{i1\_\min}$, $C_{i2\_\min}$	The minimum designed capacitance value for the input capacitors at ports 1 and 2.
$C_{i1}\mid_{ESR}$	The minimum capacitance value for the output capacitor at port 1 considering ESR.
$C_{i1}\mid_{THT}$	The minimum capacitance value for the output capacitor at port 1 considering the Total holding Time (THT).
$C_{o\_\min}$	The minimum designed capacitance value for the output capacitor.

R_o	Output load.
r_{S1}, r_{S2}	The internal resistors of switches, S_1, S_2.
r_{Lp1}, r_{Ls1}, r_{Lt1}	The internal resistors of three windings of the first coupled inductor.
r_{Lp2}, r_{Ls2}, r_{Lt2}	The internal resistors of three windings of the second coupled inductor.
r_C	Internal resistors of capacitors.
τ_{Lm1} and τ_{Lm2}	The normalized magnetizing-inductor time constants.

I. INTRODUCTION

In recent years, different types of multi-input single-output (MISO) DC-DC converters are presented for photovoltaic (PV) systems to deliver the required power and regulated voltage. Because the voltage level of PV sources is low, so a step-up DC-DC converter is needed to increase their voltage levels in practical applications. Single-input single-output (SISO) converters are suitable for low power applications in PV off-grid systems. To extract the high power from a PV system, multiple PV sources can be integrated by using only one MISO DC-DC converter instead of using multiple SISO DC-DC converters [1]–[4]. The conventional technique to integrate several PV sources is to connect each PV source separately to a SISO converter with an individual controller, and the output power of each SISO converter is delivered to a DC bus [1]. By using only one MISO converter, the number of components is much decreased; and only one control system is needed to achieve the maximum power point tracking (MPPT) of PV sources, instead of applying several MPPT controllers in the conventional PV system.

In the conventional technique of integration of multiple PV sources, multiple SISO converters can be connected either in parallel or in series at their output ports [1]–[4]. In PV systems, obtaining MPPT on each PV module, which is named as distributed MPPT (DMPPT), is necessary to increase the extracted power from PV. DMPPT may include various PV panel-converter topologies, such as parallel module integrated converters (MICs) topology, cascaded MICs topology, and MISO converters. Although DMPPT can be implemented by the SISO step-up converters, but a MISO converter for implementing DMPPT is a more cost-effective solution [1], [3]. Moreover, to achieve suitable voltage regulation of PVs by MPPT controllers, the converters with zero input current ripples are desired [5].

The structure of the converter in [6] is simple and all ports are connected to a common ground, i.e., input and output ports of the converter share the same ground, which is important for renewable energy conversion units. However, to increase the voltage gain, the duty cycle of the switches must be increased, which leads to the high voltage stress on switches and diodes. The converters in [7] and [8] have low input current ripples, which can improve the life span of the renewable energy sources, and both converters are also connected to a common ground. However, similar to the topology presented in [6], voltage gains of these converters are close to the conventional boost converter.

In [9]–[11], two-input single-output DC-DC converters are presented. These converters are connected to a common ground, except for the converter presented in [9]. All of these DC-DC converters have the low voltage stress on their switches and diodes. The switching pattern of the presented converters in [10] and [11] are interleaved, which leads to the reduced stress on semiconductor elements. However, converters with interleaved switching patterns have different conversion ratios for different ranges of duty cycles, which leads to more complexity of the control system in the whole range of duty cycles.

In [12] and [13], transformer-less multi-input multi-output (MIMO) DC-DC converters are presented. These converters utilize diode-capacitor cells to increase their voltage conversion ratio. They have the merit of low input current ripples. However, these converters suffer from being non-common grounded. Since these converters do not have transformers in their structure, extra transformers should be used to isolate the ground of DC output loads in practical implementations. However, utilizing several extra transformers to isolate the ground of non-common grounded transformer-less converters will increase the volume, size, losses, parasitic effects, the cost of implemented circuit, and decrease the efficiency. As a result, being common-grounded in multi input converters is a desirable feature, which can lead to lower size, lower cost, higher efficiency converters than non-common grounded converters.

The significant difference between the converters presented in [12] and [13] is that the output ports of the converter in [13] can provide different ranges of voltages, but the output ports of the converter in [12] can only provide a single voltage.

Transformer-based multiport DC converters are presented in [14]–[16]. The modules of the converter presented in [15] can be extended and have multi-output ports. The main drawback of the converter in [15] is its high input current ripples, but the converters in [14] and [16] are isolated with low input current ripples.

To explain the importance and necessity of a non-isolated topology for the proposed converter, the non-isolated converter topology does not have any galvanic isolation between input and output sides, variations on the input side directly affect the output side of the converter. On the other hand, having a separate ground in isolated converters means it does not impose any effect of the input over the output side of the converter, so it can operate on a wide range of inputs and generate a stable output. Safety concern is a common reason to use an isolated converter. Isolation of a converter's input and output ports enhances the safety of consumers on the load side, also prevents short circuit currents on the load side passing through and reaching the source side.

To achieve isolation, isolated converters use transformers in their structures (one transformer for a single-input single-output converter, and several transformers for

a multi-input multi-output (MIMO) converter), causing a higher volume, higher cost, lower power density and lower efficiency than non-isolated converters; while non-isolated converters don't need such isolation transformers. Another issue is isolated converters require expensive measurement equipment, for example, isolated probes, to measure currents. In an isolated MIMO converter, several isolated probes are needed, which significantly increase the overall cost. Therefore, if the safety of consumers is not a concern, non-isolated converters are good choice for multi-input converters. Isolated converters also persist several significant issues, such as leakage inductance, core saturation, thermal effect, high voltage spikes across the switches, and huge size, which make them costly compared to non-isolated converters.

The proposed multi-input DC-DC converter in this paper is for integrated PV applications with multiple PV sources supplying a high voltage DC bus, where isolating input and output terminals is not necessary. The most important feature for the proposed converter in this paper is to achieve high power density, small size, high efficiency, and low cost. In this case, a non-isolated topology is an ideal choice.

It is recognized in the literature that non-isolated DC-DC converter topologies are more beneficial and feasible options than isolated converter topologies for renewable energy applications, despite certain issues, such as high duty cycle ratio, low voltage gain, and additional circuitry in non-isolated DC-DC converter topologies. To overcome existing technical issues and improve the performance of non-isolated DC-DC converters for renewable energy applications, we have conducted research and proposed the novel multi-input non-isolated DC-DC converter topology in this paper.

DC-DC converters presented in [17]–[19] are three-port coupled-inductor-based converters. These converters have utilized a high number of components and their input ports cannot be extended.

Multiple-input high step-up DC-DC converters can be used in grid-connected PV power generation systems due to the following advantages [1], [3], [4], [10], [11], [20], [21]:

1) In the multi-input converter with N input ports, its component number is lower than a N-input power conversion system utilizing N individual SISO converters. By adding a lower number of components, more input DC ports (PV sources) can be added to the system to achieve the high output power level of DC bus. As a result, the cost is decreased by using multi-input converters with the capability of having extendable input ports.
2) By using the MISO converter, only one control system is needed to achieve the maximum power point tracking (MPPT) of PV sources, while the conventional PV system requires several MPPT controllers.
3) Multi-input converters are capable to supply the load under the condition of turning-off one input port, i.e., when one of the input ports does not deliver the power and is turned off, the other port can still supply the load, which is the feature required in grid-connected PV systems. Although using two SISO converters satisfy this requirement, double number of components and double number of control systems are needed, which results in the decreased efficiency and increased costs.
4) Considering that the extracted voltage of PV sources is low, a step-up DC-DC converter is required to increase the low input voltage level of PV sources (in the range of 10-30 V) to the high voltage level of DC bus (in the range of 380-400 V).

Moreover, based on [10], [11], and [21], most of traditional multi-input single-output converters and dual-input single-output converters are interleaved multi-phase and two-phase converters.

A multi-phase converter utilizes a higher number of components to achieve the reduced voltage and current stress on switches and diodes than a single-phase converter, and thus, to achieve the improved efficiency. Because when the current and voltage stress on switches is decreased, conduction losses are decreased accordingly, which results in the improved efficiency than the single-phase type. For example, the voltage and current stress on semiconductors for a conventional boost two-phase converter is reduced to only half of that for a conventional single-phase converter by using a double amount of components. The efficiency of the two-phase boost converter is improved compared to the conventional single-phase boost converter.

A multi-phase converter does need a more complicated control system than a single-phase converter due to multiple different voltage gain functions (for example the two phase converters have two different voltage gain functions for duty cycles lower or higher than 0.5). Consequently, in multi-phase converters with the increased number of input voltage sources, the number of voltage gain functions also increases, leading to a complicated control system.

In [22], a PV system using two-input DC-DC converter with buck–boost operation has been presented, where a PV panel and an ac line are integrated to supply the load through the two-input DC-DC converter. In this system, when input power from PV panels is not generated at night, the commercial ac line delivers power to the load. As a result, stable output power is available.

For multi-input single-output converters with the ability to add more input renewable energy sources, if the load needs higher power by adding an extra input port that interfaces an extra power source, and by making small changes in the control system, more power can be transferred to the load by using less semiconductor number and occupying less volume. On the other hand, having multi-input renewable energy sources makes the supply of the converter more reliable, which means whenever one of the sources is not generating power or generating less power than normal, the load will be supplied by other sources. In general, multi-input converters have advantages, such as possible to simultaneously use two or more power sources, lower cost due to applying less passive components, smaller size of the converter, and larger power generation because of using several power

sources [23]. In Fig. 1 (a), the distributed PV system by using several SISO converters is shown; Fig. 1(b) illustrates the distributed PV system with a MISO converter.

In [24], coupled inductor-based converters with high voltage gain are presented. In [25], a high voltage gain converter based on switched capacitor cell is proposed, it is a three-phase converter with a narrow duty cycle range for achieving its optimum performance, and it has three voltage gain functions which need a complicated control system. Converters in [24] and [25] are SISO converters with high input current ripples, so they are not suitable for PV applications.

The main contribution of this paper is to propose a multi-input single-output high step-up converter with the following advantages: 1) using a MISO converter (Fig. 1(b)) instead of several SISO converters (Fig. 1(a)) for integrated PV source applications can decrease the number of components and the size of the converter); 2) input current ripples in input ports are be cancelled for the whole range of duty cycles; 3) comparing to other conventional converters of same type, the proposed converter has the highest voltage gain (to increase the low input voltage of PV sources), and decreased power losses due to less component counts; 4) the proposed converter has low voltage stresses on diodes; 5) it has extendable structure with an extendable number of input ports (which can decrease the system's cost when several PV sources are integrated); 6) the proposed converter has a single voltage gain function for the whole range of the duty cycle D ($0 < D < 1$), this feature leads to a simple control system for the output voltage regulation; 7) The proposed converter is common-grounded for all input ports which makes it applicable for integration of several PV sources.

Finally, the accuracy performance of proposed converter is verified by using the theoretical and experimental results.

The paper is organized as follows: In Section II, the structure and operating principles of the proposed multi-input single-output converter are explained for the continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and critical parameters and scenarios (the voltage and current stresses on switches, average currents of switches and inductors, voltage gain, expandable converter analysis, required conditions for cancelling input current ripples, design consideration) are also analyzed and obtained in this section; to clarify the better performance of the proposed circuit, it is compared with other recently reported similar converters in the literature and the comparison results are presented in Section III; To verify the practical operation of the proposed converter, the circuit is implemented in laboratory and the experimental results are reconfirmed by comparing with theoretical results in Section IV; and conclusions are drawn in Section V.

II. OPERATING PRINCIPLES OF THE PROPOSED TWO-INPUT, SINGLE-OUTPUT CONVERTER

The main power circuit of the proposed converter in the form of two-input, single-output and its equivalent circuit by using a transformer model of coupled inductors are shown in Figs. 2(a) and 2(b), respectively. The power circuit of the proposed converter with extendable input module stages are illustrated in Fig. 2(c). In this part, we first study the proposed converter in the form of two-input single-output in this section, then we will expand it to the general form of multi-input single-output in the following section.

In Fig. 2(a), in each input module stage, a coupled inductor is used to increase the voltage gain and eliminate input current ripples. Each coupled inductor has the magnetizing inductor of L_m and leakage inductor of L_k. The first, second and third winding of each coupled inductor has n_p, n_s and n_t turns, respectively. As a result, the turns ratio of second and third windings of each coupled inductor is considered as $N_s = n_s/n_p$ and $N_t = n_t/n_p$. In the proposed converter, to eliminate the input current ripple, the turns ratio of third winding of each coupled inductor is considered as $N_t = n_t/n_p = 1$ ($N_{t1} = n_{t1}/n_{p1} = 1$ and $N_{t2} = n_{t2}/n_{p2} = 1$).

In the coupled inductors, the coupling coefficient K is defined as $K = \sqrt{L_m/(L_m + L_k)}$, i.e., the ratio of inductances L_k and L_m is defined as $(L_k/L_m) = (1 - K^2)/K^2$. Since the chosen capacitors are large enough, the voltage across the capacitors C_{i1}, C_{i2}, C_1, C_2 are considered as constant voltage levels with magnitudes of $V_{Ci1} = V_{i1}$, $V_{Ci2} = V_{i2}$, V_{C1}, V_{C2}, respectively. The switching pattern of switches, voltage and current waveforms are shown in Fig. 3. The proposed converter has two switches with the same trigger pulses, and thus, a simple switching pattern is needed.

The proposed converter has two operating modes during a switching period as shown in Fig. 4. The two modes, Mode 1 and Mode 2, are explained in detail below.

Mode 1 [$t_0 \le t < t_1$***]:*** This mode starts with turning on the switches, S_1 and S_2; while the diodes, D_1 and D_2, are off. The equivalent circuit of Mode 1 is shown in Fig. 4(a). The voltages of the inductors, v_{Lm1} and v_{Lm2}, are determined as $v_{Lm1} = V_{i1}$ and $v_{Lm2} = V_{i2} + V_{C1} + n_{s1}v_{Lm1} = V_{i2} + V_{C1} + n_{s1}V_{i1}$, respectively. Consequently, the currents of the inductors, i_{Lm1}, i_{Lm2}, are calculated as follows:

$$i_{Lm1} = (V_{i1}/L_{m1})\,(t - t_0) + I_{\ell 1} \quad (1)$$

$$i_{Lm2} = (V_{i2} + V_{C1} + n_{s1}V_{i1})\,(t - t_0)/L_{m2} + I_{\ell 2} \quad (2)$$

where the initial currents i_{Lm1} and i_{Lm2} in Mode 1 are $I_{\ell 1}$ and $I_{\ell 2}$, respectively.

Mode 2 [$t_1 \le t < t_2$***]:*** At the beginning of this mode, the switches, S_1 and S_2, are turned off, and the diodes, D_1 and D_2, are turned on. The equivalent circuit of Mode 2 is shown in Fig. 4(b). So The voltages of the inductors, v_{Lm1} and v_{Lm2}, are obtained as $v_{Lm1} = (V_{i1} - V_{C1})/(1 + n_{s1})$ and $v_{Lm2} = (V_{i2} - V_{C2})/(1 + n_{s2})$, respectively. Consequently, the currents of the inductors, i_{Lm1}, i_{Lm2} are calculated by

$$i_{Lm1} = (V_{i1} - V_{C1})\,(t - t_0)/[(1 + n_{s1})L_{m1}] + I_{h1} \quad (3)$$

$$i_{Lm2} = (V_{i2} - V_{C2})\,(t - t_0)/[(1 + n_{s2})L_{m2}] + I_{h2} \quad (4)$$

where the initial currents i_{Lm1} and i_{Lm2} in Mode 2 are I_{h1} and I_{h2}, respectively.

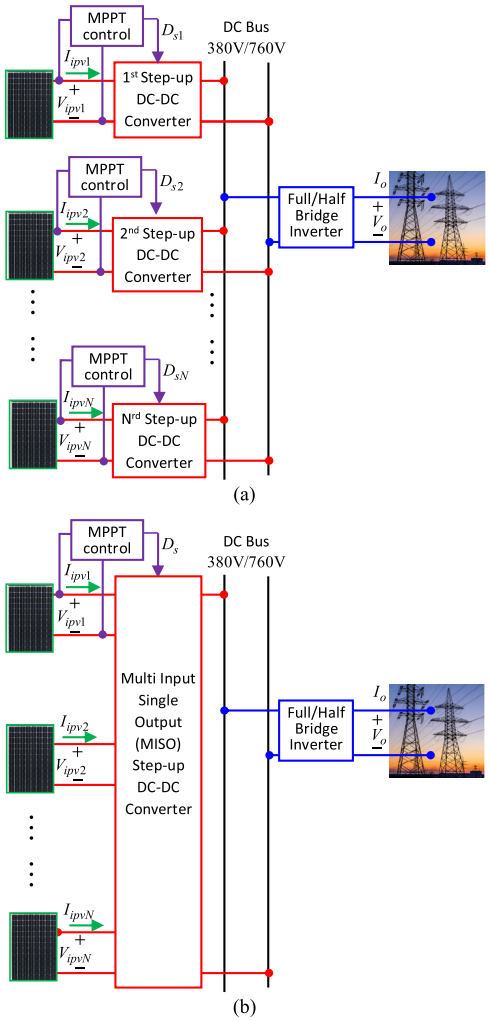

FIGURE 1. The distributed PV system: (a) using several SISO converters (conventional systems), (b) using a MISO converter.

A. VOLTAGE GAIN AND VOLTAGES OF CAPACITORS

By considering the voltage balance law for the inductors L_{m2} and L_{m1}, the average voltages across the inductors during a switching period should be equal to zero as follows:

$$\tilde{v}_{Lm1} = DV_{i1} + (1-D)[(V_{i1} - V_{C1})/(1+n_{s1})] = 0 \quad (5)$$

$$\tilde{v}_{Lm2} = D(V_{i2} + V_{C1} + n_{s1}V_{i1}) + (1-D)(V_{i2} - V_{C2})/(1+n_{s2}) = 0 \quad (6)$$

By simplifying (5) and (6), we have

$$V_{C1} = [(1+n_{s1}D)/(1-D)]\,V_{i1} \quad (7)$$

$$V_o = V_{C2} = \frac{(1+n_{s1})(1+n_{s2})D}{(1-D)^2}V_{i1} + \frac{1+n_{s2}D}{1-D}V_{i2} \quad (8)$$

B. VOLTAGE STRESS ON DIODES AND SWITCHES

During Mode 1 ($0 \le t < DT_s$), the diodes D_1 and D_2 are off, and the voltage stress on diodes are calculated by

$$V_{D1} = n_{s1}v_{Lm1} + V_{C1} = n_{s1}\,V_{i1} + V_{C1} = (1+n_{s1})\,V_{i1}/(1-D) \quad (9)$$

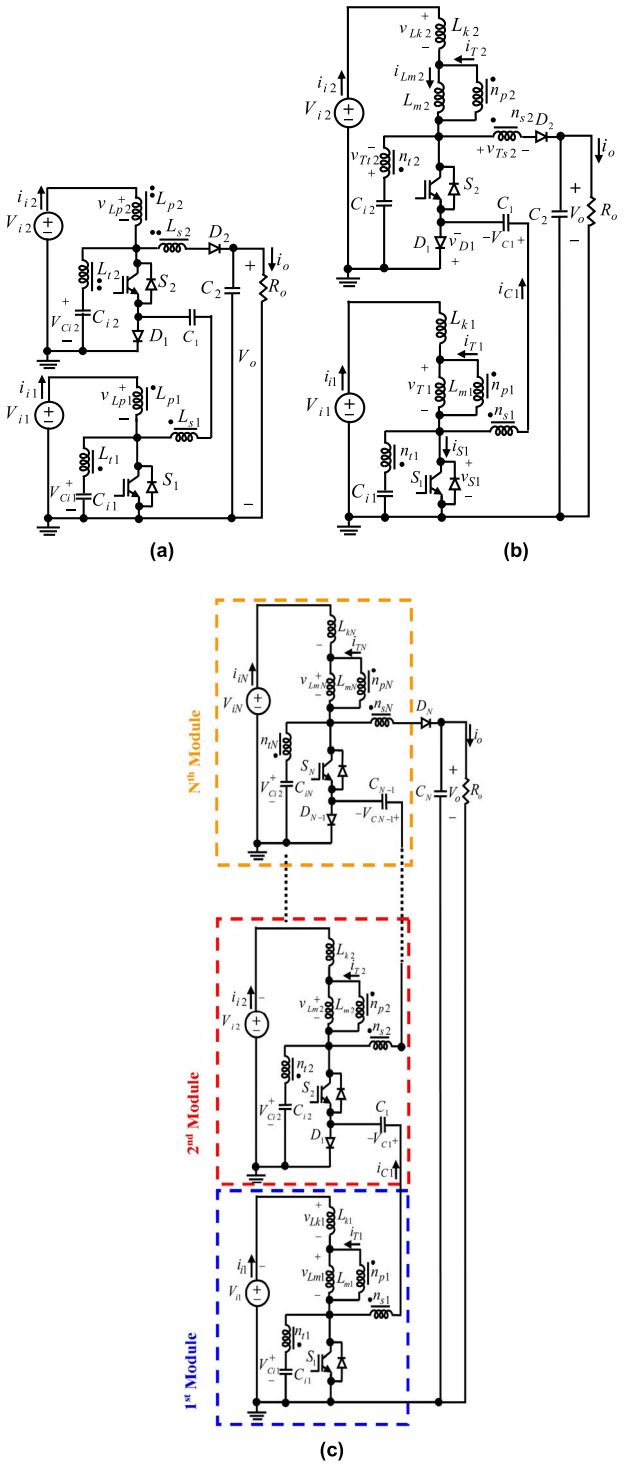

FIGURE 2. (a) The proposed converter; (b) Equivalent power circuit of the proposed converter by using transformer model; (c) The proposed developed converter.

$$V_{D2} = [(1+n_{s1})(1+n_{s2})]V_{i1}/(1-D)^2 + (1+n_{s2})V_{i2}/(1-D) \quad (10)$$

During Mode 2 ($DT_s \le t < T_s$), the switches S_1 and S_2 are off, and the voltage stress on switches can be

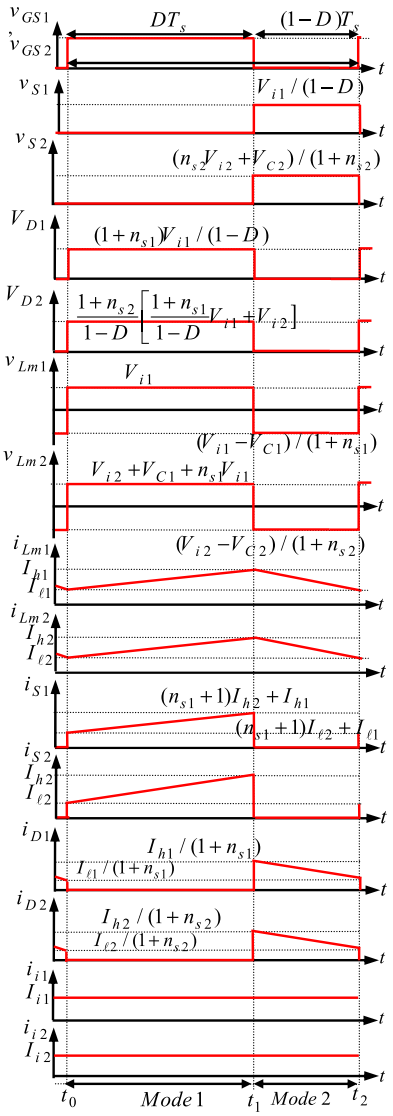

FIGURE 3. Voltage and current waveforms of the proposed converter for the CCM operation.

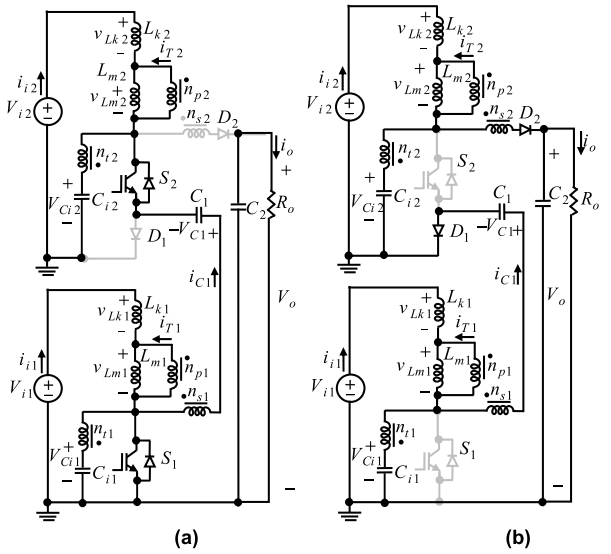

FIGURE 4. The equivalent circuits of the proposed converter: (a) Mode 1; (b) Mode 2.

obtained by

$$V_{S1} = n_{s1}\, v_{Lm1} + V_{C1} = V_{i1}/(1-D) \quad (11)$$

$$V_{S2} = [(1+n_{s1})D]V_{i1}/(1-D)^2 + V_{i2}/(1-D) \quad (12)$$

Based on (11) and (12), the voltage stress on the switches are lower than the high output voltage. $V_{i1} = 18\,V$, $V_{i2} = 12\,V$.

The voltage stresses on switches and diodes at the switching moment are calculated depending to input voltages using (9)-(12). As a result, the switching voltage of switches and diodes over the three input voltage levels of $V_{i1} = V_{i2} = 30\,V$, $V_{i1} = V_{i2} = 20\,V$, and $V_{i1} = V_{i2} = 10\,V$ for the whole range of duty cycles ($0 < D < 1$) is plotted in Fig. 5. In Fig. 5, the turn ratio of the coupled inductors is considered as $n_{s1} = n_{s2} = 1.5$.

As shown in Table 4 in Section VI, the parameters for the implemented prototype's power circuit are selected as $V_{i1} = 18\,V$, $V_{i2} = 12\,V$, $n_{s1} = n_{s2} = 1.5$, $D = 0.6$ to achieve the output voltage as $V_o = 470\,V$, which is applicable to supply the output load of the DC bus as shown in Figure 1. Therefore, the turn ratio used to plot Figure 5 is $n_{s1} = n_{s2} = 1.5$, the purpose is to provide a theoretical analysis for voltage stress on switches and diodes before choosing suitable switches and diodes for the prototype. In Figure 5, the region between the plotted green curve ($V_{i1} = V_{i2} = 10\,V$ (and blue curve ($V_{i1} = V_{i2} = 20\,V$ (for the duty cycle equal to 0.6 shows the range of voltage stress levels on switches and diodes, which include the experimental operating point.

Using (8), $n_{s1} = n_{s2} = 1.5$, $D = 0.6$, and $\mathrm{V_{i1}} = \mathrm{V_{i2}}$, the output voltage is derived as $\mathrm{V_o} = 28.18\ \mathrm{V_i}$. For $\mathrm{V_{i1}} = \mathrm{V_{i2}} = 10$ V and $\mathrm{V_{i1}} = \mathrm{V_{i2}} = 20$ V, the output voltages are calculated as 281.8 V and 563.75 V, respectively. Since we choose the output voltage of the implemented prototype to be 470 V, the exact values of voltage stress on switches and diodes for the prototype during experiments are $\mathrm{V_{S1-exp}} = 45$ V, $\mathrm{V_{S2-exp}} = 198.7$ V, $\mathrm{V_{D1-exp}} = 112.5$ V, $\mathrm{V_{D2-exp}} = 770$ V, which are displayed as red points in Figure 5. Figure 5 gives a theoretical insight of voltage stress values for the operating point of the prototype during experiments, which is helpful in the component selection for the prototype.

The voltage stresses on switches and diodes at the switching moment versus seven different turn ratios and the duty cycle for the constant input voltage values is illustrated in Figure 6. To plot this figure, the input voltage values are the same as the selected values for experimental implementation ($V_{i1} = 18\,V$ and $V_{i2} = 12\,V$). In Fig. 6, the turn ratios equal to 1, 1.5, 2, 2.5, 3, 3.5, and 4 are used. Moreover, voltage stresses on switches and diodes under a constant duty cycle of $D = 0.6$ and the constant turn ratio of coupled inductors of $n_{s1} = n_{s2} = 1.5$ versus the input voltage in the range of $0 < V_{i1} = V_{i2} < 30\,V$ is plotted in Fig. 7.

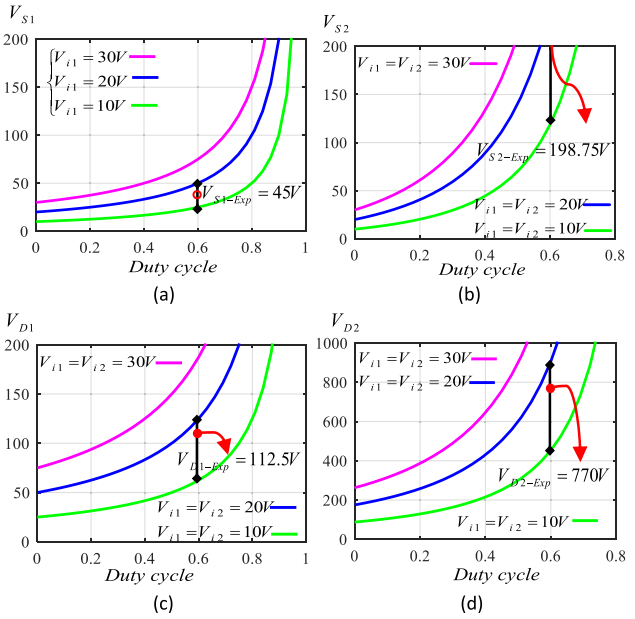

FIGURE 5. Voltage stresses on semiconductors at the switching moment versus three different input voltage levels and the duty cycle D for $n_{s1} = n_{s2} = 1.5$: (a) V_{S1}; (b) V_{S2}; (c) V_{D1}; (d) V_{D2}.

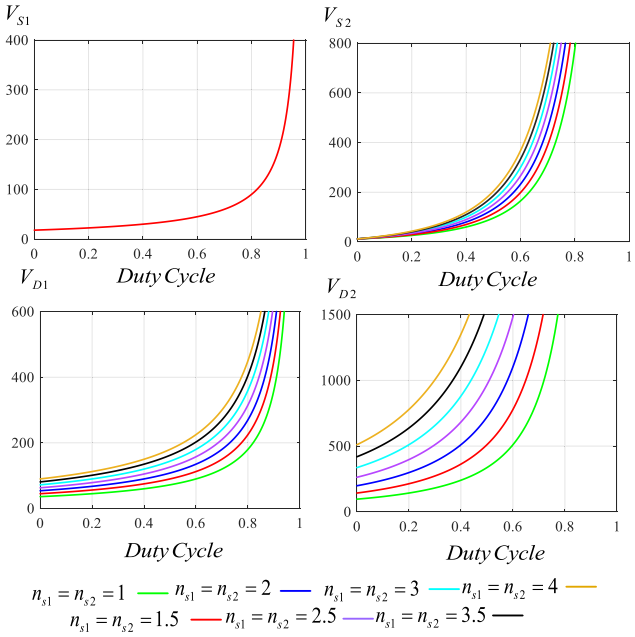

FIGURE 6. Voltage stresses on switches and diodes at the switching moment versus the seven different turn ratio and the duty cycle D for $V_{i1} = 18V$ and $V_{i2} = 12V$.

C. AVERAGE CURRENTS OF SWITCHES

During Mode 1 ($0 \leq t < DT_s$), the switches S_1 and S_2 are on, and the currents flowing through the second transformer's windings are written as $i_{T2} + i_{Tt2} + n_{s2}i_{Ts2} = 0$. By applying Kirchhoffs Current Law (KCL) in the second stage, the current stress on the switch S_2 is calculated by

$$i_{S2} = i_{i2} + i_{Tt2} = i_{i2} - i_{T2} = i_{i2} - (i_{i2} - i_{Lm2}) = i_{Lm2} \tag{13}$$

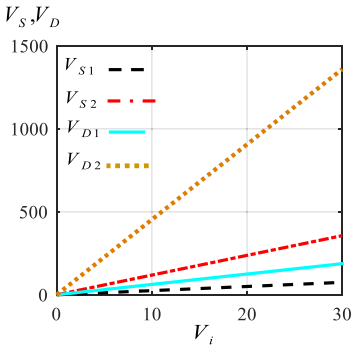

FIGURE 7. Voltage stresses on switches and diodes at the switching moment versus the input voltage level for $D = 0.6$ and $n_{s1} = n_{s2} = 1.5$.

Based on Fig. 4(a), the currents flowing through the first transformer's windings can be written as $i_{T1} + i_{Tt1} - n_{s1}i_{S2} = 0$. By applying KCL in the first stage, the current stress on the switch S_1 is calculated by

$$i_{S1} = i_{i1} + i_{Tt1} + i_{S2} = (n_{s1} + 1)i_{Lm2} + i_{Lm1} \tag{14}$$

D. AVERAGE CURRENTS OF DIODES

During Mode 2 ($DT_s \leq t < T_s$), the diodes D_1 and D_2 are conducting. As a result, the current stresses on diodes D_1 and D_2 during Mode 2 can be obtained by

$$i_{D1} = i_{Lm1}/(1 + n_{s1}) \tag{15}$$
$$i_{D2} = i_{Lm2}/(1 + n_{s2}) \tag{16}$$

Based on Fig. 2(b), the average currents passing through diodes and switches during a switching period are calculated as $I_{D2} = I_o$, $I_{S2} = I_{D1} = I_{i1} - I_o$, $I_{S1} = I_{i2}$. These equations are obtained based on that the average currents passing through the capacitors are equal to zero.

E. AVERAGE CURRENTS OF CAPACITORS AND INDUCTORS

At the steady state, the current balance law for capacitors should be verified. Therefore, the average current of the capacitors C_1 and C_2 during a switching period are equal to zero. Therefore, the average current of the capacitors C_1 and C_2 can be written as follows:

$$\tilde{i}_{C1} = D(-i_{Lm2}) + (1 - D)[i_{Lm1}/(1 + n_{s1})] = 0 \tag{17}$$
$$\tilde{i}_{C2} = D(-i_o) + (1 - D)[i_{Lm2}/(1 + n_{s2}) - i_o] = 0 \tag{18}$$

By simplifying (17)-(18), the average values of the inductors' currents are calculated as:

$$I_{Lm2} = (1 + n_{s2})I_o/(1 - D) \tag{19}$$
$$I_{Lm1} = \frac{D(1 + n_{s1})}{1 - D} I_{Lm2} = \frac{D(1 + n_{s1})(1 + n_{s2})}{(1 - D)^2} I_o \tag{20}$$

As a result, the maximum and minimum values of currents i_{Lm1} and i_{Lm2} are written as I_{h1}, I_{h2} and $I_{\ell 1}$, $I_{\ell 2}$, respectively by

$$I_{h1} = I_{Lm1} + \frac{\Delta i_{Lm1}}{2} = \frac{D(1 + n_{s1})(1 + n_{s2})}{(1 - D)^2} I_o + \frac{V_{i1}\, DT_s}{2L_{m1}} \tag{21}$$

$$I_{\ell 1} = I_{Lm1} - \frac{\Delta i_{Lm1}}{2} = \frac{D(1+n_{s1})(1+n_{s2})}{(1-D)^2} I_o - \frac{V_{i1}\, DT_s}{2L_{m1}} \tag{22}$$

$$I_{h2} = I_{Lm2} + \frac{\Delta i_{Lm2}}{2} = \frac{1+n_{s2}}{1-D} I_o + \frac{(V_{i2} + V_{C1} + n_{s1}\, V_{i1})\, DT_s}{2L_{m2}} \tag{23}$$

$$I_{\ell 2} = I_{Lm2} - \frac{\Delta i_{Lm2}}{2} = \frac{1+n_{s2}}{1-D} I_o - \frac{(V_{i2} + V_{C1} + n_{s1}\, V_{i1})\, DT_s}{2L_{m2}} \tag{24}$$

Consequently, the maximum currents of switches and diodes can be written as

$$i_{S2-\max} = I_{h2} \tag{25}$$

$$i_{S1-\max} = (n_{s1}+1) I_{h2} + I_{h1} \tag{26}$$

$$i_{D1-\max} = I_{h1}/(n_{s1}+1) \tag{27}$$

$$i_{D2-\max} = I_{h2}/(1+n_{s2}) \tag{28}$$

By considering that at the steady state, the average currents of the capacitors are equal to zero, the average input current of the first and second stages are calculated by

$$I_{i1} = I_{Lm1} + I_{T1} = I_{Lm1} = [D(1+n_{s1})(1+n_{s2})/(1-D)^2]\, I_o \tag{29}$$

$$I_{i2} = I_{Lm2} + I_{T2} = I_{Lm2} - n_{s2}\, I_o = (1+n_{s2}D) I_o/(1-D) \tag{30}$$

As a result, the switching current crossing through the switches and diodes over the three input voltage levels of $V_{i1} = V_{i2} = 10\,V$, $V_{i1} = V_{i2} = 20\,V$, $V_{i1} = V_{i2} = 30\,V$ for the whole range of duty cycle ($0 < D < 1$) is plotted in Fig. 8. In Fig. 8, the turns ratio of coupled inductors are considered as $n_{s1} = n_{s2} = 1.5$. Moreover, the current stresses on switches and diodes under a constant duty cycle of $D = 0.6$ and a constant turn ratio of the coupled inductors of $n_{s1} = n_{s2} = 1.5$ versus the input voltage in the range of $0 < V_{i1} = V_{i2} < 30\,V$ is plotted in Fig. 9.

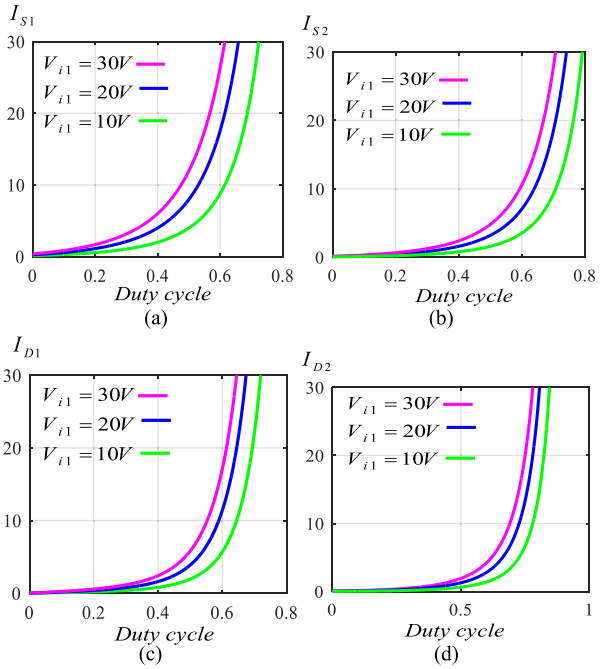

FIGURE 8. The maximum current stresses on semiconductors at the switching moment versus three different input voltage levels and the duty cycle D for $n_{s1} = n_{s2} = 1.5$; (a) I_{S1}; (b) I_{S2}; (c) I_{D1}; (d) I_{D2}.

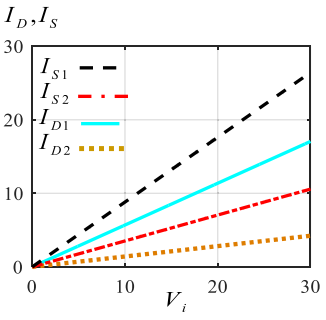

FIGURE 9. The maximum current stresses on switches and diodes at the switching moment versus the input voltage level for $D = 0.6$ and $n_{s1} = n_{s2} = 1.5$.

F. VOLTAGE GAIN OF PROPOSED CONVERTER CONSIDERING EQUIVALENT SERIES RESISTANCE OF COMPONENTS

In this part, equations of the voltages on capacitors and the output voltage of the proposed converter by considering Equivalent Series Resistance (ESR) of all components are calculated. Fig. 10 shows the equivalent circuits of the proposed converter considering ESR of components in the two operating modes during a switching period.

By considering the voltage balance law for the inductors L_{m2} and L_{m1}, the voltage of the capacitor V_{C1} and the output voltage are obtained as follows:

$$V_{C1} = [(1+n_{s1}D)/(1-D)]\, V_{i1} - [D(1+n_{s1})/(1-D)]\,(r_{Lp1} + r_{S1}/D) I_{i1} - [r_{Lp1} I_{i1} + (r_{Ls1} + r_{C1} + r_{D1})(I_{i2} - I_o)/(1-D)] \tag{31}$$

$$V_o = \left[\frac{(1+n_{s1})(1+n_{s2})D}{(1-D)^2} V_{i1} + \frac{1+n_{s2}D}{1-D} V_{i2}\right] \times \frac{1}{1+F/R_o} \tag{32}$$

where the parameter F is defined as follows:

$$F = \frac{(1+n_{s2})D}{(1-D)} \times \left[\begin{array}{l} \frac{(1+n_{s1})D}{(1-D)}(r_{Lp1} + \frac{r_{S1}}{D}) a_1 + r_{Lp1} a_1 \\ + \frac{(r_{Ls1} + r_{C1} + r_{D1})(a_2 - 1)}{(1-D)} + r_{Lp2} a_2 + \\ + \frac{(r_{S2} + r_{C1} + r_{Ls1})(a_2 - 1)}{D} + \frac{r_{S1} a_1}{D} + \\ + n_{S1} a_1 (r_{Lp1} + r_{S1}/D) \end{array}\right] + r_{Lp2} a_2 + (r_{Ls2} + r_{D2} - D r_{C2})/(1-D) \tag{33}$$

where the output current can be replaced as $I_o = V_o/R_o$, and the parameters a_1 and a_2 can be defined by $a_1 = I_{i1}/I_o = [D(1 + n_{s1})(1 + n_{s2})/(1 - D)^2]$ and $a_2 = I_{i2}/I_o = (1 + n_{s2}D)/(1 - D)$.

The voltage gain of the proposed converter including ESRs of inductors, diodes and switches can be plotted in Fig. 11. The ESRs of components are $r_{S1} = 8\,m\,\Omega$, $r_{S2} = 6.6\,m\,\Omega$, $r_{D1} = 5.8\,m\,\Omega$, $r_{D2} = 8.3\,m\,\Omega$, $r_{C1} = r_{C2} = 0.05\,\Omega$, $r_{Lp1} = r_{Lp2} = r_{Ls1} = r_{Ls2} = r_{Lt1} = r_{Lt2} = 0.02\,\Omega$. The other parameters are $n_{S1} = n_{S2} = 1.5$, $V_{i1} = 18\ V$, $V_{i2} = 12\ V$ which are the same parameters used for the experimental prototype circuit. The output load is selected as $R_o = 2000\Omega$, $R_o = 1500\Omega$, $R_o = 1000\Omega$ and $R_o = 500\Omega$ for the curves with the color of blue, purple, green, and red, respectively, which are plotted based on (32).

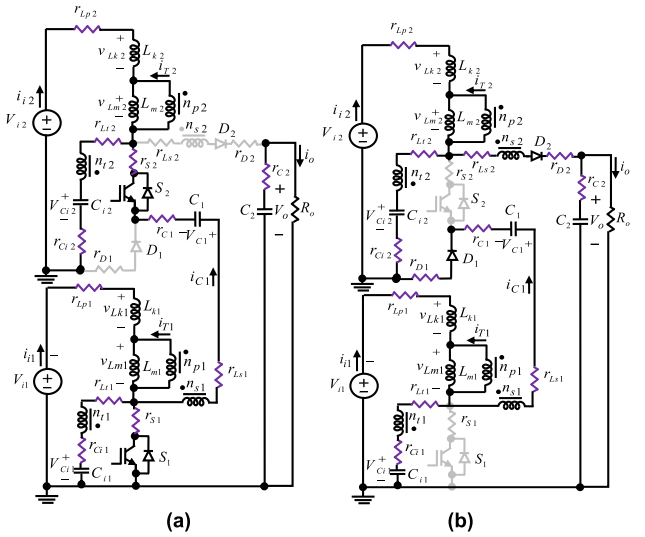

FIGURE 10. The equivalent circuits of the proposed converter considering ESR of components: (a) Mode 1; (b) Mode 2.

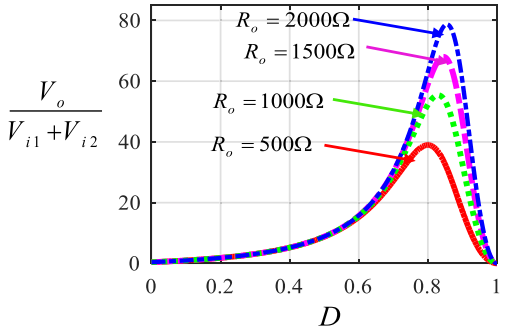

FIGURE 11. The voltage gain versus the duty cycle including ESRs of inductors, switches and diodes.

As a result, the maximum achievable voltage gain values for the proposed converter for four different output loads ($R_o = 2000\Omega$, $R_o = 1500\Omega$, $R_o = 1000\Omega$, and $R_o = 500\Omega$) are different, because the output power P_o would change ($P_o = V_o^2/R_o$) when the output load R_o changes. In Fig. 11, the maximum achievable voltage gains are 39, 55, 70 and 80 for Ro equal to 500 Ω, 1000 Ω, 1500 Ω, and 2000 Ω, respectively. As shown in Figure 11, the duty cycle corresponding to the maximum voltage gains is around 0.8 for different output load values. The maximum achievable voltage gain increases with the increase of the output load. Ref [21] did the similar calculation and plots for voltage gains of the converter.

G. DISCONTINUOUS CONDUCTION MODE OPERATION OF THE PROPOSED CONVERTER

1) OPERATION MODES

The proposed converter has four operating modes in the discontinuous conduction mode (DCM) operation.

The theoretical waveforms of voltages and currents of the proposed converter in DCM operation are shown in Fig. 12.

Mode 1 ($t_0 \le t < t_1$): In this mode, only the switches, S_1 and S_2, are conducting, while the diodes, D_1 and D_2, are off. Considering Fig. 2(b), we have $v_{Lm2} = V_{i2} + V_{C1} + n_{s1}v_{Lm1} = V_{i2} + V_{C1} + n_{s1}V_{i1}$.

Mode 2 ($t_1 \le t < t_2$): In this mode, the switches, S_1 and S_2, are turned off, and the diodes, D_1 and D_2, are turned on. As a result considering Fig. 2(b), the voltages, v_{Lm1} and v_{Lm2}, are obtained by $v_{Lm1} = (V_{i1} - V_{C1})/(1 + n_{s1})$ and $v_{Lm2} = (V_{i2} - V_{C2})/(1 + n_{s2})$, respectively.

Mode 3 ($t_2 \le t < t_3$): This mode starts by decreasing the inductor current i_{Lm2} to zero at the end of the previous mode, then the diode D_2 would be turned off at the beginning moment of this mode. As a result, in Mode 3, only the diode D_1 is conducting in Fig. 2(b), while other switches and the diode are off. Under this condition, the voltages, v_{Lm1} and v_{Lm2}, are equal to $v_{Lm1} = (V_{i1} - V_{C1})/(1 + n_{s1})$ and zero, respectively.

Mode 4 ($t_3 \le t < t_4$): *In* the beginning of this mode, the inductor current i_{Lm1} decreases to zero, and all diodes and switches are turned off. Consequently, from Fig. 2(b) the voltages, v_{Lm1} and v_{Lm2}, are equal to zero.

2) VOLTAGE GAIN AND CAPACITORS' VOLTAGES FOR (DCM) OPERATION

By considering the voltage balance law for the inductors L_{m2} and L_{m1}, the average voltages across the inductors during a switching period should be equal to zero as follows:

$$\tilde{v}_{Lm1} = DV_{i1} + \alpha_1[(V_{i1} - V_{C1})/(1 + n_{s1})] = 0 \quad (34)$$

$$\tilde{v}_{Lm2} = D(V_{i2} + V_{C1} + n_{s1}V_{i1}) + \alpha_2\frac{V_{i2} - V_{C2}}{1 + n_{s2}} = 0 \quad (35)$$

Consequently, the output voltage under DCM condition is

$$\begin{aligned} V_o = V_{C2} &= \frac{D(V_{i2} + V_{C1} + n_{s1}V_{i1})(1 + n_{s2})}{\alpha_2} + V_{i2} \\ &= \frac{D(1 + n_{s2})(1 + n_{s1})}{\alpha_2}\left(\frac{\alpha_1 + D}{\alpha_1}\right)V_{i1} \\ &\quad + \frac{D(1 + n_{s2}) + \alpha_2}{\alpha_2}V_{i2} \end{aligned} \quad (36)$$

At the steady state, the current balance law for capacitors should be verified. Therefore, the average currents of the

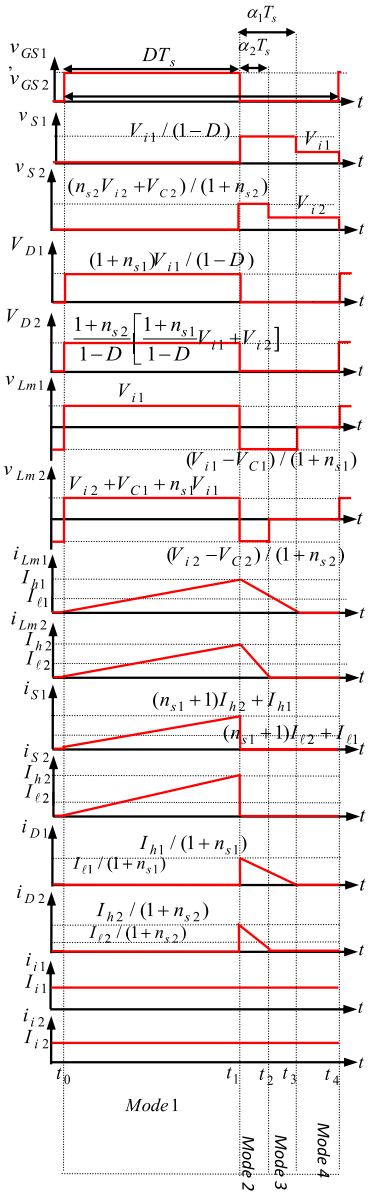

FIGURE 12. Voltage and current waveforms of the proposed converter under the DCM operation.

inductors are

$$I_{Lm1} = [D(1+n_{s1})(1+n_{s2})]I_o/\alpha_1\alpha_2 \quad (37)$$

$$I_{Lm2} = [(1+n_{s2})/\alpha_2]\,I_o \quad (38)$$

On the other hand, considering waveforms of i_{Lm1} and i_{Lm2} in Fig. 12, it can be written as follows:

$$I_{Lm1} = (1/2)\Delta i_{Lm1}(D+\alpha_1) = (1/2)(V_{i1}/L_{m1})DT_s(D+\alpha_1) \quad (39)$$

$$I_{Lm2} = (1/2)\left[\frac{\alpha_1+D}{\alpha_1}(1+n_{s1})V_{i1}+V_{i2}\right]\frac{DT_s}{L_{m2}}(D+\alpha_2) \quad (40)$$

To simplify the analysis, the parameters, α_1 and α_2, are assumed to be equal ($\alpha_1 = \alpha_2 = \alpha$), and input voltages are the same values, $V_{i1} = V_{i2} = V_i$. By defining the normalized magnetizing-inductor time constants, τ_{Lm1} and τ_{Lm2}, as $\tau_{Lm1} = f_sL_{m1}/R_o$ and $\tau_{Lm2} = f_sL_{m2}/R_o$, the parameter α can be rewritten as follows:

$$\alpha = \frac{\tau_{Lm1}}{2\tau_{Lm2}}D(1+n_{s1})\left[2+n_{s1}\pm\sqrt{(2+n_{s1})^2+\frac{4}{L_{m1}}\tau_2}\right] \quad (41)$$

Consequently, the voltage conversion ratio (V_o/V_i) for DCM operation can be calculated as follows;

$$\frac{V_o}{V_i}|_{DCM} = \frac{D(1+n_{s2})(1+n_{s1})}{\alpha}\left(\frac{\alpha+D}{\alpha}\right) + \frac{D(1+n_{s2})+\alpha}{\alpha} \quad (42)$$

H. DESIGN CONSIDERATIONS

By considering Fig.13(a) in the top waveform of the inductance current, the average value of the current passing through the inductance $L_{m1}(L_{m1})$ is calculated equal to the trapezoid area under the red waveform of i_{Lm1}. As a result, I_{Lm1} can be calculated as $I_{Lm1-CCM} = I_{\ell 1} + \Delta i_{Lm1}/2$. Therefore, I_{Lm1} has a larger value than the half of the inductance current ripple ($\Delta i_{Lm1}/2$) in the CCM operation mode, i.e., $I_{Lm1} > \Delta i_{Lm1}/2$.

In the DCM operation, by considering the current waveform of bottom figure of Fig. 13(a), the average value of the current passing through the inductance $L_{m1}(L_{m1})$ is calculated equal to the trapezoid area under the red waveform of i_{Lm1}. As a result, I_{Lm1} can be calculated as $I_{Lm1-DCM} = S_\Delta = (\Delta i_{Lm1}/2)(\alpha_1 + D)$. According to the bottom figure of Fig. 13(a), it can be seen that $(\alpha_1 + D)T_s < T_s$ or $(\alpha_1 + D) < 1$ So in the DCM operation, I_{Lm1} has a smaller value than the half of the inductance current ripple ($\Delta i_{Lm1}/2$), i.e., $I_{Lm1} < \Delta i_{Lm1}/2$.

Consequently, the following inequalities has to be verified to achieve CCM operation of the proposed converter.

$$L_{m1} > \frac{(1-D)^2R_oV_{i1}}{2(1+n_{s1})\,(1+n_{s2})\,V_of_s} \quad (43)$$

$$L_{m2} > \frac{[V_{i2}+(1+n_{s1})\,V_{i1}/(1-D)]\,R_oD\,(1-D)}{2\,(1+n_{s2})\,V_of_s} \quad (44)$$

where the average output current I_o is calculated by $I_o = V_o/R_o$. Accordingly, simplifying above inequalities, the boundary normalized magnetizing-inductor time constants, $\tau_{Lm1,B}$ and $\tau_{Lm2,B}$, are calculated as follows:

$$\tau_{Lm1,B} = \frac{(1-D)^3/[2(1+n_{s1})\,(1+n_{s2})]}{(1+n_{s1})(1+n_{s2})D/(1-D)+V_{i2}(1+n_{s2}D)/V_{i1}} \quad (45)$$

$$\tau_{Lm2,B} = \frac{[1+n_{s1}+V_{i2}(1-D)/V_{i1}]D\,(1-D)/[2\,(1+n_{s2})]}{[(1+n_{s1})(1+n_{s2})D/(1-D)+(1+n_{s2}D)\,V_{i2}/V_{i1}]} \quad (46)$$

Fig. 13 (b) shows the boundary region between DCM and CCM operating modes of the proposed converter over the

parameters, $\tau_{Lm1,B}$, $\tau_{Lm2,B}$ and D. In left figure of Fig. 13(b), if τ_{Lm1} is larger than $\tau_{Lm1,B}$, the proposed converter is operated under CCM. In right figure of Fig. 13(b), if τ_{Lm2} is larger than $\tau_{Lm2,B}$, the proposed converter is operated under CCM.

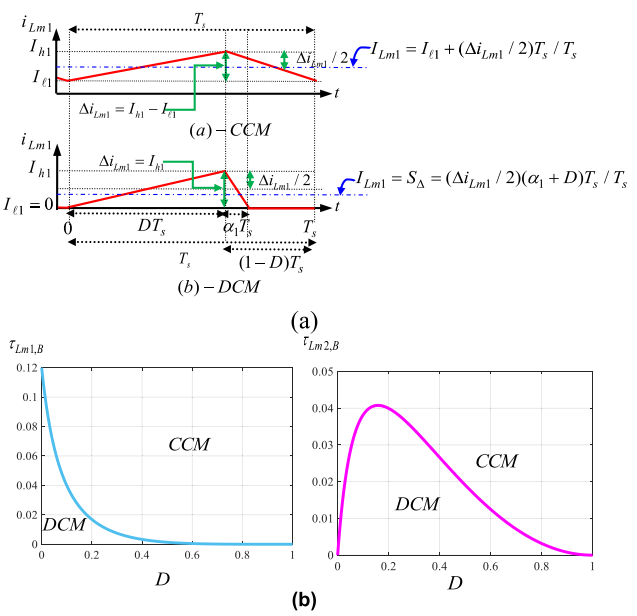

FIGURE 13. (a) Comparing the current waveform of i_{Lm1} for CCM and DCM operation; (b) The boundary region between DCM and CCM operation modes of the proposed converter under $n_{s1} = n_{s2} = 1.5$ and $V_{i2}/V_{i1} = 12V/18V$ with respect to parameters, D, $\tau_{Lm1,B}$, $\tau_{Lm2,B}$.

To obtain a more accurate design for the capacitors, the peak-to-peak value of the output voltage ripple is equal to the sum of the voltage ripple across each output capacitor (ΔV_{Co}), and voltage ripple caused by the ESR of the output capacitor ($\Delta V_{Co-ESR} = r_{Co}\Delta I_{Co}$). An important condition in the design of the output capacitor is the hold-up time requirement for the step-load response [9]. Therefore, the minimum values of capacitors C_{i1}, C_{i2}, C_1, C_2 are calculated as specified in Table 1, which are calculated for their maximum voltage ripples, $\Delta V_C = (1\%)\ V_C - r_C \Delta I_C$ and are used to verify the inequalities in Table 1.

III. OPERATING PRINCIPLES OF THE PROPOSED MULTI-INPUT, SINGLE-OUTPUT CONVERTER

The proposed multi-input converter is achieved by increasing input modules in Fig. 2(b). In the multi-input converter, as it can be seen from Fig. 2(c), there are N ($N = 1, 2, 3, 4, \ldots$) number of input voltage sources ($V_{i1}, V_{i2}, \ldots, V_{i(N-1)}, V_{iN}$). This converter uses N number of diodes ($D_1, D_2, \ldots, D_{N-1}, D_N$), N number of capacitors ($C_1, C_2, \ldots, C_{N-1}, C_N$), N number of switches ($S_1, S_2, \ldots, S_{N-1}, S_N$), and N number of coupled inductors with turns ratios of ($n_{s1}, n_{s2}, \ldots, n_{s(N-1)}, n_{sN}$).

A. VOLTAGE GAIN AND VOLTAGES OF CAPACITORS

By considering the voltage balance law for the inductors $L_{m1}, L_{m2}, \ldots L_{mN}$ and $N = 3$, the average voltages across the inductors during a switching period should be obtained using (5), (6), and the following equation:

$$\tilde{v}_{Lm3} = D\,[V_{i3} + V_{C2} + n_{s2}V_{i2} + (1+n_{s2})\,(V_{C1} + n_{s1}V_{i1})] + (1-D)[(V_{i3} - V_{C3})/(1+n_{s3})] = 0 \quad (47)$$

The capacitor voltages V_{C1}, V_{C2}, V_{C3} are calculated by

$$V_{C3} = D(1+n_{s1})(1+n_{s2})(1+n_{s3})\,V_{i1}/(1-D)^3 + D\,(1+n_{s2})\,(1+n_{s3})\,V_{i2}/(1-D)^2 + (1+n_{s3}D)\,V_{i3}/(1-D) \quad (48)$$

As a result, the voltage of the capacitor C_4 by considering $N = 4$ can be determined as follows:

$$V_{C4} = [D(1+n_{s1})(1+n_{s2})(1+n_{s3})(1+n_{s4})/(1-D)^4]\,V_{i1} + [D(1+n_{s2})(1+n_{s3})(1+n_{s4})/(1-D)^3]\,V_{i2} + [D(1+n_{s3})(1+n_{s4})/(1-D)^2]\,V_{i3} + [(1+n_{s4}D)/(1-D)]\,V_{i4} \quad (49)$$

In a similar way, the voltage across the kth ($k = 1, 2, 3, 4, \ldots, N$) capacitor for the proposed converter with N input modules is calculated by

$$V_{Ck} = D\sum_{j=1}^{k-1}\frac{(1+n_{sj})(1+n_{sj+1})\ldots(1+n_{sN})}{(1-D)^{k-j+1}}V_{ij} + \frac{1+n_{sk}D}{1-D}V_{ik} \quad (50)$$

As a result, by increasing input stages of the proposed converter, the voltage gain can be increased.

B. VOLTAGE STRESS ON DIODES AND SWITCHES

During Mode 1 ($0 \le t < DT_s$), the diodes $D_1, D_2, \ldots, D_{N-1}, D_N$ are off, and the voltage stress on the k^{th} diode ($k = 1, 2, 3, 4, \ldots, N$) is calculated by

$$V_{Dk} = \sum_{j=1}^{k-1}\frac{(1+n_{sj})(1+n_{sj+1})\ldots(1+n_{sk})}{(1-D)^{k-j+1}}V_{ij} + \frac{1+n_{sk}}{1-D}V_{ik} \quad (51)$$

TABLE 1. The minimum values of capacitors.

C_{2_min}	$C_{2\_min}\big\vert_{ESR} = D/\left\{\left[(1\%) - \frac{r_C}{R_o(1-D)}\right]R_o f_s\right\}$, $C_{2\_min}\big\vert_{THT} = V_o/[0.01\,V_o\,R_o(0.1\,f_s)]$, $[C_{2\_min} = \max(C_{2\_min}\big\vert_{ESR}, C_{2\_min}\big\vert_{THT})]$
C_{1_min}	$C_{1\_min} = D/\left\{\left[\frac{r_C}{R_o}\frac{1}{1-D} - \frac{(1\%)\,V_C\,(1-D)}{(1+n_{s2})\,V_o}\right]R_o\,f_s\right\}$, $V_{C1} = [(1+n_{s1}D)/(1-D)]V_{i1}$
C_{i1_min}	$C_{i1\_min} = D/\left\{\left[\frac{r_C}{R_o}\frac{1}{1-D} - (1\%)\frac{V_{i2}}{n_{s2}\,V_o}\right]R_o\,f_s\right\}$
C_{i2_min}	$C_{i2\_min} = D/\left\{\left[\frac{r_C}{R_o}\frac{1}{1-D} - (1\%)\frac{V_{i1}\,(1-D)}{n_{s1}\,(1+n_{s2})\,V_o}\right]R_o\,f_s\right\}$

During Mode 2 ($DT_s \leq t < T_s$), the switches $S_1, S_2, \ldots, S_{N-1}, S_N$ are off, and the voltage stress on the k^{th} switch ($k = 1, 2, 3, 4, \ldots, N$) can be calculated by

$$V_{Sk} = D\sum_{j=1}^{k-1} \frac{(1+n_{sj})(1+n_{sj+1})\ldots(1+n_{sk-1})}{(1-D)^{k-j+1}} V_{ij} + \frac{1}{1-D} V_{ik} \quad (52)$$

C. AVERAGE CURRENTS OF SWITCHES

During Mode 1 ($0 \leq t < DT_s$), the switches S_1 and S_2 are on, so by applying KCL in the N^{th} stage, the current stress on the switch S_N is calculated as $i_{SN} = i_{TN} + i_{LmN} + i_{TtN} = i_{LmN}$.

By applying KCL in the $(N-1)^{th}$ stage, the current stress on the switch S_{N-1} during Mode 1 is calculated by

$$i_{SN-1} = (n_{s(N-1)} + 1) i_{LmN} + i_{Lm(N-1)} \quad (53)$$

$$i_{S(N-2)} = (n_{s(N-2)} + 1) i_{LmN-1} + i_{Lm(N-2)} \quad (54)$$

As a result, in the k^{th} ($k = 1, 2, 3, 4, \ldots, N$) stage, the current stress on the switch S_k is calculated by

$$i_{Sk} = (n_{sk} + 1) i_{Lm(k+1)} + i_{Lmk} \quad (55)$$

By applying KCL in the first stage, the current stress on the switch S_1 during Mode 1 is calculated as (14).

D. AVERAGE CURRENTS OF DIODES

During Mode 2 ($DT_s \leq t < T_s$), the diodes, D_1, $D_2, \ldots, D_{N-1}$, and D_N, are turning on, so the current stress on the diodes, D_1 and D_2, are obtained as (15)-(16). As a result, the current stress on the diode D_N can be derived as follows:

$$\begin{aligned} i_{DN} &= i_{iN} + i_{TtN} \\ &= i_{iN} - (n_{sN} i_{DN} + i_{TN}) = i_{LmN}/(1+n_{sN}) \end{aligned} \quad (56)$$

As a result, the current stress of the used diodes in the N-input converter during ($DT_s \leq t < T_s$) can be summarized by

$$i_{Dk} = i_{Lmk}/(1+n_{sk}) \quad \text{where } k = 1, 2, 3, \ldots, N \quad (57)$$

On the other hand, the average currents through the diodes and switches during a switching period are $I_{DN} = I_o$, $I_{Sk} = I_{D(k-1)} = I_{ik} = I_{Lmk}$ ($k = 1, 2, \ldots, N-1$) and $I_{SN} = I_{D(N-1)} = I_{iN} - I_o$.

E. AVERAGE CURRENTS OF CAPACITORS AND INDUCTORS

In steady state, the current balance law for the capacitors leads to a zero average current of capacitors $C_1, C_2, \ldots, C_{N-1}, C_N$ during a switching period. During Mode 1, the current of the capacitor C_N is equal to $-i_o$; and during Mode 2, it is obtained as $i_{CN} = i_{DN} - i_o$ or $i_{CN} = [i_{LmN}/(1+n_{sN})] - i_o$. Therefore, the average current of the capacitor C_N is determined as follows:

$$\tilde{i}_{CN} = D(-i_o) + (1-D)[i_{LmN}/(1+n_{sN}) - i_o] = 0 \quad (58)$$

The average current of capacitors $C_1, C_2, \ldots, C_{N-1}$ ($k = 1, 2, 3, \ldots, N-1$) would be obtained as follows:

$$\tilde{i}_{Ck} = D(-i_{Lm(k+1)}) + (1-D)[i_{Lmk}/(1+n_{sk})] = 0 \quad (59)$$

The average values of the inductor currents are calculated by

$$I_{LmN} = (1+n_{sN}) I_o/(1-D) \quad (60)$$

$$I_{Lmk} = \frac{D^{N-k}(1+n_{sk})\ldots.(1+n_{sN})}{(1-D)^{N-k+1}} I_o \;\&\; k = 1, 3, 4, \ldots, N-1 \quad (61)$$

In Fig. 2(b), the equation for the average currents flowing through the $1, 3, 4, \ldots, (N-1)^{th}$ transformers in steady state are written as:

$$\begin{aligned} I_{T1} &= I_{Ci1} - n_{s1} I_{C1} = 0, \ldots, I_{T(N-1)} \\ &= I_{Ci(N-1)} - n_{s(N-1)} I_{C(N-1)} = 0. \end{aligned}$$

The average currents of capacitors are equal to zero in steady state. As a result, the average input currents of first, second, …, $(N-1)^{th}$ stage are calculated by

$$I_{ik} = I_{Lmk} \;\&\; k = 1, 3, 4, \ldots, N-1 \quad (62)$$

Considering Fig. 2(b), the average input current of the N^{th} stage is calculated by

$$I_{iN} = I_{LmN} - n_{sN} I_o = (1 + n_{sN} D) I_o/(1-D) \quad (63)$$

F. INPUT CURRENTS' RIPPLE CANCELLING CONDITION

Based on Figs. 2(a) and 2(b), the inductances, L_{p1}, L_{s1}, L_{t1}, M_{12}, M_{13} and M_{23}, used in Fig. 2(a) can be replaced dependent on the used parameters in Fig. 2(b):

$$\begin{aligned} &L_{p1} = L_{m1} + L_{k1}, \quad L_{t1} = N_{t1}^2 L_{m1}, \; L_{s1} = N_{s1}^2 L_{m1}, \\ &M_{13} = M_{31} = N_{t1} L_{m1}, \quad M_{12} = M_{21} = N_{s1} L_{m1}, \\ &M_{23} = M_{32} = N_{t1} N_{s1} L_{m1}. \end{aligned}$$

In the same way, the second coupled inductor in Fig. 2(a) is modelled as shown in Fig. 2(b). The voltages across the first, second and third windings of the first coupled inductor in Fig. 1(a) can be written as follows:

$$v_{Lp1} = L_{p1}(di_{Lp1}/dt) + M_{21}(di_{Ls1}/dt) + M_{31}(di_{Lt1}/dt) \quad (64)$$

$$v_{Ls1} = M_{12}(di_{Lp1}/dt) + L_{s1}(di_{Ls1}/dt) + M_{32}(di_{Lt1}/dt) \quad (65)$$

$$v_{Lt1} = M_{13}(di_{Lp1}/dt) + M_{23}(di_{Ls1}/dt) + L_{t1}(di_{Lt1}/dt) \quad (66)$$

The equivalent circuits of the proposed converter in Modes 1 and 2 using the coupled inductor model are shown in Fig. 14.

1) INPUT CURRENT RIPPLE CANCELATION IN THE FIRST STAGE

In Mode 1, the switches, S_1 and S_2, conduct and the diodes, D_1 and D_2, are turned off. According to Fig. 14(a), applying the KVL law in voltage loops and the KCL law in current nodes will result in the following equations:

$$v_{Lp1} = V_{i1} \quad (67)$$

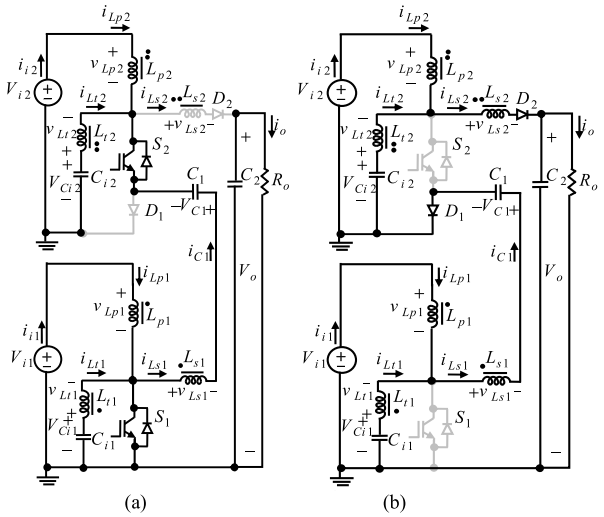

FIGURE 14. Equivalent circuits of the proposed converter in Modes 1 and 2 using the coupled inductor model: (a) Mode 1; (b) Mode 2.

$$v_{Lt1} = V_{Ci1} = V_{i1} \tag{68}$$
$$v_{Ls1} - v_{Lp2} = -V_{i2} - V_{C1} \tag{69}$$
$$v_{Lp2} - v_{Lt2} + V_{Ci2} - V_{i2} = 0 \quad OR\ v_{Lp2} = v_{Lt2} \tag{70}$$
$$i_{Lp2} + i_{Lt2} = -i_{Ls1} \tag{71}$$
$$i_{Ls2} = 0 \tag{72}$$

From (4), we have

$$di_{Lp2}/dt + di_{Lt2}/dt = -di_{Ls1}/dt \tag{73}$$

Consequently, considering (64)-(66) and (67)-(73), a linear equation system can be obtained as (74), shown at the bottom of the page.

Therefore, after solving the linear equation system in [74], the value of the parameter di_{Lp1}/dt can be determined by

$$di_{Lp1}/dt = \frac{\begin{aligned}&[-\beta_1(L_{t1} - M_{pt1})\,V_{i1} - \beta_2\beta_3(V_{i2} + V_{C1})\\&- \beta_3 M_{st1}(M_{st1} - M_{ps1})V_{i1}]\end{aligned}}{\beta_2\beta_3 M_{ps1} + \beta_1\beta_5 - \beta_4\beta_3 M_{st1}} \tag{75}$$

where the five parameters, β_1, β_2, β_3, β_4 and β_5, are defined as follows:

$$\beta_1 = (L_{p2} + L_{s1})(L_{t2} - M_{pt2}) + (L_{s1} + M_{pt2})(L_{p2} - M_{pt2}) \tag{76}$$

$$\beta_2 = M_{st1}M_{pt1} - L_{t1}M_{ps1} \tag{77}$$
$$\beta_3 = L_{p2} + L_{t2} - 2M_{pt2} \tag{78}$$
$$\beta_4 = L_{p1}M_{st1} - M_{ps1}M_{pt1} \tag{79}$$
$$\beta_5 = L_{p1}L_{t1} - M_{pt1} \tag{80}$$

To achieve zero input current ripples at the first stage in Mode 1, the equation $di_{in1}/dt = di_{Lp1}/dt = 0$ should be verified. Considering the parameter β_2 and by substituting parameters of the transformer model in (77), it is found that the parameter β_2 is equal to zero.

$$\begin{aligned}\beta_2 &= M_{st1}M_{pt1} - L_{t1}M_{ps1}\\ &= (N_{t1}N_{s1}L_{m1})\,(N_{t1}L_{m1}) - \left(N_{t1}{}^2 L_{m1}\right)(N_{s1}L_{m1}) = 0\end{aligned} \tag{81}$$

Equ. (75) can then be simplified as follows:

$$di_{Lp1}/dt = \frac{\beta_1\left(L_{t1} - M_{pt1}\right) + \beta_3 M_{st1}\left(M_{st1} - M_{ps1}\right)}{\beta_4\beta_3 M_{st1} - \beta_1\beta_5} V_{i1} \tag{82}$$

As a result, the numerator of the mentioned fraction in (11) should be equal to zero. Then, the parameters $(L_{t1} - M_{pt1})$ and $(M_{st1} - M_{ps1})$ in (82) should be equal to zero:

$$\begin{aligned}L_{t1} - M_{pt1} &= N_{t1}^2 L_{m1} - N_{t1}L_{m1}\\ &= N_{t1}L_{m1}\,(1 - N_{t1}) = 0\end{aligned} \tag{83}$$
$$\begin{aligned}M_{st1} - M_{ps1} &= N_{t1}N_{s1}L_{m1} - N_{s1}L_{m1}\\ &= N_{s1}L_{m1}\,(N_{t1} - 1) = 0\end{aligned} \tag{84}$$

Consequently, the third winding turn ratio should be $N_{t1} = 1$. Since the denominator in (82) should not be zero, as a result,

$$\beta_3 \neq 0 \& \beta_4 \neq 0 \tag{85}$$
$$\begin{aligned}\beta_3 &= L_{p2} + L_{t2} - 2M_{pt2} = L_{m2} + L_{k2} + N_{t2}^2 L_{m2}\\ &\quad - 2N_{t2}L_{m2} = (1 + N_{t2}^2 - 2N_{t2})L_{m2} + L_{k2}\\ &= (N_{t2} - 1)^2 L_{m2} + L_{k2} = L_{k2} \neq 0\end{aligned} \tag{86}$$
$$\begin{aligned}\beta_4 &= L_{p1}M_{st1} - M_{ps1}M_{pt1}\\ &= (L_{m1} + L_{k1})(N_{t1}N_{s1}L_{m1}) - (N_{s1}L_{m1})(N_{t1}L_{m1})\\ &= (N_{t1}N_{s1}L_{m1})L_{k1} \neq 0\end{aligned} \tag{87}$$

$$\begin{cases} 1) -\left\{L_{s1}\left[1 + \dfrac{L_{p2} - M_{pt2}}{L_{t2} - M_{pt2}}\right] + L_{p2} + M_{pt2}\dfrac{L_{p2} - M_{pt2}}{L_{t2} - M_{pt2}}\right\}\dfrac{di_{Lp2}}{dt} \\ \qquad\qquad M_{ps1}\dfrac{di_{Lp1}}{dt} + M_{st1}\dfrac{di_{Lt1}}{dt} = -V_{i2} - V_{C1} \\ 2)\, L_{p1}\dfrac{di_{Lp1}}{dt} - M_{ps1}\left[1 + \dfrac{L_{p2} - M_{pt2}}{L_{t2} - M_{pt2}}\right]\dfrac{di_{Lp2}}{dt} + M_{pt1}\dfrac{di_{Lt1}}{dt} = V_{i1} \\ 3)\, M_{pt1}\dfrac{di_{Lp1}}{dt} - M_{st1}\left[1 + \dfrac{L_{p2} - M_{pt2}}{L_{t2} - M_{pt2}}\right]\dfrac{di_{Lp2}}{dt} + L_{t1}\dfrac{di_{Lt1}}{dt} = V_{i1} \end{cases} \tag{74}$$

The required conditions to achieve zero input current ripples in the first stage in Mode 1 are derived as follows:

$$N_{t1} = 1$$
$$L_{k1} \neq 0 \& L_{k2} \neq 0 \tag{88}$$

Therefore, the current ripples at the first stage is eliminated during Mode 1 by having the conditions of $N_{t1} = 1$ and $L_{k1} \neq 0$, $L_{k2} \neq 0$, which are independent to the duty cycle of switches, and only depend on the values of third winding turn ratio (N_t) of the coupled inductor and leakage inductance (L_k).

In Mode 2, the switches, S_1 and S_2, are off and the diodes, D_1 and D_2, are turned on. In this mode, by applying the KVL and KCL in Fig. 14 (b), we have

$$v_{Lp1} = v_{Lt1} \tag{89}$$
$$v_{Lp1} + v_{Ls1} = V_{i1} - V_{C1} \tag{90}$$
$$i_{Lt1} + i_{Lp1} = i_{Ls1} \tag{91}$$

Considering (1)-(3) and (64)-(66), we have, (92), as shown at the bottom of the page. Equ. (92) can be rewritten by

$$di_{Lp1}/dt = (V_{i1} - V_{C1})\alpha_1/(\alpha_1\alpha_2 + \alpha_3\alpha_4) \tag{93}$$

The required conditions for cancelling input current ripples at the first stage in Mode 2 can be obtained by solving the equation $di_{in1}/dt = di_{Lp1}/dt = 0$. The numerator of the mentioned fraction in (92), should be equal to zero. Then, the parameter α_1 in (93) should be equal to zero, so we have

$$\alpha_1 = L_{t1} + M_{st1} - M_{sp1} - M_{pt1} = 0 \tag{94}$$

On the other hand, the denominator of the written fraction in (93), should not be zero:

$$\alpha_3 = LL_{p1} + L_{t1} - 2M_{pt1} \neq 0 \tag{95}$$

Considering $\alpha_4 = M_{sp1} + M_{pt1} + M_{st1} + L_{s1}$, the parameter α_4 has a positive non-zero value. Therefore, only the parameter α_3 in the denominator of the written fraction in (93) should not be zero. Note: the inductances, L_{p1}, L_{s1}, L_{t1}, M_{12}, M_{13} and M_{23}, in Fig. 2(a) can be replaced depending on the parameters in Fig. 2(b).

Based on (94) and (95), the required conditions for cancelling input current ripples in Mode 2 are determined as follows:

$$\begin{aligned}\alpha_1 &= L_{t1} + M_{st1} - M_{sp1} - M_{pt1} \\ &= N_{t1}^2 L_{m1} + N_{t1}N_{s1}L_{m1} - N_{s1}L_{m1} - N_{t1}L_{m1} \text{ or } N_{t1} = 1 \\ &= (N_{t1}^2 + N_{t1}N_{s1} - N_{s1} - N_{t1})L_{m1} = 0 \end{aligned} \tag{96}$$
$$\begin{aligned}\alpha_3 &= L_{p1} + L_{t1} - 2M_{pt1} \neq 0 \\ &= (L_{m1} + L_{k1}) + N_{t1}^2 L_{m1} - 2N_{t1}^2 L_{m1} = L_{k1} \neq 0 \end{aligned} \tag{97}$$

Accordingly, by verifying (88) and (96)-(97), current ripples at the first stage during one switching period for the whole range of duty cycles of $0 < D < 1$ (a switching period includes both Modes 1 and 2) are eliminated under the conditions of $N_{t1} = 1$, $L_{k1} \neq 1$ and $L_{k2} \neq 0$, which are independent on the duty cycle of switches, and only dependent on the third winding of coupled inductor and leakage inductances values. As a comparison, in most conventional two phase or three phase converters, input current ripples can only be cancelled for a few duty cycle values. For example, two phase converters eliminate input current ripples only at the duty cycle of D = 0.5 (Referring to Table 2 in Section IV).

2) INPUT CURRENT RIPPLE CANCELATION IN THE SECOND STAGE

During Mode 1, the switches, S_1 and S_2, are conducting and the diodes, D_1 and D_2 are off. According to Fig. 14 (a), $i_{Ts2} = i_{Ls2} = 0$. As a result, based on Fig. 14 (a), the voltages across the first and third windings of the second coupled inductor are equal to $V_{i2} + V_{C1} + n_{s1}V_{i1}$. Accordingly, it can be derived further as follows:

$$di_{Lp2}/dt = \frac{(V_{i2} + V_{C1} + n_{s1}V_{i1})(L_{t2} - M_{13})}{(L_{t2}L_{p2} - M_{13}^2)} \tag{98}$$

Therefore, to achieve zero input current ripples at the second stage in Mode 1, the following equations should be verified:

$$L_{t2} = M_{13} \quad or\ N_{t2} = 1 \text{ and } M_{13}^2 \neq L_{p2}L_{t2} \ or\ L_{k2} \neq 0 \tag{99}$$

During Mode 2, the switches S_1 and S_2 are off and the diodes D_1 and D_2 are turned on. Based on Fig. 14 (b), the following equations can be obtained:

$$v_{Lt2} + v_{Ls2} = v_{Ls2} + v_{Lp2} = V_{i2} - V_o \tag{100}$$
$$v_{Lp2} = v_{Lt2} \quad or\ L_{p2}di_{Lp2}/dt = L_{t2}di_{Lt2}/dt \tag{101}$$
$$i_{Lp2} + i_{Lt2} = i_{Ls2} \tag{102}$$
$$di_{Lp2}/dt = (V_{i2} - V_o)D/(BD + AC) \tag{103}$$

$$\begin{aligned} di_{Lp1}/dt &= \frac{V_{i1} - V_{C1}}{\left[\frac{(L_{p1} + M_{sp1} - M_{pt1}) + \frac{(M_{sp1}+M_{pt1}+M_{st1}+L_{s1})(L_{p1}+L_{t1}-2M_{pt1})}{(L_{t1}+M_{st1}-M_{sp1}-M_{pt1})}}{}\right]} \\ &= \left[\frac{(L_{t1} + M_{st1} - M_{sp1} - M_{pt1})(V_{i1} - V_{C1})}{\left[\begin{array}{l}(L_{t1} + M_{st1} - M_{sp1} - M_{pt1})(L_{p1} + M_{sp1} - M_{pt1}) \\ +(L_{p1} + L_{t1} - 2M_{pt1})(M_{sp1} + M_{pt1} + M_{st1} + L_{s1})\end{array}\right]}\right] \end{aligned} \tag{92}$$

Therefore, the required conditions to achieve zero input current ripples at the second stage during Mode 2 are given as follows:

$$(D = L_{t2} + M_{23} - M_{12} - M_{13} = 0) \quad or \ (N_{t2} = 1) \tag{104}$$

$$(C = L_{p2} + M_{12} - M_{13} - M_{23} \neq 0) \quad or \ (L_{k2} \neq 0) \tag{105}$$

The current ripples in the second stage is eliminated during a switching period for whole range of duty cycles.

IV. ANALYSIS OF THE PROPOSED CONVERTER FOR TWO DUTY CYCLE CONDITIONS ($D_1 > D_2$ AND $D_2 > D_1$)

In this section, the theoretical analysis of the proposed converter is conducted under two conditions of duty cycles, D_1 and D_2: $D_1 > D_2$ and $D_1 < D_2$.

A. FIRST CONDITION OF DUTY CYCLES: $D_1 > D_2$

Under this condition, the proposed converter has three operating modes during a switching period as shown in Fig. 15 (a).

Mode 1 [$t_0 \leq t < t_1$]: In Fig. 15(a), this mode starts with turning on the switches, S_1 and S_2, while the two diodes, D_1 and D_2, are OFF. Its equivalent circuit of this mode is the same as that shown in Fig. 4(a). The inductor voltages, v_{Lm1}

And v_{Lm2}, are $v_{Lm1} = V_{i1}$ and $v_{Lm2} = V_{i2} + V_{C1} + n_{s1}v_{Lm1} = V_{i2} + V_{C1} + n_{s1}V_{i1}$, respectively.

As a result, this mode is the same as the first mode with the duty cycles, $D_1 = D_2 = D$.

Mode 2 [$t_1 \leq t < t_2$]: In Fig. 15(a), at the beginning moment of this mode, the switch, S_2, is turned off, and the diode, D_2, is turned on; while the switch S_1 is conducting and the diode D_1 is off. Its equivalent circuit of this mode is shown in Fig. 15(b). The inductor voltages, v_{Lm1} and v_{Lm2}, are $v_{Lm1} = V_{i1}$ and $v_{Lm2} = (V_{i2} - V_{C2})/(1 + n_{s2})$, respectively.

Mode 3 [$t_2 < t < t_3$]: In Fig. 15(a), at the beginning moment of this mode, the switch, S_1 is turned off, and the diode, D_1 is turned on; while the switch, S_2, is off, and the diode, D_2, is conducting. Its equivalent circuit of this mode is the same as the equivalent circuit of the proposed converter for $D_1 = D_2 = D$ in the second mode as shown in Fig. 4(b).

1) VOLTAGE GAIN FOR FIRST CONDITION OF DUTY CYCLES, $D_1 > D_2$

By considering the voltage balance law for the inductors L_{m2} and L_{m1}, the average voltages across the inductors during a switching period should be equal to zero as follows:

$$\tilde{v}_{Lm1} = D_1 V_{i1} + (1 - D_1)\left[(V_{i1} - V_{C1}) / (1 + n_{s1})\right] = 0 \tag{106}$$

$$\tilde{v}_{Lm2} = D_2(V_{i2} + V_{C1} + n_{s1}V_{i1}) + \frac{(1 - D_2)(V_{i2} - V_{C2})}{1 + n_{s2}} = 0 \tag{107}$$

By simplifying (5) and (6), we have

$$V_{C1} = \left[(1 + n_{s1}D_1) / (1 - D_1)\right] V_{i1} \tag{108}$$

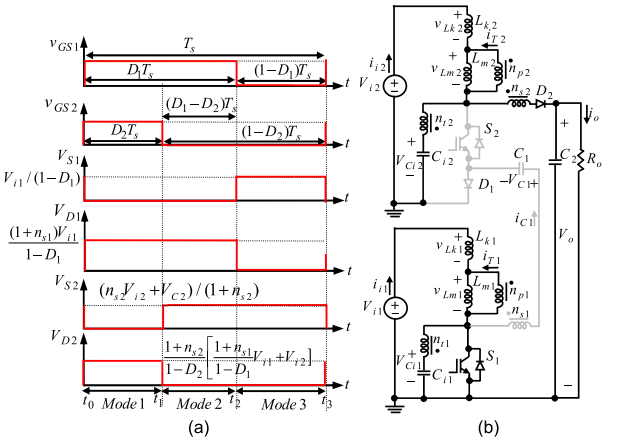

FIGURE 15. (a) Switching pattern of switches for $D_1 > D_2$ and theoretical waveforms of voltage stresses on switches and diodes; (b) equivalent circuit for *Mode 2*.

$$V_o = V_{C2} = \frac{(1 + n_{s1})(1 + n_{s2})D_2}{(1 - D_1)(1 - D_2)}V_{i1} + \frac{1 + n_{s2}D_2}{1 - D_2}V_{i2} \tag{109}$$

B. SECOND CONDITION OF DUTY CYCLES: $D_2 > D_1$

Under this condition, the proposed converter has three operating modes during a switching period as shown in Fig. 16(a).

Mode 1 [$t_0 \leq t < t_1$]: In Fig. 16(a), this mode starts with turning on the switches, S_1 and S_2, while the diodes, D_1 and D_2, are off. Its equivalent circuit of this mode is the same as that shown in Fig. 4(a). The inductor voltages, v_{Lm1} and v_{Lm2}, are determined as $v_{Lm1} = V_{i1}$ and $v_{Lm2} = V_{i2} + V_{C1} + n_{s1}v_{Lm1} = V_{i2} + V_{C1} + n_{s1}V_{i1}$, respectively.

Mode 2 [$t_1 \leq t < t_2$]: In Fig. 16(a), at the beginning moment of this mode, the switch, S_1, is turned off, and the diode, D_1, is turned on; while the switch S_2 is conducting and the diode D_2 is OFF. Its equivalent circuit of this mode is shown in Fig. 16(b). The inductor voltages, v_{Lm1} and v_{Lm2}, are $v_{Lm1} = (V_{i1} - V_{C1})/(1 + n_{s1})$ and $v_{Lm2} = V_{i2}$, respectively.

Mode 3 [$t_2 < t < t_3$]: In Fig. 16(a), at the beginning moment of this mode, the switch, S_2, is turned off, and the diode, D_2, is turned on; while the switch, S_1, is off, and the diode, D_1, is conducting. Its equivalent circuit of this mode is the same as that of the proposed converter for the condition $D_1 = D_2 = D$ as shown in Fig. 4(b). The inductor voltages, v_{Lm1} and v_{Lm2}, are obtained as $v_{Lm1} = (V_{i1} - V_{C1})/(1 + n_{s1})$ and $v_{Lm2} = (V_{i2} - V_{C2})/(1 + n_{s2})$, respectively.

C. VOLTAGE GAIN FOR SECOND CONDITION OF DUTY CYCLES, $D_2 > D_1$

By considering the voltage balance law for the inductors, L_{m2} and L_{m1}, the average voltages across the inductors during a switching period should be equal to zero as follows:

$$\tilde{v_{Lm1}} = DV_{i1} + (1 - D)\left[(V_{i1} - V_{C1}) / (1 + n_{s1})\right] = 0 \tag{110}$$

$$\tilde{v}_{Lm2} = D_1\left(V_{i2} + V_{C1} + n_{s1}V_{Ci1}\right) + (D_2 - D_1)V_{i2} + (1 - D_2)(V_{i2} - V_{C2})/(1 + n_{s2}) = 0 \tag{111}$$

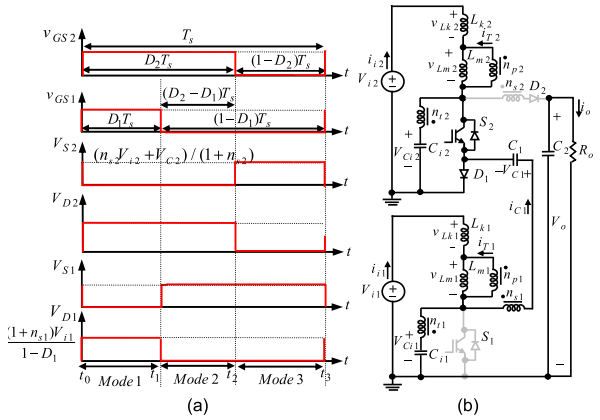

FIGURE 16. **(a) Switching pattern of switches for $D_2 > D_1$ and theoretical waveforms of voltage stresses on switches and diodes; (b) equivalent circuit for *Mode 2*.**

By simplifying (5) and (6), we have

$$| V_{C1} = [(1 + n_{s1}D) / (1 - D)] V_{i1} \tag{112}$$

$$V_0 = V_{C2} = \frac{(1 + n_{s1})(1 + n_{s2})D}{(1 - D)^2} V_{i1} + \frac{1 + n_{s2}D}{1 - D} V_{i2} \tag{113}$$

Considering the output voltage equations, (109) and (113), for both duty cycle conditions, $D_1 > D_2$ and $D_1 < D_2$, respectively, if the duty cycles D_1 and D_2 are replaced by D ($D_1 = D_2 = D$) in (109) and (113), the two equations become (8) for the output voltage V_o.

D. SMALL SIGNAL ANALYSIS AND CONTROL SYSTEM FOR THE PROPOSED CONVERTER

According to the equivalent circuits of the proposed converter in Figs. 4(a), 4(b), 15(b) and 16(b), it is assumed that the inductor currents, i_{Lk1}, i_{Lm1}, i_{Lk2} and i_{Lm2}, and the capacitor voltages, v_{Ci1}, v_{Ci2}, v_{C1} and v_{C2}, are state variables. The input voltage sources, v_{i1} and v_{i2}, are defined by the source vector u_{in}. The output voltage is v_{C2}, which should be regulated.

Accordingly, the state equations during a switching period are written as the following equations for inductors and capacitors:

$$sX = AX + B_1\tilde{d}_1 + B_2\tilde{d}_2 + B_{i1}\tilde{v}_{i1} + B_{i2}\tilde{v}_{i2} \tag{114}$$

where the state matrix A and matrices B_1, B_2, B_{i1} and B_{i2} for both conditions of $D_1 > D_2$ and $D_2 > D_1$ are obtained as explained below

1) FIRST CONDITION OF DUTY CYCLES, $D_1 > D_2$

See (115) and (116), as shown at the bottom of the next page.

2) SECOND CONDITION OF DUTY CYCLES, $D_2 > D_1$

See (117) and (118), as shown at the bottom of page 19.

The small signal equation of the output voltage can be written by

$$\tilde{v}_{C2} = CX = CB_1(sI - A)^{-1}\tilde{d}_1 + CB_2(sI - A)^{-1}\tilde{d}_2 + CB_{i1}(sI - A)^{-1}\tilde{v}_{i1} + CB_{i2}(sI - A)^{-1}\tilde{v}_{i2} \tag{119}$$

where

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{120}$$

As a result, the transfer functions of the output voltage $v_{C2} = v_o$ is obtained as follows:

$$G_1(s) = \left.\frac{\tilde{v}_{C2}}{\tilde{d}_1}\right|_{\tilde{v}_{i1}=\tilde{v}_{i2}=\tilde{d}_2=0} = \frac{G_{C2d1}(s)}{G_p(s)} = CB_1(sI - A)^{-1} \tag{121}$$

$$G_2(s) = \left.\frac{\tilde{v}_{C2}}{\tilde{d}_2}\right|_{\tilde{v}_{i1}=\tilde{v}_{i2}=\tilde{d}_1=0} = \frac{G_{C2d2}(s)}{G_p(s)} = CB_2(sI - A)^{-1} \tag{122}$$

By adjusting the PI parameters K_{p1}, K_{p2} and K_{i1} and K_{i2} of the voltage loop controllers, the closed-loop system of the proposed converter as shown in Fig. 17 can achieve a better stability performance.

$$G_{c1} = K_{p1} + \frac{K_{i1}}{s} = 0.00001 + \frac{0.01}{s} \tag{123}$$

$$G_{c2} = K_{p2} + \frac{K_{i2}}{s} = 0 + \frac{0.0041}{s} \tag{124}$$

To generate the drive signals for S_1 and S_2 in Fig. 17, the PWM technique is used, and D_1 and D_2 are compared with the sawtooth wave V_t. When D_1 is higher than V_t, S_1 is in on-state; when D_2 is larger than V_t, S_2 is in on-state.

In the first stage, the transfer function of the output voltage over the duty cycle (G_1), the open-loop transfer function ($T_{O1} = G_{c1}{}^*G_1$), the closed-loop transfer function (T_1 = feedback($G_{c1}{}^*G_1$)) considering the selected parameters in Table 4 for the experimental implemented prototype of the proposed converter are calculated as given in APENDIX. In the second stage, the transfer function of the output voltage over the duty cycle (G_2), the open-loop transfer function of ($T_{O2} = G_{c2}{}^*G_2$) and the closed-loop transfer function (T_2 = feedback($G_{c2}{}^*G_2$)) considering the parameters in Table 4 are calculated as APENDIX as well.

As a result, the bode diagrams of the open-loop transfer functions with the PI voltage controller based on the control of each of the two duty cycles D_1 and D_2 are obtained as shown in Fig. 18(a) and 18(b), respectively. From Fig. 18, it can be seen that the amplitude margin ($GM = 0 - G_{f(\varphi=180)}\,dB$) and the phase margin ($PM = \phi_{f(G=0)} + 180°$) are both greater than 0. Therefore, the closed-loop system of the proposed converter, which adopts the PI voltage controllers, can operate stably. The poles of the closed loop transfer function were calculated previously and they were located in the left half of the plane.

V. PERFORMANCE COMPARISON

Table 2 provides a comparison of the proposed converter with existing DC-DC non-isolated converters reported in the literature, focusing on:

- the operating duty cycle range,
- the total voltage gains of output ports [$G_T = V_o/(V_{i1} + V_{i1})$]

- the normalized voltage stresses on switches based on the sum of the voltage stress of switches over the output voltage ($\sum V_S/V_o$),
- the normalized voltage stresses on diodes based on the sum of the voltage stress of diodes over the output voltage ($\sum V_D/V_o$),
- the normalized current stresses of switches $[I_S/(I_1+I_2)]$ and diodes $[I_D/(I_1+I_2)]$,
- the number of switches (N_S), diodes (N_D), inductors (N_I) and capacitors (N_C),
- the total number of components (N_{Total}), and
- input current ripples (Δi_i).

The proposed converter is compared with the three step-up converters presented in [10], [11], and [21], because all converters have two input ports, single output port and are common-grounded.

By considering specifications of the converters in Table 2, Fig. 19 is plotted. To plot Fig. 19, the turns ratio of the coupled inductors in the proposed converter and the existing converter in [21] is considered as $n_{s1} = n_{s2} = n_s = 2.5$.

Fig. 19(a) shows the ratio of V_o/V_i (two times of total voltage gain ($2\,V_o/(V_{i1}+V_{i2})$) versus the duty cycle D. Where, the ratio of V_o/V_i for the presented dual input converters is obtained by considering $V_{i1} = V_{i2} = V_i$. Fig. 19(a) shows

$$X = \begin{bmatrix} \tilde{i}_{Lk1} \\ \tilde{i}_{Lm1} \\ \tilde{v}_{Ci1} \\ \tilde{v}_{C1} \\ \tilde{i}_{Lk2} \\ \tilde{i}_{Lm2} \\ \tilde{v}_{Ci2} \\ \tilde{v}_{C2} \end{bmatrix}, \quad B_{i1} = \begin{bmatrix} 1/L_{k1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \; B_{i2} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1/L_{k2} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \; B_1 = \begin{bmatrix} 0 \\ (n_{s1}\,V_{Ci1} + V_{C1})/(1+n_{s1})/L_{m1} \\ -I_{Lm1}[n_{s1}/(1+n_{s1})]/C_{i1} \\ -I_{Lm1}/(1+n_{s1})/C_1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \\ -I_{Lm2}n_{s1}/C_{i1} \\ -I_{Lm2}/C_1 \\ 0 \\ [n_{s1}V_{Ci1} + V_{C1} + V_{C2}/(1+n_{s2})]/L_{m2} \\ -[I_{Lm2}n_{s2}/(1+n_{s2})]/C_{i2} \\ -[I_{Lm2}/(1+n_{s2})]/C_2 \end{bmatrix} \tag{115}$$

$$A = \begin{bmatrix} 0 & 0 & -1/L_{k1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1+n_{s1}D_1}{(1+n_{s1})L_{m1}} & \frac{-(1-D_1)}{(1+n_{s1})L_{m1}} & 0 & 0 & 0 & 0 \\ \frac{1}{C_{i1}} & \frac{-(1+n_{s1}D_1)}{(1+n_{s1})\,C_{i1}} & 0 & 0 & 0 & -n_{s1}D_2 & 0 & 0 \\ 0 & \frac{1-D_1}{(1+n_{s1})C_1} & 0 & 0 & 0 & \frac{-D_2}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/L_{k2} & 0 \\ 0 & 0 & \frac{n_{s1}D_2}{L_{m2}} & \frac{D_2}{L_{m2}} & 0 & 0 & \frac{1}{L_{m2}} & \frac{-(1-D_2)}{(1+n_{s2})L_{m2}} \\ 0 & 0 & 0 & 0 & \frac{1}{C_{i2}} & \frac{-(1+n_{s2}D_2)}{(1+n_{s2})C_{i2}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1-D_2}{(1+n_{s2})C_2} & 0 & \frac{-1}{R_0C_2} \end{bmatrix} \tag{116}$$

that the proposed converter has higher ratio of V_o/V_i comparing to existing converters in [10], [11], and [21]. Both the proposed converter and the converter in [21] used two three-winding coupled inductors to increase the voltage gain, and eliminate input current ripples, but the proposed converter, not only has higher voltage gain than the converter in [21], but also, uses lower components number than the presented converter in [21]. It is proved that the proposed converter has the capability to operate in a wider duty cycle range ($0 < D < 1$) than the converters in [10], [11], and [21], which has been operated only for duty cycles higher than 0.5 ($0.5 < D < 1$).

In the proposed converter and the existing converter in [21], the input currents ripples are thoroughly eliminated for the whole range of duty cycles ($0 < D < 0$). However, for the conventional converters in [10] and [11], the input current ripples are eliminated only for the duty cycle D = 0.5. The converters in [10], [11], and [21] are interleaved converters and have two-phase switching pattern. Interleaving causes the converter to have two or even more numbers of conversion ratio functions, which may lead to a complicated control scheme for these converters. However, the proposed converter can provide a single voltage gain function for the whole range of duty cycle, which makes the output voltage regulation

$$X = \begin{bmatrix} \tilde{i}_{Lk1} \\ \tilde{i}_{Lm1} \\ \tilde{v}_{Ci1} \\ \tilde{v}_{C1} \\ \tilde{i}_{Lk2} \\ \tilde{i}_{Lm2} \\ \tilde{v}_{Ci2} \\ \tilde{v}_{C2} \end{bmatrix}, \quad B_{i1} = \begin{bmatrix} 1/L_{k1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \; B_{i2} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1/L_{k2} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \; B_1 = \begin{bmatrix} 0 \\ (n_{s1}\, V_{Ci1} + V_{C1})/(1+n_{s1})/L_{m1} \\ -[I_{Lm1} n_{s1}/(1+n_{s1}) + I_{Lm2} n_{s1}]/C_{i1} \\ -[I_{Lm1}/(1+n_{s1}) + I_{Lm2}]/C_1 \\ 0 \\ (n_{s1} V_{Ci1} + V_{C1})/L_{m2} \\ 0 \\ 0 \end{bmatrix},$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ (n_{s2} V_{Ci2} + V_{C2})/[(1+n_{s2})L_{m2}] \\ -[I_{Lm2} n_{s2}/(1+n_{s2})]/C_{i2} \\ -[I_{Lm2}/(1+n_{s2})]/C_2 \end{bmatrix} \tag{117}$$

$$A = \begin{bmatrix} 0 & 0 & -1/L_{k1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1+n_{s1}D_1}{(1+n_{s1})L_{m1}} & \dfrac{-(1-D_1)}{(1+n_{s1})L_{m1}} & 0 & 0 & 0 & 0 \\ \dfrac{1}{C_{i1}} & \dfrac{-(1+n_{s1}D_1)}{(1+n_{s1})\,C_{i1}} & 0 & 0 & 0 & -n_{s1}D_1 & 0 & 0 \\ 0 & \dfrac{1-D_1}{(1+n_{s1})C_1} & 0 & 0 & 0 & \dfrac{-D_1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/L_{k2} & 0 \\ 0 & 0 & \dfrac{n_{s1}D_1}{L_{m2}} & \dfrac{D_1}{L_{m2}} & 0 & 0 & \dfrac{1+n_{s2}D_2}{(1+n_{s2})L_{m2}} & \dfrac{-(1-D_2)}{(1+n_{s2})L_{m2}} \\ 0 & 0 & 0 & 0 & \dfrac{1}{C_{i2}} & \dfrac{-(1+n_{s2}D_2)}{(1+n_{s2})C_{i2}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \dfrac{1-D_2}{(1+n_{s2})C_2} & 0 & \dfrac{-1}{R_0C_2} \end{bmatrix} \tag{118}$$

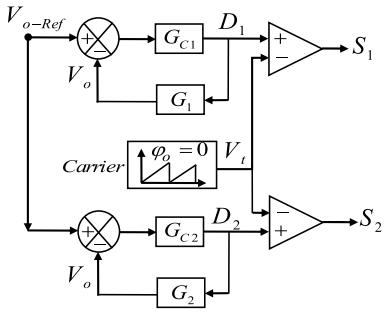

FIGURE 17. Closed loop controller of the output voltage for the proposed converter.

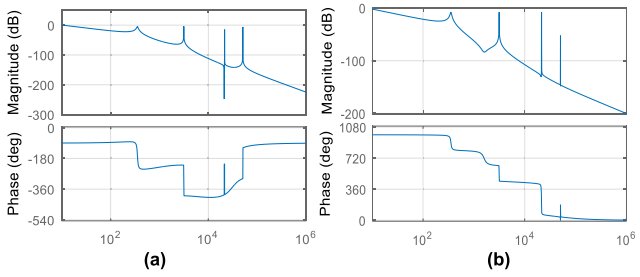

FIGURE 18. Bode plots of the open-loop transfer functions T_{O1} ($T_{O1} = G_{c1} * G_1$) and T_{O2} ($T_{O2} = G_{c2} * G_2$) with PI voltage controller; (a) bode plot for T_{O1} by controlling duty cycle of D_1; (b) bode plot for T_{O2} by controlling duty cycle of D_2.

controller much simpler than the converters in [10], [11], and [21]. In Table 2, the proposed converter has a lower total number of components ($N_{Total} = 10$) compared to the converters in [21] ($N_{Total} = 14$), in [10] ($N_{Total} = 14$), and in [11] ($N_{Total} = 12$). In most boost converters, by increasing the number of components, the voltage gain is increased, as a result, in boost converters, there is a factor of the voltage gain over the total number of components as $(V_o/V_i)/N_T$. Considering Fig. 19(b), the ratio of $(V_o/V_i)/N_T$ for the proposed converter is higher than that for the converters in [10], [11], and [21]. Fig. 19(c) shows the normalized voltage stress on switches for the compared converters, in which the proposed converter has a lower value than the converters in [10] and [11], and a higher value than the converter in [21]. Similarly, Fig. 19(d) shows the normalized voltage stress on diodes, the proposed converter has a lowest stress on its diodes compared to the converters in [10], [11], and [21]. Considering Figs. 19(e) and 18(f), the maximum normalized current stress on switches and diodes for the proposed converter (PC) are lower than that for the converters in [10], [11], and [21].

By using the theoretical analysis of the proposed converter and the three existing converters in [10], [11], and [21], Figure 19(g) is obtained, which shows the maximum voltage gain achieved considering the ESR of components under the condition with $n_{S1} = n_{S2} = 1.5$, $V_{i1} = 18\ V$, $V_{i2} = 12\ V$, $R_o = 500\Omega$ for the four converters. The converters in [21], [10], and [11] are calculated for the duty cycle ranging from 0.5 to 1. The theoretical results are compared with experimental results. Since in the real life applications, the converter typically operates in the duty cycle from 0.1 to 0.9, Figure 19(g) is plotted for this duty cycle range. In Fig. 19(g), the maximum achievable voltage gain for the proposed converter is close to 39, which is obtained at the duty cycle of 0.8. On the other hand, the maximum voltage gain is 40 in [21], close to 20 in [10] and 18 in [11], all under a duty cycle of 0.9. The voltage gain of DC boost converters will be increased with an increased duty cycle. Consequently, the proposed converter has achieved the maximum voltage gain among the four converters.

Moreover, the voltage gain considering ideal components for a constant duty cycle of 0.6 is obtained as illustrated in the third column of Table 2. It shows the proposed converter has the highest voltage gain for this constant duty cycle. The proposed converter and existing converters reported in [10], [11], and [21] have extendable structures to multi-input single-output converters. These existing converters use the multi-phase switching pattern for multi-input structures (for example for a two-input converter, the switching pattern involves two phases; and for a four-input converter, the switching pattern involves four phases), which decreases a suitable operating region for the converters (for example, in two-phase structures, the suitable operating region is obtained for the duty cycles higher than 0.5; and in four-phase structures, the suitable operating region is obtained for the duty cycles higher than 0.75).

When the number of input voltage sources increases, the suitable operation region is further limited and the control system becomes more complicated for these existing converters.

However, in the proposed converter, the switching pattern for the extendable structure with several input voltage sources is in the same way as the two-input converter by using the same switch operation with the same turning on and off moments, which result in a simple control system. Also, the multi-input structure of the proposed converter has just one voltage gain function for the whole range of duty cycles ($0 < D < 1$), which leads to a simple control system as well.

The cost benefits of the proposed DC-DC converter (PC) can be analyzed from the four aspects: 1) the total cost of implementation of power circuits and driver modules; 2) the provided power of each converter; 3) the ratio of the total cost per watt; and 4) the extracted efficiency for the operating power rating, which can be seen in Table 3. As shown in Fig. 20, the proposed converter has a lower value of the Cost per Watt [$/W], which demonstrates that the proposed converter is able to provide a higher power with lower costs. Considering the efficiency range from column 11 of Table 3 and the operating power rating in the column 13 of Table 3, the proposed converter has the highest power and efficiency comparing to other three selected converters. Fig. 21 shows the comparison results of the efficiency of the implemented circuits versus the output power value for the proposed converter and converters presented in [10], [11], and [21].

TABLE 2. Comparison results of three-port high voltage gain DC-DC converters.

Converter	Opeating Duty Cycle	$G_T = \frac{V_o}{V_{i1}+V_{i2}}$ for D=0.6	$V_o/V_i = 2G_T$ & $V_{i1}=V_{i2}=V_i$	$\Delta i_1 = 0$ $\Delta i_2 = 0$	$\sum V_S / V_o$	$\sum V_D / V_o$	$I_S/(I_1+I_2)$	$I_D/(I_1+I_2)$	N_S	N_D	N_{CI}	N_I	N_C	N_{Total}
[10]	$0.5<D<1$	6.25	$\frac{5}{1-D}$	No	$\frac{1}{5}$	$D_{1,2,3,4}:\frac{2}{5}$ $D_5:\frac{1}{5}$	$S_1:\frac{2+D}{5}$ $S_2:\frac{2}{5}$	$\frac{1-D}{5}$	2	5	-	2	5	14
[11]	$0.5<D<1$	5	$\frac{4}{1-D}$	No	$\frac{1}{4}$	$D_{1,2,3}:\frac{1}{2}$ $D_4:\frac{1}{4}$	$S_1:\frac{1+D}{4}$ $S_2:\frac{1}{2}$	$\frac{1-D}{4}$	2	4	-	2	4	12
[21]	$0.5<D<1$	For $n_s=1.5$: 11.25 For $n_s=3$: 18.5	$\frac{4+n_s(3+D)}{1-D}$	Yes	S_1,S_2 $1/[4+n_s(3+D)]$	$D_{1,2,3}:\frac{2(1+n_{s1})}{4+n_{s1}(3+D)}$ $D_4:\frac{1+n_{s1}D}{4+n_{s1}(3+D)}$	$S_1:\frac{(1+n_{s1})(1+D)}{4+n_{s1}(3+D)}$ $S_2:\frac{2(1+n_{s1})}{4+n_{s1}(3+D)}$	$\frac{1-D}{4+n_s(3+D)}$	2	4	2	-	6	14
Proposed converter (PC)	$0<D<1$	For $n_s=1.5$: 14.07 For $n_s=3$: 33.5	$\frac{(1+n_s)^2D}{(1-D)^2}+\frac{1+n_sD}{1-D}$	Yes	$S_1:\frac{1}{(1-D)G_t}$ $S_2:\frac{1+n_sD}{(1-D)^2G_t}$	$D_1:\frac{1+n_s}{(1-D)G_T}$ $D_2:\frac{2+n_s-D}{(1-D)^2G_T}(1+n_s)$	$S_1:\frac{1+n_sD}{G_T(1-D)}$ $S_2:\frac{(1+n_s)^2D}{G_T(1-D)^2}-(1/G_T)$	$D_1:\frac{(1+n_s)^2D}{G_T(1-D)^2}-(1/G_T)$ $D_2:\frac{1}{G_T}$	2	2	2	-	4	10

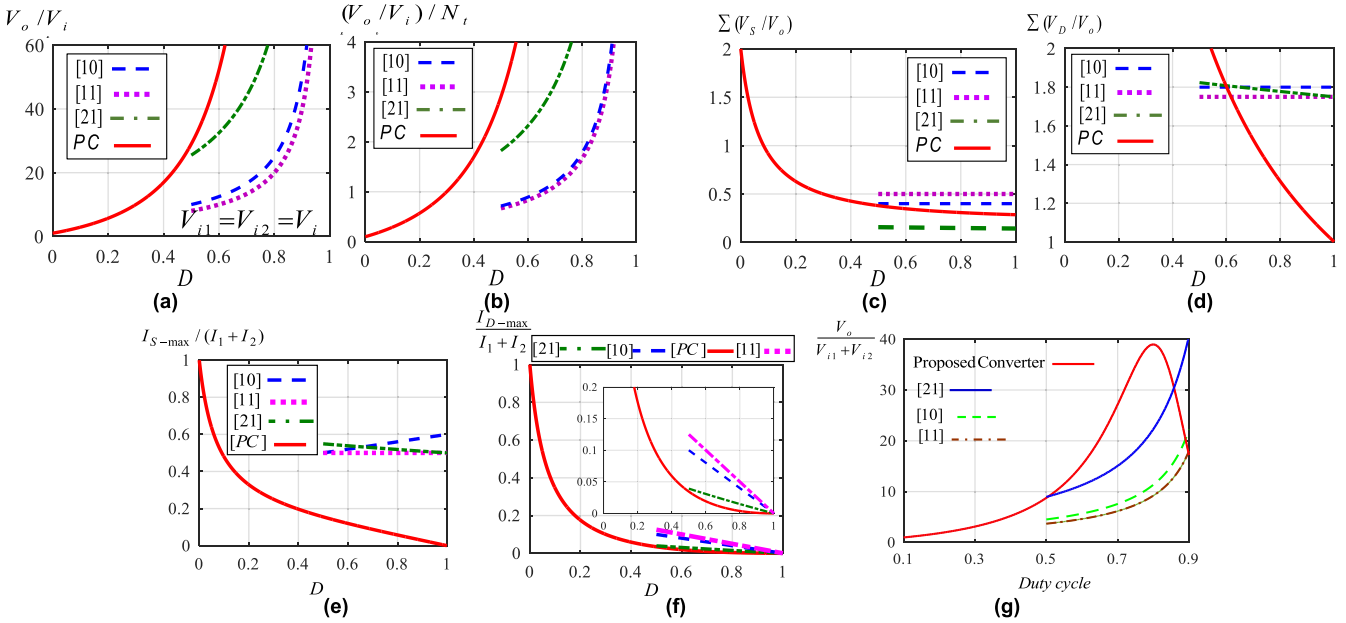

FIGURE 19. Comparative results of the proposed converter with three other dual-input converters versus the duty cycle D: (a) the total voltage gain G_T; (b) the total voltage gain G_T over the total number of components; (c) the total normalized voltage stress on switches; (d) the total normalized voltage stress on diodes; (e) the maximum normalized current stress on switches; (f) the maximum normalized current stress on diodes; (g) the maximum achieved voltage gain considering the ESR of components under the condition ($n_{S1}=n_{S2}=1.5$, $V_{i1}=18\,V$, $V_{i2}=12\,V$, $R_o=500\Omega$).

From column 9 of Table 3, it can be seen that the total cost of the proposed converter is equal to \$78.37\$, which is lower than the total cost of all other three conventional converters in [10], [11], and [21] (129\$, 110.5\$, 99.63\$). The efficiency of the proposed converter for 450 W output power is 93.5%, which is the highest value for such output power among other converters (91.3%, 91%, 92.1%). The cost-benefit plot of the proposed converter is shown in Fig. 20.

TABLE 3. The implemented prototype characteristics in the proposed DC-DC converter and the three DC-DC converters in [10], [11] and [21].

DC-DC Converter	N_S	N_D	N_I	N_C	N_{CI}	N_{total}	N_{Driver}	Total cost of components and controlling system	f_S [kHz]	Eff [%]	P_{Loss} [W]	P_o [W]	$\frac{V_o}{V_{i1}+V_{i2}}$
	Total cost of switches	Total cost of diodes	Total cost of inductors	Total cost of capacitors	Total cost of coupled inductors	Total components cost	Controlling circuit cost						Duty cycle
[10]	2: IPA075N 15N3G	5: MBR40250T	2: CTX10 0-10-52LP	4: C4ATGBW5200A 3MJ 1: B32774D4226	-	14	e	128.97 $	100	91.3	34.8	400	$\frac{390}{20+20}=9.75$
	2×6.88 $=13.76 $	5×1.71 $=8.55 $	2×18.25 $=36.4 $	4×10.64$+8.9 $=51.46$		110.17 $	18.8 $						$D=0.75$
[11]	2: STP120NF	3: UG10DCT 1: V20120C	2: CTX10 0-10-52LP	4: C1=33 uF C2=47 uF C3=10 uF C4=33 uF (MKS4F054707I00MSSD)	-	12	2 Drivers	110.48 $	100	91	18	200	$\frac{194}{20+20}=4.85$
	2×3.63 $=7.26$	3×1.05 $ 1×1.47 $=4.26 $	2×18.25 $=36.4 $	4×10.94=43.76 $		91.68	18.8 $						$D=0.6$
[21]	2: IRFP260N	4: MUR1540G	-	5: C1=C2=C3=C4=Co :180 uF (B43541B8187M000)	2: Toroid (PC40 T51×13×31)	14	2	99.63 $	30	92.1	23.7	300	$\frac{560}{20+30}=11.2$
	2×3.5 $=7 $	4×1.45 $=5.8 $		5×9.77$=48.85 $	2×9.9 $=19.8 $	81.45 $	18.8 $						$D=0.6$
Proposed converter (PC)	1: IRFP4668PbF 1: IXFK150N30X3	1: DPG60I300HA 1: DSEI 60-12A	-	4: ESU476M450AM3AA	2: Toroid (PC40 T51×13×31)	10	2	78.37 $	30	93.5	29.25	450	$\frac{470}{12+18}=15.66$
	7 $ +15.7 $=22.7$	3.56 $+4.83 $=8.39 $		4×2.17 $=8.68 $	2×9.9 $=19.8 $	59.57 $	18.8 $						$D=0.6$

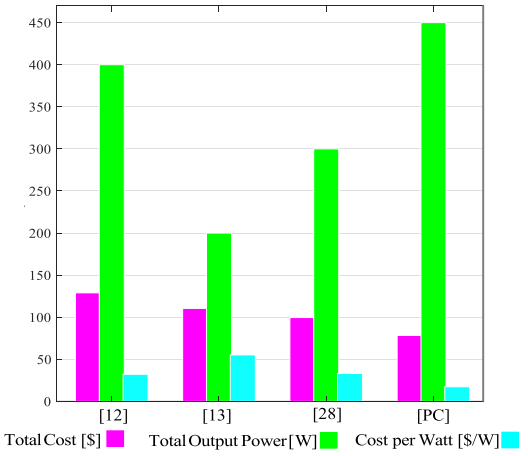

FIGURE 20. Cost benefit comparison.

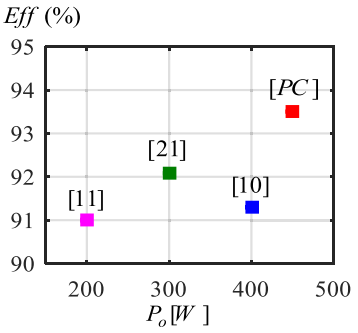

FIGURE 21. Efficiency versus output power of the implemented DISO conventional converters and the proposed converter.

The proposed converter has the highest output power, the lowest total cost of implementation, the minimum Cost per Watt [$/W] ratio comparing to three other conventional converters in [10], [11], and [21]. Note: in Fig. 20, the Cost per Watt [$/W] values of the converters are multiplied by 100, so they can be noticeable in the graph.

The last column of Table 3 shows the maximum extracted voltage gains for the chosen duty cycles for the proposed converter's prototype of this paper and prototypes of the

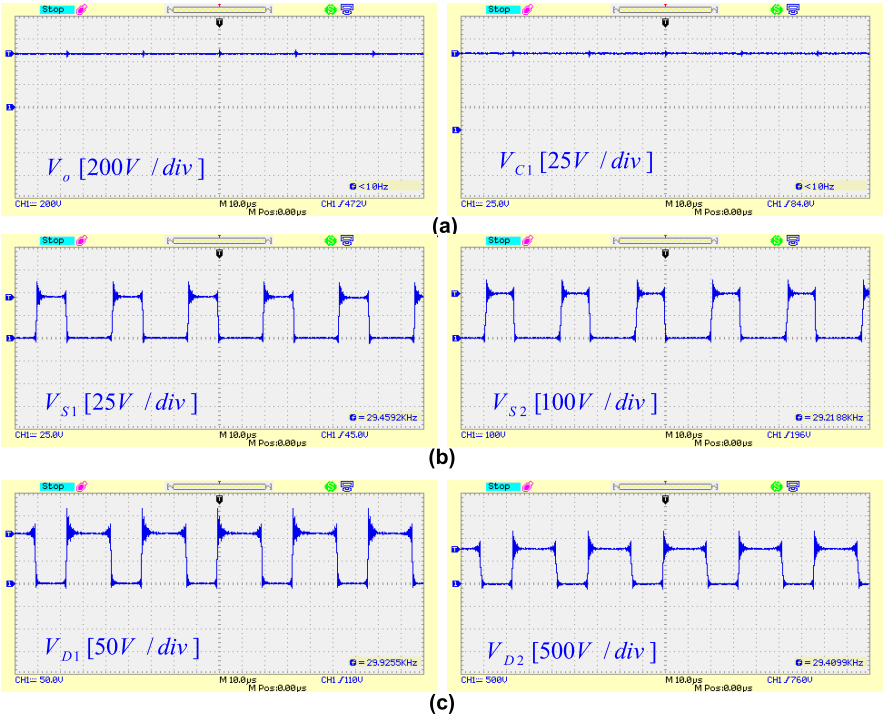

FIGURE 22. Experimental results of the voltages at the output, the capacitor C_1, the switches and the diodes: (a) V_o and V_{C1}; (b) V_{S1} and V_{S2}; (c) V_{D1} and V_{D2}.

three existing converters in [10], [11], and [21] through lab experiments. It is found that the proposed converter's prototype has achieved the highest voltage gain of 15.66 for the duty cycle of 0.6; while the extracted voltage gain from the implemented prototypes of the converters in [10], [11], and [21] are 9.75, 4.85, 11.2 for the duty cycles equal to 0.75, 0.6, 0.6, respectively.

VI. EXPERIMENTAL RESULTS

To verify the calculated theoretical results for the proposed converter, a prototype of the converter has been built and its parameters are provided in Table 4. The experimental results using the prototype were measured as shown in Figs. 22 and 23. The calculated values of voltages and currents from the theoretical analysis by using the parameters in Table 4 are given in Table 5. By a simple comparison, the calculated theoretical values in Table 5 are verified by experimental values.

Considering (43) and (44), the inductances L_{m1} and L_{m2} to achieve CCM operation of the proposed converter are calculated as $L_{m1} > 8\mu H$ and $L_{m2} > 208\mu H$ respectively. The experimental waveforms of the output voltage (V_o), the voltage across capacitor C_1(V_{C1}), the voltage across the two switches S_1 (V_{S1}), S_2(V_{S2}), and the two diodes D_1 (V_{D1}) and D_2 (V_{D2}) are shown in Fig. 22. The output voltage is measured to be about 470 V, which is acceptable according to the theoretical voltage gain of the converter given in Table 5 ($V_o = V_{C2} = 478.87\ V$). The voltage stresses of switches and diodes in Fig. 22 verify the calculated theoretical values in Table 5. For example, in the third and fourth rows of Table 5, the calculated values of voltage stress on switches from (11) and (12) during the time interval of $(1-D)T_s = 13.33[\mu\,\text{sec}]$(the turning off interval time for the switches) are calculated as $V_{S1} = 45V$ and $V_{S2} = 198.75V$, which are almost equal to the extracted results in Fig. 22(b) (the experimental values are $V_{S1} = 45V$ and $V_{S2} = 196\ V$). Moreover, in the fifth and sixth rows of Table 5, the calculated values of voltage stress on diodes from (9) and (10) during the time interval of $DT_s = 20\,[\mu\,\text{sec}]$ (the turning off interval time for the diodes) are calculated as $V_{D1} = 112.5V$ and $V_{D2} = 778.12\ V$, which are almost equal to the extracted results in Fig. 22(c) (the experimental values are $V_{D1} = 110\ V$ and $V_{D2} = 770\ V$).

The average output current based on parameters in Table 4 is calculated as $I_o = V_o/R_o = 0.95\ A$. As a result, the average input currents through the leakage inductances of the coupled inductors are calculated as $I_{i1} = 22\ A$ and $I_{i2} = 4.5\ A$ from (29) and (30), respectively. The experimental results in Fig. 23(a) indicate that average input currents are $I_{i1} = 22\ A$ and $I_{i2} = 4.5\ A$, respectively, which are very close to the calculated theoretical results. Fig. 23(a) also shows that the input current ripples are almost equal to zero with a constant dc value.

The average currents through the magnetizing inductances of the coupled inductors are calculated as $I_{Lm1} = 22.44\ A$, $I_{Lm2} = 5.98\ A$ from (19) and (20). As a result, considering (21) and (22), the maximum and minimum values of the current i_{Lm1} are theoretically calculated as $I_{h1} = 22.44\ A$,

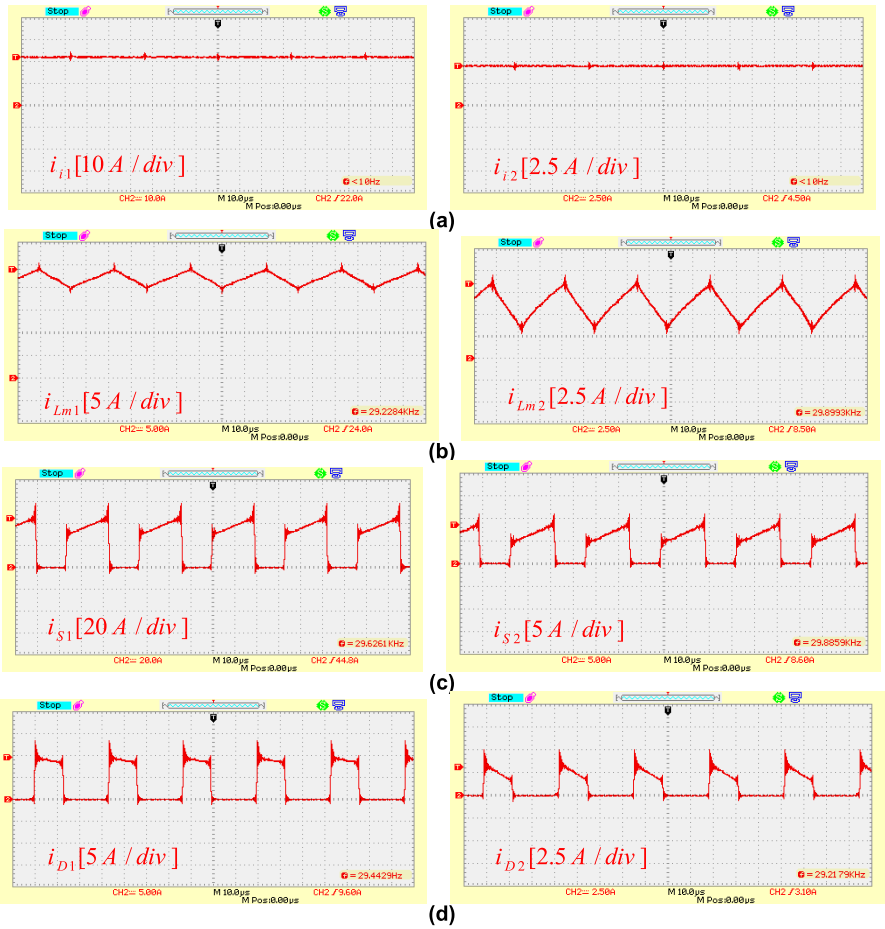

FIGURE 23. Experimental results of the currents of input ports, magnetizing inductances of the coupled inductors, switches and diodes: (a) i_{i1} and i_{i2}; (b) i_{Lm1} and i_{Lm2}; (c) i_{S1} and i_{S2}; (d) i_{D1} and i_{D2}.

TABLE 4. Prototype parameters.

Voltages, Power, and Load	$V_{i1}=18\,V$, $V_{i2}=12\,V$, $V_o=470\,V$, $P_o=450\,W$, $R_o=500\Omega$
Capacitors, Duty cycle, and Frequency	$C_{i1}=C_{i2}=C_1=C_2=100\mu F$: ESU476M450AM $D=0.6$, $f_s=30\,kHz$
Inductors	$L_{m1}=100\mu H$, $L_{k1}=4\mu H$, $n_{S1}=1.5$, $n_{t1}=1$, $n_{t2}=1$ $L_{m2}=500\mu H$, $L_{k2}=22.5\mu H$, $n_{S2}=1.5$, Type: Toroid (PC40 T51×13×31)
Switches	S_1 : IRFP4668PbF, S_2 : IXFK150N30X3
Diodes	D_1 : DPG60I300HA, D_2 : DSEI 60-12A

$I_{\ell 1} = 20.64\ A$, respectively. The experimental results in the left graph of Fig. 23(b) indicate that the maximum and minimum values of the current i_{Lm1} are $I_{h1} = 24\ A$ and $I_{\ell 1} = 20\ A$, respectively, which are very close to the calculated theoretical results.

In the similar way, considering (23), the maximum value of current i_{Lm2} is theoretically calculated as $I_{h2} = 8.47\ A$, the experimental result in right graph of Fig. 23(b) shows that the maximum value of current i_{Lm2} is $I_{h2} = 8.5\ A$, which is very close to the calculated theoretical results.

Moreover, considering (25)-(28), the maximum currents through the switches and diodes are calculated as $i_{S1-\max} = (n_{s1}+1)I_{h2} + I_{h1} = 45.41A$, $i_{S2-\max} = I_{h2} = 8.47A$, $i_{D1-\max} = I_{h1}/(n_{s1}+1) = 9.6A$, $i_{D2-\max} = I_{h2}/(1+n_{s2}) = 3.38\ A$.

Considering Figs. 23(c) and 23(d), the maximum current values of the switches and diodes are calculated as $i_{S1-\max} = 44.8A$, $i_{S2-\max} = 8.6A$, $i_{D1-\max} = 9.6A$, $i_{D2-\max} = 3.1\,A$, which are almost equal to the theoretical values.

In Fig. 23(a), the input current ripples of the proposed converter is equal to zero. The measured current waveforms for the switches and diodes of the prototype demonstrate that the mean value of the experimental current waveforms in Fig. 23 can easily verify the calculated values in Table 5. The measured efficiency using the parameters of the implemented prototype from Table 4 is equal to 93.5% for the

TABLE 5. The calculated theoretical values under experimental conditions.

Output power	$P_o = V_o^2 / R_o = 450\,W$
V_{C1} (Eq. 7), V_o (Eq. 8)	$V_{C1} = 4.75 V_{i1} = 85.5\,V$, $V_o = V_{C2} = 478.87\,V$
V_{S1} (Eq. 11)	$V_{S1} = 45\,V$ during $(1-D)\,T_S$
V_{S2} (Eq. 12)	$V_{S2} = 198.75\,V$ during $(1-D)\,T_S$
V_{D1} (Eq. 9)	$V_{D1} = 112.5\,V$ during DT_S
V_{D2} (Eq. 10)	$V_{D2} = 778.12\,V$ during DT_S
Output current	$I_o = V_o / R_o = 0.95\,A$
I_{Lm1} and I_{Lm2} (Eq. 20, Eq. 19)	$I_{Lm1} = 22.44\,A$, $I_{Lm2} = 5.98\,A$
Current ripple of inductances	$\Delta i_{Lm1} = 3.6\,A$, $\Delta i_{Lm2} = 4.98\,A$
Maximum and minimum of i_{Lm1} (Eq. 21 and 22)	$I_{h1} = 24.24\,A$, $I_{\ell 1} = 20.64\,A$
Maximum and minimum values of i_{Lm2} (Eq. 23 and 24)	$I_{h2} = 8.47\,A$, $I_{\ell 2} = 3.49\,A$
Average input currents of I_{i1} and I_{i2} (Eq. 29, Eq. 30)	$I_{i1} = I_{Lm1} = 22.44\,A$ $I_{i2} = (1+n_{s2})D\,I_o / (1-D) = 4.54\,A$
Average currents of the switches during a switching period	$I_{S1} = D[(1+n_{s1})I_{Lm2} + I_{Lm1}] = I_{i2} = 4.54\,A$, $I_{S2} = I_{D1} = I_{i1} - I_o = 21.48\,A$, $I_{D2} = I_o = 0.95\,A$
i_{S1} (Eq. 14)	$i_{S1} = (1+n_{s1})i_{Lm2} + i_{Lm1}$ $[i_{S1-\max} = 45.41\,A,\quad i_{S1-\min} = 29.36\,A]$ during DT_s
i_{S2} (Eq. 13)	$i_{S2} = i_{Lm2}$ during DT_s
i_{D1} (Eq. 15)	$i_{D1} = i_{Lm1} / (1+n_{s1})$ $[i_{D1-\max} = 9.6\,A, i_{D1-\min} = 8.25\,A]$ during $(1-D)\,T_s$
i_{D2} (Eq. 16)	$i_{D2} = i_{Lm2} / (1+n_{s2})$ during $(1-D)\,T_s$

extracted power of 450 W. The experimental efficiency of the proposed converter vs. various output power P_o (P_o is equal to 150 W, 250 W, 350 W, and 450 W) are obtained as shown in Fig. 24. The experimental prototype of the proposed converter is shown in Fig. 25.

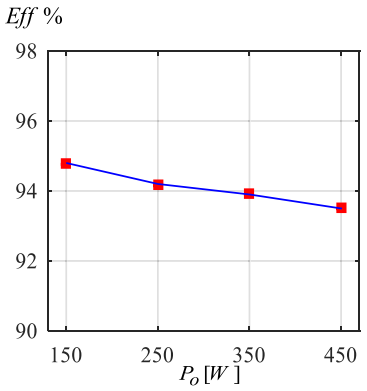

FIGURE 24. The experimental efficiency of the proposed converter versus the output power.

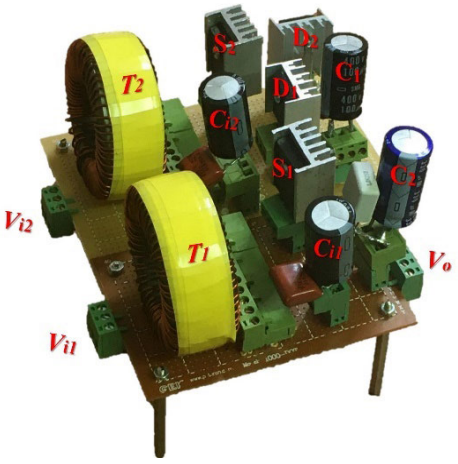

FIGURE 25. The implemented prototype of the proposed converter.

Therefore, the extracted controller block with the specified PI parameters as equations (123) and (124) are applied to

$$
\begin{aligned}
G_1 &= -5.601e11^5 - 8.467e15s^4 - 6.97e20s^3 - 3.072e23s^2 - 1.991e29s + 1.536e33s^8 + 20\,s^7 + 3.028e09s^6 \\
&\quad + 6.054e10s^5 + 1.207e18s^4 + 2.41e19s^3 + 1.177e25s^2 + 2.237e26s + 1.456e30 \\
T_{O1} &= -5.601e06s^6 - 9.027e10s^5 - 7.055e15s^4 - 1.004e19s^3 - 1.995e24s^2 + 1.337e28s + 1.536e31s^9 + 20\,s^8 \\
&\quad + 3.028e09s^7 + 6.054e10s^6 + 1.207e18s^5 + 2.41e19s^4 + 1.177e25s^3 + 2.237e26s^2 + 1.456e30s \\
T_1 &= -5.601e06s^6 - 9.027e10s^5 - 7.055e15s^4 - 1.004e19s^3 - 1.995e24s^2 + 1.337e28s + 1.536e31s^9 + 20\,s^8 \\
&\quad + 3.028e09s^7 + 6.054e10s^6 + 1.207e18s^5 + 2.409e19s^4 + 1.177e25s^3 + 2.217e26s^2 + 1.47e30s + 1.536e31 \\
G_2 &= -23920s^7 + 9.616e08s^6 - 7.29e13s^5 + 2.889e18s^4 - 2.958e22s^3 + 1.1e27s^2 - 4.01e29s + 2.735e33s^8 + 20\,s^7 \\
&\quad + 3.028e09s^6 + 6.054e10s^5 + 1.207e18s^4 + 2.41e19s^3 + 1.177e25s^2 + 2.237e26s + 1.456e30 \\
T_{O2} &= -122s^7 + 4.904e06s^6 - 3.718e11s^5 + 1.474e16s^4 - 1.509e20s^3 + 5.612e24s^2 - 2.045e27s + 1.395e31s^9 + 20\,s^8 \\
&\quad + 3.028e09s^7 + 6.054e10s^6 + 1.207e18s^5 + 2.41e19s^4 + 1.177e25s^3 + 2.237e26s^2 + 1.456e30s \\
T_2 &= -122s^7 + 4.904e06s^6 - 3.718e11s^5 + 1.474e16s^4 - 1.509e20s^3 + 5.612e24s^2 - 2.045e27s + 1.395e31s^9 + 20\,s^8 \\
&\quad + 3.028e09s^7 + 6.055e10s^6 + 1.207e18s^5 + 2.411e19s^4 + 1.177e25s^3 + 2.293e26s^2 + 1.454e30s + 1.395e31
\end{aligned}
$$

generate the required codes of the pulses of switches S_1 and S_2 to be interfaced with Lunchpad C2000 280049C. As a result, the generated pulses S_1 and S_2 from Lunchpad 280049C are applied as gate-source trigger pulses of switches.

VII. CONCLUSION

In this paper, a DC-DC multi-input and single-output boost converter with a high voltage gain is proposed, which is applicable in PV systems. The number of input modules of the proposed converter is expandable, and its voltage gain can be further increased by increasing the number of input modules. Its voltage gain can also be increased by increasing turns ratio of the coupled inductors. In the proposed converter, input current ripples of the input modules are eliminated by utilizing a capacitor and the third winding of the coupled inductors. The proposed converter has the merit of achieving one voltage gain function for the whole range of duty cycles compared to conventional interleaved multi-input converters, which can make the output voltage regulation controller much simpler. The voltage stress on switches of the proposed converter is low.

APPENDIX

G_1, T_{O1}, T_1, G_2, T_{O2}, and T_2, as shown at the bottom of the previous page.

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