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A 12-bit 100MS/s SAR ADC With Equivalent Split-Capacitor and LSB-Averaging in 14-nm CMOS FinFET

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ABSTRACT This paper presents an energy-saving and high-resolution successive approximation register (SAR) analog-to-digital converter (ADC) with 14-nm CMOS FinFET technology for wireless communication system. An Equivalent Split-Capacitor is proposed to enlarge redundancy range and alleviate the settling error of the bridge capacitor array. A hybrid capacitor switching procedure is adopted to reduce power consumption and the variation of input common-mode voltage of the comparator. Measurement results of the 14-nm CMOS SAR-ADC achieves a SNDR of 61.29 dB and 58.34dB at low and Nyquist input frequency, respectively, resulting in figure-of-merits(FoMs) of 8.2 and 11.15fJ/conversion-step, respectively. The ADC core occupies an active area 0.112mm^2.

INDEX TERMS SAR ADC, 14-nm CMOS FinFET, equivalent split-capacitor, hybrid capacitor switching procedure, figure-of-merits (FoMs).

I. INTRODUCTION

With the rapid development of wireless communication and integrated circuit, people's daily life is becoming more convenient and intelligent. Electronic devices such as tablet computers and smart phones are playing a more and more important role in people's daily life. The battery life has a great impact on the experience of these handheld devices. Low-power chips are very helpful to prolong the service time of the battery. The ADC is a very important block in the wireless receiver, it converts analog signals to the digital signals and then transmits them to digital baseband. Therefore, the ADC with low-power architecture becomes more and more attractive. The successive approximation register(SAR) ADC is compatible with advanced digital technology and the structure of SAR ADC is simple, which makes it energy-efficient architecture. It takes several cycles for SAR ADC to finish one conversion. However, with the continuous advancement of CMOS technology, the channel length of the transistor keeps decreasing. The conversion speed of SAR ADC has been greatly improved. The single-channel SAR ADC with 10-bit to 12-bit resolutions has achieved a sampling rate of more than 100MS/s with excellent efficiency and small area [1]–[3].

Although pipelined ADC also achieves the 100MS/s-200MS/s sampling rates with 10 bit-12 bit, pipelined ADC consumes more power than SAR ADC under advanced CMOS technology. The pipelined ADC needs high-performance operational amplifier, which burns up power. Besides, the supply voltage becomes lower and lower in advanced CMOS process, which reduces the output signal swing and gain of the operational amplifier. Increasing sampling capacitance can improve signal-to-noise ratio(SNR) of the pipelined ADC. However, it generates a lot of power dissipation. The SAR ADC consists of DAC capacitor array, comparator and digital control logic circuit. The dynamic comparator is preferred because lower power can be achieved. More and more digital control logic circuits are realized by dynamic logic, which consumes less power dissipation. Besides, advanced technology is beneficial to save power dissipation of asynchronous digital control circuit. Many energy-efficient capacitor switching processes can greatly save the power dissipation of the capacitor array.

Advanced CMOS technology is also beneficial to improve the speed of the comparator and digital control logic. Even if supply voltage is reduced, the SAR ADC also achieves

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full-scale signal swing, which results in relatively small sampling capacitance. Therefore, SAR ADC shows excellent performance under advanced CMOS process.

Generally, M-bit SAR ADC requires N cycles to finish one conversion (N > M). Each cycle consists of the settling time of the DAC, the resolving time of the comparator and the delay of the digital control logic. For improving sampling rate of the SAR ADC, the corresponding time of these three parts should be reduced. The double-tail latch [4] and the triple-tail latch [5] are proposed to reduce the resolving time of the comparator. Asynchronous dynamic control logic is used to reduce delay [6]–[8]. The settling error of the DAC capacitor array can produce wrong output codes of SAR ADC. Settling error of DAC capacitor array should be less than 0.5LSB to make sure the quantization is correct. However, it needs to take much time for capacitive DAC to stabilize, which seriously increases the power dissipation of the reference voltage and degrades the speed of the ADC. In order to alleviate settling error of DAC, some redundant schemes have been proposed. A non-binary redundancy [9] can relax requirement for the settling error and a certain range error can be tolerated. However, non-binary redundancy needs extra control circuit, which increases the complexity of design. Besides, the scaling of DAC capacitor sizes is 1.85, which is difficult to match the layout. The binary-scaled-error compensation [10] inserts several extra capacitors in the DAC to provide compensative voltage. However, extra capacitors increase the sampling capacitance and cause small input range. Binary-Scaled-Recombination-Weighting SAR ADC [11] and Redundant Based on Split-Capacitor [12] technique split the MSB capacitor to several groups, which are either added to LSBs groups or inserted in original capacitors array. However, it is not suitable for DAC capacitor array based on the bridge-capacitor structure.

DAC capacitor array has a great impact on the performance of the SAR ADC. The total capacitance of DAC capacitor array determines the thermal noise(KT/C). The value of unit capacitor affects the matching accuracy and linearity. Power dissipation of capacitor network depends on different switching methods. Conventional switching procedure is inefficient. Many low-power switching procedures are proposed to save the power dissipation of the DAC network. The split capacitor switching procedure saves the power consumption in the down transition [13]. However, this method does not reduce total capacitance of DAC capacitor array. The monotonic switching procedure [14] reduces the capacitance of DAC capacitor by 50%. Besides, it does not require the upward transition, which saves much power consumption. However, the common mode voltage of DAC capacitor array converges from half of the $V_{ref}$to ground, which causes the dynamic offset of the comparator and degrades the performance of ADC. Vcm-based switching method [15] also greatly reduces the power dissipation. However, it requires an extra reference voltage V_{cm} and lots of switches. The variation of the common mode voltage is reduced by 50% in switchback switching process [16]. Bidirectional single-side switch technique [17] reduces the capacitance by 75% and the variation of common mode voltage by 50%. However, it needs complex control logic and extra reference voltage V_{cm}.

The reference voltage in the SAR ADC is provided by reference voltage buffer(RVB). When off-chip the RVB is adopted in SAR ADC, the parasitic inductance of bonding wires and PCB trace causes the reference voltage ringing and degrades the settling of DAC. A large decoupling capacitor is needed to stabilize the reference voltage, which occupies the a lot of area. The parasitic inductance of bonding wires does not exit when on-chip RVB is adopted. The on-chip RVB can reduce the power consumption and chip size.

This paper proposed an equivalent split-capacitor which can enlarge redundancy range and alleviate the settling error of the bridge capacitor array. Besides, a hybrid capacitor switching process is proposed. Compared with the monotonic switching process, the proposed hybrid capacitor switching process reduces the variation of common mode voltage by 93.75%. The reference voltage buffer and the clock generator have an important impact on the performance of the SAR ADC. The structure and design of these two blocks are also discussed in this paper. The proposed SAR ADC achieves 8.2fJ/conversion-step and occupies an active area 0.112mm^2.

The remainder of this paper is as follows. The section II presents the overall architecture of the proposed SAR ADC. The section III describes the proposed techniques, including an equivalent split-capacitor based on the bridge capacitor array and the hybrid switching procedure. The section IV presents key building blocks implementation, including bootstrapped switch, high-speed and low-noise comparator, digital control logic, reference voltage buffer and clock generator. The measurement results of proposed SAR ADC and comparison to recent works are shown in section V. Finally, the conclusion is summarized in section VI.

II. ADC OVERALL ARCHITECTURE

Fig. 1 shows the overall architecture of the proposed SAR ADC. The top SAR ADC is composed of clock generator, reference voltage buffer and ADC core. Clock generator is used to provide the sampling clock for the bootstrapped switch. The vinclk and vipclk are differential sinusoidal signal with the frequency of the 400MHz. Clock generator converts the differential input sinusoidal signal to single-ended output square wave, then yields the square wave with a duty cycle of 25% though logical operation. The clock jitter of the clock generator will cause the uncertainty of the sampling time. The larger clock jitter is, that is, the higher uncertainty of the sampling time. As a result, the lower SNR can be achieved. The clock generator with low clock jitter is applied in this design. The RVB provides the reference voltage VREF for capacitor array of ADC core. A large decoupling capacitor is not needed when on-chip RVB is used, which reduces the area of the SAR ADC. In addition, the RVB can reduce the VREF ringing caused by parasitic inductance of bonding wires, which can improve SNR and reduce power dissipation. For a 12-bit, 100MS/s SAR ADC, DAC capacitor array must

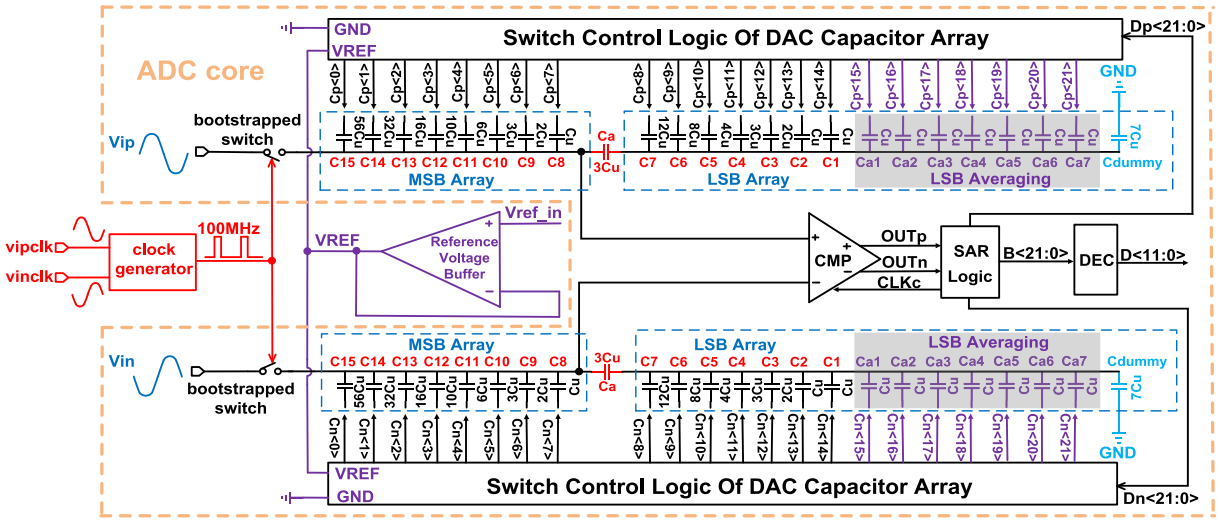

FIGURE 1. The overall architecture of the proposed SAR ADC.

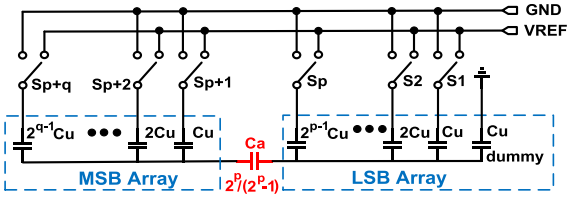

FIGURE 2. The conventional N-bit bridge capacitor array.

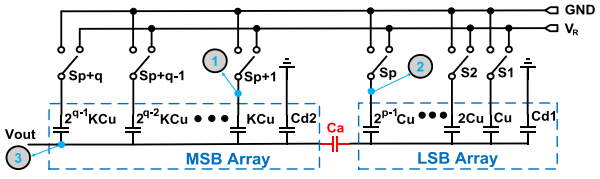

FIGURE 3. The bridge capacitor array with integer Ca.

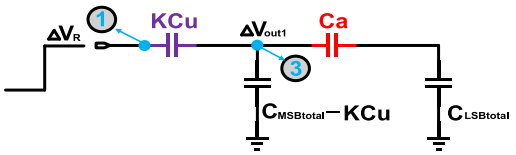

FIGURE 4. The delta V_R is applied at the node 1.

be settled in a very short period of time, which needs a high-speed RVB. An open-loop RVB with replica source follower(SF) [18] is applied in this design, which has a small output resistance and wide bandwidth. The RVB with this architecture can shorten the settling time of the capacitor array.

The ADC core consists of bootstrapped switch, DAC capacitor array, dynamic comparator, SAR logic, switch control logic of DAC capacitor array and digital error correction(DEC). The top-plate sampling is used to improved the speed of the SAR ADC. The bridge capacitor array can reduce the amounts of the unit capacitor. Thus, the larger unit capacitance can be used, which reduces the mismatch of the unit capacitor. The capacitor array consists of MSB array and LSB array. An integer bridge capacitor Ca is used to reduce the mismatch in the layout. In order to alleviate DAC settling time issue, redundancy based on bridge capacitor is proposed. At the same time, LSB averaging technique [19] is used to relax requirements for the comparator noise in LSB array. A hybrid capacitor switching process is used to reduce the variation of input common-mode voltage of the comparator and power dissipation of DAC capacitor array. A multistage comparator with differential inverter [8] is used to improve the speed and reduce the noise. Firstly, the input signals Vip and Vin are sampled to the top plates of DAC capacitor arrays during the sampling period. After the sampling, the comparator makes the first comparison. The SAR logic generates control signals Dn<21:0> and Dp<21:0> according to the OUTp and OUTn. Then, switch control logic controls capacitor array switch to VREF or GND. At the same time, the CLKc resets the comparator. When the capacitor arrays complete charge redistribution, the comparator makes the second comparison. The SAR ADC continues repeating the process until the last bit is determined. Finally, the DEC converts the original digital codes B<21:0> to binary codes D<11:0>.

III. THE PROPOSED EQUIVALENT SPLIT-CAPACITOR AND HYBRID CAPACITOR SWITCHING

A. EQUIVALENT SPLIT-CAPACITOR

For SAR ADC with the binary weighted DAC capacitor array, the number of the unit capacitor increases exponential with the resolution. However, the bridge capacitor array has less number of unit capacitor compared with binary weighted DAC capacitor array. Thus, the bridge capacitor array has less

interconnections, which can reduce the parasitic capacitance, power dissipation and improve the speed. Fig. 2 shows the conventional N-bit bridge DAC capacitor array. The bridge capacitor array is composed of p-bit LSB array and q-bit MSB array. The bridge capacitor Ca is not an integer but a fraction, which is not conducive to layout matching and causes the non-linearity. In Fig. 3, the voltage V_R is applied at the node 1 and the node 2 respectively. When the voltage ΔV_R is applied at the node 1, the corresponding equivalent circuit is shown in Fig. 4. When the voltage ΔV_R is applied at the node 2, the corresponding equivalent circuit is shown in Fig. 5. In order to maintain correct weighting, the voltage ΔV_{out1} is the twice the voltage ΔV_{out2}. $C_{MSBtotal}$ is the sum of capacitance of the all capacitors in MSB array, $C_{MSBtotal}$ is shown as equation (1). $C_{LSBtotal}$ is the sum of capacitance of the all capacitors in the LSB array, $C_{LSBtotal}$ is shown as equation (2).

$$C_{MSBtotal} = \left(2^q - 1\right) KC_u + C_{d2} \tag{1}$$

$$C_{LSBtotal} = \left(2^p - 1\right) C_u + C_{d1} \tag{2}$$

In Fig. 4, the voltage ΔV_{out1} of the node 3 is shown as equation (3).

$$\Delta V_{out1} = \frac{KC_u}{\frac{C_a C_{LSBtotal}}{C_a + C_{LSBtotal}} + C_{MSBtotal}} \Delta V_R \tag{3}$$

In Fig. 5, the voltage ΔV_{out2} of the node 3 is shown as equation (4).

$$\Delta V_{out2} = \frac{2^{p-1} C_u}{\frac{C_a C_{MSBtotal}}{C_a + C_{MSBtotal}} + C_{LSBtotal}} \frac{C_a}{C_a + C_{MSBtotal}} \Delta V_R \tag{4}$$

$$\Delta V_{out1} = 2\Delta V_{out2} \tag{5}$$

From the equation (5), the equation (6) can be obtained.

$$\frac{C_a}{C_u} = \frac{K}{2^p - K} \frac{C_{LSBtotal}}{C_u} = \frac{K}{2^p - K} \frac{\left(2^p - 1\right) C_u + C_{d1}}{C_u} \tag{6}$$

From the equation(6), as long as the value of K, p and C_{d1} is appropriate, the integer C_a can be obtained. In this design, 12-bit DAC capacitor array is divided into 8-bit MSB array and 4-bit LSB array. In order to save the area, the K = 1 in the equation(6). In the case K = 1, p = 4, the equation(6) can be written the equation(7).

$$\frac{C_a}{C_u} == \frac{1}{16 - 1} \frac{15C_u + C_{d1}}{C_u} \tag{7}$$

In the equation(7), when C_{d1} is equal to$15C_u$, C_a is equal to $2C_u$. When C_{d1} is equal to $30C_u$, C_a is equal to $3C_u$. Too large C_a will cause large the parasitic capacitance, which is detrimental to the linearity of the ADC. In this design, C_a is equal to $3C_u$.

In order to reduce the parasitic capacitance of the bridge capacitor, the layout of the DAC capacitor array needs to be compact and symmetrical. Besides, the LSB averaging method can alleviate the influence of the parasitic capacitance.

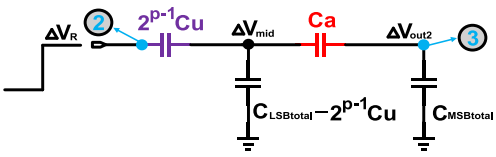

FIGURE 5. The delta V_R is applied at the node 2.

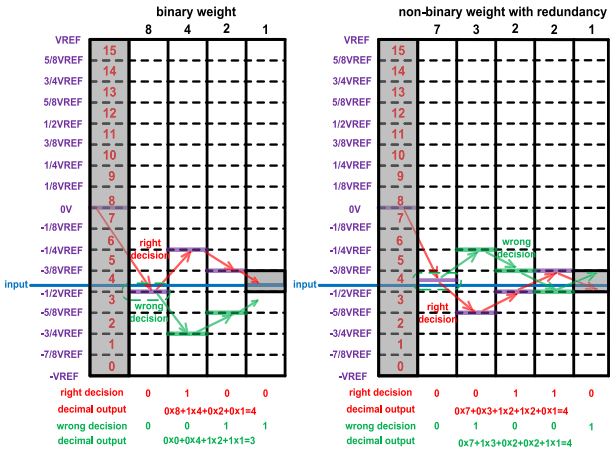

FIGURE 6. The 4-bit binary weight and non-binary weight with redundancy SAR search algorithm.

The SAR ADC can get the correct conversion only when settling error of DAC is less than 1/2LSB, which will consume a lot of power and reduce the speed of the ADC. The redundancy can alleviate the DAC settling issues. The Fig. 6 shows the 4-bit binary weight and non-binary weight with redundancy SAR search algorithm.

In Fig. 6, the blue line represents the input signal of SAR ADC. The red line represents the search path with right decision. The green line represents the search path with wrong decision. In the binary-weight SAR ADC, right decimal output is $0 \times 8 + 1 \times 4 + 0 \times 2 + 0 \times 1 = 4$. If the wrong decision occurs in the second comparison, the decimal output is $0 \times 0 + 0 \times 4 + 1 \times 2 + 1 \times 1 = 3$. A wrong decision can not be corrected in this algorithm. In the non-binary weight with redundancy SAR ADC, the right decimal output is $0 \times 7 + 0 \times 3 + 1 \times 2 + 1 \times 2 + 0 \times 1 = 4$. If the wrong decision occurs in the second comparison, the decimal output is $0 \times 7 + 1 \times 3 + 0 \times 2 + 0 \times 2 + 1 \times 1 = 4$. In this redundant algorithm, a wrong decision can be corrected as long as subsequent comparisons are all correct.

For M bit SAR ADC, it needs N (N> M) steps to finish conversion if the redundancy is introduced. W_j represents the weighting of the j-th step. If a wrong decision occurs in the j-th step, the error can be corrected when W_j must satisfy the

$$W_j < \sum_{i=j+1}^{N} W_i \tag{8}$$

Fig. 7 shows the conventional 12 bit bridge capacitor array. 12-bit DAC capacitor array is divided into 8-bit MSB array

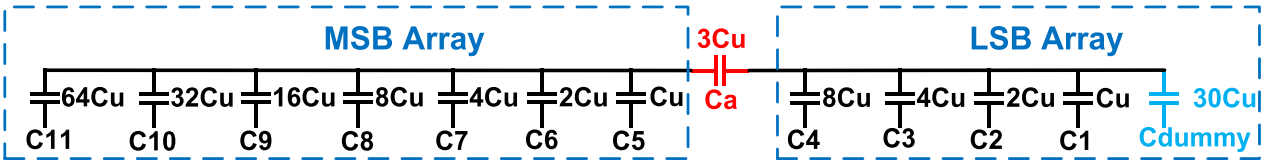

FIGURE 7. The conventional bridge capacitor array without redundancy.

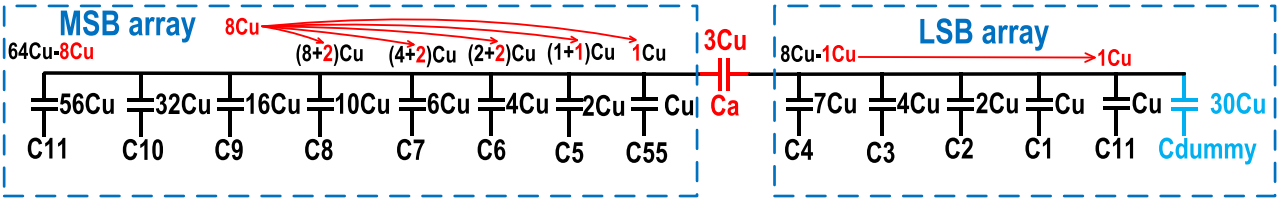

FIGURE 8. The binary-scaled recombination method [11] in bridge structure.

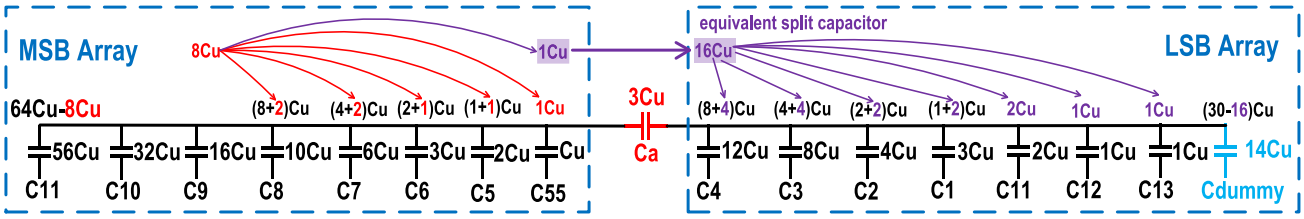

FIGURE 9. The proposed equivalent split-capacitor in bridge structure.

and 4-bit LSB array. There is no redundancy in the DAC capacitor array. Therefore, it can not alleviate settling issue of the DAC. The binary-scaled recombination method [11] is applied to bridge capacitor array in Fig. 8. In Fig. 8, the MSB capacitor C11 is divided in two parts, $56C_u$ and $8(2^3)C_u$. Next, $8C_u$ is divided into $2C_u$, $2C_u$, $2C_u$, $1C_u$ and $1C_u$ respectively. These groups are added to other groups or inserted in MSB array. The same method is applied to LSB array. However, weighting of the capacitor C55 is 32LSB, the sum of total weighting of LSB array is 31LSB. The weighting of the capacitor C55 is larger than the sum of total weighting of LSB array. Therefore, there is no redundancy in the capacitor C55. The weighting of the capacitor C55 is large. If a wrong decision occurs in the comparison cycle corresponding to the capacitor C55, which will produce the wrong digital output and affect the performance of the ADC.

Equivalent split-capacitor is proposed in Fig. 9 to solve the redundancy problem of the capacitor C55. The MSB capacitor C11 is divided in two groups, $56C_u$ and $8C_u$. Next, $8C_u$ is divided into $2C_u$, $2C_u$, $1C_u$, $1C_u$, $1C_u$, $1C_u$. The capacitors $2C_u$, $2C_u$, $1C_u$ and $1C_u$ are added to the capacitors C8, C7, C6 and C5. $1C_u$ is inserted to MSB array to form the capacitor C55. The remaining purple $1C_u$ is ready to be allocated to the LSB array. Due to the existence of the bridge capacitor Ca, the purple capacitor $1C_u$ can not be directly placed in the LSB array. In the Fig. 9, the weighting of the capacitor C55 is 32LSB in the MSB array and the weighing of the capacitor C13 is the 2LSB in the LSB array. In other words, the weighting of the unit capacitor C_u is 32LSB in the MSB array and the weighting of the unit capacitor C_u is 2LSB in the LSB array. The weighting of the unit capacitor C_u in the MSB is 16 times the weighting of the unit capacitor C_u in the LSB array. Therefore, the purple the $1C_u$ in the MSB array is equivalent $16C_u$ in the LSB array. The $16C_u$ is called the equivalent bridge capacitor. When $16C_u$ is added to LSB array, the linearity of LSB array will change. The capacitor Cdummy changes from $30C_u$ to $14C_u$ to keep the linearity of ADC unchanged. The equivalent split capacitor $16C_u$ is divided into seven groups, $4C_u$, $4C_u$, $2C_u$, $2C_u$, $2C_u$, $1C_u$, $1C_u$. These groups are added to other groups or inserted in LSB array. In Fig. 9, the sum of total weighting of LSB array is 63LSB, which is larger than the weighting of the capacitor C55. Therefore, there is redundancy in the capacitor C55. If a wrong judgment occurs in the comparison cycle corresponding to the capacitor C55, which can be corrected.

Table 1 shows the comparison of redundant range with different redundant schemes. In the 8th cycle(the last cycle of MSB array), the redundant range is 0 LSB in [20] and the redundant range is 32 LSB in proposed equivalent split-capacitor method. The weighting of the 8th cycle is relatively large. If the wrong decision is made in the 8th cycle, the performance of ADC will degrade. The proposed

TABLE 1. The comparison of redundant method.

	proposed equivalent spilt capacitor		binary-scaled recombination[20]	
	16-bit cycles to convert 12-bit		14-bit cycles to convert 12-bit	
number of bit-cycling	bit weighting	redundancy range(LSB)	bit weighting	redundancy Range(LSB)
1	1792	512	1792	512
2	1024	256	1024	256
3	512	256	512	256
4	320	128	320	128
5	192	64	192	64
6	96	64	128	0
7	64	32	64	0
8	32	32	32	0
9	24	16	14	4
10	16	8	8	2
11	8	8	4	2
12	6	4	2	2
13	4	2	2	0
14	2	2	1	0
15	2	0		
16	1	0		

equivalent split-capacitor method can provide a certain range redundancy to tolerate DAC settling error. Besides, there is no redundancy in the 6th and the 7th cycle in [20]. However, the proposed method has redundancy in the 6th and the 7th cycle. Therefore, proposed hybrid redundancy is suitable for the bridge structure and high-resolution ADC.

The digital output can be expressed as:

$$\begin{aligned} Dout &= B_{15} \times 2^5 \times \left(2^6 - 2^3\right) + B_{14} \times 2^5 \times 2^5 \\ &\quad + B_{13}2^5 \times 2^4 + B_{12} \times 2^5 \times \left(2^3 + 2\right) \\ &\quad + B_{11} \times 2^5 \times \left(2^2 + 2\right) + B_{10} \times 2^5 \times \left(2 + 2^0\right) \\ &\quad + B_9 \times 2^5 \times 2 + B_8 \times 2^5 \times 2^0 \\ &\quad + B_7 \times 2 \times \left(2^3 + 2^2\right) + B_6 \times 2 \times 2^3 \\ &\quad + B_5 \times 2 \times 2^2 + B_4 \times 2 \times \left(2 + 2^0\right) \\ &\quad + B_3 \times 2 \times 2 + B_2 \times 2 + B_l \times 2 + B_0 \qquad (9) \\ &= 2^{10} \times (B_{15} + B_{14}) + 2^9 \\ &\quad \times (B_{15} + B_{13}) + 2^8 \times (B_{15} + B_{12}) + 2^7 \times B_{11} \\ &\quad + 2^6 \times (B_{12} + B_{11} + B_{10} + B_9) + 2^5 \\ &\quad \times (B_{10} + B_8) + 2^4 \times (B_7 + B_6) \\ &\quad + 2^3 \times (B_7 + B_5) + 2^2 \\ &\quad \times (B_4 + B_3) + 2 \times (B_4 + B_2 + B_l) + B_0 \qquad (10) \end{aligned}$$

16-bit original output digital codes are converted to 12-bit binary codes by the logical operation in Fig. 10. The schematic of digital error correction(DEC) is shown in Fig. 11. The DEC is composed of 12 D-type Flip Flops(DFF) and 11 full-adders(FA). The CLKs is sampling clock from the clock generator in Fig. 11.

Reducing the noise of the comparator requires a lot of power dissipation. The adaptive-tracking-average technique [19] is used to relax requirement for the noise of the comparator. In order to average the comparator noise, the multiple comparison of LSB is used in the adaptive-tracking-average. In Fig.12, seven purple unit capacitors Ca1 to Ca7 are added to the DAC capacitor array to repeat LSB decision

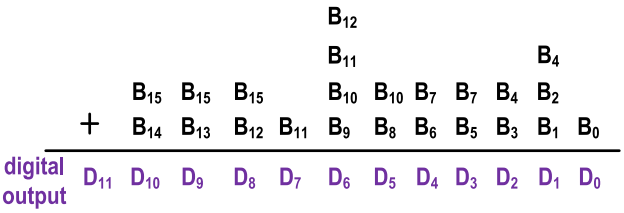

FIGURE 10. Digital error correction logic.

7 times. In order to keep the weighting of the LSB array unchanged, Seven unit capacitors Ca1 to Ca7 are split from the capacitor Cdummy. As a result, the capacitor Cdummy changes from $14C_u$ to $7C_u$. Fig. 12 is the DAC capacitor array with equivalent split-capacitor and the LSB averaging.

B. THE PROPOSED HYBRID CAPACITOR SWITCHING PROCEDURE

The power dissipation of DAC capacitor array accounts for a large proportion among SAR ADC power. The power dissipation of the DAC capacitor array is determined by the switching methods and the total capacitance of DAC capacitor array. The power dissipation produced by different switching procedures varies greatly for the same capacitor array. The conventional switching procedure is not energy-efficient. The monotonic switching procedure [14] can greatly reduce the power consumption. Nevertheless, its common-mode voltage is not constant and changes from half of Vref to the ground in the process of the quantization, which causes the variation of comparator offset voltage and degrades the linearity of the SAR ADC. Compared with the monotonic switching process, the variation of the common mode voltage is reduced by 50% using the bidirectional single-side switching procedure. However, this variation is still relatively large and affects the dynamic offset of the comparator and SNR of SAR ADC.

The hybrid capacitor switching procedure is proposed to reduce the variation of the common mode voltage and the power dissipation of the DAC capacitor array. Fig.13 shows a 4-bit examples of proposed switching process. When ADC is sampling, the MSB capacitors are connected to the Vcm. The MSB-1 capacitors are connected to the ground and other capacitors are connected to the Vref. The input signals Vip and Vin are sampled to top plates of the capacitor array by the bootstrapped switch. After sampling, the comparator makes the first comparison and there is no power consumption in the capacitor array. When the first comparison is finished, the proposed switching process switches the MSB capacitor from Vcm to ground or Vref. After the second comparison, one of the MSB-1 capacitor is switched from ground to Vref. Then, the proposed process switches other capacitors from Vref to ground. The power consumption of each conversion process is shown in Fig. 13.

In the split monotonic switching procedure, the MSB capacitor and MSB-1 capacitor in the DAC capacitor array are connected to the VREF. However, the MSB capacitor is

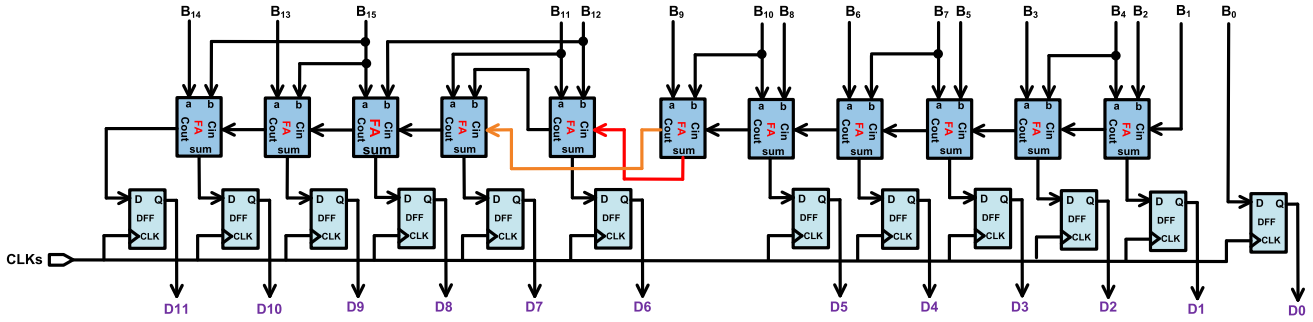

FIGURE 11. Implementation of digital error correction.

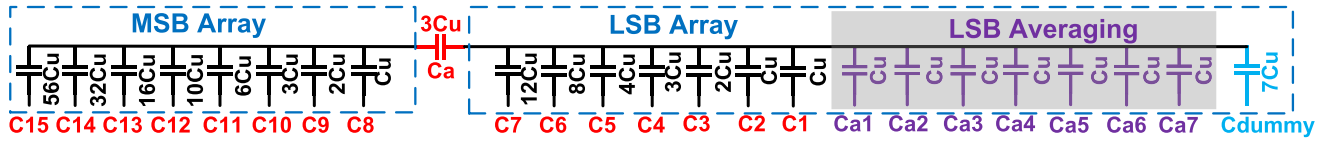

FIGURE 12. The DAC capacitor array with equivalent split-capacitor and the LSB averaging.

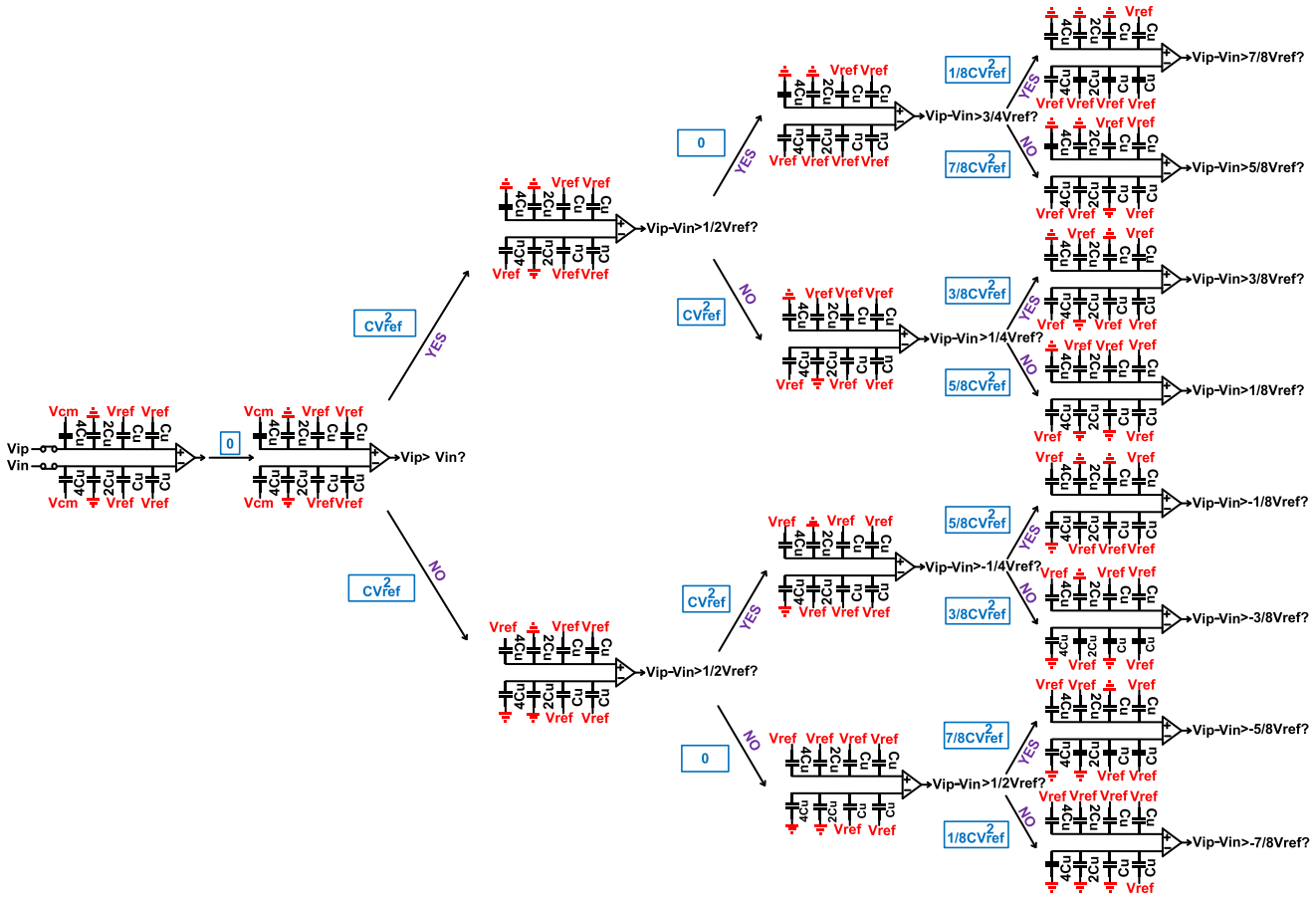

FIGURE 13. The proposed hybrid switching procedure.

connected to Vcm and MSB-1 capacitor is connected to the ground in the proposed hybrid capacitor switching procedure. Due to different connection modes of the MSB and MSB-1 capacitors, the variation of common mode voltage of the proposed switching procedure and the split monotonic switching procedure is different.

For n-bit SAR ADC, Only 2^{n-1} unit capacitors are needed in the proposed hybrid switching process. If probability of

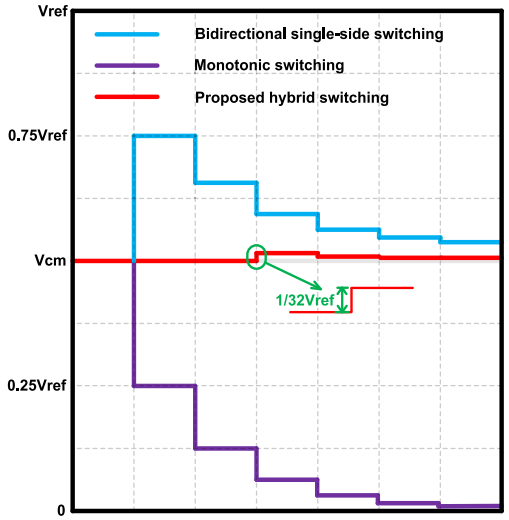

FIGURE 14. Common voltage variation of DAC capacitor array.

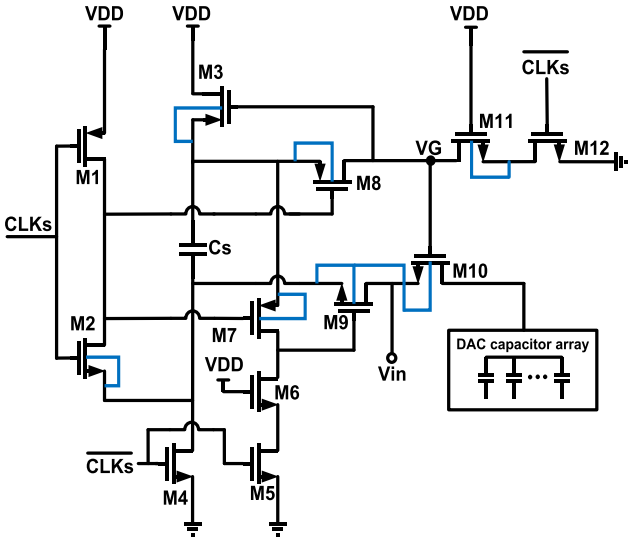

FIGURE 15. Bootstrapped switch.

occurrence of each binary digital output code is equal, the averaging power consumption for the conventional switching process can be expressed as

$$E_{ave,con} = \sum_{i=1}^{n} 2^{n+1-2i}\left(2^{i}-1\right) CV_{ref}^{2} \tag{11}$$

the averaging power consumption for the monotonic switching process can be expressed as

$$E_{ave,mono} = \sum_{i=1}^{n-1}\left(2^{n-2-i}\right) CV_{ref}^{2} \tag{12}$$

the averaging power consumption for the hybrid switching process can be expressed as

$$E_{ave,proposed} = \left(2^{n-4}+2^{n-5}+\sum_{i=4}^{n} 2^{n-1-i}\right) CV_{ref}^{2}, \quad (n \geq 4) \tag{13}$$

For 12-bit SAR ADC, the conventional switching process consumes $5459.33CV_{ref}^{2}$ and the monotonic switching process consumes $1023.5CV_{ref}^{2}$. The proposed hybrid switching procedure consumes $639.5CV_{ref}^{2}$. The power consumption of the proposed hybrid capacitor switching process is 88.2% less than the conventional switching procedure and 37.5% less than the monotonic switching procedure. Table 2 shows power consumption of each output code for 4-bit the DAC capacitor array based on the monotonic capacitor switching process and proposed hybrid capacitor switching process. For 4-bit SAR ADC, the LSB capacitor is not switched after the fourth comparison. Therefore, the power consumption corresponding to the output codes 0000 and 0001 is equal. The same is true for other output codes. The power dissipation corresponding to each binary digital output code of the proposed capacitor switching process is smaller than that of the monotonic capacitor switching process in the table 2.

In Fig. 13, only the MSB capacitor is connected to the Vcm during the sampling. For N(N $\geq$ 6) bit SAR ADC, when SAR ADC is sampling, the MSB, MSB-1 and MSB-2 capacitors are connected to Vcm. The MSB-4 capacitors are connected to ground and other capacitors are connected to Vref. The capacitor switching procedure is same as that in Fig. 13. The common mode voltage variation of DAC capacitor array is shown in Fig. 14. Common mode voltage changes from Vcm to ground in monotonic capacitor switching process. The common mode voltage variation is reduced by 50% and converges to Vcm in the bidirectional switching procedure. Common mode voltage variation is reduced by 93.75% and converges to the Vcm in the proposed switching process. Therefore, it alleviates the need for the special comparator and avoids the degradation of the linearity. In order to avoid Vcm, the MSB, MSB-1 and MSB-2 capacitors are divided into two equal halves. One half is connected to ground and other half is connected to Vref.

The proposed capacitor switching procedure can not only reduce power consumption, but also reduce the variation of common mode voltage.

IV. IMPLEMENTATION OF KEY BUILDING BLOCKS

The fundamental building blocks of the proposed SAR ADC include the bootstrapped switch, the three-stage low-noise comparator, the asynchronous digital control logic, the DAC capacitor array, the reference voltage buffer and the clock generator. The design consideration of these building blocks are described in following subsections.

A. BOOTSTRAPPED SWITCH

The bootstrapped switch is used to sample the input signals to the DAC capacitor array. The performance of the bootstrapped switch will degrade at high frequency. In order to solve this problem, an improved bootstrapped switch is proposed in [21], as shown in Fig. 15. When CLKs is low, transistors M4, M5, M6, M11 and M12 are on, transistors

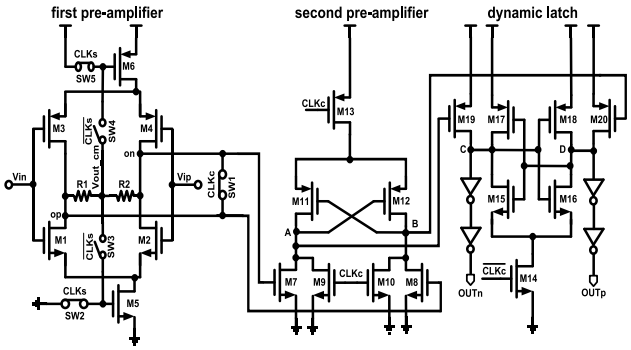

FIGURE 16. A three-stage comparator based on inverter.

TABLE 2. Power consumption of each output code for 4-bit DAC capacitor array.

	proposed hybrid capacitor switching procedure	monotonic capacitor switching procedure [14]
output code	power consumption of each code	power consumption of each code
0000	$9/8CV_{ref}^2$	$21/8CV_{ref}^2$
0001	$9/8CV_{ref}^2$	$21/8CV_{ref}^2$
0010	$15/8CV_{ref}^2$	$27/8CV_{ref}^2$
0011	$15/8CV_{ref}^2$	$27/8CV_{ref}^2$
0100	$19/8CV_{ref}^2$	$31/8CV_{ref}^2$
0101	$19/8CV_{ref}^2$	$31/8CV_{ref}^2$
0110	$21/8CV_{ref}^2$	$33/8CV_{ref}^2$
0111	$21/8CV_{ref}^2$	$33/8CV_{ref}^2$
1000	$21/8CV_{ref}^2$	$33/8CV_{ref}^2$
1001	$21/8CV_{ref}^2$	$33/8CV_{ref}^2$
1010	$19/8CV_{ref}^2$	$31/8CV_{ref}^2$
1011	$19/8CV_{ref}^2$	$31/8CV_{ref}^2$
1100	$15/8CV_{ref}^2$	$27/8CV_{ref}^2$
1101	$15/8CV_{ref}^2$	$27/8CV_{ref}^2$
1110	$9/8CV_{ref}^2$	$21/8CV_{ref}^2$
1111	$9/8CV_{ref}^2$	$21/8CV_{ref}^2$

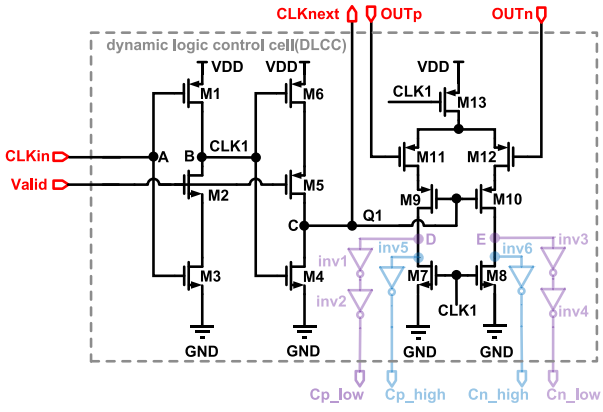

FIGURE 17. Dynamic logic control cell.

M9 and M10 are off, transistor M3 charges capacitor Cs to VDD. At this time, the bootstrapped switch is in the hold state. When sampling clock CLKs is VDD, transis-

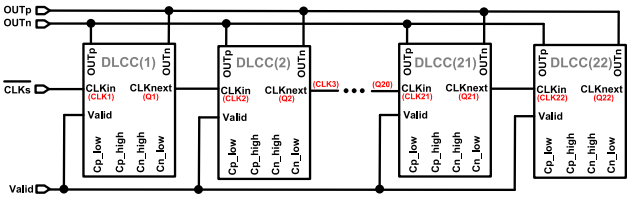

FIGURE 18. Asynchronous dynamic control logic.

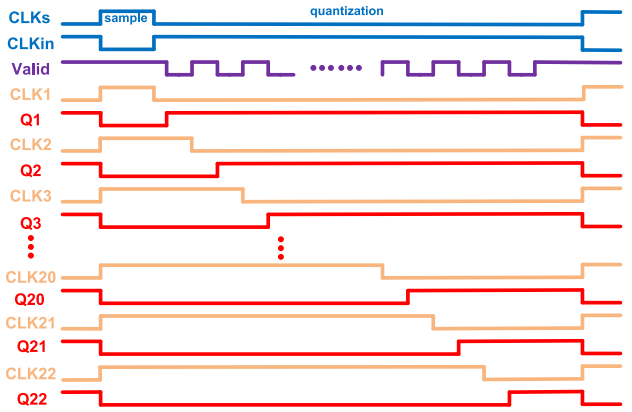

FIGURE 19. Timing of asynchronous dynamic control logic.

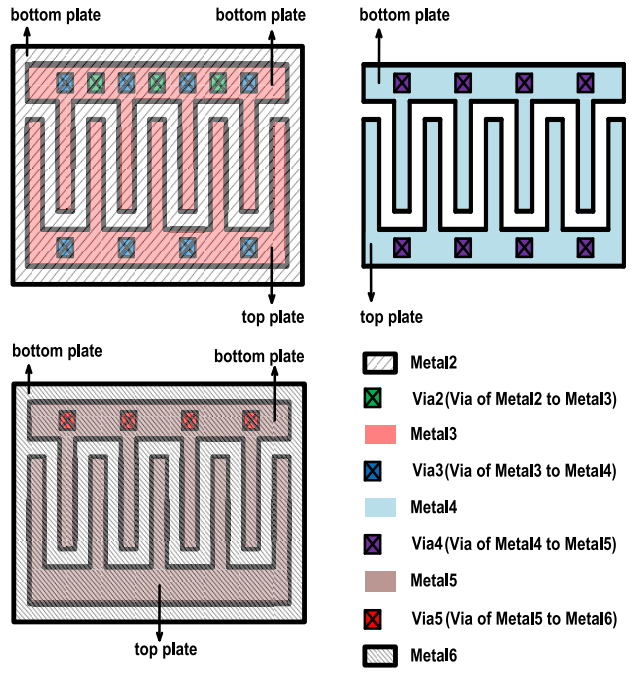

FIGURE 20. The structure of the unit capacitor.

tors M8 and M7 are on, the V_{gs} of the transistor M10 is VDD. At this time, the bootstrapped is in the tracking state.

Compared with the conventional bootstrapped switch [22], the gates of transistors M9 and M10 are not connected together. Transistor M9 is controlled by transistors M7, M6 and M5. As a result, the capacitive load of the node VG is reduced and VG can quickly follow Vin. The bulks of

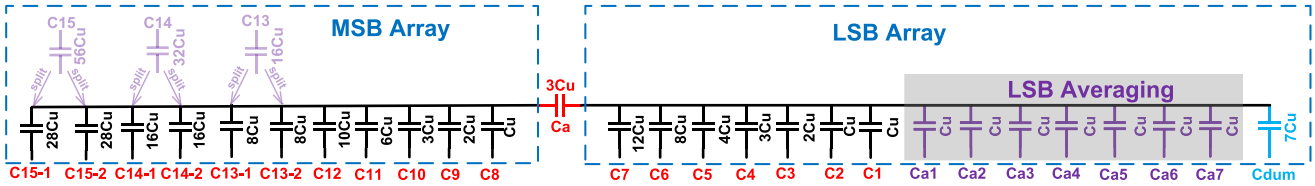

FIGURE 21. The DAC capacitor array.

Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum
Dum	Dum	Dum	C11	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	Dum	Dum	Dum
Dum	Dum	C11	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	Ca	Dum
Dum	C11	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	Ca	C2	Dum
Dum	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	Ca	C7	Ca1	Dum
Dum	C10	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	C12	C7	C6	Ca2	Dum
Dum	C15-1	C10	C15-1	C15-2	C14-1	C14-2	C12	C7	C6	Ca4	Ca3	Dum
Dum	C10	C15-1	C15-2	C14-1	C14-2	C12	C7	C6	Cdummy	Dum	Dum	Dum
Dum	C15-1	C15-2	C14-1	C14-2	C12	C7	C6	C5	Cdummy	Dum	Dum	Dum
Dum	C15-2	C14-1	C14-2	C12	C7	C6	C5	C3	Cdummy	Dum	Dum	Dum
Dum	C15-2	C14-1	C14-2	C12	C7	C6	C5	C3	Cdummy	Dum	Dum	Dum
Dum	C15-1	C15-2	C14-1	C14-2	C12	C7	C6	C5	Cdummy	Dum	Dum	Dum
Dum	C9	C15-1	C15-2	C14-1	C14-2	C12	C7	C6	Cdummy	Dum	Dum	Dum
Dum	C15-1	C9	C15-1	C15-2	C14-1	C14-2	C12	C7	Cdummy	Dum	Dum	Dum
Dum	C8	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	C12	C7	Ca5	Ca6	Dum
Dum	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	C4	C7	Ca7	Dum
Dum	C11	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	C4	C1	Dum
Dum	Dum	C11	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	C14-1	C14-2	C4	Dum
Dum	Dum	Dum	C11	C13-1	C13-2	C15-1	C15-2	C15-1	C15-2	Dum	Dum	Dum
Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum	Dum

FIGURE 22. The layout floorplan of DAC capacitor array.

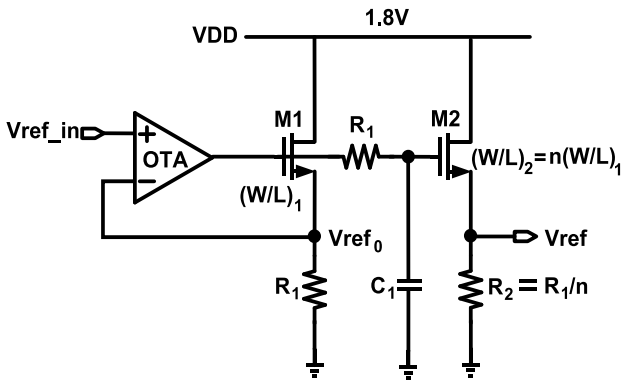

FIGURE 23. Topology of reference voltage buffer.

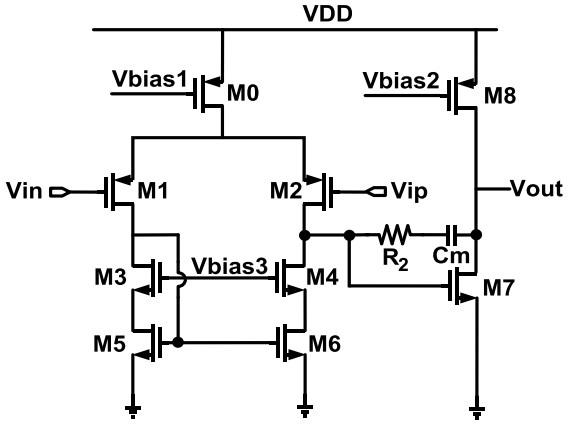

FIGURE 24. Schematic of OTA.

transistors M7, M8, M9 and M3 in critical loops are tied to their sources to avoid body effect and reduce on-resistance. The bulk of the transistor M10 is tied to the bottom-plate of Cs. In the tracking state, the bulk and source of transistor M10 are connected together because transistor M10 is on. In hold state, the bulk of transistor M10 is connected to ground rather than input signal, which does not require a dummy transistor of M10 to eliminate input signal feedback in [11].

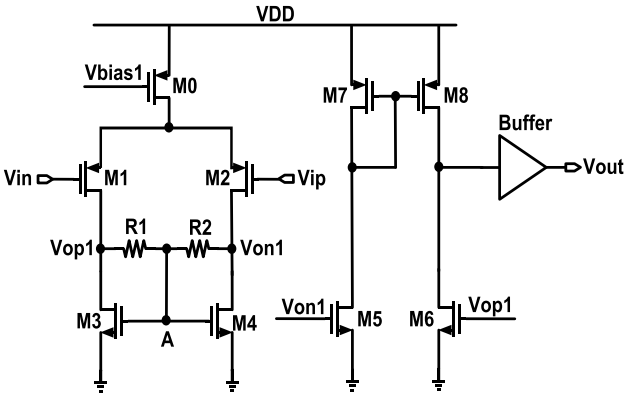

FIGURE 25. Clock generator circuit.

B. A THREE-STAGE COMPARATOR

The comparator has a great influence on the performance of SAR ADC. The noise of comparator affects the SNR of the SAR ADC. However, the tradeoff between the noise and power dissipation is not linear. The resolving time of comparator affects the speed of the ADC. Fig. 16 shows a multistage comparator with the inverter [8], which can aachieve low noise and high speed. The first stage is the inverter with common mode voltage feedback, which can achieve high gain and suppress the noise and offset. The second stage is half latch, which can further amplify the signal. The third stage is the dynamic latch, which affects the resolving time of the comparator. Resistors R1 and R2 sense output voltage Vout_cm to control transistors M5 and M6, which can stabilize output common mode voltage. When ADC is sampling, CLKs is high and transistors M6 and M5 are off. As a result, the first stage does not work, which can save power dissipation. When CLKs is ground and CLKc is VDD, transistors M13 and M14 are off, transistors MS1 and MS2 are on, the nodes M and N are low. Transistors MS3 and MS4 are on, the nodes P and Q are high. At this time, the comparator are in reset state. When CLKs is low and CLKc is low, transistors M13 and M14 are on, the first stage compares the input differential signals Vin and Vip. The second stage forces one of the nodes M and N to be high and the other to be low. Transistors MS3 and MS4 in the third stage amplify outputs of the second pre-amplifier to the dynamic latch in the third stage, which forces one of nodes P and Q to be low and other to be high. The noise of the three-stage comparator based on the differential inverters is 56 uv(rms) by the spectre transient simulation.

C. ASYNCHRONOUS DYNAMIC CONTROL LOGIC

In order to save the power dissipation and improve the speed, asynchronous dynamic control logic is used. Fig. 17 shows the dynamic logic control cell(DLCC). OUTn and OUTp represent results of compariosn. Valid indicates the state of the comparator. CLKs is sampling clock and CLKin is the inverse of the CLKs. When Valid is VDD and CLKin is ground, transistor M1 is on, node B is VDD. Transistors

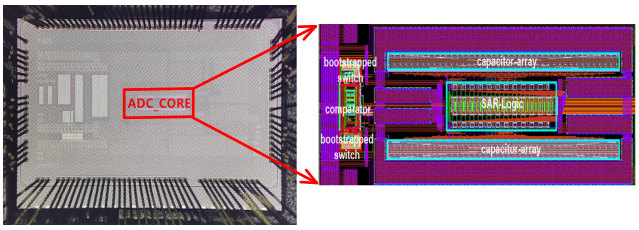

FIGURE 26. Chip photograph and layout zoomed-in view of SAR ADC.

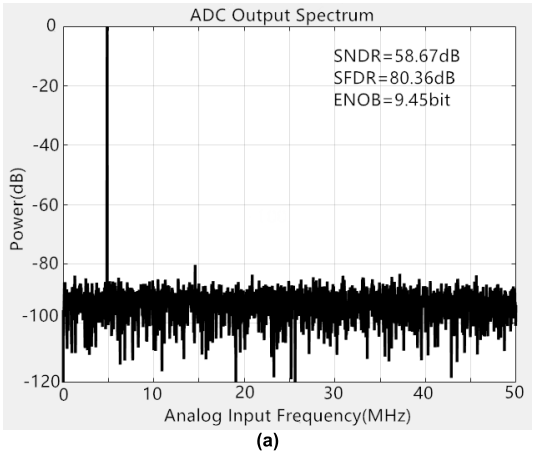

FIGURE 27. Measured spectrum at Fin = 4.85MHz (a) and 49.85MHz (b) with Fs = 100MS/s when LSB averaging is not carried out.

M5 and M6 are off, transistor M4 discharges the node C to ground. Transistor M13 is off and transistors M7 and M8 are on, the nodes D and E are ground. Sp_low and Sn_low are low, Sp_high and Sn_high are high. Sp_low, Sn_low, Sp_high and Sn_high are connected to the bottom plates of differential the capacitor array. When ADC is sampling, bottom plates of MSB-3 capacitors and the halves of MSB, MSB-1 and MSB-2 capacitors are connected to Sn_low and Sp_low. Bottom plates of the other halves of MSB, MSB-1 and MSB-2 and other capacitors are connected to Sp_high and Sn_high. After sampling, the comparator starts comparing input signals. At this time, Valid is VDD and CLKs is ground. Transistors M2 and M3 are on, the node B are ground. Transistor M13 turns on and transistors M9 and M10

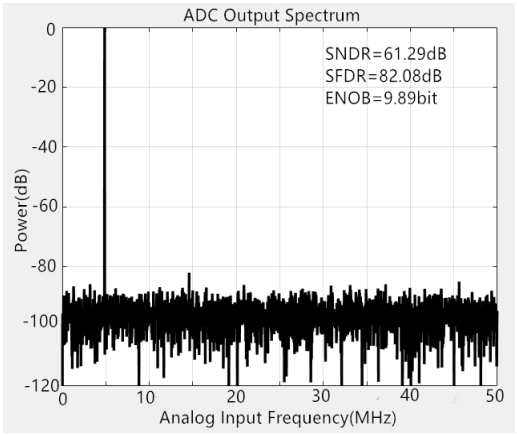

FIGURE 28. Measured spectrum at Fin = 4.85MHz (a) and 49.85MHz (b) with Fs = 100MS/s when LSB averaging is carried out.

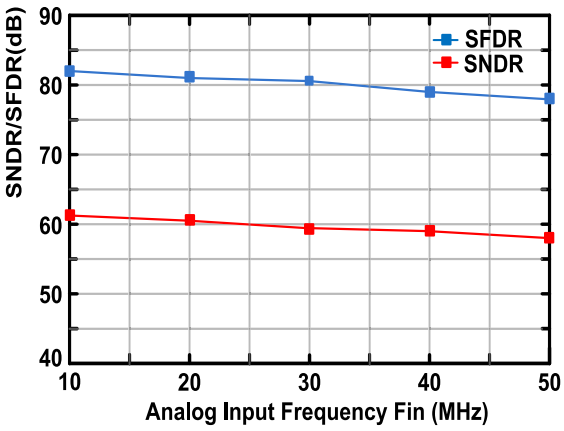

FIGURE 29. Measured SNDR and SFDR versus analog input frequency Fin when Fs = 100MS/s.

are also on. One of the transistors M11 and M12 is off and other is on depending on OUTn and OUTp. Therefore, one of the nodes D and E is low and the other is high. DAC capacitor array starts settling during this period. After that, Valid becomes low and transistor M5 charges the node C to VDD. As a result, transistors M9 and M10 turn off and the voltage of the nodes D and E keeps unchanged. Next, the comparator makes second comparison until the LSB is determined. Asynchronous dynamic control logic is shown as Fig. 18 and timing of asynchronous dynamic control logic is shown as Fig. 19.

D. CAPACITOR ARRAY

The Metal-Oxide-Metal(MOM) capacitor is selected as the unit capacitor of DAC capacitor array. Fig. 20 shows the structure of the unit capacitor, which is composed of 5layers of metal from Metal2 to Metal6. The Metal3 to Metal5 layers are interdigital capacitors. The Metal3 layer capacitor and Metal4 layer capacitor are connected by Via3. The Metal4 layer capacitor and Metal5 layer capacitor are connected by Via4. The bottom plate of Metal3 layer capacitor and Metal2 are connected by Via2. The bottom plate of Metal5 layer capacitor and Metal6 are connected by Via5. Metal2 and Metal6 layers are flat plates, which are used as the bottom plate of the unit capacitor. Besides, Metal2 and Metal6 can shield influence of surrounding parasitism on the unit capacitor. The value of the unit capacitor is 6.8fF based on standard parasitic extraction tool. The active area of the unit capacitor is 1.96um $\times$1.198um. Total capacitance of differential DAC capacitor arrays is about 1.75pF. Fig. 21 shows the DAC capacitor array. The number of unit capacitors in DAC capacitor array is not integer power exponent of 2. Besides, there is a bridge capacitor Ca in the capacitor array. The layout floorplan of DAC capacitor array in Fig. 22 is proposed to achieve good matching of DAC capacitor array. The purple DUM represents dummy capacitors in Fig. 22.

E. REFERENCE VOLTAGE BUFFER

Reference voltage buffer(RVB) provides the reference voltage for DAC capacitor arrays. When off-chip RVB is used, there is parasitic inductance of bonding wires, traces of PCB and mutual inductance, which will cause the ringing of the reference voltage and degrade the DAC settling. In order to stabilize the reference voltage within 0.5LSB, much time needs to be allocated to DAC capacitor arrays to settle, which reduces the speed of the ADC. A large decouple capacitor can reduce the ringing of the reference voltage. However, it occupies a lot of area. On-chip RVB can reduce the ringing of the reference voltage. Fig. 23 shows the schematic of RVB. The proposed redundant method in this paper can reduce demand for RVB bandwidth. Two replica source followers are used in Fig. 23. The (W/L)2 of transistor M2 is n times (W/L)1 of the transistor M1 and resistance of resistor R1 is n times resistance of resistor R2. Therefore, Vref is equal to Vref0 in the static state. In order to eliminate bulk-effect, the sources of transistors M1 and M2 are connected to their respective bulks. The open-loop source follower has small output impedance, which is beneficial to accelerate the DAC settling. The output impedance of source follower is $(1/g_{m2})//R_2$. Resistor R_1 and capacitor C_1 forms a low pass filter to isolate kickback noise from the ADC. The Vref_in is equal to 0.8V. The supply voltage VDD is 1.8V.

TABLE 3. Performance summary and comparison.

		This work	[11]	[20]	[24]	[25]	[26]
Architecture		SAR	SAR	SAR	SAR	SAR	SAR
CMOS Techcnology		14nm	20nm	65nm	65nm	40nm	40nm
Resolution(bits)		12	10	12	11	12	12
Supply Voltage(V)		0.8	1	1.2	1.2	0.9	1
Sampling Rates(MS/s)		100	320	100	100	150	120
SNDR(dB)	@LF	61.29	57.1	63.18	60	61.7	60.33
	@Nyquist	58.34	50.9	55.01	58.82	56.2	58.1
SFDR(dB)	@LF	82.08	78.1	81.17	74	74.4	72.9
	@Nyquist	78.02	58.6	75.33	74.61	63.5	72
ENOB(bits)	@LF	9.89	9.2	10.2	9.67	9.95	9.72
	@Nyquist	9.40	8.16	8.8	9.51	9.0	9.35
Power(mW)		0.78	1.52	0.8	1.6	1.5	1.9
FoM (fJ/conv-step)	@LF	8.2	8.1	6.94	19.2	10.3	18.7
	@Nyquist	11.15	16.5	17.6	21.9	18.5	24.26
Reference Buffer Included?		NO*	NO*	NO	NO	NO	NO

* Reference Buffer is realized on chip, but power is not included in the calculation.

OTA in Fig. 23 is a two-stage amplifier. Fig. 24 shows the schematic of OTA. The first stage is differential amplifier with current mirror load. The second stage is common-source amplifier. When $R_2 > 1/g_{m7}$, the resistor R_2 and the capacitor C_m form a left plane zero($1/(R_2C_m)$), which can compensate phase margin(PM) and reduce power consumption. Generally, $1/(3g_{m1}) > R_2 > 1/g_{m7}$.

F. CLOCK GENERATOR

Clock generator is used to provide the sampling clock for ADC. The clock jitter has a great impact on the performance of ADC. The larger clock jitter is, that is, the higher uncertainty of the sampling time. For sinusoidal signal of $V_{in} = A\cos(2\pi f_{in})$, the clock jitter power is given by:

$$P_{jitter} = \frac{A^2}{2}\left(2\pi f_{in}\sigma_{jitter}\right)^2 \tag{14}$$

where, σ_{jitter} is root-mean-square jitter.

Clock generator with low clock jitter is very beneficial to high-resolution ADC. Fig. 25 shows low clock jitter circuit [23], which consists of three stages. The first stage is differential amplifier with active load, which can suppress the common-mode noise. Resistors R1 and R2 form common-mode feedback circuit, which provides appropriate static working point for the node A and stabilize voltage at the node A. The second stage is differential-to-single-ended conversion, which has a large impact on the clock edge slope and clock jitter. The third stage is digital buffer, which is used to generate square wave. The digital buffer needs to have large gain and produce noise as less as possible. The clock jitter of the clock generator is 140fs by simulation.

V. MEASURMENT RESULTS

The prototype SAR ADC is fabricated using 1P8M 14-nm CMOS FinFET technology. Fig. 26 shows the chip photograph and the layout zoomed-in view of the SAR ADC core occupies an active area of $0.112mm^2$.

Fig. 27 shows the measured spectrum with inputs at 4.85MHz and 49.85MHz with 100MS/s Fs when LSB averaging is not carried out. At Fin = 4.85MHz, the measured SNDR and SFDR are 58.67dB and 80.36dB, respectively. When input frequency increases to 49.85MHz, the measured SNDR and SFDR are 56.01dB and 76.5dB. Fig. 28 shows the measured spectrum with inputs at 4.85MHz and 49.85MHz with 100MS/s Fs when LSB averaging is carried out. At Fin = 4.85MHz, the measured the SNDR and SFDR are 61.29dB and 82.08dB. When input frequency increases to 49.85MHz, the measured the SNDR and SFDR are 58.34dB and 78.02dB. At Fin = 4.85MHz, SNDR, SFDR and ENOB are increased by 2.62dB, 1.72dB and 0.44bit respectively. At Fin = 49.85MHz, SNDR, SFDR and ENOB are increased by 2.33dB, 1.52dB and 0.39bit, respectively. Through comparison between Fig. 27 and Fig. 28, the LSB averaging is helpful to improve the ENOB.

Fig. 29 shows the measured SNDR and SFDR versus analog input frequency Fin when Fs = 100MS/s.

The power consumption of ADC is 0.78mW including comparator, bootstrapped switch, DAC capacitor array and digital control logic. This power consumption does not include the power consumption of the reference voltage buffer and the clock generator. The proposed SAR ADC achieved a figure-of-merit(FOM) of 8.2 and 11.15 fJ/conversion-step at low-frequency input and Nyquist input frequency, respectively. Table.3 summaries the performance and compares our work with recent arts, the proposed SAR ADC has reached the level of the research front. Besides, the FoM of the proposed SAR ADC at Nyquist is lowest among ADCs [11], [20], [24]–[26].

VI. CONCLUSION

A 12-bit 100MS/s SAR ADC with the clock generator and on-chip reference voltage buffer is presented in this paper. In order to enlarge the redundancy range and alleviate settling error of bridge DAC capacitor array, an equivalent bridge-capacitor is proposed. A hybrid capacitor switching procedure is adopted to reduce power dissipation and the variation of input common-mode voltage of the comparator. Fabricated in 14nm CMOS FinFET technology, the proposed SAR ADC consumes the 0.78mW. The ADC achieves a SNDR of 61.29dB and 58.34dB at low and Nyquist input frequency, respectively, resulting in FoMs of 8.2 and 11.15fJ/convesion step, respectively.

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