IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 27, 2021, accepted December 5, 2021, date of publication December 10, 2021,
date of current version December 21, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3134282

On the Design of 7/9-Rate Sparse Code for Spin-Torque Transfer Magnetic Random Access Memory

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This research is funded by Vietnam National Foundation for Science and Technology Development (NAFOSTED) under grant number 102.04-2019.307.

ABSTRACT A design of 7/9-rate sparse code for spin-torque transfer magnetic random access memory (STT-MRAM) is proposed in this work. The STT-MRAM using spin-polarized current through magnetic tunnel junction (MTJ) to write data is one of the most promising candidates for the next-generation nonvolatile memory technologies in consumer and data center applications. The proposed code is designed to exploit the asymmetric write failure feature of the STT-MRAM. In particular, 7-bit user-data sequences incoming the encoder is encoded into 9-bit codewords, where the Hamming weights of the codewords are equal to 2 and 4 only. A single look-up table accomplishes encoding, whereas the maximum likelihood decoding is deployed in this work. Simulation results demonstrate that the designed code can provide significant improvements for the reliability of STT-MRAM under the effect of both write and read errors.

INDEX TERMS Nonvolatile RAM, spin-torque transfer magnetic random access memory (STT-MRAM), sparse codes, asymmetric write error rate.

I. INTRODUCTION

Memory is one of the essential blocks for all consumer devices. The memories occupying nearly all of the silicon area in system-on-chips consume a significant power of the system [1]. One of the best solutions to energy consumption issues is replacing volatile memory with nonvolatile memory (NVM) [2]. Recently, nonvolatile memories have been widely used in consumer electronics such as smartphones, automotive devices, IoT devices, and AI-aided systems. With fascinating features such as high density, low power consumption, and suitable portable device, the NAND flash memory is dominant in the current NVM market [3], [4]. Emerging memory technologies such as magnetic random access memory (MRAM), resistive random access memory (ReRAM) are expected to replace the conventional memories for the consumer as well as data center applications [5]. Spintronics is also one of the most exciting topics in today's nanotechnology. Spin-torque transfer magnetic random access memory (STT-MRAM) using spin-polarized current through magnetic tunnel junction (MTJ) to write data is regarded as the most promising candidate for the next generation of NVM technologies. Because of its main characteristics of nonvolatility, nanosecond write/read speeds with low latency, endurance, and reliability, STT-MRAM is very useful in many applications. Significantly, the STT-MRAM is expected to replace both static RAM (SRAM) and dynamic RAM (DRAM) that are commonly used for the cache memories and CPU main memory, respectively [5]. Moreover, the MRAM technology provides lower power consumption, higher write/read speeds, better reliability, and longer endurance than Flash memory technology. As a result, it is also definitively recognized as an attractive candidate for dominating the NVM market instead of the Flash memory.

As mentioned above, STT-MRAM devices provide various fascinating advantages to becoming the best dominating NVM market. However, they also face several major technical challenges like any other kind of established memory. Some central issues that significantly degrade the STT-MRAM performance can be briefly addressed [1].

The variations of the MTJ storage element in its geometry and resistance are to change the access process of the

The associate editor coordinating the review of this manuscript and approving it for publication was Zesong Fei.

STT-MRAM. This issue is often referred to as the impact of process variations. It is the leading cause of MTJ conductance and switching threshold current deviations.

The reliability of STT-MRAM is also related to synchronization. For synchronous designs, the write time is usually a fixed value and could lead to some memory cells not finishing the state transitions during the fixed given wire time.

The MTJ resistance may be switched without memory access because the thermal fluctuation increases the randomness for switching in STT MRAM further. Last but not least, an accidental switching of MTJ during the read operation results in a read disturbance. All of the disturbances lead to both the write error and the read error. Moreover, any imperfect manufacturing also degrades significant performance. It is straightforward to note that the severity of these effects will be exacerbated with scaling.

Advanced channel coding and signal processing techniques are the primary approaches to improving system performance and overcoming the above-posted challenges. The increasing demands for ultra-high-density information storage systems and the continuously dropping price for digital integrated circuits (ICs) have motivated sophisticated digital signal processing and coding techniques to the information storage systems. Several novel schemes for the next-generation data storage proposed in [6]–[8] can be applied to STT-MRAM with some modification. The bulk of this study is for advanced channel coding schemes.

Channel codes in data storage devices can be categorized into constrained coding, error-correction coding (ECC), and error-correction constrained coding. Several novel constrained codes are proposed, i.e., novel RLL and spectrum shaping codes, for data transmission and recording with reasonable encoding and decoding complexity but a high code rate [9]–[12]. These suggested code's primary purpose is to shape the user data to strengthen it to be less prone to errors and better support for the synchronization. For the ECC codes, an overview of error correction for Flash was summarized in [13]. A typical 4/6 error-correction constrained code to mitigate the effect of intertrack-interference for bit-patterned recording systems was also presented in [14]. Moreover, 64/71-rate regular Hamming code and 64/72-rate extended Hamming codes were suggested for STT-MRAM [15], [16].

The implementation of ECC codes can significantly increase the computational complexity of the system. Moreover, as reported in [17], the conventional ECCs, such as Hamming and BCH code, offer the same error-correcting capability for both bit-flipping directions. As a result, the codes may not be the best option to handle the asymmetric errors. In this study, a 7/9-rate spare code belonging to the class of constrained code is proposed to overcome the errors in STT-MRAM. The motivation of this work comes from the asymmetry of the write error rate in STT-MRAM. Without loss of generality, we herein denote the low resistance state (LRS) and a high resistance state (HRS) as logical values of "0" and "1", respectively. This issue can be described as the wire error rate for $0 \rightarrow 1$ switchings being much higher than that for $1 \rightarrow 0$. In other words, the number of 0 to 1 transitions and 1 to 0 transitions mainly affects the reliability of the write operation. By exploiting the feature, we are interested in designing a new 7/9-rate sparse code with a very simple encoder and decoder to improve the reliability of STT-MRAM. The proposed code reduces the number of "1", i.e., reducing $0 \rightarrow 1$ switching, in the incoming data. In particular, 7-bit user-data sequences incoming the encoder is encoded into 9-bit codewords, where the Hamming weights of the codewords are equal to 2 and 4 only. This technique is always to ensure that the weight of the output codewords is always less than half of the codeword length. As a result, the encoder output data is sparse, and the write failure rate can be eliminated significantly.

The remainder of this paper is organized as follows. Section II presents the STT-MRAM channel model as a communication channel that incorporates both the wire errors and read errors. The preliminary sparse codes and the proposed code are analyzed and presented in Section III. Simulation results and discussion are shown in Section IV. Finally, the concluding remarks are shown in Section V.

II. CHANNEL MODEL FOR STT-MRAM

A. STT-MRAM STORAGE TECHNOLOGY

An STT-MRAM device includes two main elements of an MTJ and an nMOS transistor. The nMOS serves as the access control part, whereas the MTJ, the basic block of MRAM devices, is used as the storage one. Fig. 1 illustrates typical structures of the MTJ. As can be seen that the MTJ consists of two ferromagnetic layers and one ultrathin tunneling oxide layer. One of the ferromagnetic layers with a fixed orientation is a reference layer. The other layer whose magnetization can be changed is generally referred to as a free layer. The data stored in the MTJ cell depends on the relative magnetization state of the ferromagnetic layers. If the magnetization directions between the reference layer and free layer are antiparallel (AP), the MTJ is in a high resistance state to representing a bit logic of "1." Otherwise, the magnetization directions are parallel (P), the MTJ is in a low resistance state to representing a bit logic of "0." Fig. 2 illustrates a typical STT-MRAM cell structure of one-transistor-one-MTJ (1T1J) and its switching.

A passing current through the MTJ is needed for write and read operations. In particular, if the bit line (BL) and word line (WL) are fed to the supply voltage while the source line (SL) is grounded, the current goes from the free layer to the reference layer for writing 0. In the reversed case, if the BL is grounded while the WL and SL are fed to the supply, the current is reversed for writing 1. For a read operation, the access transistor is first to turn on. A relatively small read current in the same direction as the write current is passed through the MTJ. The resulting voltage is compared with a

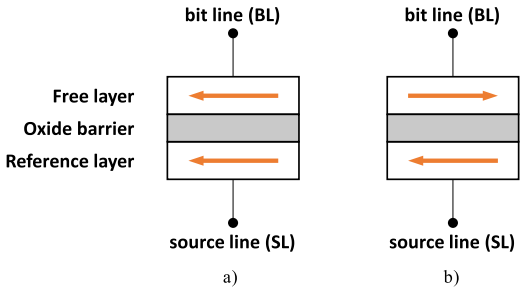

FIGURE 1. MTJ. a) Parallel magnetization representing a bit logic of "0." b) Antiparallel magnetization representing a bit logic of "1."

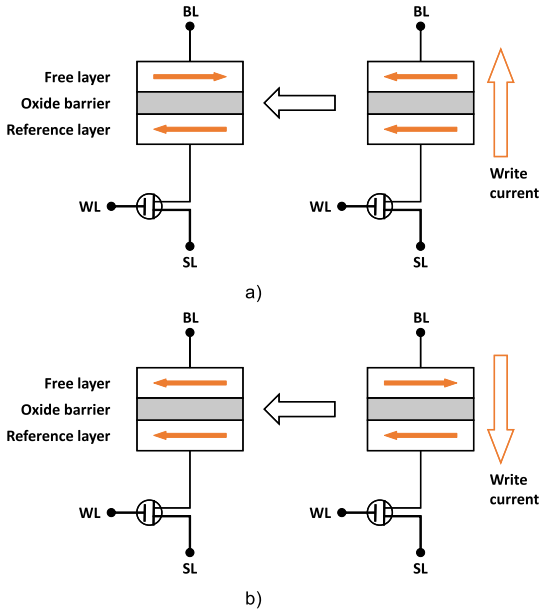

FIGURE 2. 1T1J. a) 0 to 1 transition. b) 1 to 0 transition.

reference voltage value to determine the current logic level stored in the MTJ.

B. RELIABILITY OF WRITING AND READING OPERATIONS FOR STT-MRAM

As mentioned above, the data reliability of STT-MRAM is degraded significantly by the failures of read and write operations. A write error occurs if the switching current is not enough as the required switching current before the MTJ switching completes. This leads to the memory cells fail in $0 \rightarrow 1$ switchings or $1 \rightarrow 0$ switchings. The primary causes of this issue come from the impacts of inherent thermal fluctuations and process variations. It is also reported that the write failure is asymmetric [18]. The failure probability of $0 \rightarrow 1$ switchings is much higher than that of $1 \rightarrow 0$ switchings. In particular, the transition of 0 to 1 requires a longer write pulse (a larger current) than that of 1 to 0. This means that the uncertainty of the write pulse of transition 0 to 1 is more prominent than that of transition 1 to 0. As a result, the failure probability of $0 \rightarrow 1$ switching is higher than that of $1 \rightarrow 0$ switching. It is also important to note that the write operations are accomplished by passing a current through an STT-RAM cell, and the write currents are the reverse of each other, corresponding to writing a "0" or a "1". The switching current while writing a "1" is lower than writing a "0". This write error failure asymmetry is further aggravated under the process variations and different biasing conditions. The asymmetric wire failure is the primary contributor to wire errors in STT-MRAM.

The read errors of STT-MRAM can be categorized into two types: read decision errors and read disturb errors. The read decision error means the failure of sensing the memory cell resistance during the reading. The read disturb errors occur the reading accidentally disturbs the memory content due to an undesirable large current. Moreover, it is interesting to note that since the read current can only be set to either the write-0 direction or the write-1 direction, the read disturb error is only in one order. That means, for instance, if the read current is turned on in the write-0 direction, then the erroneous $1 \rightarrow 0$ switching can happen only. In the other case of turning on the read current in the write-1 direction, the erroneous $0 \rightarrow 1$ switching is prone to the read disturb error. These disturbing errors can be lowered by lowering the read current. Yet, the reliability of sensing with small read currents can increase the read decision errors. Therefore, the value of read current needs to be selected appropriately.

C. CASCADED CHANNEL MODEL

To facilitate the implementation of signal processing techniques, a model channel of STT-MRAM is essential. A good channel model can describe the characteristics of the medium and the effects degrading the system performance. Some of such works have been introduced in [16], [19]. In this work, we adopt the STT-RAM cascaded channel model suggested by Cai and Immink [16]. The channel model is briefly addressed as follows.

Let P_1, P_0, and P_r denote the write error rate for $0 \rightarrow 1$ switching, the write error rate for $1 \rightarrow 0$ switching, and the read disturb error rate, respectively. As presented above, the write and read failure rates are the leading cause to degrade the system performance. The cascaded channel model is a combination of write error and read error models for the system under consideration. In particular, a binary asymmetric channel (BAC) is used to describe the write error. The error probabilities for $0 \rightarrow 1$ and $1 \rightarrow 0$ of the BAC are given by $P_0/2$ and $P_1/2$, respectively. The read disturb error is modeled as a $\mathbf{Z}$ channel. Finally, the read decision error is modeled by a Gaussian mixture channel (GMC). A Gaussian variable R_0 given its mean and variance of μ_0 and σ_0 is represented for low resistance. A Gaussian variable R_1 given its mean and variance of μ_1 and σ_1 has represented a high resistance, respectively. Fig. 3 shows the block diagram of the cascaded channel model with write-0 and write-1 directions. The signal $\boldsymbol{c}$ is first passed through the wire error model BAC, then the read disturb error model $\mathbf{Z}$, and finally, the GMC model. Moreover, to simplify the model, we can further

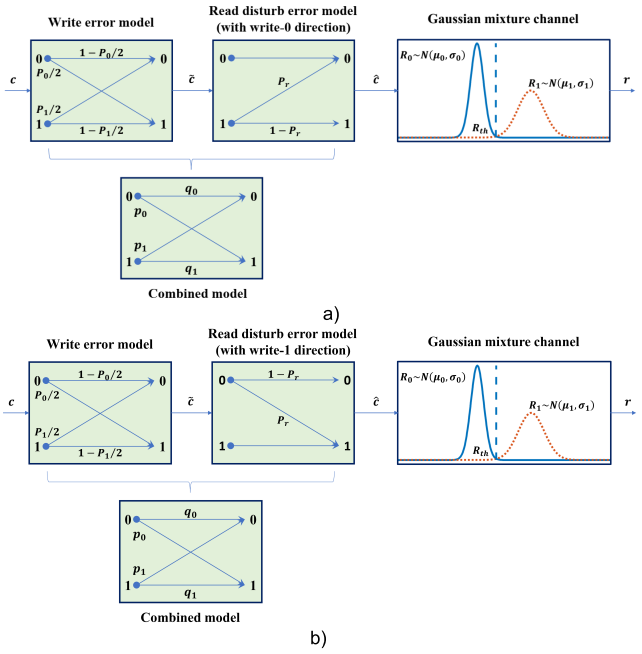

FIGURE 3. Cascaded STT-MRAM model. a) Reading with write-0 direction. b) Reading with write-1 direction.

combine the BAC and **Z** channels. The crossover probabilities after combination can be expressed as follows,

For the case of write-0,

$$p_0 = \frac{P_0}{2}(1-P_r); \quad p_1 = \frac{P_1}{2} + \left(1-\frac{P_1}{2}\right)P_r$$
$$q_0 = \left(1-\frac{P_0}{2}\right) + \frac{P_0}{2}P_r; \quad q_1 = \left(1-\frac{P_1}{2}\right)(1-P_r) \quad (1)$$

For the case of write-1,

$$p_0 = \frac{P_0}{2} + \left(1-\frac{P_0}{2}\right)P_r; \quad p_1 = \frac{P_1}{2} + (1-P_r)$$
$$q_0 = \left(1-\frac{P_0}{2}\right)(1-P_r); \quad q_1 = \left(1-\frac{P_1}{2}\right) + \frac{P_1}{2}P_r \quad (2)$$

III. PROPOSED SPARSE CODES FOR STT-MRAM

A. PRELIMINARIES

Based on the above analysis, asymmetry is the main feature of the write failure rate in STT-MRAM systems. The failure probability of $0 \rightarrow 1$ switching P_1 is much higher than that of $1 \rightarrow 0$ switching P_0. In other words, higher amplitude and latency of write current, hence a higher bit error rate (BER), is needed to write logic "1", compared to write logic "0." As a result, the more the number of $0 \rightarrow 1$ switchings, the higher BER is.

Constrained (modulation) codes have been used in commercial data storage systems for a long time [13]. These codes have an essential role in preventing interference and supporting system synchronization. Significantly, the constrained codes are also helpful when dealing with intercell coupling for the NVM devices. Recently, a series of advanced constrained codes have been proposed for the next-generation high-density data storage systems. As mentioned in [9], [10], the authors recommend spectral shaping codes with a wide frequency range of suppressed power density for better coding designs for digital consumer electronics products.

The sparse codes are regarded as a subclass of the constrained code. The sparse encoding schemes change the distribution of logic "1" and "0" to make logic bit "0" more predominant at the output of the encoder. The capacity-approaching spares codes have been recently proposed for the ReRAM devices [12]. Moreover, the codes are also valuable for reducing inter-page interference for the holographic storage.

Under the asymmetric write failure rate of STT-MRAM, leveraging the sparse coding scheme to reduce $0 \rightarrow 1$ switchings is a very potential approach.

In this study, we are interested in designing a 7/9-rate spare code for STT-MRAM. The 7-bits user data sequences are encoded into 9-bits codewords such that the weight of the output codewords is always smaller than or equal to 4.

B. ENCODING AND DECODING OF THE PROPOSED CODE

In particular, let us consider a binary sequence of length n with its weight w. There are precise $\binom{n}{w}$ sequences with the weight of w. The sparse encoding is to generate the output codeword of the encoder with its weight $w < \lfloor \frac{n}{2} \rfloor$. As a consequence, there are total S sequences with the weight of at most $\lfloor \frac{n}{2} \rfloor$,

$$S = \sum_{w=0}^{\lfloor \frac{n}{2} \rfloor} \binom{n}{w} \quad (3)$$

For the proposed code, there are 256 such sequences, i.e.,

$$S = \sum_{w=0}^{\lfloor \frac{n}{2} \rfloor} \binom{n}{w} = \sum_{w=0}^{4} \binom{9}{w} = \binom{9}{0} + \binom{9}{1} + \binom{9}{2} + \binom{9}{3} + \binom{9}{4}$$

It is possible to use $\log\left(\sum_{w=0}^{4}\binom{9}{w}\right)$ bits to represent the whole of these sequences. In other words, the 256 sequences are good enough to construct an 8/9-rate sparse code for STT-MRAM. On the other hand, it is straightforward to note that the Hamming distance of the 8/9-rate code equals 1. To increase the noise margin of the system and aid the decoding performance, we proceed to selectively select the appropriate set of codewords, hereafter referred to as a codebook S_w. In particular, the codebook only includes the sequences of the weight of 2 and 4. All codewords with the weight of 2 are in the codebook, i.e., there are $36 = \binom{9}{2}$ such sequences. To get the 128 codewords for the target of constructing the 7/9-rate sparse code, the remaining codewords are taken from the codeword set of the weight of 4.

FIGURE 4. Block diagram of the system.

The 128 selected codewords of the codebook S_w are shown in Table 1.

User data is encoded into the sparse codewords using a single look-up table (LUT) of size $128 = 2^7$. As shown in Table 1, the sparse codewords are numbered from $\boldsymbol{c_0}$ to $\boldsymbol{c_{127}}$ from top to bottom and from left to right. The stream of source data is delivered in sequences of 7-bits and then are translated by the encoder into 9-bits sparse codewords according to a 1:1 mapping rule. It means the 7-bits information sequences from '0000000' to '1111111' are transformed into 9-bits codewords from $\boldsymbol{c_0}$ to $\boldsymbol{c_{127}}$, respectively.

The maximum likelihood (ML) decoding of the sparse code is deployed to retrieve the user information. The codeword in the LUT with the closest Euclidean distance to the received one is selected, and the corresponding user data sequence is decoded. In particular, the Euclidean distance of the received codeword to the whole of the codebook can be calculated as follows,

$$d\left(r_i, c_i\right) = \sqrt{\sum_{j=1}^{9} \left|r_{ij} - c_{ij}\right|^2} \tag{4}$$

where r_i is the i^{th} received codeword, c_i is the i^{th} codeword of the codebook, r_{ij} is the j^{th} bit of the i^{th} received codeword, and c_{ij} is the j^{th} bit of the i^{th} codeword of the codebook.

To take advantage of the complete received information, the noisy received sequence $\boldsymbol{r}$ is fed directly to the input of the decoder without any thresholding detection. Moreover, as shown in Fig. 4., the input sequence of the decoder is attenuated by a factor α in our implementation. Suppose the factor is too large or too small. In that case, the information received from the channel can affect the performance of the Euclidean-based decoding (shown in the next section), and therefore the system performance degraded significantly. A judicious selection for the attenuator factor is helping to improve the performance of the ML decoding.

IV. SIMULATION RESULTS AND DISCUSSION

A block diagram of the system is illustrated in Fig. 4. The user data sequence $u_i \in u$ is encoded by the proposed encoder. The output of the encoder $c_i \in c$ is then written into the STT-MRAM channel. The received signal $r_i \in r$ is decoded by the proposed decoder to achieve the original user data $\widehat{u}_i \in \widehat{u}$.

Experimental parameters taken from [16], [20] are used for our simulations herein. Thereby, an STT-RAM cell designed with a predictive technology model 45nm technology is selected as a reference technology node. The values of μ_0 and μ_1 are set as 1 $k\Omega$ and 2 $k\Omega$, respectively; and $\sigma_0/\mu_0 = \sigma_1/\mu_1$. The resistance distributions can be adjusted by changing the ratio σ_0/μ_0(and hence σ_1/μ_1), reflecting the severity of the read decision errors. That means a significant value of σ_0/μ_0 (and therefore σ_1/μ_1) represents a worse fabrication process resulting in more read decision errors. In contrast, a small σ_0/μ_0 value (and hence σ_1/μ_1) means a better fabrication process and thus fewer read decision errors. Moreover, it is well known [16], [21], [22] that the error probabilities of P_0 and P_r are two orders of magnitude lower than P_1. The different error probabilities P_1 account for the influence of different write errors and read disturb errors.

Furthermore, we consider an offset of resistance caused by the increase of temperature, which only occurs with the high resistance state R_1. The offset is regarded as a Gaussian distribution where its mean and standard deviation are μ_{ofs} and σ_{ofs}, respectively.

To verify the effectiveness of the attenuate factor for the proposed code, we first consider the system without any offset. We adopt a fixed wire error rate of $P_1 = 2 \times 10^{-4}$ [16]. The BER and frame error rate (FER) performances of the system are estimated at $\sigma_0/\mu_0 = 10\%$. As shown in Fig. 5, the system performance is relatively low if the attenuator is not applied. The BER is reduced significantly when the attenuator increases and the attenuator's best range is from 2.5 to 3. The performance becomes worse as the value is more significant or equal to 4. We take the attenuator of 2.5 for subsequence simulations.

TABLE 1. Set of selected codewords.

111100000	110001010	101001010	100011100
000000011	000100010	001000100	001101001
111010000	110001001	101001001	100011010
000000101	000100100	001000111	001110001
111001000	110000110	101000110	100010101
000000110	000100111	001001000	001110010
111000100	110000101	101000101	100010011
000001001	000101000	001001011	001110100
111000010	110000011	101000011	100010000
000001010	000101011	001001101	010000001
111000001	110000000	101000000	100001101
000001100	000101101	001010000	010000010
110110000	101110000	100110100	100001011
000001111	000101110	001010011	010000100
110101000	101101000	100110010	100001000
000010001	000110000	001010101	010000111
110100100	101100100	100110001	100000111
000010010	000110011	001010110	010001000
110100010	101100010	100101100	100000100
000010100	000110101	001011001	010001011
110100001	101100001	100101010	100000010
000010111	000110110	001011010	010001101
110011000	101011000	100101001	100000001
000011000	000111001	001011100	010010000
110010100	101010100	100100110	011101000
000011011	000111010	001100000	010010011
110010010	101010010	100100101	011100100
000011101	000111100	001100011	010010101
110010001	101010001	100100011	010011001
000011110	001000001	001100101	011011000
110001100	101001100	100100000	010100000
000100001	001000010	001100110	011000000

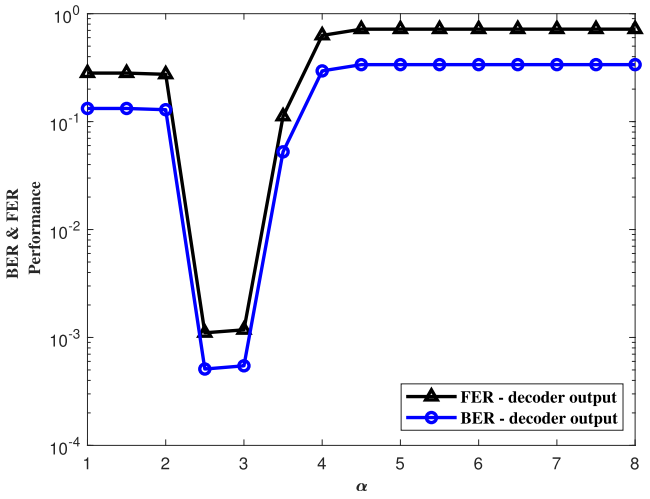

FIGURE 5. Performance according to attenuator.

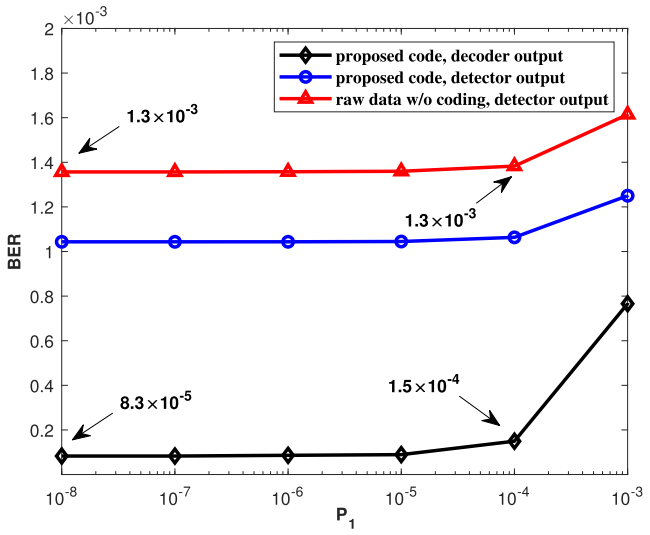

FIGURE 6. BER performance according to write error rate P_1.

The next part shows the system performance under different write and read disturb errors. Simulations are carried out at $\sigma_0/\mu_0 = 9\%$. Fig. 6 shows the BER performance of the proposed code and the user data without encoding according to different write error rates. Observe from Fig. 6 there is an error floor for the raw data and the proposed code. Yet, the error floor of the proposed code is significantly lower than that of raw data. In particular, the error floor of the raw user data is about 10^{-3} BER, while that of the proposed code is about 10^{-5} BER. The error floor is almost constant as the error probability P_1 is smaller or equal to 10^{-4} and 10^{-5} for the raw data without encoding and the proposed code, respectively. Furthermore, it is also observed that at the wire error rate P_1 of 10^{-4}, the system aided by the proposed code reduces the BER performance significantly to about 1.5×10^{-4} BER, compared to the 1.3×10^{-4} BER of the raw data.

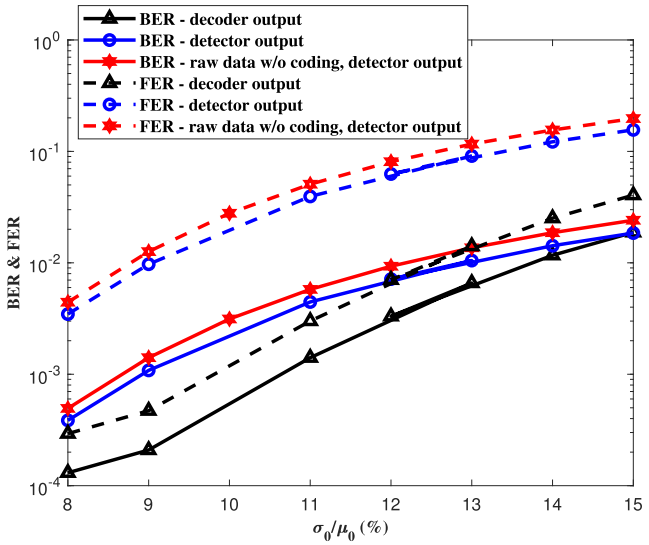

FIGURE 7. Performance comparison between the proposed code and raw data.

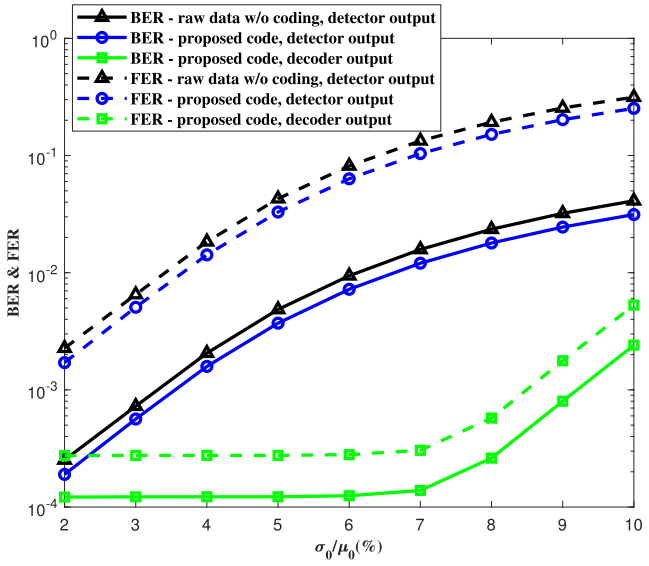

FIGURE 8. Performance comparison between the proposed code and raw data with an offset of $\mu_{ofs} = -0.2k\Omega$ and $\sigma_{ofs}/\mu_1 = 4\%$.

Fig. 7 shows the comparison of BER and FER performances between the raw data w/o coding and the proposed code. In the case of the raw data, a conventional threshold detector with a threshold of $(\mu_0 + \mu_1)/2$ is used to detect the received signal. The BER and FER performances of the proposed code are significantly improved compared to the unencoded raw signal. For example, the proposed code provides a quality gain of about 2.2% over the unencoded raw signal at 10^{-3} BER. However, this gain also decreases when the severity of the read decision errors (σ_0/μ_0) is increased. It is also worth noting that the performance of the output of the decoder is also significantly improved compared to that of the detector. As the resistance spread σ_0/μ_0 is increased, the gain of the decoder compared to the detector is also

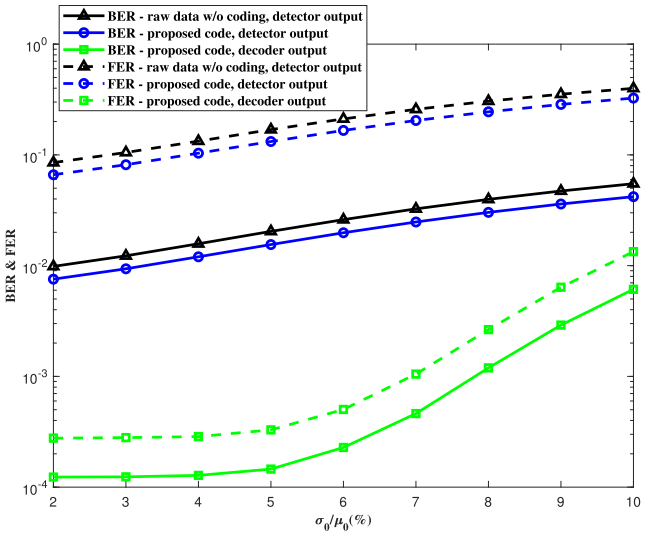

FIGURE 9. Performance comparison between the proposed code and raw data with an offset of $\mu_{ofs} = -0.2k\Omega$ and $\sigma_{ofs}/\mu_1 = 7\%$.

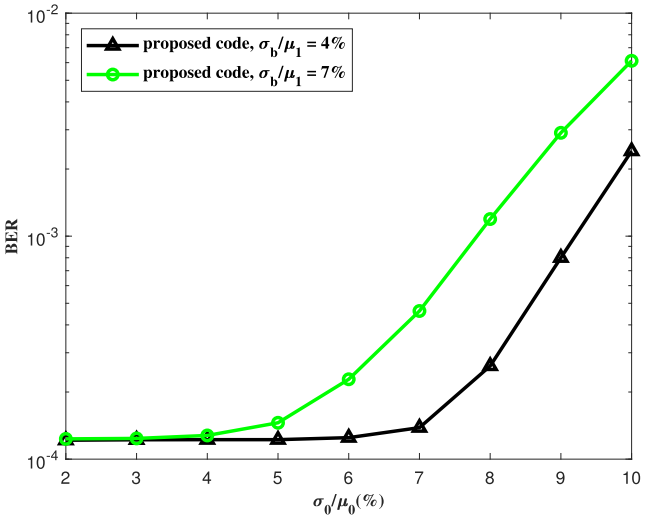

FIGURE 10. BER performance of the proposed code with an offset of $\mu_{ofs} = -0.2k\Omega$, at $\sigma_{ofs}/\mu_1 = 4\%$ and $\sigma_{ofs}/\mu_1 = 7\%$.

gradually reduced. The performance of the decoder and detector shows signs of converging together when the σ_0/μ_0 ratio is about 15%.

Finally, we consider the performance of the proposed code under the effect of different offsets. Figs. 8, 9, and 10 show BER and FER performances of the proposed code with a fixed mean value of $\mu_{ofs} = -0.2k\Omega$ and different normalized root mean squared values σ_{ofs}/μ_1 of 4% and 7% [23]. The proposed code outperforms the raw data without coding for both cases. It can be easily observed that the performance of the proposed code decreases very slowly as the read errors (σ_0/μ_0) are increased. In contrast, the performance of the system without coding degrades significantly. For instance, for the case of $\sigma_{ofs}/\mu_1 = 4\%$, if the σ_0/μ_0 is in the range of from 2% to 7%, the system's performance with coding is virtually non-degradable (around 10^{-4} BER), whereas that of the system without coding degrades from 10^{-4} BER to 10^{-2} BER. The same situation occurs at $\sigma_{ofs}/\mu_1 = 7\%$ when the σ_0/μ_0 is in range of from 2% to 5%, Figs. 8 and 9 also show an important feature that the system using the proposed code is less sensitive to offsets. Fig. 10 shows a performance comparison of the proposed code under the influence of different normalized offset variations. As the read decision error $\sigma_0/\mu_0 < 5\%$, the performance of the proposed code under the influence of $\sigma_{ofs}/\mu_1 = 4\%$ and $\sigma_{ofs}/\mu_1 = 7\%$ is not significantly different. However, if the $\sigma_0/\mu_0 \geq 5\%$, the system performance deterioration under the effect of a higher deviation becomes more apparent.

Finally, we would like to emphasize that this work is done from the perspective of coding theory only. The cost of implementing the coding scheme, such as energy, performance, and area, depends strongly on the implementation technology and choice of circuit architectures. Therefore, more detailed and specific discussions of aspects related to circuit design are beyond the scope of this paper.

V. CONCLUSION

In this work, we have addressed the operation and challenge of STT-MRAM. The bulk of this work focuses on reducing the write failure rate by exploiting their asymmetry feature. We have proposed a novel 7/9-rate spare code with a simple encoder and decoder. The proposed code attempts to reduce writing logic ''1'' and improves the wire failure rate in STT-MRAM. The simulation results show that the proposed code achieves gains of about more than 2% of σ_0/μ_0 compared to the raw data without coding. Moreover, the BER performance of STT-MRAM aided by the proposed code is much better than that of the system without data encoding under offset effects. Another point worth noting is that there is a high error floor at write error rate regions lower than 10^{-5} since the proposed code cannot correct errors yet. Therefore, an error-correction sparse code with reasonable complexity is a potential approach for further improving the performance of the STT-MRAM.

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