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Enhanced Voltage Sorting Algorithm for Balancing the Capacitor Voltage in Modular Multilevel Converter

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ABSTRACT In this paper, an enhanced voltage sorting algorithm is proposed for balancing each sub module capacitor voltage in modular multilevel converter (MMC). However, the submodule (SM) voltage strategy becomes more complex when it increases to a number of levels, which eventually increases voltage ripples and circulating current. In order to overcome this problem, an enhanced voltage sorting algorithm is proposed, which implies an enhanced control logic function for capacitor voltage balancing of the converter. The switching pattern of each SM floating capacitor is determined based on the modulating signal methodology, which is then compared with the hybrid state condition using arm current direction in the MMC. Additionally, the generated hybrid signals are once again compared with the dynamic implicit number by conjoining the switching logic state variables. Due to this comparison of logic function, the capacitor voltage is balanced properly and reduces the capacitor ripple voltage to a permissible limit compared to the conventional method. Hence, compared to other balancing techniques, the circulating current is reduced by using conventional control techniques. The desired pulse signals for the power devices are obtained based on the multi carrier pulse width modulation techniques. The superior performance of the proposed algorithm is tested using MATLAB/Simulink software and real time laboratory hardware setup for different load conditions. Apart from this, the effective performance of the proposed method has been validated in the HVDC transmission system.

INDEX TERMS Enhanced voltage sorting (EVS) algorithm, hybrid state condition, modulation methodology, modular multilevel converter (MMC), dynamic implicit number, HVDC system.

I. INTRODUCTION

The modular structure based Voltage Source Converter (VSC) has become an efficient converter for high voltage applications. This engrossed many researchers to focus on its technical challenges associated for reliable operation and extend it to various low power applications. In addition to this, its modular and voltage scalable features, have become a growing attention in industrial applications compared to traditional converter [1]–[4]. The MMC was first proposed in 2003 [5] for wide power range applications, which were further extended to medium power applications such as variable speed drives, static compensator [6], [7] etc. At first, the Siemens installed the MMC for HVDC system in San Francisco during the year 2010, followed by ABB in Germany during the year 2012 for offshore wind farm applications. So, based on several features such as reliable operation, harmonic performances, modularity, high efficiency, voltage scalability, redundancy, low voltage stress (dv/dt), and low power rated submodules made the converter applicable to HVDC system [8], offshore wind plant [9], multi-terminal system [10], ship board application [11], motor dives, static compensator, and AC transmission system [12]. Furthermore, many researchers are focusing on implementing the converter for large scale photovoltaics applications, microgrid system [13], renewable sourced grid integration [14], [15] etc.

The most important factor that depends on the safe and reliable operation of MMC are proper capacitor balancing techniques, circulating current suppression, and ripple voltage minimization. In that, the capacitor balancing techniques plays an important role in controlling each SM capacitor

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voltage, also it controls the output line current and voltage of the MMC. The ripple voltage in each SM capacitor is increased due to the uneven balancing of the floating capacitor connected in the MMC. This causes increase in harmonic components and circulating current in each converter leg. Similarly, the increase in circulating current affects the peak value of the arm current and also increases the switching and conduction losses of the converter. Hence suppressing the capacitor ripple voltage and circulating current are the important features of MMC. In order to overcome the aforementioned problem, a proper voltage balancing algorithm, modulation schemes and control methods are needed for reliable operation of MMC. Many different voltage balancing techniques are proposed based on balancing the capacitor voltage, in that the most widely used method is voltage sorting algorithm. Generally, these algorithm are used to control each SM connected in converter leg (upper and lower arm), by sorting the capacitor voltage by either descending or ascending order using the arm current (i_{arm}) direction [16], [17]. However these techniques are simple and reliable, but it affects stability and increases the computational burden to the converter, when it is subjected to a high frequency switching process and also increases the circulating current. An average voltage balancing technique is proposed in [18] and [19], discusses that balancing each SM capacitor voltage based on a separate controller and then it is incorporated with average modulating reference signals for generating the switching pulse signal for MMC. However, this technique causes an uneven balancing when subjected to high switching frequency and thus eventually increases the capacitor ripple voltage. Furthermore, many control methods are proposed by many researchers to rectify the voltage balancing issues. The closed loop control approach [20], [21] used to balance the capacitor voltage using feedback controller and the obtained signal is once again adjusted using phase shifted modulating signals. Based on phase shifting, the capacitor voltage is balanced properly but it causes more complexity in control function. The open loop balancing approach [22], [23] simplifies the capacitor balancing issues based on the carrier rotation and switching gate signal pattern without measuring the SM capacitor voltage. The open loop approach reduces the ripple voltage of the capacitor to a certain limit, however it takes a lot of processing time and response during the low dynamic condition. To overcome that, a decentralized control method [24] is proposed to control each power module capacitor and to minimize the voltage ripple factor to a permissible limit. This method can only able to control the dual line frequency components and applicable constant load condition. In [25], back stepping control method suppresses the circulating current by nonlinear control variables are incorporated with the Lyapunov theory and generates the multi stage control variables. These variables are combined with the virtual feedback controller and stabilizes the dynamic response. The generalized control approach [26], [27], injects a zero sequence voltage to the energy balancing algorithm and then optimized the current stress in the arm of MMC. This method eliminates the second and fourth harmonic components and the capacitor ripple voltage. Apart from the voltage sorting algorithm, the modulating signal based balancing techniques are proposed in many literatures. The most widely used modulating techniques are nearest level techniques [28], multilevel carrier techniques [25], carrier phase shifted modulation [29], [30] and space vector modulation [31], [32]. The multilevel carrier and nearest level have widespread applications for balancing different SM topologies in MMC. They provide a unique advantage in terms of control function, system complexity, safe and reliable operation.

In this paper, an enhanced voltage sorting algorithm is proposed for balancing the capacitor voltage of MMC. The level shift (phase disposition) modulation scheme is applied for generating the switching pulse signal for the power devices. The acquired pulse signals are modulated into two methods, one is modulation signal methodology and another is enhanced voltage sorting algorithm. The modulating signal methodology is proposed for restructuring the pulse signal into multiple signals (divided and cumulative signals) and then it is incorporated into the proposed algorithm. The same signal pattern can be applicable to N number of SM without any modifications. Likewise, in voltage sorting algorithm, the acquired signals from modulation methodology are compared with upper and lower arm voltage based on i_{arm} direction, which generates hybrid state signals. Furthermore, hybrid signals are once again sorted out to produce dynamic implicit number by comparing with number of SM, modulation index and cumulative signal. Finally, the dynamic implicit signals are compared with switching logic state signals and produces the gate signals for the power devices connected in the MMC. Hence, the superior performance of the proposed algorithm is tested using dynamic load conditions by simulation and real time hardware setup.

The structure of the paper is arranged as follows: the basic structure of MMC and mathematical model are discussed in Section II. In Section III, the modulation schemes, proposed enhanced voltage sorting algorithm, and HVDC system are presented. Section IV discusses about the performance of the proposed techniques in simulation and real time hardware environment. Section V discusses about the comparative performance analysis and section VI depicts the conclusion.

II. OPERATING PRINCIPLE OF MMC

A. BASIC STRUCTURE

The schematic arrangement of MMC is shown in figure 1. It consist of three converter leg, an input voltage source (DC), an arm inductor and a three phase load. The DC input (V_{dc}) splits into positive ($+V_{dc}/2$) and negative ($-V_{dc}/2$) side, with midpoint as grounded (O). The each converter leg consists of two arms as upper and lower, each arm consists of series connected in N number of SM, where each SM consist of switching devices and floating capacitor. The arm inductor connected in between each arm of the converter, reduces the circulating current. The circulating current flows in each arm

is due to the occurrence of high frequency DC component which flows during each switching operation.

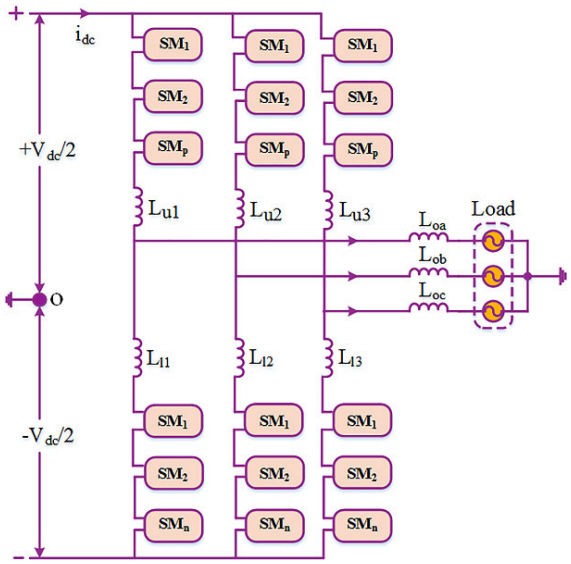

FIGURE 1. Schematic arrangement of MMC.

The desired three phase output is taken from midpoint of the converter through load resistance and inductor. Generally the sizing of MMC mostly depends upon the selection of appropriate arm inductor, floating capacitor, number of SM and power devices. The Half Bridge SM (HB-SM) shown in figure 2, is used as an appropriate SM topology for MMC. The HB-SM consists of two switching devices (T_1 & T_2) and a floating capacitor (C). Each of the switching devices is interconnected with an antiparallel diode (D_1 & D_2). However, switching operation of the power devices primarily depends upon the arm current (i_{arm}) flowing in the converter. The HB-SM generates two level output that is, 0 and $+V_C$, based on four modes of operation such as charging, discharging and two bypass.

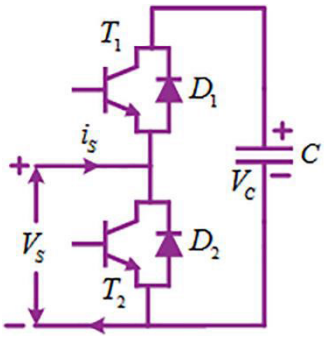

FIGURE 2. Single SM of half bridge topology.

The overall operating modes of HB-SM with arm current direction and switching state is illustrated in Table 1. During charging mode, the diode D_1 will be forward bias and charges the capacitor C, arm current ($i_{arm}>0$) flows from input source V_S, D_1, C to negative of V_S. Likewise in discharging mode, the switch T_1 will be forward bias and discharges the capacitor voltage (V_C), arm current ($i_{arm}<0$) flows through negative of V_S, C, T_1 to positive of V_S. In bypass mode, the switch T_2 will be forward bias and bypass the input V_S, generates zero voltage as an output, which is described in Table 1.

TABLE 1. Sequence of single half bridge.

Switch Status	Arm Current	Direction of I_{arm}	Capacitor Mode	Capacitor Voltage
T_1 off, T_2 off	$i_{arm}>0$	D_1 & C	Charging	Increases
T_2 on, T_1 off	$i_{arm}>0$	T_2	Bypass	Constant
T_2 off, T_1 on	$i_{arm}<0$	T_1 & C	Discharging	Decreases
T_2 on, T_1 off	$i_{arm}<0$	D_2	Bypass	Constant

B. MATHEMATICAL MODEL

The study of dynamic and steady state behavior of the converter can be evaluated by modelling each and every parameter into a simplified model, which reduces the computational time and system complexity. There are many different approaches which are used for modelling the MMC parameters. In that phasor control model, equivalent circuit model and simulation model are most widely used, as illustrated by [33]. Compared to several different models, the equivalent circuit model is most feasible and simple technique for reliable operation of the MMC. The equivalent circuit model has several advantages compared to other techniques such as easy in converting the control variables, takes less computational time and can be easily converted to decoupled models [34], [35]. The figure 3 depicts, the single stage equivalent circuit model of MMC. However, only single phase are considered for modelling purposes, the same can be applicable for the other two phases of the MMC. It consists of controlled voltage sources, arm and load resistance, arm inductor and load. The N number of SM capacitor voltages are converted into a controlled voltage sources (V_{us}, V_{ls}). The arm and load resistance (R_{ua}, R_{la} & R_{oa}) are generally a negligible value, which is used to determine the power loss in the converter.

The arm inductor (L_{u1} & L_{l1}) are used to limit the instantaneous change in arm current flowing in each arm during switching function. The input DC supply is split into positive ($+V_{dc}/2$) and negative ($-V_{dc}/2$) supply, using the ground terminal (O) connected at the midpoint. The upper arm voltage is obtained from $+V_{dc}/2$ to the ground terminal, similarly lower arm voltage can be determined from $-V_{dc}/2$ to O. The controlled voltage sources (V_{us}) is nothing but a cumulative capacitor voltage of total number of SM connected in upper arm, whereas the Voltage source (V_{ls}) is cumulative output of lower arm. The current flowing in each arm primarily depends upon the input DC current, phase current and the circulating current, which is obtained by,

$$i_{us}^{x} = \frac{i_{m}^{x}}{3} + i_{mc}^{x} + \frac{i_{dc}}{2} \tag{1}$$

$$i_{ls}^{x} = i_{mc}^{x} - \frac{i_{m}^{x}}{3} + \frac{i_{dc}}{2} \tag{2}$$

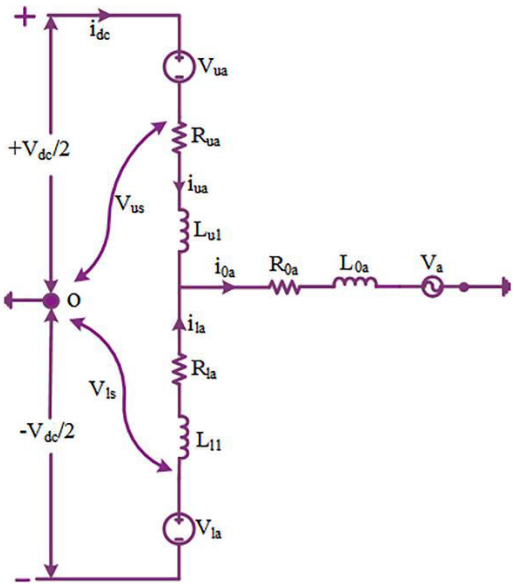

FIGURE 3. Single stage equivalent circuit model.

where, for ∀x∈Phase R, Y & B. The circulating current can be determined by,

$$i^x_{mc} = \frac{1}{2}\left[i^x_{us} + i^x_{ls}\right] - \frac{i^x_m}{3} \tag{3}$$

$$i^x_{La} = \left[i^x_{us} - i^x_{ls}\right] \tag{4}$$

The load current is determined by differentiating i^x_{us} &i^x_{ls}. The dynamic voltage behavior of the upper and lower voltage are determined by,

$$V^x_{us} = \left[\begin{array}{l} \frac{V_{DC}}{2} - \frac{L^x_{u1}d\left(i^x_{us}\right)}{dt} - R^x_{ua}i^x_{us} + \frac{L^x_{0a}d\left(i^x_{0a}\right)}{dt} \\ +R^x_{0a}i^x_{0a} + V^x_a\sqrt{a^2+b^2} \end{array}\right] \tag{5}$$

$$V^x_{ls} = \left[\begin{array}{l} \frac{V_{DC}}{2} - \frac{L^x_{l1}d\left(i^x_{ls}\right)}{dt} - R^x_{la}i^x_{ls} + \frac{L^x_{0a}d\left(i^x_{0a}\right)}{dt} \\ +R^x_{0a}i^x_{0a} + V^x_a \end{array}\right] \tag{6}$$

Substituting the value of upper and lower arm current from equation (5) & (6) and by differentiating the equation,

$$V^x_a = \left[\begin{array}{l} \frac{\left(V^x_{us} - V^x_{ls}\right)}{2} - R^x_{0a}\left(i^x_{us} + i^x_{ls}\right) \\ -\frac{L^x_{0a}d\left(i^x_{us} + i^x_{ls}\right)}{2dt} \end{array}\right] \tag{7}$$

By substituting equation (4) in (7), the output voltage can be rewritten as,

$$V^x_a = \left[\frac{\left(V^x_{us} - V^x_{ls}\right)}{2} - R^x_{0a}i^x_{0a} - \frac{L^x_{0a}di^x_{0a}}{2dt}\right] \tag{8}$$

Similarly, if the converter is connected to the grid connected system, the common mode voltage (V^x_{cm}) will be considered for obtaining the output voltage. Hence the equation (8) can be reformed as,

$$V^x_a = \left[\frac{\left(V^x_{us} - V^x_{ls}\right)}{2} - R^x_{0a}i^x_{0a} - \frac{L^x_{0a}di^x_{0a}}{2dt} + V^x_{cm}\right] \tag{9}$$

Apart from the circulating current, output voltage and capacitor ripple voltage plays an important factor for reliable operation of MMC. Hence the dynamic condition of circulating current and ripple voltage have to be considered for equivalent circuit model. The circulating current can be determined by substituting the equation (3) in (7) and differentiating,

$$\frac{di^x_{mc}}{dt} = \left[\frac{V^x_{us} - V^x_{ls}}{2L^x_{0a}} - \frac{V^x_a}{2} - R^x_{0a}i^x_{mc} + \frac{V_{DC}}{2}\right] \tag{10}$$

In the same way, if the common mode current (i^x_{cm}) (if applicable) are considered, it can be obtained by,

$$\frac{di^x_{cm}}{dt} = \left[\begin{array}{l} \frac{\left(V^x_{ls} - V^x_{us}\right)}{6L^x_{0a}} - 3L^x_{0a}\frac{di^x_{0a}}{dt} \\ -\frac{R_0i^x_{0a}}{2} - 2V^x_a \end{array}\right] \tag{11}$$

The capacitor ripple voltage of each (upper and lower) arm can be determined by,

$$\frac{dV^x_{rpu}}{dt} = \frac{1 * i^x_{us}}{NC}\left[\frac{i^x_m}{3} + i^x_{mc} + \frac{i_{dc}}{2}\right] \tag{12}$$

$$\frac{dV^x_{rpl}}{dt} = \frac{1 * i^x_{ls}}{NC}\left[i^x_{mc} - \frac{i^x_m}{3} + \frac{i_{dc}}{2}\right] \tag{13}$$

Hence the dynamic behavior of MMC are modelled based on the single stage equivalent circuit model, which eventually reduces the computational time and control complexity. Apart from this, it also helps in reducing system complexity when subjected to increase in number of voltage levels and also for the grid connected system.

III. PROPOSED ENHANCED VOLTAGE SORTING (EVS) ALGORITHM

A. PULSE WIDTH MODULATION (PWM) TECHNIQUE

The pulse signals required for switching the power devices are generated based on the modulation techniques. There are different PWM schemes available, in that, multi carrier based PWM techniques are most widely used for MMC. The multi carrier techniques splits into two types based on the carrier arrangement such as Level Shift carrier PWM and Phase Shift carrier PWM. The Phase Shift carrier technique is used to generate multiple triangular signals based on phase shifting, whereas the level shift carrier technique generates signals based on the level shifting with the reference signal (sinusoidal). The level shift PWM technique again splits into three types such as: phase disposition, alternate phase opposition disposition and phase opposition disposition. The phase disposition (PD) based Level Shift carrier is used as a modulating technique for the proposed EVS algorithm. The effective performances of the proposed method is implemented by selecting the number of SM as 4 (N=4). The level shifting PWM techniques generates 2N+1 voltage levels for each leg of the converter. The number of level can be determined by,

$$N_l = 2N_{SM} + 1 \tag{14}$$

The generation of modulating signal for either single leg or three leg of the MMC are evaluated based on the open and

closed loop control approach. Apart from this, many different modulating approach have been proposed based on the application such as d/q synchronous reference frame approach for decoupled current model [36], decoupled average sample based modulating techniques for wide power range applications [16], active power decoupling method [31] and field and vector oriented control for variable speed motor drive application [6]. These modulating approach have unique advantage when compared to the conventional method. In this paper, an open loop modulating signal methodology is used for generating the gate pulses to the proposed EVS algorithm, which is quite simple and takes less computational time for processing. Apart from this, the proposed EVS algorithm is tested with simple passive loading conditions, hence an open loop modulating signal approach has been far better for the comparative analysis. The reference voltage signals for comparing both arm voltage can be determined by,

$$\begin{aligned} V_{up}^{ref} &= \frac{V_{dc}}{2} - V_{am}\sin(\omega t) \\ V_{lp}^{ref} &= \frac{V_{dc}}{2} + V_{am}\sin(\omega t) \end{aligned} \tag{15}$$

where, V_{am} refers to amplitude voltage, which can be obtained by,

$$V_{am} = M * \frac{V_{dc}}{2} \tag{16}$$

where M→Modulation Index of range between $0 \leq M \leq 1$. By substituting the equation (16) in (15) the upper and lower reference voltage for modulating methods are determined by,

$$\begin{aligned} V_{up}^{ref} &= \frac{V_{dc}}{2}[1 - (M * \sin\omega t)] \\ V_{lp}^{ref} &= \frac{V_{dc}}{2}[1 + (M * \sin\omega t)] \end{aligned} \tag{17}$$

The (15), (16) and (17) depicts the reference voltage generated for upper and arm voltage of converter. The modulating signal methodology applicable for single converter leg [i.e. the same can be applicable for other two phases of the converter leg except the ω has to be changed into $\pm 2\pi/3$] of MMC are depicted in figure 4. This approach is suitable for any type of multi carrier PWM techniques. At first, the comparison of reference signal with carrier signals are done using logical comparator method, which generates switching signals (R_s). The obtained R_s are once again compared with Carrier Rotation (CR) signal (as proposed in [37]), which are referred as divided signal (D_S). This D_S pulse signal is split into two ways, upper arm (D_1 to D_4) and lower arm (D_5 to D_8) signals. The obtained upper and lower arm signals are manipulated with weighting factor (λ_{sn}) [24] to determine desired Cumulative Signal (C_S) for the converter.

Henceforth, the obtained signal from the modulating method are provided as input to the proposed EVS algorithm. These various switching operation in modulating signal methodology are shown in Table 2.

TABLE 2. Switching function methodology.

Sorting of Switching Signal		Carrier Signal	C_S	
Upper	Lower		Upper	Lower
R_{s1}>CR=D_1	R_{u1}>CR=D_5		D_1>λ_{sn}=C_{S1}	D_5>λ_{sn}=C_{S5}
R_{s2}>CR=D_2	R_{u2}>CR=D_6	$S_{w1} \approx S_{w8}$	D_2>λ_{sn}=C_{S2}	D_6>λ_{sn}=C_{S6}
R_{s3}>CR=D_3	R_{u3}>CR=D_7		D_3>λ_{sn}=C_{S3}	D_7>λ_{sn}=C_{S7}
R_{s4}>CR= D_4	R_{u4}>CR=D_8		D_4>λ_{sn}=C_{S4}	D_8>λ_{sn}=C_{S8}

B. PROPOSED EVS ALGORITHM

The balancing of each SM floating capacitor plays a key factor for safe, reliable and dynamic operations of MMC. However, balancing the capacitor voltage primarily depends upon the sorting of capacitor voltage (charging and discharging), which eventually based on direction of the arm current (i_{arm}). However, the arm current decides the minimum ($i_{arm} \leq 0$) and maximum ($i_{arm} \geq 0$) number of voltage to be inserted for balancing the capacitor voltage in each SM. Many different voltage sorting algorithms have been proposed based on the selection of number of SM to be inserted for balancing the capacitor [17], [20]. Though they have unique advantages compared to the conventional method, it causes more complexity when the number of SM are increased. Apart from this, it increases the capacitor voltage ripple, circulating current during dynamic loading conditions and also affects the harmonic performances.

Furthermore, some of the balancing algorithm [22] affects the stability of the converter, when the number of voltage levels are increased. Apart from this, the capacitor voltage balancing based on the modulating strategies are applicable to a certain level [28]. Hence the selection of voltage balancing algorithm primarily focused upon the simplified control techniques, safe and reliable operation, less computational time, control complexity, proper modulating strategy and redundant switching operation. Based on the above mentioned features, an Enhanced Voltage Sorting (EVS) Algorithm is proposed for balancing the capacitor voltage of MMC. The proposed techniques consists of both modulating strategy (for pulse generation) and capacitor balancing algorithm. As discussed on the previous section, the floating capacitor in each SM cannot be balanced using the modulation methods as shown in figure 4, because it is primarily used only for pulse generation and doesn't consider the SM capacitor voltage. The concept of EVS algorithm is illustrated in detail as a flowchart in figure 5.

Initially, each input parameters required for the selection of number of SM is measured before starting of the voltage balancing process. The selection of each upper and lower arm SM capacitor voltage is measured based on the direction of the i_{arm} as depicted in the Table 1. The switching signals for each SM capacitor is obtained by modulating methodology as described in figure 4 and Table 2. The sorting of each

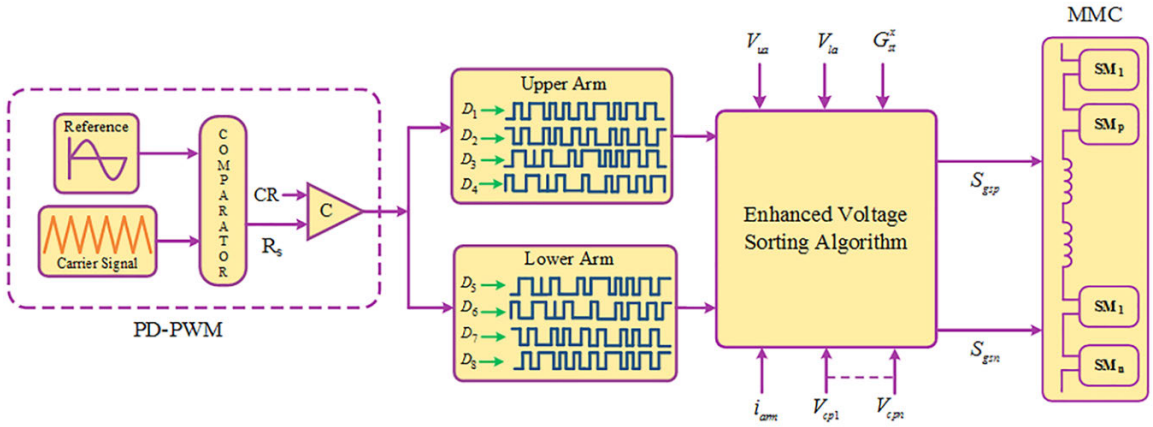

FIGURE 4. Modulating signal methodology for single converter leg of MMC.

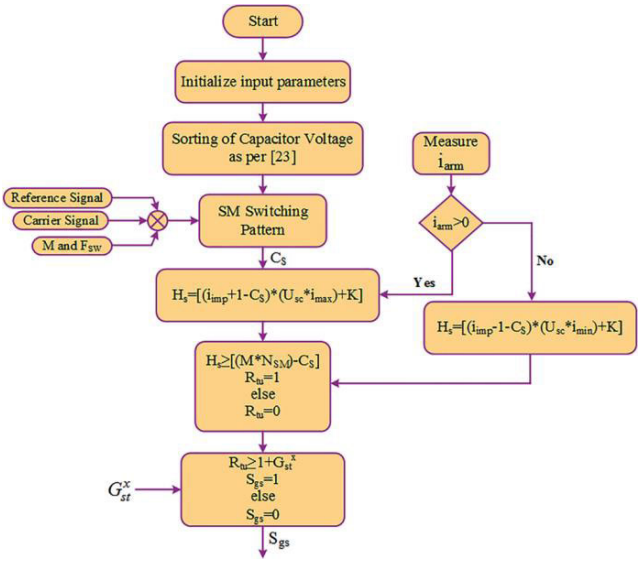

FIGURE 5. Flow chart of enhanced voltage sorting (EVS) algorithm.

capacitor voltage (V_{cpn}) by ascending order are evaluated based on the method proposed by [23]. Eventually by comparing the D_S with the λ_{sn}, the C_S signal are obtained for the next stage of balancing algorithm. Arm current (i_{arm}) flowing in each SM is measured based upon the minimum and maximum values (i.e. Charging and discharging state of capacitor) and are analyzed for selection process. When the i_{arm} is maximum (≥ 0), highest voltage from the SM is obtained in the output. Likewise, if i_{arm} is minimum (≤ 0), lowest voltage is inserted to the SM. At first stage, thus the selection of actual capacitor voltage are determined by manipulating hybrid state (H_S) condition, based on i_{arm} direction, sorted capacitor voltage and Cumulative Signal (C_S). The hybrid state (H_S) condition are determined by,

$$H_s = [(I_{imp} + 1 - C_S) * (U_{sc} * i_{\max}) + K] \quad (18)$$

$$H_s = [(I_{imp} - 1 - C_S) * (U_{sc} * i_{\min}) + K] \quad (19)$$

where I_{imp} represents the implicit random number and U_{sc} refers the actual capacitor voltage. The implicit random number (I_{imp}) $\in \{1, 2, 3 \ldots\ldots, N+1, N]$ as proposed by [19]. Hence the equation (18) and (19) represents the hybrid state condition of actual capacitor voltage of the converter. Thus the obtained H_S signals are again compared with modulation index (M), total number of SM (N_{SM}) selected with the C_S, which generates dynamic implicit number (R_{tu}).

$$H_S \geq [(M * N_{SM}) - C_S] \quad (20)$$

The R_{tu} used to control the arm voltage of the MMC during steady state as well as dynamic conditions. Thus the obtained dynamic implicit values are again compared with the switching logic state signals (G_{st}^x).

$$G_{st}^x = \left[\omega_a + \left(T_s * k) * \frac{180}{\pi}\right)\right] \quad (21)$$

where, $\omega_a = 2\pi f$ and T_s refers to sampling time period. The variables applicable for modelling the proposed EVS algorithm are described briefly in nomenclature (Table 3). Based on the comparison, the gate pulse (S_{gs}) required for switching the power devices in each SM is manipulated by comparing R_{tu} with (21). The gate pulse obtained from the final stage of the voltage balancing algorithm are evaluated using the switching logic state signals. If the compared gate pulse causes any overlap, the voltage balancing algorithm will modify gate pulse by reshuffling the switching logic state signals, and generates a new control variables to the switching devices, otherwise it doesn't change with the present switching condition. In spite of several advantages, there are some shortcomings related to proposed EVS algorithm, such as DC fault handling capability (required additional redundant SM), small amount of disturbances (voltage spike) created during transient condition and required separate controller for mitigating common mode voltage (for grid connected system and variable speed drives application).

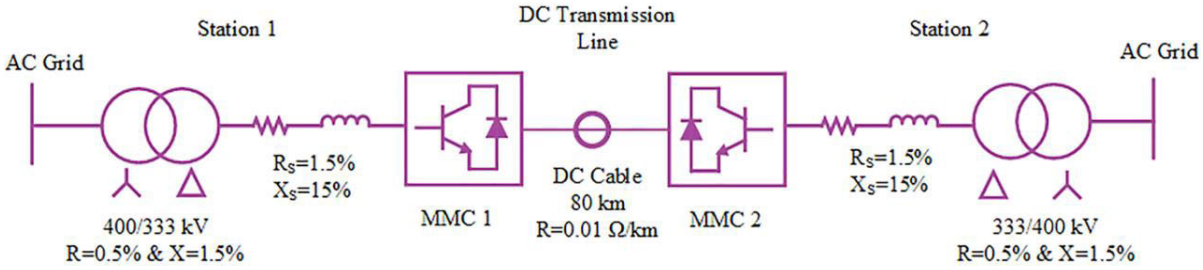

FIGURE 6. MMC based HVDC system.

TABLE 3. Nomenclature.

Variables	Description	Variables	Description
i_{arm}	Arm Current	L^x_{u1}, L^x_{l1}	Arm inductance of each phase
V_{us}, V_{ls}	Controlled voltage Source	R^x_{ua}, R^x_{la}	Resistance of upper and lower arm
i^x_{us}	Upper arm current flowing in each phase	R^x_{0a}, L^x_{0a}	Load resistance and inductance
λsn	Weighting Factor	V^{ref}_{up} , V^{ref}_{lp}	Upper and lower arm reference voltage
i^x_{mc}	Circulating current	i^x_{0a}	Load current of each phase
i_{dc}	Input DC current	V^x_a	Load voltage of each phase
i^x_m	Phase current	V^x_{rpu} , V^x_{rpl}	Ripple voltage of upper and lower arm of each phase.
i^x_{La}	load current of each phase	I_{imp}	Implicit Random numbers
V^x_{us}, V^x_{ls}	Upper and lower arm voltage of each phase	U_{sc}	Actual capacitor voltage
V_{DC}	Input DC supply	H_S	Hybrid State
C_S	Cumulative Signal	M	Modulation Index
K	Delay Constant	G^x_{st}	Switching Logic State Signal
ω_a	Angular Displacement	V^x_{cm}	Common Mode Voltage
V^{ryb}_g , i^{ryb}_g	Grid side voltage and current	V^{ryb}_a , i_{ryb}	Converter side voltage and current
R_S	Source Resistance	i_{max} , i_{min}	Maximum and Minimum Current

C. MMC-BASED HVDC SYSTEM

The proposed EVS algorithm based MMC are verified by implementing in HVDC transmission system, which are shown in figure 6. It consists of two converter station (station 1 and 2), AC grid, DC transmission cable, two transformer one is step down transformer at station 1 and other is step up transformer connected at station 2. The complete rating of the each parameters connected in HVDC systems are illustrated in figure 6. The main control function of HVDC includes real and reactive power, DC side voltage, grid side AC voltage and current. Generally for HVDC system, vector control strategy are most preferred control techniques for AC and DC side. These types of control strategy requires a separate voltage balancing algorithm to measure the capacitor voltage, arm voltage, circulating current etc. Hence the proposed EVS algorithm are implemented with vector control strategy as proposed by [23], without any modification, because of its simple and reliable control function, takes less computational time and performances better when subjected to any dynamic changes occurred in the system. The AC side voltage can be determined by,

$$V^{ryb}_a - V^{ryb}_g = \left[(0.5 * R_s) - \left(L\frac{di_{ryb}}{dt}\right)\right] \tag{22}$$

$$i_{ryb} = \left[(1.5 * R_S) - \left(i^{ryb}_g\right) + \left(\frac{1}{L_{0a}} * V^{ryb}_g\right)\right] \tag{23}$$

Similarly the real and reactive power are obtained by,

$$P_{ryb} = 1.5\left(V^{ryb}_g * i^{ryb}_g\right) \tag{24}$$

$$Q_{ryb} = 1.5 * \left(V^{ryb}_a * i_{ryb}\right) \tag{25}$$

The (22) to (25) are the major control parameters for the proposed EVS algorithm for the HVDC system. One of the major advantages of vector control strategy is that, they perform quite well in dq frame instead of abc synchronization frame when compared to the other controller. It is mostly

multi-variant controller, which can be able to control two or more inputs and outputs. Hence these control strategies are most suitable for open and closed control approach for HVDC system study.

IV. SIMULATION AND REAL TIME HARDWARE STUDY

The performances of the EVS algorithm are verified using MATLAB simulation software and also using real time hardware prototype. The simulation study involves two categories, one is testing the EVS method with variable load conditions and other one is implementing in the HVDC transmission system study. Thus the widespread robust performances results are discussed in below sections.

A. SIMULATION STUDY

The proposed voltage sorting algorithm are validated using MATLAB simulation software and the designed values applicable for simulation studies of MMC are illustrated in Table 4. The performances of the proposed algorithm using Half Bridge as SM topologies are validated by applying the parameters values (shown in Table 4) to the converter (figure 1). Since the number of SM selected for each arm is 4, the capacitor voltage of each SM is charged and discharged at 25% of the input voltage. Apart from this, the values required for arm inductor, floating capacitor and load parameters are illustrated in Table 4. The gate pulse signals required for the voltage balancing algorithm are obtained from PD-PWM technique (shown in figure 4) and the switching frequency for the carrier signals are taken as 2 kHz. Furthermore, the dynamic performances of the proposed balancing techniques are analyzed with conventional method and also tested with variable load conditions.

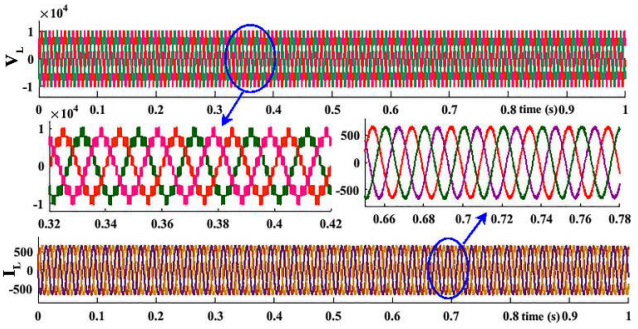

FIGURE 7. Load voltage and current waveform of the proposed balancing algorithm.

The line voltage and current waveform of the EVS algorithm is illustrated in figure 7. From figure 7, it clearly indicates that, the three phase output voltage and current of the MMC are evenly balanced based on the proposed method without any distortion, and also with less ripple voltage. Based on the load resistance and inductance value (Table 4), the load voltage are balanced to 2.5 kV per level in each arm of the converter. The detailed output characteristics of three phase voltage are indicated at the time interval of 0.32 to 0.42s, similarly for three phase current is indicated at 0.66 to 0.78s. The SM floating capacitor voltage for upper and lower arm of phase R is illustrated in figure 8. Thus from figure 8, capacitor voltage of each SM is evenly balanced based on the proper switching pattern obtained from the EVS algorithm. Each capacitor is balanced at 25% of the rated voltage (i.e. is 2.5kV) and with 4.2% of ripple voltage.

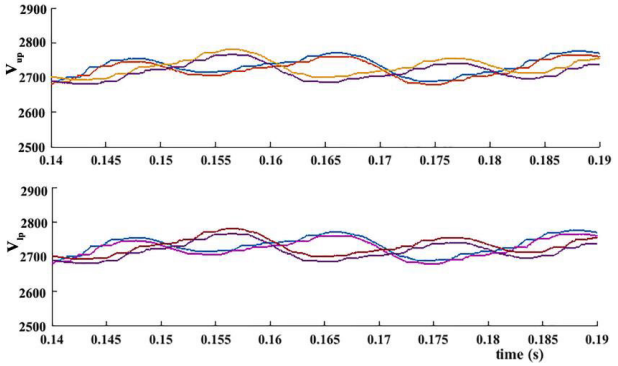

FIGURE 8. SM upper and lower capacitor voltage (N=4/arm).

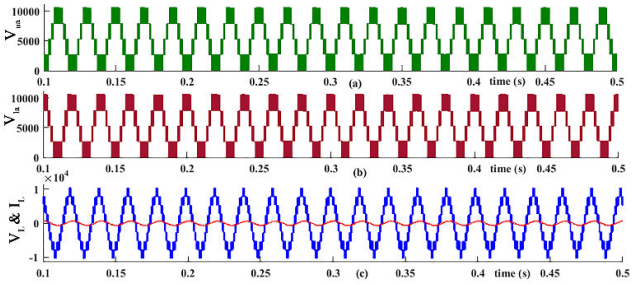

FIGURE 9. Voltage waveform of phase R (a) upper arm voltage (V_{up}), (b) lower arm voltage (V_{lp}) and (c) line voltage and current (V_L & I_L).

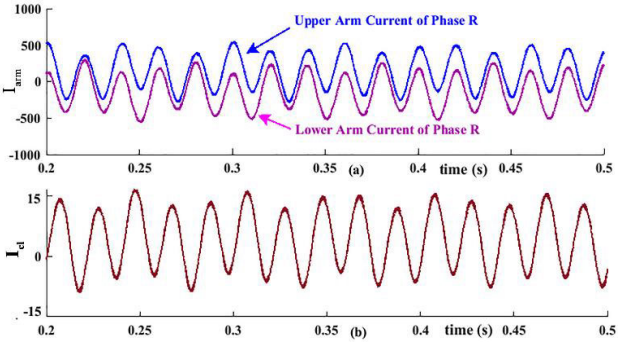

FIGURE 10. Current waveform of phase R (a) arm current, (b) circulating current.

Similarly, the each arm voltage of the MMC is depicted in figure 9, which also indicates the superior and steady state performance of the EVS algorithm. The upper and lower arm voltage (V_{ua} & V_{la}) of Phase R is depicted in figure 9 (a) & (b). Furthermore, the combined load voltage

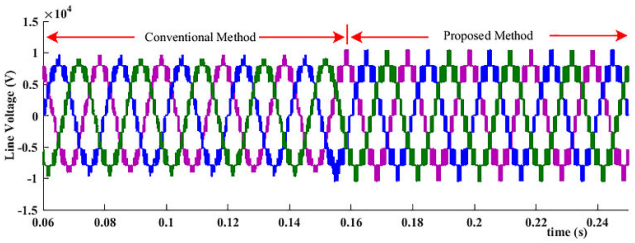

FIGURE 11. Output voltage comparison of proposed method versus conventional method.

(V_L) and current (I_L) characteristics of Phase R is illustrated in figure 9 (c). Apart from this, the arm current and circulating current of phase R are depicted in figure 10. It consist of less harmonic components presents in the peak to peak of the arm current [figure 10 (a)] and also circulating current [figure 10 (b)] flowing in each converter leg are suppressed at an permissible limit. Hence from figure 8 to 10 illustrates the performances of the EVS algorithm for the MMC, during fixed load conditions.

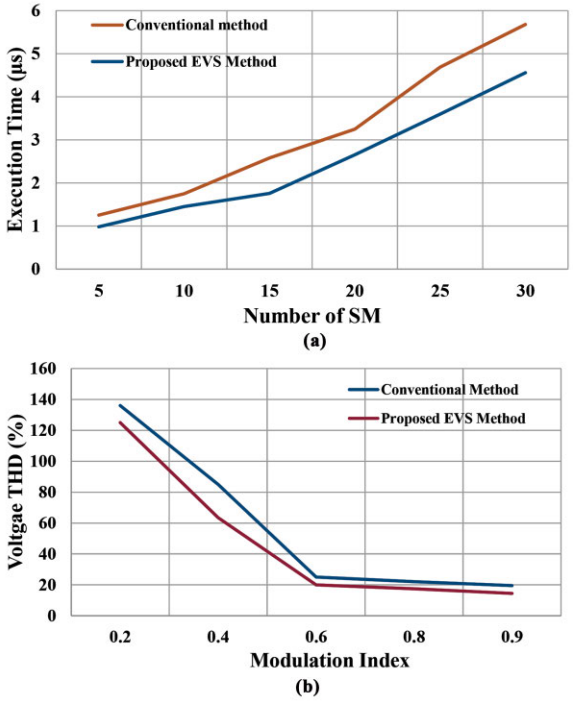

FIGURE 12. Comparative analysis of proposed method versus conventional method (a) Execution time and (b) Voltage THD (%).

These individual characteristic waveforms proves the superior performances of the proposed method in terms of reducing the capacitor ripple voltage, suppressing the circulating current, reliable operation when subjected to increase in SM voltage level, superior harmonic performances and equal reverse blocking voltage. Figure 11 illustrates the output voltage comparison between the conventional method and the proposed method. Initially, the converter is simulated with the conventional balancing method during the time interval

TABLE 4. Simulation and experimental parameters.

Parameters	Simulation	Experiment
DC Voltage	11 kV	400 V
Capacitance (C)	836 µf	73 µf
Arm Inductance (L_1)	8.5 mH	2.6 mH
Arm Resistance (R_1)	0.1 Ω	0.1 Ω
Number of SM	4	4
Load Resistance (R_O)	18 Ω	7.2 Ω
Load Inductance (L_O)	40 mH	4.92 mH
Switching Frequency (F_{sw})	2kHz	2kHz

of 0 to 0.16 s and then switched on to the proposed method with constant load condition. Compared to conventional, the EVS algorithm has less distorted voltage waveform, and also doesn't diverge from the nominal value. Similarly, the figure 12 illustrates the comparative analysis of proposed method with conventional method in terms of execution time and also the Voltage Total Harmonics Distortion (THD). The figure 12 (a) describes the characteristics relation between execution time and the number of SM. Similarly, figure 12 (b) illustrates the comparison between modulation index with respect to the voltage THD (%). These comparative analysis once again proves the effective performances of the proposed method with traditional algorithm.

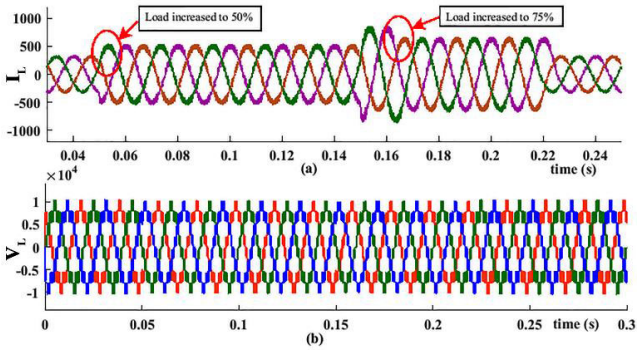

FIGURE 13. Dynamic variation (a) Load Voltage and (b) Load Current.

To verify the stability and reliable operation, the converter has to be tested with dynamic load condition, which is depicted in figure 13. During the dynamic load condition, the proposed voltage balancing method yields better results in terms of output current characteristics [shown in figure 13 (a)] and output voltage [shown in figure 13 (b)]. Furthermore, the proposed method performances are validated using variable load condition. Initially, at 0 to 0.05s the converter is tested with 25% of the rated load, and then it is increased to 50% (0.06 to 0.16s) and 75% (0.16 to 0.22s) load condition, which is depicted in figure 13. Similarly by varying the load, the performance of capacitor voltage of each SM is also analyzed and depicted in figure 14.

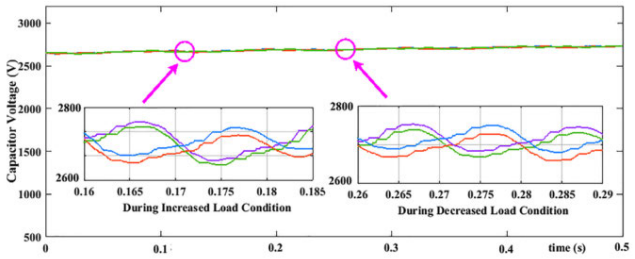

FIGURE 14. Capacitor voltage condition.

Figure 14 illustrates that, in spite of dynamic changes in the load current, SM capacitor is charged and discharged at equal amount of time without any external disturbances. When the load current increases to 50% and 75%, the capacitor ripple voltage are slightly increased to 5.43% and 6.82%, respectively. Therefore, the proposed enhanced voltage sorting algorithm has superior performances when subjected to fixed load conditions and dynamic load conditions. Apart from this, the performances of capacitor ripple voltage and circulating current are far better compared to the conventional method.

B. HVDC SYSTEM STUDY

The circuit parameters used for the HVDC system study are illustrated in figure 6 and Table 5. The AC side grid voltage, real and reactive power of station 1 are controlled by MMC 1 and similarly DC link voltage, real and reactive power are controlled by MMC 2. The validation of dynamic performance of the system can be attained by implying a step change in the reference values of grid voltage and power.

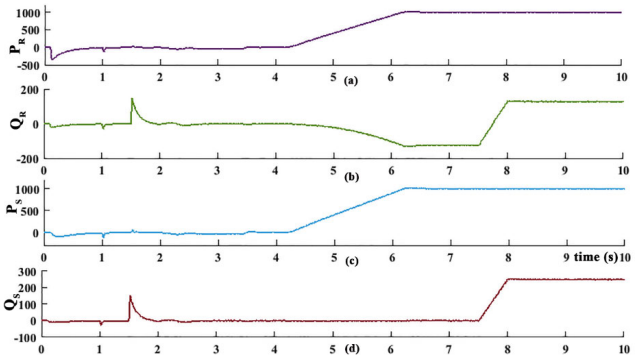

FIGURE 15. (a) Real power of station 1 (P_R), (b) Reactive power of station 1 (Q_R), (c) Real power of station 2 (P_S) and (d) Reactive power of station 2 (QS).

The step change in the reference of values of real and reactive power (P&Q) are applied at two time variation, one at 4.3 s and another one at 5.3 s, which is shown in figure 15. Initially, at 4.3 s, the real power of station 1 and 2 are distorted at short duration and attains steady state in short span of time [shown in figure 15 (a) & (c)], whereas the reactive power station 1 and 2 takes much time to deviate from the disturbances and attains its steady state, which are

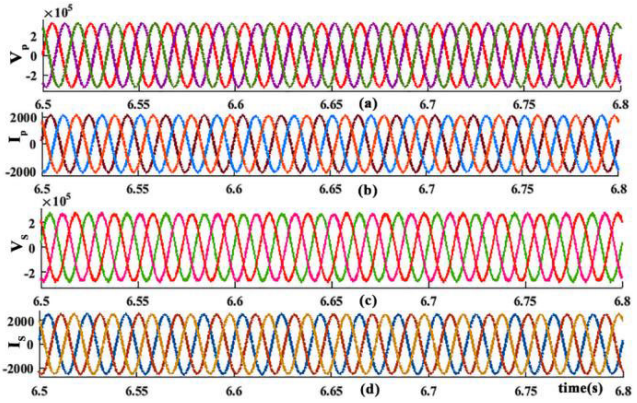

FIGURE 16. AC grid voltage and current waveform (a) primary side voltage (VP) (b) primary side current (IP) of station 1, (c) secondary side voltage (VS) (d) secondary side current (IS) of station 2.

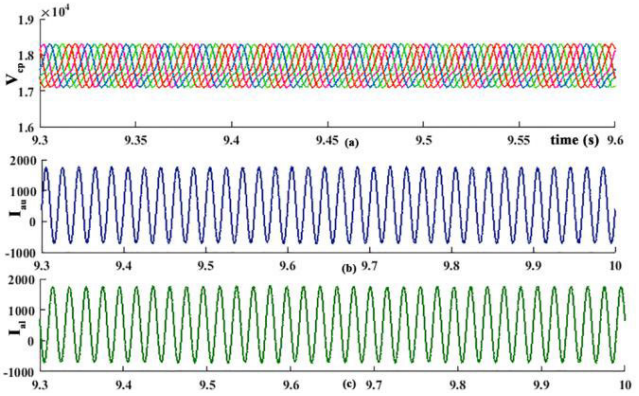

FIGURE 17. (a) Capacitor voltage of SM (V_{cp}), (b) upper arm current (I_{au}) and (c) lower arm current (I_{al}) of phase R.

shown in figure 15 (b) & (d). The small distortion at 1.3 s in figure 15 (b) & (d) due to transient occurred during breaker switching operation. Similarly, the same step changes are applied to the reference values of real and reactive power at 5.3 s and performs better compared to the first step. Thus from figure 15 concludes that, the real and reactive power recovers towards the stable conditions at short interval of time in spite of large disturbances.

TABLE 5. Simulation parameters for HVDC system.

Parameters	Simulation
Power	1000 MVA
Grid Voltage	400 kV
Transformer rating at Station1	400/333kV
Transformer rating at Station 2	333/400 kV
DC link Voltage	640 kV
Number of SM	50
Arm Inductance	40 mH
Frequency	50 Hz
Arm Capacitance	15 mF

The figure 16 illustrates the AC side grid voltage and current of station 1 and 2. The figure 16 (a) & (b) describes primary side grid AC voltage and current, similarly figure 16 (c) & (d) denotes secondary side of grid AC voltage and current. The primary side of grid voltage and current attains stability in spite of large disturbances occurred, this shows the effective performances of EVS algorithm and vector controller in obtaining fast response during large disturbances without affecting the system stability. Likewise the performances of each SM capacitor voltage is balanced properly to their nominal values during steady state and dynamic responses and ripple voltages are minimal, which are shown in figure 17. The figure 17 illustrates the performances of each SM capacitor voltage [figure 17 (a)], upper arm current [figure 17 (b)] and lower arm current [figure 17 (c)] of Phase R. Hence in spite of large disturbances occurred in the system, the capacitor voltage ripple maintains to the minimum values. The robust performances of proposed EVS algorithm are analyzed using variable load conditions and also with the HVDC system.

C. REAL TIME HARDWARE STUDY

The superior performances of the simulation study are validated by low power hardware setup, which is illustrated in figure 18 and the parameters used for designing the experiment are depicted in Table 4. The effective performances of MMC is based on the proposed method are validated using half bridge as SM topology and the number of SM selected is 4/arm. The number of triangular carrier signals used for generating switching pulse for the power devices are 4. The experimental setup consist of DC input sources, controller, MMC, Digital signal Oscilloscope (DSO) and the three phase load. The controller used in the experiment are used for generating the desired pulse signal for MMC and also for the signal conditioning. The pulse required for switching the power devices are obtained using triangular carrier signal [i.e. as discussed in the section III (A)].

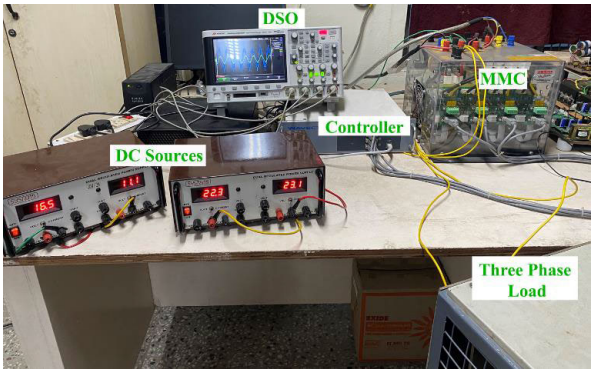

FIGURE 18. Experimental setup.

Based on the triangular carrier arrangement, the maximum number of voltage levels generated at the output of the converter will be nine level. The experimental setup are designed in such a way that, the voltage level of the converter

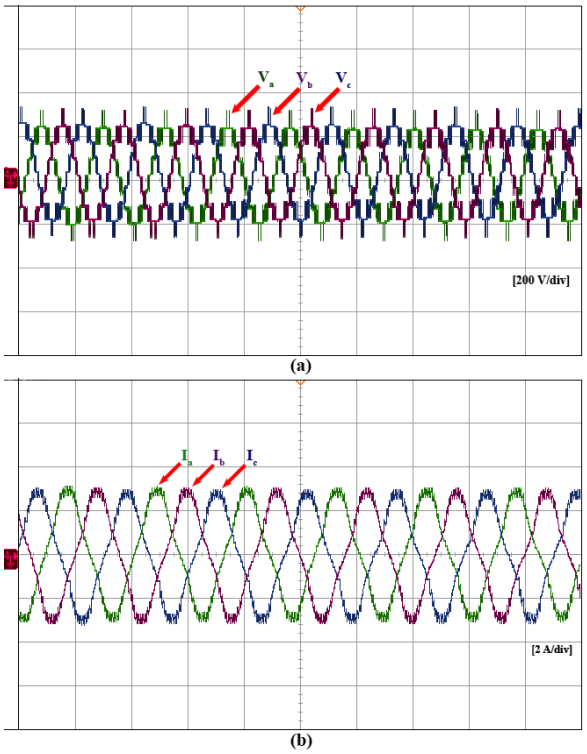

FIGURE 19. Three phase output waveform (a) Load Voltage and (b) Load Current.

can be increased by just increasing the number of SM cascaded, without change in any control parameters. The three phase line voltage and current waveform are represented in figure 19. Figure 19 (a) illustrates the three phase line to line voltage [200 V/div], which intimates that it is balanced properly similar to that of the simulation output without any external disturbances. Similarly, the line current [2 A/div] is obtained nearer to sinusoidal signal without the presence of harmonic components, shown in figure 19 (b).

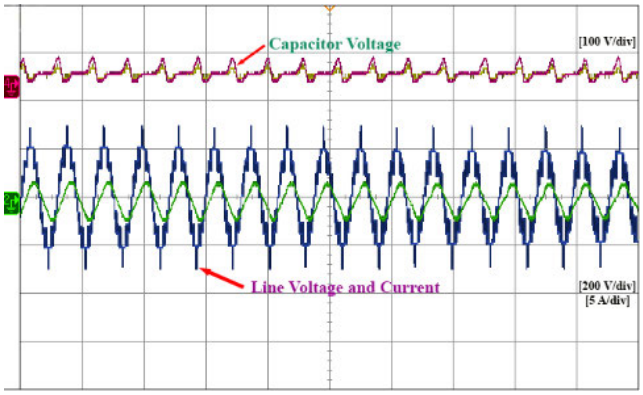

FIGURE 20. Experimental results of SM capacitor voltage and line components.

Furthermore, the performances of capacitor voltage of each SM is compared with line quantities of phase R is represented in figure 20. This shows that, the proposed sorting

TABLE 6. Comparative study of different balancing method.

S.No	Voltage Ripple (%)		Circulating current (%)	Capacitor Ripple (%)	THD (%)	Control Complexity	Total Losses (kW)
	50% of load	75% of load					
[17]	8.8	10.6	≤ 6.3	≤7.23	8.32	High	3.65
[19], [21]	9.6	11.2	≤ 7.6	≤6.56	6.58	Low	4.1
[28]	11.67	12.0	≤ 8.9	≤5.92	7.32	High	4.8
[31], [36]	8.4	13.6	≤ 8.63	≤8.3	6.23	Moderate	3.213
[EVS]	7.68	9.2	≤ 6.3	≤4.3	5.78	Low	2.78

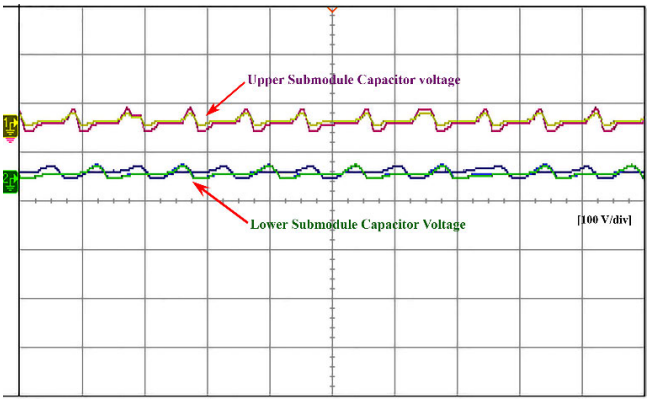

FIGURE 21. SM capacitor voltage of Phase R.

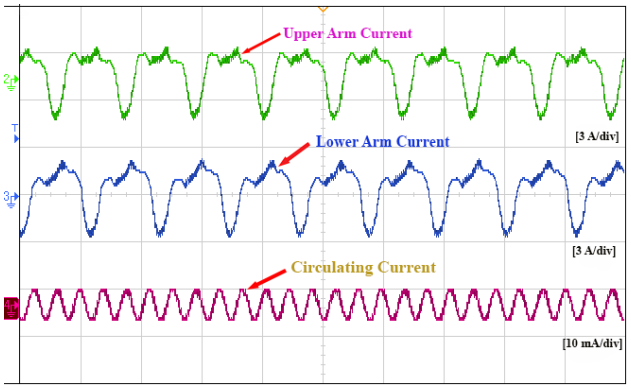

FIGURE 22. Arm current and circulating current of Phase R.

algorithm yields better results compared to other voltage balancing techniques. Where the output line voltage and current obtained for each phase is 200 V/div and similarly for each capacitor voltage is 100 V/div. The arm (upper and lower) SM floating capacitor voltage of Phase R is illustrated in figure 21. From figure 21, it denotes that the charging and discharging of each SM capacitor is obtained uniformly and also the voltage balancing of each capacitor is achieved with less voltage ripple in each phases of MMC. Similarly, the circulating current and arm current characteristics of phase R are depicted in figure 22. The arm current (upper and lower) flowing in between source to load of phase R represents that, the effect of DC components in AC output of the converter is less. Furthermore, the upper and lower arm voltage of the

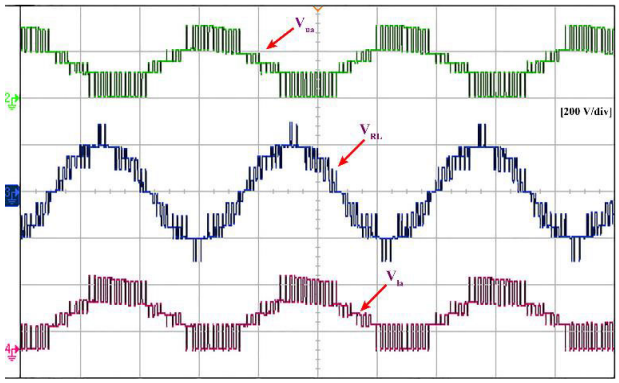

FIGURE 23. Arm voltage (V_{ua}&V_{la}) with the output voltage (V_{RL}) of Phase R [200 V/div].

MMC are depicted in figure 23. Thus from the above results, the enhanced voltage sorting algorithm has superior performances in terms of balancing the capacitor voltage in each SM, which henceforth reduces ripple voltage and suppresses the circulating current within the permissible limit.

V. COMPARATIVE STUDY

The superior performances of the proposed voltage balancing algorithm are analyzed with different balancing algorithm and the comparative results are depicted in Table 6. For better understanding, the conduction and switching loss of MMC are calculated for different power rating and their performance characteristics are depicted in figure 24. In figure 24 (a) & (b), compared to different voltage balancing methods, the proposed voltage balancing has better performance in terms of conduction and switching loss. Apart from this, comparative analysis of different balancing techniques subjected to voltage ripple, circulating current, Total harmonics distortion (THD), control complexity and total loss are analyzed and the results are depicted in Table 6. The voltage ripple are calculated by testing the different balancing methods by two different load conditions such as 50% and 75%. Based on the analysis, the proposed sorting algorithm yields the better performances compared to other algorithms. Similarly, the same testing are performed to analyze circulating current, THD etc., and their performances are tabulated. The comparative study of voltage ripple are analyzed in terms of % because during the different load conditions the increase

in the ripple voltage can be easily understood. Similarly, the same can be analyzed for circulating current suppression. Hence, from the comparative study, the proposed sorting algorithm yield superior performances compared to other voltage balancing techniques.

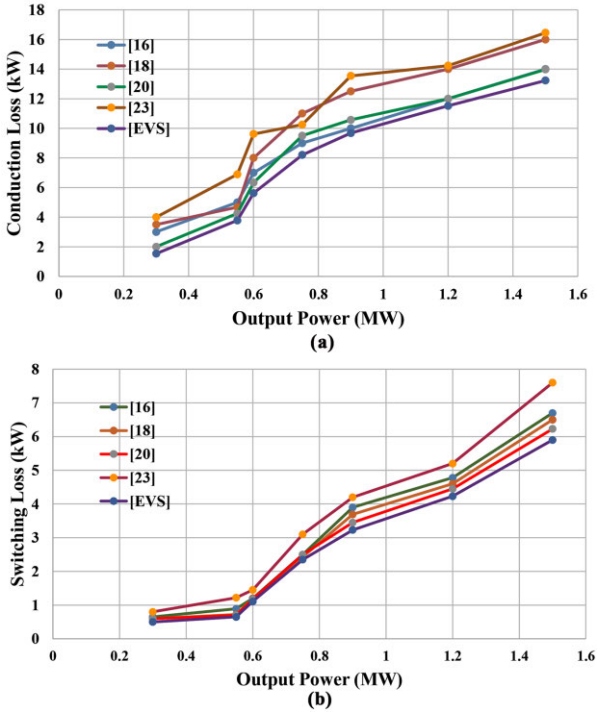

FIGURE 24. Comparison of power loss (a) Conduction loss and (b) Switching loss.

VI. CONCLUSION

Thus the paper illustrates the superior performances of enhanced voltage sorting algorithm applicable to the modular multilevel converter. Apart from the voltage balancing operation, the proposed method is used to reduce the ripple voltage of the floating capacitor and also subdues the circulating current to prescribed limit, which henceforth increases the efficiency, stability, safe and reliable operation of MMC. The proposed algorithm rectifies the SM capacitor issues by generating a pulse signal pattern based on modulation methodology and the obtained signals are then compared with hybrid state condition and dynamic implicit number variables from the voltage sorting algorithm. This comparative process will generate a dynamic switching signal which are henceforth compared with switching logic state signals and generates the desired switching signals for the power devices. Hence by doing so, the capacitor voltage are balanced uniformly during steady state as well as dynamic conditions. Likewise, it also reduces the ripple voltage to a permissible limit and suppresses the circulating current compared to the conventional method. However, in future, the proposed EVS method will be tested with DC fault handling capability, common mode voltage issues and variable switching frequency performances. Thus the superior performances of the enhanced voltage sorting algorithm are tested by variable load conditions and HVDC system using MATLAB/Simulink software and real time hardware prototype environment.

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