IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received October 31, 2021, accepted December 3, 2021, date of publication December 7, 2021, date of current version December 20, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3133575

Role of Schottky Barrier Height Modulation on the Reverse Bias Current Behavior of MIS(p) Tunnel Diodes

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This work was supported in part by the Ministry of Science and Technology, Taiwan, under Grant MOST 110-2221-E-002-140 and Grant MOST 110-2622-8-002-014.

ABSTRACT Current and capacitance characteristics of Al/SiO_2/Si(p) metal-insulator-semiconductor tunnel diode (MISTD) with oxide thickness in the range of about 2-4 nm were fabricated and studied in detail in this work. We found that the saturation reverse bias current will increase with oxide thickness in this range of oxide thickness. This non-intuitive phenomenon is caused by different levels of Schottky barrier height modulation (SBHM), which leads to the injection of the majority from metal. The majority current of Al/SiO_2/Si(p) MISTD is usually neglected because of the blocking of the oxide layer and the Schottky barrier. The mechanism and numerical analysis of SBHM are discussed in this work. SBHM is significant when the oxide is thin enough for the majority to tunnel from metal to semiconductor and thick enough to hold a part of the minority inversion layer. In this specific oxide thickness range, increasing oxide thickness will increase the ability to hold the inversion layer, thus leading to higher oxide voltage (V_{ox}) and stronger SBHM. As a result, we find that stronger SBHM lets more majority have enough energy to inject from metal to semiconductor and cause higher reverse saturation current in MISTD with thicker oxide. With the numerical analysis in our work, we also predict this non-intuitive phenomenon will start to turn around when oxide thickness is thicker than about 33Å. This phenomenon indicated that majority current is an un-neglectable component when the oxide is thick enough to hold the inversion layer partially. The analysis in this work is also helpful to complete the missing part of the theory describing the current behavior of MISTD.

INDEX TERMS Metal-insulator-semiconductor (MIS), Schottky diode, Schottky barrier height, ultra-thin oxide.

I. INTRODUCTION

The dimension of MOSFET keeps scaling down to improve area consumption, power consumption, and operation speed. At the same time, operation voltage is also scaled down to avoid the breakdown of the devices. However, decreasing gate voltage and channel length will decrease the gate's ability to control the channel and lead to serious short channel effects. To overcome the problem, thinner oxide should be adopted to increase gate control. With keep thinning of oxide, significant gate leakage becomes a considerable problem needed to be solved. Metal-insulator-semiconductor (MIS) tunnel structure with ultrathin insulator layer is not considered when serving as a part of traditional transistors because of its high leakage current [1] and the problem of nonuniformity [2]. At this time, high-k material appears and gets huge success [1] because high-k can keep high gate control with a thick dielectric layer. Nowadays, most of the studies of gate dielectrics are focused on high-k materials. Previously, some works still finely described the current behavior of metal-insulator-semiconductor tunnel diode (MISTD). Green *et al.* developed the theory [3], and Shewchun *et al.* experiment [4]

The associate editor coordinating the review of this manuscript and approving it for publication was Sneh Saurabh.

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in 1974. Reference [3] considered that $Al/SiO_2/Si(p)$ MISTD is a minority device and the experiment in [4] confirmed the theory quite well. In 2001, Lin *et al.* further discussed the current behavior of $Al/SiO_2/Si(p)$ MISTD [5]. Reference [5] further confirmed that the current of $Al/SiO_2/Si(p)$ MISTD is dominated by the minority and finely describe the generation mechanism of MISTD. However, some studies of MISTD find that the current behavior is difficult to be described by [3]–[5]. For example, studies focus on deep depletion [6], fringing field [7], [8], oxide nonuniformity [6], [9], and carrier lifetime [10] all find increasing reverse bias current with oxide thickness. This phenomenon is difficult to be interpreted by [3]–[5]. We find that the critical point is the oxide thickness. Devices with oxide thickness of 18Å and 13-18Å were fabricated in [4] and [5], respectively. Oxide with such thickness is difficult to hold inversion charge and builds significant oxide voltage. Thus, we considered that the current and capacitance behaviors of MISTD with oxide thick enough to hold the inversion charge partially are a relatively unknown field. To get a deeper understanding of MISTD's mechanism, a model connecting the observed characteristics between current and capacitance behavior of MISTD is fundamental and is of interest for the possible application of MISTD.

In [6]–[10], we can find that the reverse bias saturation current increases with oxide thickness. This phenomenon is believed to be caused by the Schottky barrier height modulating (SBHM) when a thin insulator layer is located between metal and semiconductor. However, previous works only briefly gave the concept but not the detailed mechanism of the phenomenon. In this work, devices with four different oxide thicknesses also show the same phenomenon. Detailed analysis on this phenomenon was performed, and a relatively complete model was derived.

II. EXPERIMENTAL

In this work, a boron-doped p-type silicon substrate with a doping concentration of 10^{16} cm^{-3} and surface crystal orientation of (100) was adopted as substrate. Radio Corporation of America (RCA) clean process was used to remove organic particles, metal ion, and native oxide on the wafer. After the RCA clean, thin oxide with thickness between 27∼31Å was grown by anodization [11] in de-ionized water at room temperature. A rapid thermal annealing (RTA) process (950 °C, 15s in 20 torr N_2 ambient) was followed after the oxide growth to improve the oxide quality. An aluminum layer with a thickness of 200 nm was then thermally evaporated on the oxide as the top electrode. After forming the aluminum layer, we do the patterning and wet etching to define circle devices with a diameter of 170 μm (the area is 2.27×10^{-4} cm^2). The back oxide was then removed by buffer oxide etchant (BOE) process after the definition of the pattern. At last, an aluminum layer with a thickness of 200 nm was thermally evaporated as back contact. The schematic of the devices is attached in Fig. 1(a).

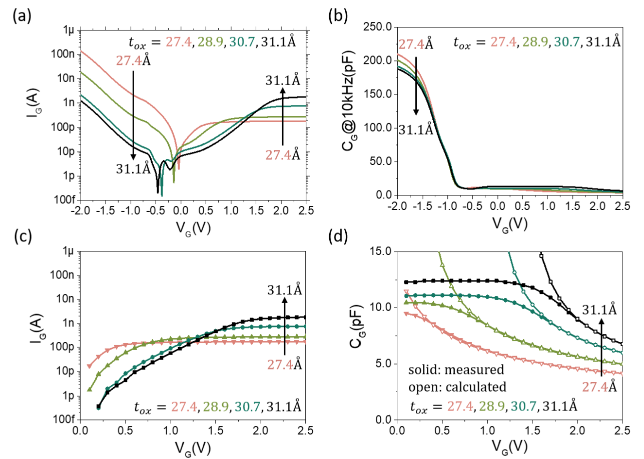

FIGURE 1. (a) and (b) are I_G-V_G and C_G-V_G sweeping from −2 to 3V and −2 to 2V, respectively. The schematic of the devices is also attached in (a). (c) and (d) are steady-state characteristics of I_G-V_G and C_G-V_G, respectively. The steady-state is measured by biasing the device at each voltage for 10 seconds from 0.1 to 2.5V in a step of 0.1V increment.

The devices with four different oxide thicknesses were then measured by Agilent B1500A. Figs. 1(a) and (b) show the I_G-V_G sweeping from −2V to 2.5V and high-frequency capacitance C_G-V_G sweeping from −2 to 2.5V at 10 kHz, respectively. This figure named the electrode as gate, the measured current as I_G, and the measured capacitance as C_G. We then extracted the oxide thickness from interpolating I_G at $V_G = -0.9$V with our database. The equation used to do the interpolate is

$$t_{ox} = t_{ox1} + (t_{ox2} - t_{ox1}) \frac{(\log(I_{G1}) - \log(I_G))}{(\log(I_{G1}) - \log(I_{G2}))}, \quad (1)$$

where t_{ox} is oxide thickness of the target device, t_{ox1} and t_{ox2} are oxide thickness of devices chosen from the database, I_G is current of the target device at $V_G = -0.9$V, I_{G1} and I_{G2} are current of devices with oxide thickness t_{ox1} and t_{ox2} at $V_G = -0.9$V. I_{G1} and I_{G2} are chosen to agree with the condition $I_{G2}<I_G<I_{G1}$. t_{ox1} and t_{ox2} are determined by taking the transmission electron microscopy (TEM) graph. The oxide thicknesses of the four devices in this work are 27.4, 28.9, 30.7, and 31.1Å. We can intuitively figure out that devices with thicker oxide will have a lower leakage current. The matches with the result we measured in the negative and small positive parts as shown in Fig. 1(a). However, the situation starts to turn around at a larger positive bias (reverse bias for MIS with p-type substrate). When the bias voltage exceeds about +1.5V, we can observe that devices with thicker oxide will have larger saturation currents. This result is complete reverse to the trend of negative bias currents. To finely and precisely ensure this phenomenon, we measured I_G and C_G by biasing the devices at each voltage for 10 seconds to avoid the transient effect. The I_G and C_G's measured results from 0.1 to 2.5V in a step of 0.1V increment were shown in Figs. 1(c) and (d), respectively. The observation is stable and reproducible.

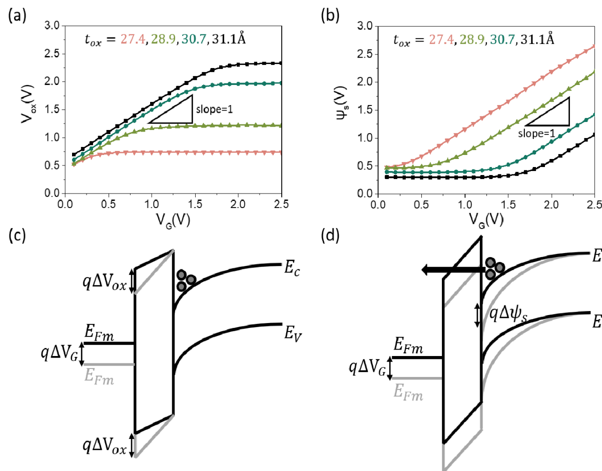

FIGURE 2. (a) and (b) are extracted oxide voltage (V_{ox}) and band bending (ψ_S) from C_G-V_G. (c) shows the band diagram when the oxide is able to hold the inversion charges under low voltage, and the applied voltage mainly drops across oxide, i.e., ΔV_{ox} increases with ΔV_G. (d) shows the band diagram under high voltage, and the oxide is unable to hold the inversion charges. The device starts to deep depletion, and most of the applied voltage drops on the substrate, i.e., $\Delta\psi_S$ increases with ΔV_G.

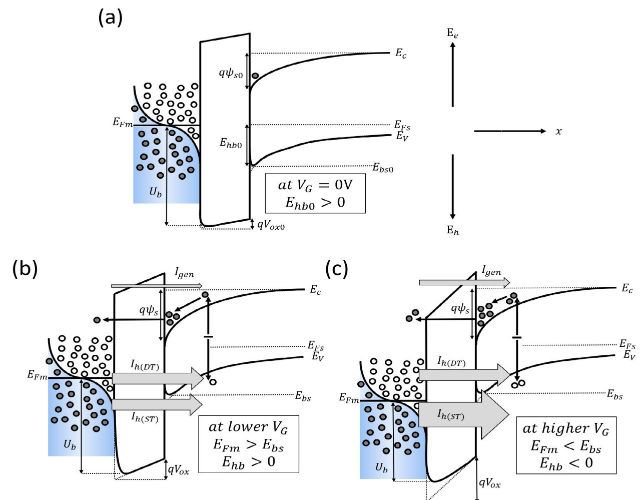

FIGURE 3. (a) Shows the band diagram at $V_G = 0$V. (b) shows the band diagram with small V_G applied, and there is still a positive hole barrier (E_{hb}). (c) shows the band diagram with relatively larger V_G applied, and the hole barrier (E_{hb}) is modulated to a negative value.

III. RESULT AND DISCUSSION

A. EXTRACTION OF OXIDE VOLTAGE AND SURFACE BAND BENDING

Oxide voltage (V_{ox}) and surface band bending (ψ_s) are the two most important parameters when calculating tunneling probability, Schottky barrier height and depletion region. To get these two important parameters, analyzing capacitance-voltage relation is a useful tool [12]. However, the traditional method in [12] is only suitable for metal-oxide-semiconductor (MOS) capacitance with thick oxide. Thus, the traditional method is needed to be slightly adjusted. A universal method considering deep depletion and oxide nonuniformity was reported in [6]. In our work, this method was adopted to analyze the behavior of our C_G-V_G curves. The calculated results were plotted in Fig.1 (d) and were compared with the measured result. These calculated results assuming deep depletion of devices were plotted by open symbols. Fig.1 (d) shows that the measured curves keep at a constant value at a small bias voltage. This is the same as the traditional MOS capacitor. However, the capacitance value then starts to decrease when the bias voltage is larger than a critical value. The tendency of decreasing capacitance can fit quite well with the calculated results assuming deep depletion. This indicates that the MISTD acts like a traditional MOS capacitor at low voltage but starts deep depletion at high voltage. Fig. 1 (d) shows that samples with thicker oxide can hold inversion charges to a higher voltage, and samples with thinner oxide go into deep depletion at a lower voltage. These results can be more clearly seen in Figs. 2(a) and (b), which are V_{ox} and ψ_s extracted from the measured results in Fig. 1(d). In Fig. 2(a), we can see that V_{ox} increases at almost the same rate of V_G at low voltage because the V_{ox} keeps increasing with inversion charges, as shown by the band diagram in Fig. 2(c). On the contrary, in Fig. 2(b), we see that ψ_s increases at almost the same rate of V_G at high voltage. The band diagram indicating the increase of ψ_s with V_G is shown in Fig. 2(d). The phenomenon of holding inversion charges at low voltage and going into deep depletion at high voltage can only be observed at steady-state measurement or sweeping at extremely slow speed. This is because the oxide is tunnelable so that the inversion charges keep leaking when the electrons are generating. It takes time to form the inversion layer. In our work, we bias at each voltage for 10 seconds, and if the rate of electron generating is larger than the rate of leaking, the steady-state inversion layer will have enough time to form, and most of the applied voltage will drop on V_{ox}. However, the tunneling probability will exponentially increase with increasing of V_{ox}. At a critical voltage, the magnitude of the generated electrons cannot overcome the leaked electrons. Then the device starts to deep depletion. In this situation, most of the applied voltage will drop on ψ_s. With the extracted V_{ox} and ψ_s, we can further calculate the current components of MISTD according to these two parameters.

B. MINORITY CURRENT (GENERATION CURRENT)

Before calculating of SBHM and majority injection, minority current is first calculated here. Minority current is a usually considered as a dominate component of MISTD [3]–[5]. This component is easy to figure out because an inversion layer is held by thin oxide and keeps leaking electrons to the electrode. The minority supplied by silicon substrate due to generation should balance the leaked electrons. When $V_G = 0$ as shown in Fig. 3(a), the leaked electrons are balanced by electrons emission from metal to silicon, and no net current occurs. However, in Figs. 3(b) and (c) with V_G applied, the inversion charges start to have a net leaking rate and need the supplement of electrons by generation.

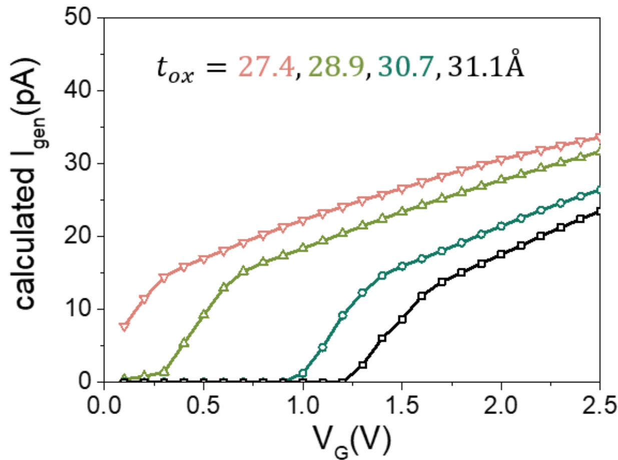

FIGURE 4. The calculated electron generation current of four devices with different oxide thicknesses.

There are two supply sources of electrons. The first component is the minority diffusion from bulk, and the second is the thermal generation of the minority within the depletion region. In semiconductors with relatively low intrinsic carriers (such as silicon), the diffusion component of the minority is about two to three orders lower than generation current and is negligible [13]. Because of the low proportion of diffusion current, we only considered the generation current here. We then started from the Shockley-Read-Hall model [13] for the recombination rate as represented by (2), as shown at the bottom of the page, where σ_n and σ_p are capture cross-sections of electron and hole, v_{th} is the thermal velocity of the carrier, n and p are carrier concentrations of electron and hole, n_i is intrinsic carrier concentration, $N_t(E_t)$ is the number of bulk traps depending on energy level, E_t is energy level of trap, and E_i is intrinsic Fermi level. Usually, only active bulk traps near the mid gap are considered. At the same time, $1/(\sigma_n v_{th} N_t) \approx 1/(\sigma_p v_{th} N_t) = 1/(\sigma v_{th} N_t)$ is usually adopted. When the device starts to deep depletion, the amount of carriers starts to decrease. The generation rate in the bulk of silicon can finally be reduced to

$$G = -U \approx \frac{n_i[1 - \exp(-q\Delta\phi/kT)]}{\frac{2}{\sigma v_{th} N_t}}, \tag{3}$$

where $\Delta\phi$ is the difference of electron and hole quasi-Fermi levels. Though $\Delta\phi$ is an undetectable value, we can use the difference of band bending $\Delta\psi_s$ between considered voltage and initial band bending to replace this value. At last, we integrate through the depletion region W_d to calculate generation current.

$$I_{gen} = q\int_0^{W_d} \frac{n_i\left[1 - \exp\left(-\frac{q\Delta\psi_s}{kT}\right)\right]}{\tau} dx, \tag{4}$$

In equation (4), carrier lifetime $\tau = 1/(\sigma v_{th} N_t) = 10^{-6}$ s [14] are adopted. The calculated result is plotted in Fig. 4.

The result makes sense at first glance because MISTD with thicker oxide needs less generation carrier to balance the leakage current. Thus, thicker oxide has a lower generation current. However, this result of considering only generation current is not complete to explain the whole measured results. When only considering generation current, reverse bias current decrease with increasing oxide thickness. This is different from the measured result. By the way, the value of calculated generation currents is in the range of tens of pico-ampere, which are far below the measured results (up to the order of nano-ampere). Clearly, the current-thickness relation cannot be decided by only considering minority current. However, when comparing the measured result in Fig. 1(c) and the generation current in Fig. 4, we can find that the measured current starts to saturate when the generation current starts to appear. This indicated that the current of MISTD starts to saturate when the oxide becomes leak enough and difficult to hold the generated minority. In this situation, the inversion layer is difficult to increase, and oxide voltage V_{ox} starts to pinch at a saturation value. Though generation current cannot fully describe the current behavior of MISTD, we can still conclude that the current of MISTD is strongly influenced by the generation and accumulation of minority. To further analyze the other current components of MISTD, the majority current calculation was discussed below.

C. MAJORITY CURRENT WITH CARRIER ENERGY HIGHER THAN SILICON BARRIER

The majority is usually neglected when analyzing the reverse bias current of MISTD because of the blocking of oxide and the Schottky barrier of silicon. However, we will show that the injection of the majority current is important in this oxide thickness range because of SBHM. To calculate the majority current, we can use the concept of the Schottky diode. The reverse bias current of Schottky diode is mainly calculated from the integral of the metal's carriers which have energy higher than silicon barrier and thermal emission into silicon [15] (to be mentioned that the carrier conducting in aluminum is hole [16]). However, MISTD has two properties different from the traditional Schottky diode. First, a thin oxide is located between metal and silicon; thus, the tunneling probabilities of different energy levels need to be considered.

$$U = \frac{(np - n_i^2)}{\frac{1}{\sigma_p v_{th} N_t(E_t)}\left[n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right] + \frac{1}{\sigma_n v_{th} N_t(E_t)}\left[p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right]}, \tag{2}$$

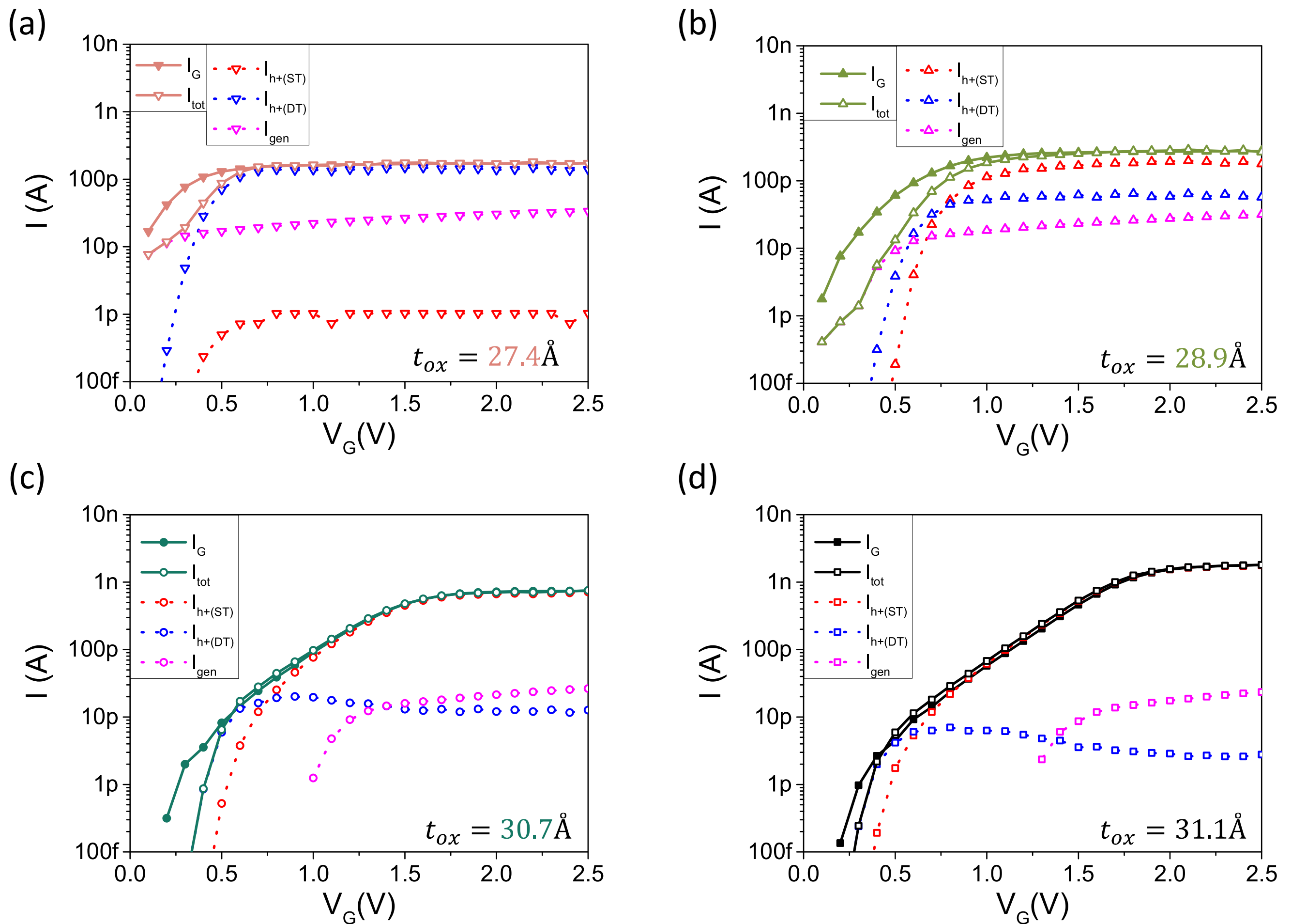

FIGURE 5. (a), (b), (c), and (d) are the measured current and the calculated results of four currents, i.e., I_{tot}, $I_{h(ST)}$, $I_{h(DT)}$, and I_{gen} in log scale with the oxide thickness of 27.4, 28.9, 30.7 and 31.1Å, respectively. The measured currents are presented by solid symbols, while the calculated results open symbols.

Second, as shown in Fig. 3, we can observe that the Schottky barrier height of MISTD strongly depends on V_{ox}. If we calculate the energy barrier between metal Fermi level (E_{Fm}) and the top of Schottky barrier of silicon (E_{bs}) in Fig. 3 by the equation

$$E_{hb} = -(E_{bs} - E_{Fm}), \tag{5}$$

where E_{hb} is the calculated hole Schottky barrier height, E_{bs} is the top of silicon barrier, and E_{Fm} is the Fermi level of metal. It is clear that the hole Schottky barrier height can even be modulated from a positive value (as shown in Figs. 3(a) and (b) with zero and lower V_G) to a negative value (as shown in Fig. 3(c) with higher V_G). To be mentioned that holes have higher energy at the lower position in the band diagram; thus, a negative sign is added in equation (5). Because of the modulation of hole Schottky barrier height, different barrier height at different bias voltage also needs to be considered. At the same time, the majority (hole) with energy higher than the Schottky barrier only need to tunnel through the oxide; thus, we labeled it as $I_{h(ST)}$ where "h" indicated hole and "ST" indicated single tunneling. $I_{h(ST)}$ is also plotted in Figs. 3 (b) and (c). Then we can write down $I_{h(ST)}$ as

$$\begin{aligned} I_{h(ST)} &= \mathrm{Aq} \int_{v_x > v_{x0}(V_{ox})}^{+\infty} v_x P_{t,ox}\left(V_{ox}, v_x\right) N\left(v\right) f_{Fh}\left(E_h\right) dv \\ &= \frac{2\mathrm{Aq} m_h^{*3}}{h^3} \int_{v_{x0}(V_{ox})}^{+\infty} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \frac{v_x P_{t,ox}\left(V_{ox}, v_x\right)}{1 + \exp\left(\frac{E_h - E_{Fm}}{kT}\right)} \\ &\quad \times dv_z dv_y dv_x, \end{aligned} \tag{6}$$

where A is the area of the devices, q is the charge per carrier, v_x is the component of hole velocity perpendicular to the surface of silicon (the direction of x is also labeled in Fig. 3), $v_{x0}(V_{ox})$ is the velocity of hole that needs to overcome the hole Schottky barrier in silicon, $P_{t,ox}(V_{ox}, v_x)$ is oxide tunneling probability, $N(v)=(4\pi v^2)2m_h^*/h^3$ is the density of state in metal, m_h^* is the effective mass of hole in aluminum, h is Planck constant, $v = (v_x^2 + v_y^2 + v_z^2)^{1/2}$ is the velocity of hole, f_{Fh} (E_h) is Fermi-Dirac distribution of hole and $E_h = m_h^* v^2/2$ is the kinetic energy of hole. E_h is

increasing toward the bottom of the band diagram as labeled in Fig. 3. We again mentioned that the carriers in aluminum are holes [16]; thus, we can do the calculation in the viewpoint of the hole. Equation (6) sources from the equation of traditional Schottky diode [15], except three important adjustments are considered, 1) oxide tunneling probability $P_{t,ox}(V_{ox}, v_x)$ is inserted, 2) $v_{x0}(V_{ox})$ depends on V_{ox} because of Schottky barrier height modulation and 3) a full Fermi-Dirac distribution is considered. Traditionally, the Boltzmann approximation is adopted when calculating the current of the Schottky diode because the Schottky barrier is usually larger than 3kT. However, in the case of MISTD, the hole Schottky barrier will be modulated from positive value to negative value, as shown in Fig. 3. When the Fermi level of metal (E_{Fm}) is modulating near the top of the silicon barrier (E_{bs}), the occupancy probability of tunnelable hole is neither Boltzmann distribution nor step function; thus the full Fermi-Dirac distribution is considered. After doing the integral, we can further reduce equation (6) into

$$\begin{aligned} I_{h(ST)} &= \frac{4\pi m_h^* AqkT}{h^3} \int_{v_{x0}(V_{ox})}^{+\infty} v_x P_{t,ox}(V_{ox}, v_x) \\ &\quad \times \ln(1 + e^{-\frac{E_{hx}-E_{Fm}}{kT}}) dv_x \\ &= \frac{4\pi m_h^* AqkT}{h^3} \int_{E_{hb}(V_{ox})}^{+\infty} P_{t,ox}(V_{ox}, E') \ln(1+e^{-\frac{E'}{kT}}) dE', \end{aligned} \tag{7}$$

where $E_{hb}(V_{ox})$ is hole Schottky barrier height calculated from equation (5), $E'=E_{hx}-E_{Fm}$ is the difference between hole energy and Fermi energy, and $E_{hx}=m_h^* v_x^2/2$ is hole kinetic energy in the x-direction. With the assist of the band diagram in Fig. 3 and the including of image force lowering, we can write down that

$$\begin{aligned} E_{hb}(V_{ox}) = E_{hb0} - q[(V_{ox} - V_{ox0}) \\ +(\Delta\phi_{im,Si} - \Delta\phi_{im,Si0})] \end{aligned} \tag{8}$$

where E_{hb0} is hole Schottky barrier height at $V_G = 0$ V. The situation of the band diagram at $V_G = 0$ V is plotted in Fig. 3(a). ψ_{s0}, $\Delta\phi_{im,Si0}$, and V_{ox0} are band bending, image force lowering, and oxide voltage at zero voltage, respectively. The term $q(V_{ox}-V_{ox0})$ in equation (8) indicates the Schottky barrier height modulation of MISTD. Then we adopt the tunneling probability by using WKB approximation [17]

$$P_{t,ox}(V_{ox}, E') = \exp[-\frac{4\sqrt{2m_{ox}^*}}{3\hbar q E_{ox}}((U_b)^{\frac{3}{2}} + (U_b - qV_{ox})^{\frac{3}{2}})], \tag{9}$$

where $m_{ox}^* = 0.58$ is the hole effective mass in oxide extracted by Fowler–Nordheim tunneling current [18], ε_{ox} is the oxide field, and U_b is the oxide barrier height looking from metal by the hole. The dependency of U_b and E' can be written down as

$$U_b = U_{b0} - E' - q\Delta\phi_{im,ox}, \tag{10}$$

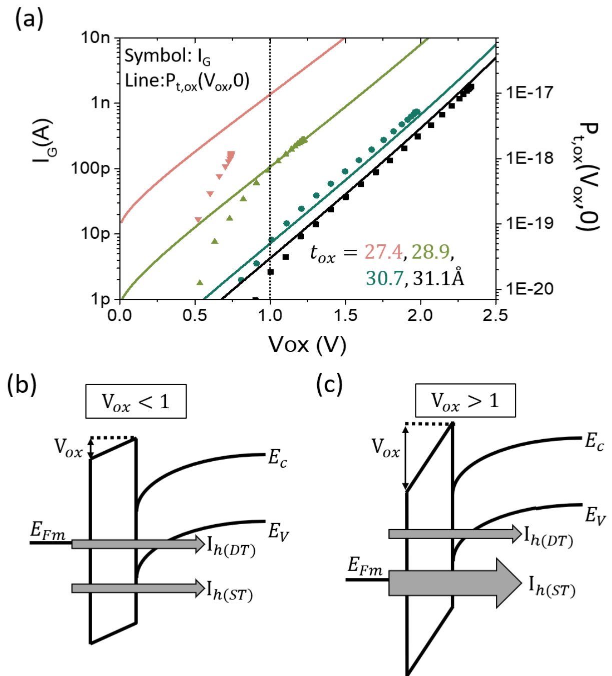

FIGURE 6. (a) Is measured current and calculated hole tunneling probability versus V_{ox}. (b), and (c) are band diagrams of slight and strong SBHM, respectively.

where U_{b0} is the oxide barrier height seen from the Fermi level of metal by the hole. At the same time, the image force lowering of oxide $q\Delta\phi_{im,ox}$ is also considered. Theoretically, U_{b0} is 5.8eV. However, because of the nonuniformity of oxide [2, 6, 9], trap assist tunneling [19], and the existence of SiO_x layer for about 5Å [2], a lower value of $U_{b0} = 4.3$eV is adopted to fit the experimental result. Though 4.3eV is lower than the theoretical value, it still much higher than 3.1eV, which is the theoretical barrier seen by electrons when electrons tunnel from silicon to metal. This fitting barrier height indicates that minority do not dominate the currents. At last, from equations (7) to (10), we can build a model that depends on ψ_s and V_{ox}, which are extracted from the C_G-V_G curve. In this model, only one fitting parameter $U_{b0}$is used. The calculated result of $I_{h(ST)}$ for devices are plotted by red open symbols in Fig. 5 in log scale. From Fig. 5, we observe that $I_{h(ST)}$ only matches the measured results at higher bias voltage for two thicker devices. This indicates that $I_{h(ST)}$ is not very correct at low oxide voltage. In other words, $I_{h(ST)}$ is not complete for total current when the SBHM is not strong enough. When there is only a slight SBHM, a positive hole Schottky barrier (E_{hb}) exists; thus, most holes do not have enough energy to overcome the hole Schottky barrier in silicon. In this case, most holes need to tunnel through the oxide and then tunnel through the hole Schottky barrier in silicon to inject into the substrate. In the next section, we will discuss this current component.

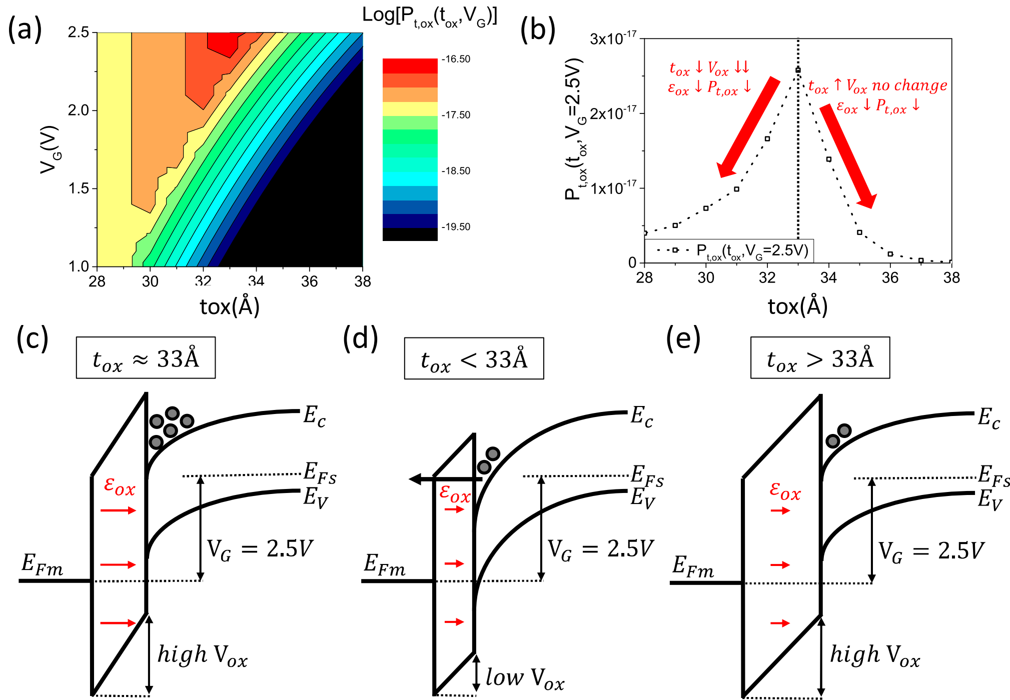

FIGURE 7. (a) Is hole tunneling probability near E_{Fm} at different oxide thickness and bias voltage. (b) is the extracted value from (a) at $V_G = 2.5V$. (c), (d), and (e) are band diagrams of MISTD with the oxide thickness around, thinner than, and thicker than 33Å.

D. MAJORITY CURRENT WITH CARRIER ENERGY LOWER THAN SILICON BARRIER

Because the majority current with energy lower than silicon barrier needs to tunnel through the oxide and the hole Schottky barrier in silicon as shown in Figs. 3(b) and (c), we named this current component as $I_{h(DT)}$, where "h" indicates hole and "DT" indicates double tunneling. With the help of the concept above, we can write down $I_{h(DT)}$ as

$$I_{h(DT)} = \frac{4\pi m_h^* AqkT}{h^3} \int_{-\infty}^{E_{hb}(V_{ox})} P_{t,ox}\left(V_{ox}, E'\right) \times P_{t,Si}\left(V_{ox}, E'\right) \ln(1 + e^{-\frac{E'}{kT}})dE', \quad (11)$$

This equation is similar to equation (7), except the integral range was changed, and the tunneling probability of silicon barrier $P_{t,Si}(V_{ox},E')$ was inserted. Here, we assumed silicon barrier as a triangular barrier and adopted the tunneling probability as

$$P_{t,Si}\left(V_{ox}, E_x\right) = \exp[-\frac{4\sqrt{2m_{si}^*}}{3\hbar q \mathcal{E}_{Si}}\left(U_{b,Si}\right)^{\frac{3}{2}}], \quad (12)$$

where $\mathcal{E}_{Si}$ is the surface field of silicon and $U_{b,Si}$ is the silicon hole Schottky barrier height seen by holes in the metal. $\mathcal{E}_{Si}$ is calculated by Poisson's equation. Using the equations (11), and (12), we can calculate $I_{h(DT)}$, which was plotted in blue open symbol in Fig. 5. At the same time, the generation current plotted in the pink open symbol is also shown in Fig. 5. At last, the total currents $I_{tot} = I_{gen} + I_{h(ST)} + I_{h(DT)}$ were summed up and plotted in Fig. 5. In Fig. 5, we can find that I_{tot} has the tendency that its magnitude is very close to the measured current. This indicated that I_{gen}, $I_{h(ST)}$, and $I_{h(DT)}$ give each contribution to the current of MISTD. However, if we look closer into the calculated results, we can find that the importance of each component will vary with different oxide thicknesses and applied voltage.

E. PREDICT THE CRITICAL THICKNESS OF MISTD

The model built above can describe the phenomenon of a larger reverse bias current at MISTD with thicker oxide. However, it is imaginary that the importance of SBHM and majority injection will start to decrease if the oxide is thick enough to block the majority in metal. When the oxide thickness increases above a critical thickness, the reverse bias current of MISTD will start to decrease. A more straightforward method to quickly predict reverse bias current is adopted to predict this critical oxide thickness. From Fig. 3(c), we can find that if the SBHM is strong enough, the total current is dominated by $I_{h(ST)}$. Thus, in this simplified method, we only considered $I_{h(ST)}$. When only considering $I_{h(ST)}$, two concepts can be considered to simplify the calculation further. First, because the tunneling probability strongly depends on the hole energy, we assumed that the tunneling of holes with energy much lower than holes near E_{Fm} is negligible. Second, because the magnitude of holes with energy higher than holes near E_{Fm} will decay exponentially with energy, thus the tunneling hole current with too high energy is also negligible. From the two concepts above, we can assume that $I_{h(ST)}$ is only dominated by the tunneling holes near E_{Fm}. As a result, if the Schottky

barrier height modulation is strong enough, the current tendency will strongly depend on the hole tunneling probability near E_{Fm}. Thus, we plotted the variation of oxide tunneling probability versus V_{ox} in Fig. 6(a) by using equation (9) at $E'=0$. At the same time, the measured current is also labeled in solid symbol in Fig. 6(a). In Fig. 6(a), we can observe that equation (9) can match the tendency of measured I_G when oxide thickness is thick enough, and V_{ox} is modulated to higher than about 1V. The band diagram of this situation with strong SBHM is also plotted in Fig. 6(c). When V_{ox} is smaller than about 1V, $I_{h(DT)}$ starts to play an important role. We can observe a steeper increasing slope but a lower value of I_G in this range of V_{ox}. This situation of slight SBHM is also plotted in Fig. 6(b).

At last, we calculated equation (9) in the conditions of thicker oxide thickness (28-38Å) and higher bias voltage (1-2.5V) to predict the critical thickness of MISTD. The calculated result is plotted in Fig. 7(a). In Fig. 7(a), we can observe that when the bias voltage is high enough, the current will increase with oxide thickness at first and then turn around at a critical thickness. We extract the value at $V_G=2.5V$ of Fig. 7(a) to find out the critical thickness. The extracted value is plotted in Fig. 7(b). From Fig. 7(b), we can point out the critical thickness is around 33Å. A classic equation of voltage distribution on MIS capacitor [20]

$$V_G = V_{FB} + V_{ox} + \psi_s \tag{13}$$

can be used to describe this phenomenon. Where V_{FB} is flat band voltage. When the oxide thickness is around 33Å, the oxide can hold the inversion charge and keep ψ_s at $2\phi_b$ (ϕ_b is the difference between Fermi level and mid-gap at the bulk of silicon). Thus, V_{ox} can be modulated to a high value. High V_{ox} leads to high oxide field and hole tunneling probability. The band diagram of this situation is plotted in Fig. 7(c). However, when the oxide becomes thinner, it is difficult to hold inversion charge. The ratio of ψ_s to V_{ox} becomes larger, therefore the device will have lower V_{ox}, lower oxide field, and lower hole tunneling probability, as shown in Fig. 7(d). On the other hand, oxide thicker than 33Å can keep ψ_s at $2\phi_b$ and modulate V_{ox} to high value, but less inversion charge is needed, and a lower oxide field is built. This situation is plotted in Fig. 7(e). At last, we conclude that oxide thickness around 33Å can reach strong SBHM and optimal hole tunneling probability. This is the critical thickness of Al/SiO2/Si(p) MISTD.

IV. CONCLUSION

In this work, we build a complete model, based on the traditional model of Schottky diode, to derive the current behavior of MISTD. The majority injection from metal plays a significant role in a specific oxide thickness range because of SBHM. We also predict that the importance of the majority current will start to decrease at about 33Å, and the device's behavior will start to close to the traditional MIS capacitor. As a result, we conclude that the majority current is an important current component for MISTD at this range of oxide thickness and bias voltage. This range may be determined by metal work function, semiconductor bandgap, substrate doping type. . .etc.

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