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Improving Inverter Output Current Controller Under Unbalanced Conditions by Using Virtual Impedance

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ABSTRACT Nowadays, three-phase inverters have been commonly used in power systems, especially in renewable energy and motor drives applications. In many applications, the inverter has to generate balanced sinusoidal three-phase currents even though it is connected to an unbalanced system. Methods to suppress unbalanced currents commonly use decomposition of the unbalanced currents to their positive and negative sequence components. Thus, the positive and negative sequence currents can be controlled separately. However, this method is complicated because of the existence of sequence transformation block, a lot of signals to be controlled, and affect the transient response significantly. This paper proposes a novel method with detailed analysis to balance the inverter output currents under unbalanced AC side conditions without sequence transformation and affecting the transient response. The proposed method is based on virtual impedance concept that is inserted in series to the inverter output. The proposed virtual impedance is an additional control algorithm that changes the inverter behaviour into the one that has a real impedance connected to it. As it is virtual, the virtual impedance can be designed in such a way so that just the unbalanced signal is affected. Because there is no sequence transformation, the positive and negative sequence currents are not controlled separately. Simulation and experiment results show the effectiveness of the proposed method to suppress 12.13% current unbalance to only 2.27%. Meanwhile, the result is also compared to the conventional dual-reference method, proving the proposed method does not affect the transient response of the current reference.

INDEX TERMS Current controller, three-phase inverter, unbalanced system, virtual impedance.

I. INTRODUCTION

Nowadays, three-phase inverters are commonly used in renewable energy generation systems and AC drives. In many applications, the inverter has to generate a balanced sinusoidal three-phase output current. Due to the line impedance and grid voltage unbalances, however, the inverter output currents can be unbalanced. Under unbalanced conditions, the inverter will generate negative sequence current component that is detrimental to the grid and loads. Moreover, in electric motors, this negative sequence current may cause torque pulsation that should be avoided.

By knowing the fact that three-phase unbalanced currents can be decomposed into positive and negative sequence components, a control idea to compensate the negative sequence current was introduced in [1]–[3]. This control scheme is called dual reference control scheme. By using this control technique, the negative sequence current is suppressed to reduce the current unbalance. However, this control needs transformation of unbalanced currents to their sequence components, so two current controllers are needed which is complex and the design cannot be done separately. Furthermore, the positive and negative sequence controllers work in

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synchronous reference frame (SRF), which require many control signals

Unbalance in AC side produces 2nd harmonic oscillation in DC side. To improve the performance of dual reference control scheme, as mentioned before, 2nd harmonic notch filter is added to the control scheme. This method has been proposed in [4], [5]. However, not only complicated but the existence of notch filter may change the dynamic response of the power converter significantly. Such as in [6], [7], using 2nd harmonic filter to reduce oscillation adds overshoot and makes transient response slower. These drawbacks are undesirable in several applications.

To suppress current imbalance and keep the response speed, dual reference control based on proportional-resonant (PR) control is introduced in [8], [9]. PR controller may reduce the settling time and overshoot, so qualitatively the transient response is better. However, sensitivity becomes an issue in PR controller. It is mandatory to tune the converter perfectly in order to reduce current imbalance. If the cut-off frequency of the PR controller is not tuned well, then the compensator may fail to suppress the unbalanced current.

To get rid of the existence of 2 current controllers, a new method is introduced in [10], [11]. In these papers, active and reactive powers are controlled, instead of currents. To avoid extraction of positive and negative sequence currents, 90° of delay is added to the voltage measurement to calculate power. Using power control, current unbalance is successfully suppressed. However, the complexity remains the same, because this method only changes the algorithm of current sequence transformation to power calculation with time delay. In several applications, the time delay may disturb the system's stability.

Another method to suppress current unbalance is based on virtual impedance [12]–[16]. Instead of using 2nd harmonic filter, the virtual impedance is used to suppress the negative sequence current. This method still uses dual reference current control scheme, which is complicated as mentioned above. Moreover, in these works, virtual impedance may also affect the transient response of the system. Virtual impedance and active power filter concept to suppress unbalanced currents without dual reference current control was proposed in [17]–[19]. However, the performance under transient condition was not observed, which also an important issue.

Based on the aforementioned discussion, the main drawbacks of existing methods are complexity due to the sequence transformation and the effects to transient response, such as overshoot and settling time. This paper proposes a new method to improve the performance of inverter output current controller under unbalanced conditions without using sequence transformation and changing the transient response. The proposed method is based on a new virtual impedance concept that is connected in series to the inverter. Here, the virtual impedance is not only designed to suppress the disturbance but also not to affect the transient response of reference current. These features have not been proposed in previous works, as far as the author's concern.

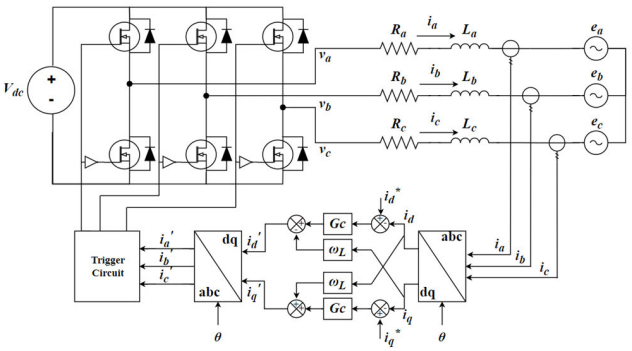

FIGURE 1. Three-phase inverter circuit with synchronous reference frame control.

A virtual impedance is an additional control algorithm that changes the inverter behaviour into the one that has a real impedance connected to it. As it is virtual, it can be designed in such a way so that only the unbalanced signal is affected. This virtual impedance is different to the virtual impedance concept that is used in reactive power sharing [20], limiting the short circuit current [21], stabilizing cascaded systems [22]–[25], and reducing harmonics [26], [27]. Several simulated and experimental results are included to show the effectiveness of the proposed method.

The structure of this paper consists of seven sections. The second section discusses the effect of unbalance conditions on the three-phase inverter current and its controller performance. The third section explains the implementation of virtual impedance in the control scheme. In section four, method to determine virtual impedance value is explained. Simulation results are discussed in section five, followed by experimental results in section six. Finally, the conclusion of the proposed method is written in section seven.

II. INVERTER CURRENT CONTROLLER PERFORMANCE UNDER UNBALANCED CONDITIONS

A synchronous reference frame (SRF) current controller as shown in Fig. 1 is commonly used to control the inverter output current. In Fig. 1, V_{dc} is DC input voltage, v_a, v_b, and v_c are output voltage of inverter, e_a, e_b, e_c can be the electromotive force (emf) of motor/grid voltage, R_a, R_b, R_c and L_a, L_b, L_c are the line resistance and inductance of phase a, b, and c respectively, i_a, i_b, and i_c are the three-phase output currents, i_q and i_d are the transformed output currents in SRF, i_q^* and i_d^* are the output currents reference, G_c is a proportional-integral (PI) current controller, ω_L is the cross-coupling that exists due to the frame transformation, and θ is the angle generated by phase locked-loop (PLL) to ensure synchronization between current reference and grid voltage.

Under balanced conditions, the inverter output currents will become almost sinusoidal and balance. In SRF, a balanced sinusoidal three-phase currents will become DC currents. Therefore, the PI controller works with DC quantities and as a result the steady-state error will become zero. In contrast, under unbalanced conditions, the inverter

output currents will become unbalance, so they can be decomposed to the positive and negative sequences as shown in (1). I^+ and I^- are the magnitudes of positive and negative sequence currents respectively. To transform output currents from abc frame to SRF, transformation matrix, $T(\theta)$ as shown in (2) is used. The result of this transformation is shown in (3).

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} I^+\cos(\theta) + I^-\cos(\theta) \\ I^+\cos\left(\theta - \frac{2\pi}{3}\right) + I^-\cos(\theta + \frac{2\pi}{3}) \\ I^+\cos\left(\theta + \frac{2\pi}{3}\right) + I^-\cos(\theta - \frac{2\pi}{3}) \end{bmatrix} \quad (1)$$

$$T(\theta) = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} i_q \\ i_d \end{bmatrix} = T(\theta)\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} I^+ + I^- cos(2\theta) \\ I^- sin(2\theta) \end{bmatrix} \quad (3)$$

From (3) it can be observed that in the SRF, the transformation of positive sequence results in DC quantities, whereas the negative sequence results in oscillation at twice of the fundamental frequency (2nd harmonic). The oscillation caused by the negative sequence cannot be eliminated by using just a proportional-integral (PI) current controller. How to suppress these oscillating currents by using the proposed virtual impedance will be discussed in the next section.

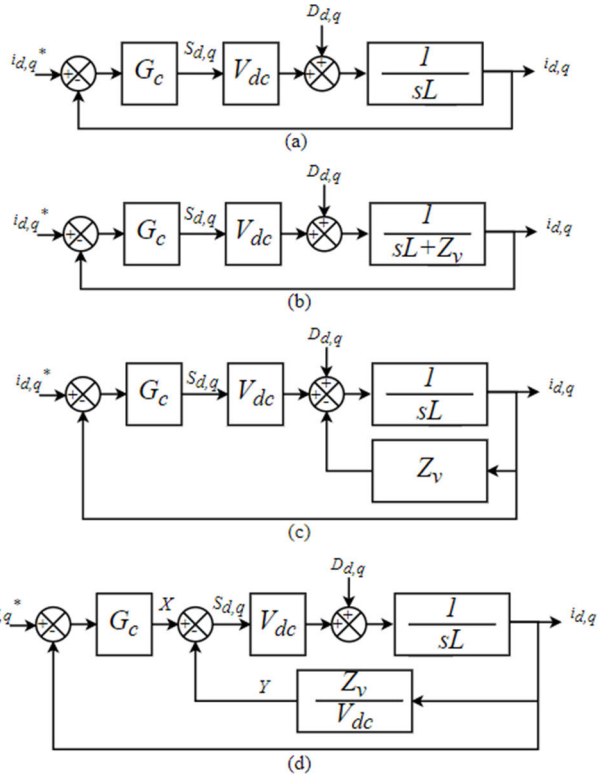

FIGURE 2. Process of designing virtual impedance (a) Initial block diagram of three-phase inverter in SRF, (b) Adding impedance in series with inverter output, (c) Illustration of voltage drop due to the series impedance, (d) Modifying the added-impedance to control scheme (virtual impedance).

III. VIRTUAL IMPEDANCE CONCEPT

Virtual impedance is a concept of control technique that makes the system feels an effect of the addition of a real impedance without its existence in the system [28]. By using this technique, the characteristic of the added impedance can be controlled as needed, such as resistive, inductive, capacitive, and a combination of them to form filter characteristics. The benefit of using virtual impedance is no additional power losses in the system and no voltage drop across the line because it is implemented in the control scheme. Another benefit is virtual impedance can be added by not changing the transient response of the system's reference value [29], [30]. This feature is useful because the virtual impedance will only respond the disturbance signal. In other words, there are two degrees of freedom in the control system, namely the reference response and disturbance response. So, the current PI controller and virtual impedance can be designed separately without affecting each other.

The three-phase inverter block diagram in SRF is shown in Fig. 2a. In this figure, $D_{d,q}$ is the disturbance in SRF (in this case is the unbalanced output current including the cross-coupling effect). $S_{d,q}$ is the switching function in synchronous frame. G_c is the current PI controller, shown in (4), where K_p and T are the proportional constant and integrator time constant respectively, and L is the load inductance. Here, the effect of R is assumed to be much smaller than L, so it is not included in calculation.

$$G_c(s) = K_p + \frac{1}{sT} \quad (4)$$

A simple method to suppress the unbalance effect is by adding an impedance Z_v in series to the load as shown in the block diagram in Fig. 2b. The series impedance may block the 2nd harmonic oscillations is SRF, so unbalanced current is able to be suppressed. However, adding a real impedance will increase the losses and size of the inverter. Moreover, the impedance Z_v also reduces the voltage across the line by the amount that is proportional to the load current multiplied by Z_v. Fig. 2c redraws the block diagram in Fig. 2b to show this effect more clearly. To move Z_v into the controller domain, Fig. 2c is further modified into the one in Fig. 2d. Now, the voltage across the added impedance is scaled by the DC voltage, and then used to reduce the voltage command from the controller. It can be seen that the transfer functions of the systems in Figs. 2b, 2c and 2d are the same, shown in (5). From (5), the suppression of disturbance is determined by the value of the impedance Z_v. The higher value of Z_v, the better the disturbance suppression.

$$i_{d,q} = \frac{G_c V_{dc}}{sL + Z_v + G_c V_{dc}} i^*_{d,q} + \frac{1}{sL + Z_v + G_c V_{dc}} D_{d,q} \quad (5)$$

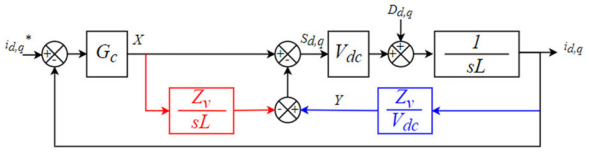

FIGURE 3. Proposed virtual impedance control scheme.

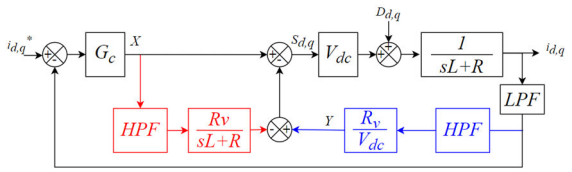

FIGURE 4. Control scheme with virtual resistor.

Although the virtual impedance in Fig. 2d is effective to suppress the effect of unbalance, (5) shows that the response of the load current to the reference is also affected. With higher Z_v value, the transient response will become slower. This is undesirable because the current controller and the virtual impedance cannot be designed separately. Other than that, high value of Z_v may also lead the system to instability. The following discussion explains the process of designing a virtual impedance to only affect the disturbance so it can be added as a plug-in block, avoiding the need to retune an already existing controller.

Suppose the output node of current controller is X and the output node of Z_v/V_{dc} block is Y. From Fig. 2d, if node Y is released from the summing junction, the equations of load current and node Y can be obtained as shown in (6) and (7) respectively.

$$i_{d,q} = \frac{XV_{dc} + D_{d,q}}{sL} \tag{6}$$

$$Y = \frac{i_{d,q}Z_v}{V_{dc}} \tag{7}$$

By substituting (6) into (7), the equation of node Y is shown in (8). Here, X component is related to reference current. Thus, to remove the effect of virtual impedance on the current reference, Y component should be compensated by XZ_v/sL. The control scheme now is shown in Fig. 3 and output current equation becomes (9). From (9), the virtual impedance will not affect the response to the current reference anymore whilst at the same time, it suppresses the disturbance.

$$Y = \frac{XZ_v}{sL} + \frac{D_{d,q}Z_v}{sLV_{dc}} \tag{8}$$

$$i_{d,q} = \frac{G_cV_{dc}}{sL + G_cV_{dc}} i_{d,q}^* + \frac{D_{d,q}}{sL + Z_v + G_cV_{dc}(1 + \frac{Z_v}{sL})} \tag{9}$$

As mentioned, the characteristic of virtual impedance can be chosen as desired. In this research, the performance of three types of virtual impedances are observed, which are virtual resistor, virtual inductor, and virtual resistor in series with virtual inductor. Each of them will be discussed in more detail in the following subsections.

A. VIRTUAL RESISTOR

By substituting Z_v with R_v, the red block in Fig. 3 becomes an integrator, whereas the blue block becomes a constant. The integrator (R_v/sL) may amplify the DC offset produced by the current controller, so it needs to be transformed into a low-pass filter (LPF) by adding the effect of load resistance (R). At the same time, a first-order high-pass filter (HPF) is added to ensure the elimination of DC signal. Due to the existence of HPF in the red block, the blue block in Fig. 3 needs an HPF as well to keep the virtual impedance algorithm from affecting reference signal. This can be proven using the same method discussed to modify Fig. 2d to Fig. 3. The control scheme for when a virtual resistor is used is shown in Fig. 4. Here, another additional first-order LPF is added as common practice to suppress undesired noise from current sensor. There is no relation between this LPF with virtual resistor control scheme.

The equation of output current is shown in (10). Here, the virtual resistor will not affect the reference current and higher value of virtual resistor should suppress the disturbance signal more.

$$i_{d,q} = \frac{G_cV_{dc}}{sL + R + G_cV_{dc}} i_{d,q}^* + \frac{D_{d,q}}{sL + R + R_vHPF + V_{dc}G_c(1 + \frac{R_vHPF}{sL+R})} \tag{10}$$

B. VIRTUAL INDUCTOR

By substituting Z_v with sL_v, the red block in Fig. 3 becomes a constant, whereas the blue block becomes a differentiator. A differentiator inherently amplifies high frequency signals, such as noise from A/D conversion, so has to be paired with an LPF. However, an LPF has already been put in place as a common practice in the system, as explained in the previous section. Therefore, implementing a virtual inductor does not need any additional component, as shown in Fig. 5.

The transfer function for the system in Fig. 5 is shown in (11). From (11), it is clear that virtual inductor will not affect the reference current and higher value of virtual inductor should suppress the disturbance signal more.

$$i_{d,q} = \frac{G_cV_{dc}}{sL + G_cV_{dc}} i_{d,q}^* + \frac{D_{d,q}}{s(L + L_v) + G_cV_{dc}(1 + \frac{L_v}{L})} \tag{11}$$

C. VIRTUAL RESISTOR IN SERIES WITH VIRTUAL INDUCTOR

By substituting Z_v with $R_v + sL_v$ the red block in Fig. 3 now becomes low pass filter, whereas the blue block becomes differentiator. Amplification of high frequency from differentiator has been reduced by the LPF that already exists. The equation of output current after addition of combination

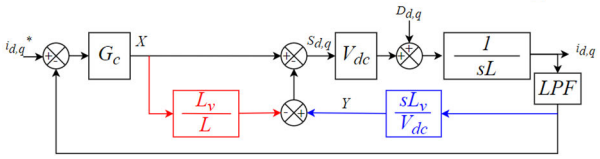

FIGURE 5. Control scheme with virtual inductor.

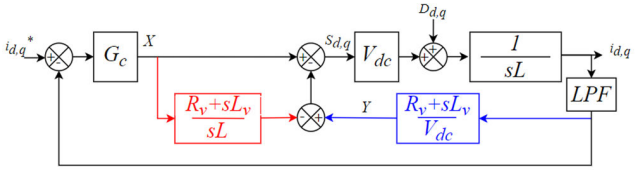

FIGURE 6. Control scheme with virtual resistor in series with virtual inductor.

virtual resistor in series with virtual inductor is shown in (12) and the control scheme in Fig. 6. Similar to using only virtual resistor or virtual inductor, virtual resistor in series with virtual inductor do not affect the response to current reference, and the disturbance suppression capability increases with their values.

$$i_{d,q} = \frac{G_c V_{dc} i_{d,q}^*}{sL + G_c V_{dc}} + \frac{D_{d,q}}{s\,(L + L_v) + R_v + G_c V_{dc}(1 + \frac{sL_v + R_v}{sL})} \tag{12}$$

D. FREQUENCY RESPONSE WITH VIRTUAL IMPEDANCE

Output currents transfer functions have been obtained from previous analysis and shown in (10)-(12). Transfer functions of reference current are same and are not affected by any type of virtual impedances. Here, virtual impedance is added to only affect the disturbance signals. So, transfer function of output current to disturbance signals is observed further. This transfer function will be called as disturbance response for shorter.

Fig. 7 shows the magnitude bode plot of disturbance response before and after adding virtual impedance. Here, the parameter of PI current controller and virtual impedance value used to draw the bode plot are same as used in simulation and experiment. As discussed before, in SRF, unbalanced current produces oscillation in 2nd harmonic. From Fig. 7, not only 2nd order harmonic is suppressed, but also other higher order harmonics. Higher order current harmonics may appear in SRF due to not ideal conditions, such as existence of dead time and distorted grid voltage. This shows the simplicity design of virtual impedance that may suppress all current harmonic contents. Also, with higher value of virtual impedance, then higher suppression is obtained. Another point to note is the combination in series of virtual resistor and inductor gives the highest suppression among the three types.

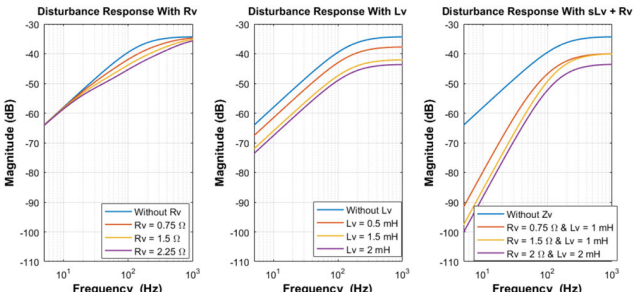

FIGURE 7. Magnitude bode plot of disturbance response for each virtual impedance type.

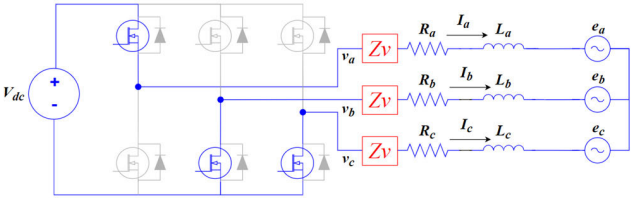

FIGURE 8. One switching process of three-phase inverter.

IV. DETERMINING VIRTUAL IMPEDANCE VALUE

By looking at Fig. 7, disturbance signals will be suppressed higher when high value of virtual impedance is used. So, by intuition, there is no limit in determining virtual impedance value. However, this is not true because we have to consider the inverter output voltage due to addition of virtual impedance.

Suppose from Fig. 8, one switching process of the inverter is marked blue. Here, v_{ab} is the inverter line-to-line output voltage, I_a, I_b, and I_c are the amplitude of phase currents. The value of v_{ab} is determined by modulation index (m_a) of the inverter, as written in (13). After adding virtual impedance and assuming balance conditions, the KVL of v_{ab} is shown in (14). Here, e_{ab} is the line-to-line voltage of grid/emf.

$$v_{ab} = m_a V_{dc} \tag{13}$$

$$v_{ab} = \frac{3}{2}\left(|Z_v| + R_a + j\omega L_a\right) I_a + e_{ab} \tag{14}$$

Inverter's line-to-line output voltage should not exceed its DC voltage value, in other words, it should not be operated in over-modulation condition. This means the value of m_a is always less than 1. So that, the maximum value of inverter's line-to-line output voltage is same as DC input voltage. To ensure inverter's modulation performance, in this research maximum m_a is chosen to be 0.9. By assuming inverter output voltage to 90% of its maximum value, KVL in (14) should not exceed 90% of the DC input voltage, as shown in (15). Solving this inequality, the maximum virtual impedance value is obtained in (16). If the virtual impedance design fails to meet this requirement, then inverter will operate in

TABLE 1. Simulation and experiment parameters.

Symbol	Parameter	Value
V_{dc}	DC input voltage	100 V
f	Inverter output frequency	50 Hz
f_{sw}	Switching frequency	10 kHz
L_a, L_b, L_c	Line inductance of each phase	1 mH
R_a, R_b, R_c	Line resistance of each phase	1.1 Ω, 1 Ω, 1.3 Ω
e_a, e_b, e_c	Grid rms voltage	29 V, 35 V, 34 V
K_p	Proportional constant	0.5
T	Integrator time constant	1 ms
fc_LPF	LPF cut-off frequency	2.5 kHz
fc_HPF	HPF cut-off frequency	50 Hz
-	Simulation time step	10 µs

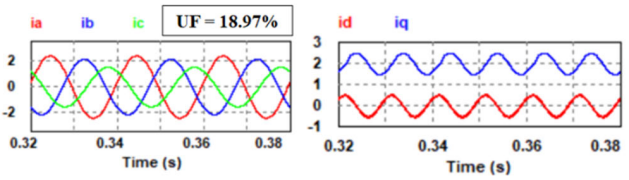

FIGURE 9. Simulation result of output current in abc (left) and synchronous frame (right).

over-modulation condition, which is undesired.

$$v_{ab} = 0.9V_{dc} \geq \frac{3}{2}\left(|Z_v| + |R_a + j\omega L_a|\right) I_a + e_{ab} \quad (15)$$

$$|Z_v| \leq \frac{2}{3}\left(\frac{0.9V_{dc} - e_{ab}}{I_a}\right) - |R_a + j\omega L_a| \quad (16)$$

V. SIMULATION RESULTS

To verify the effectiveness of the proposed method, first, a simulation is done for the three-phase inverter depicted in Fig. 1 by using PSIM software before doing the experiment. The simulation parameters are shown in Table 1. In this research, the unbalance is caused by both unbalanced grid voltages and line impedances.

A. OSCILLATION IN SRF UNDER UNBALANCED CONDITION

In this simulation, to maintain the inverter under unity power factor, current reference in d frame is set to 0 while q frame is set to 2 A. Under unbalanced grid voltage and line impedance, inverter output current in abc frame and SRF are shown in Fig. 9. Those unbalances force the inverter output current to become unbalance. Thus, 2nd order harmonic oscillation appears in SRF as discussed before. The current controller manages to maintain the average output current same as the reference in synchronous frame, but it fails to maintain the peak currents equal in abc frame. In this case, the unbalance factor of inverter output current is 18.97%. 2nd order harmonic will be suppressed using the proposed virtual impedance method.

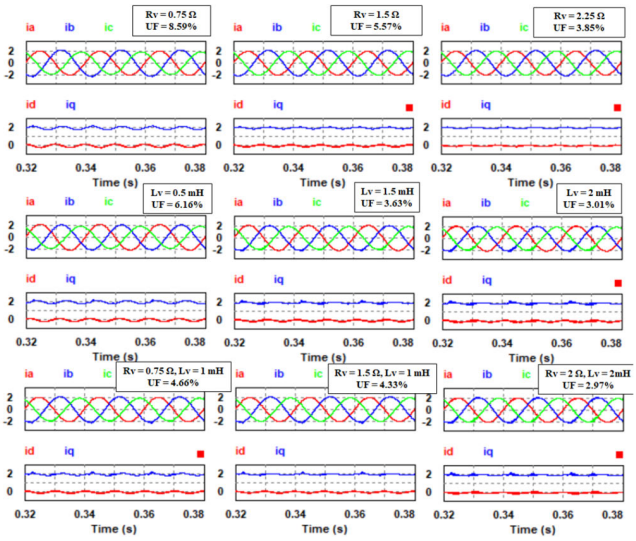

FIGURE 10. Simulation results of output currents in abc and SRF after addition of virtual impedances.

B. VIRTUAL IMPEDANCE EFFECT IN STEADY STATE CONDITION

Using parameters given in Table 1 and taking all highest value for grid voltage and line resistance, the maximum value of virtual impedance can be calculated using (16). Substituting each parameter, maximum value of virtual impedance is 3.72 Ω. Therefore, virtual impedance chosen to depict the bode plot in Fig. 7 is below this value.

In steady state condition, the simulation results are shown in Fig. 10. The improvement in q and d currents is notable as the virtual impedance values are increased. Second order harmonic oscillation in SRF is reduced significantly. In abc frame, the currents are getting balanced, indicated by the decreasing unbalance factor. The unbalance factor decreases significantly due to the addition of virtual impedance. With additional 2 Ω and 2 mH, the unbalance factor goes down to about 1/6 of the original case.

To observe the suppression capability of each virtual impedance type, FFT analysis is performed to the q and d currents. The results are shown in Fig. 11. It is clear that not only the value of virtual impedance that affects the suppression level, but also, the impedance type. Among the three types, the combination of virtual resistor and inductor gives the best disturbance suppression, especially at 2nd harmonic content. This follows the transfer functions in (10)-(12) and bode plot in Fig. 7.

C. VIRTUAL IMPEDANCE EFFECT IN TRANSIENT CONDITION

Not only observing the suppression capability in steady state condition, the transient response of reference current is also observed. This is done to prove that virtual impedance will not affect current reference response due to the modification of block diagram from Fig. 2d to Fig. 3. In this case, the virtual impedance that gives the best suppression is chosen, that is the

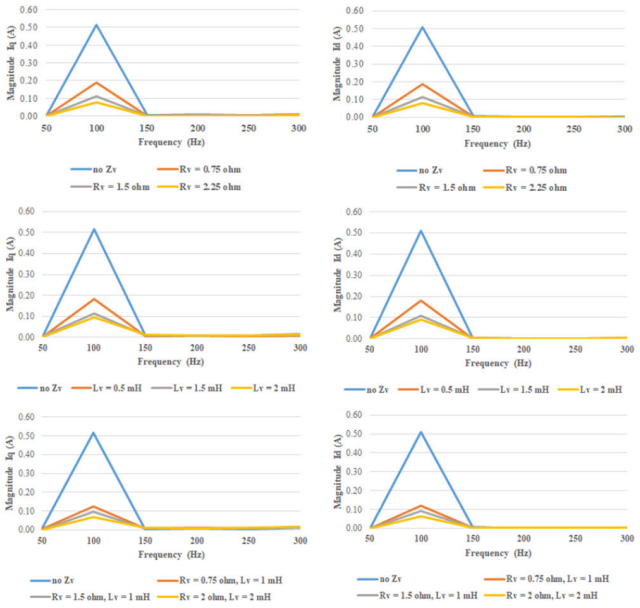

FIGURE 11. Frequency spectrum of simulated i_q and i_d.

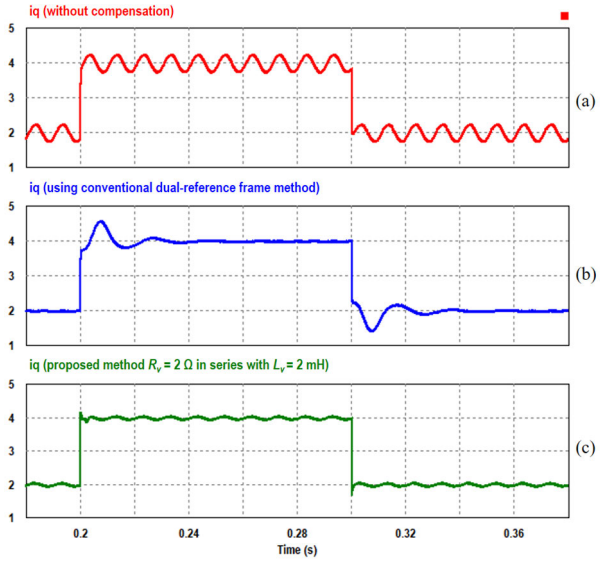

FIGURE 12. Simulation results of output current transient response (a) without compensation, (b) using conventional dual-reference frame method, (c) proposed method with $R_V = 2\ \Omega$ in series with $L_V = 2$ mH.

combination of 2 Ω virtual resistor and 2 mH virtual inductor. The current reference is changed from 2 A to 4 A and vice versa.

The results of transient response simulation are shown in Fig. 12. This simulation also compares the proposed method performance with conventional dual-reference frame method using the same circuit parameters in Table 1. The main idea of this conventional method is to decompose the unbalanced currents into their positive and negative sequence components. The negative sequence current is compensated to be 0 in SRF, so that the three-phase currents are balance. Using this method, 4 signals have to be controlled, which are d-q axis currents of positive sequence and d-q axis currents of negative sequence. Meanwhile, the proposed method only uses one pair of d-q signals.

From the simulation result, the effectiveness of the proposed method can be clearly observed. There is no change in settling time between uncompensated current and using the proposed method. However, using the conventional dual-reference frame method, the transient speed is slower and followed by high overshoot, even though the control parameters are same. This verifies that the proposed method has two degrees of freedom for its controller. Here, the virtual impedance can be designed separately without having to retune the PI current controller. The virtual impedance will only respond the disturbance signal, in this case is the unbalanced current. This behaviour cannot be achieved by using common current control techniques described in [6], [7].

Although having strong advantage in the transient response, the proposed method also comes with disadvantage. From Fig. 12, it is clear that the performance of the conventional method in steady state is better that the proposed method. This is because the capability to nullified the negative sequence currents using the separated controllers, while the proposed method only suppresses it. In the proposed method, the capability of unbalance suppression is determined by the value of virtual impedance. As discussed, higher virtual impedance valued will give higher suppression. However, there is a maximum value of allowed virtual impedance, determined by the circuit parameters, which also has been discussed in Section IV. In spite of the existence of suppression limit, the proposed method has significantly shown that it can suppress such high value of unbalanced factor (from 18.97% unbalance factor to only 2.97%).

The performance to suppress the unbalanced current is compared for each method, which are discussed in Section I. The comparison is shown in Table 2. From here, it is known that some advantages of the proposed method are no sequence decomposition, only 2 controlled signals, and does not affect transient response of reference current. The only disadvantage is already discussed, which is the limit of suppression and sensitive (will be discussed after experimental results).

The capability of virtual impedance to suppress unbalanced currents have been proven by simulation results. Next, experimental setup is made to prove the capability practically.

VI. EXPERIMENTAL RESULTS

After successfully simulating the performance of the proposed method, an experiment based on Fig. 1 is set up. The parameters of this experiment are same as used in simulation, shown in Table 1. Fig. 13 shows the experiment set up in running condition. IRFP260N MOSFETs are used to implement the power switches and Launchpad Development Kit featuring a C2000 microcontroller to control the switches. The DC input voltage is obtained from single-phase transformer connected to single-phase rectifier. Large filter capacitor (4.7 mF) is placed in the output terminal of rectifier to produce DC voltage as pure as possible.

TABLE 2. Performance comparison of unbalanced current suppression methods.

Methods	Needs positive-negative sequence decomposition	Total controlled signals	Adds transient overshoot	Slower settling time	Additional notes
Dual-reference control [1-3]	Yes	4	Yes	Yes	Theoretically may nullify negative sequence current
Dual-reference control with notch filter [4-7]	Yes	4	Yes	Yes	
Dual-reference control with proportional-resonant [8, 9]	Yes	4	Yes	No	
Active & reactive power based controller [10, 11]	No	3	Not discussed	Not discussed	
Dual-reference control with virtual impedance [12-16]	Yes	4	Yes	Yes	
Virtual impedance and active power filter without dual-reference control [17-19]	No	2-4	Not discussed	Not discussed	May only suppress the magnitude of negative sequence current
Proposed virtual impedance method	No	2	No	No	

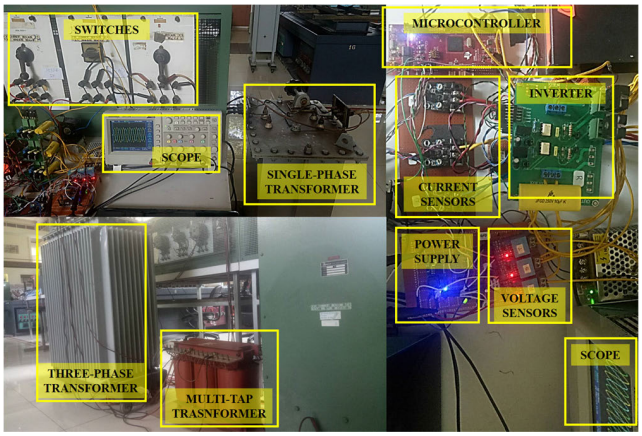

FIGURE 13. Experiment set up in running condition.

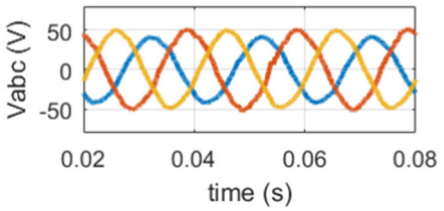

FIGURE 14. Experiment result of unbalanced grid voltage.

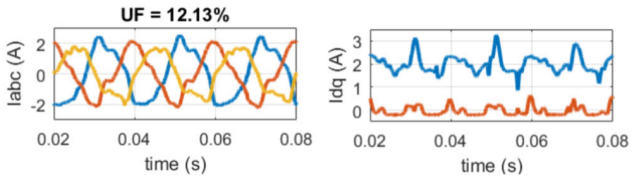

FIGURE 15. Experiment results of output currents in abc (left) and synchronous frame (right).

Unbalance in the grid voltage is obtained from three-phase transformer connected to multi-tap three-phase transformer. Using the taps, output voltage of each phase is adjusted. Experiment data from oscilloscope are processed in MATLAB to view the waveforms, calculate unbalance factor, and perform FFT analysis.

A. OSCILLATION IN SRF UNDER UNBALANCED CONDITION

First, the grid voltage from voltage sensor is shown in Fig. 14. The grid voltages are unbalanced and slightly distorted. In this condition, the output currents of the inverter are unbalanced and severely distorted, as shown in Fig. 15. The distortion is caused by the voltage quality and dead time. The unbalance factor in this condition is 12.13%. In SRF, the dominant oscillation occurs at twice the fundamental frequency, similar to the simulation results. Other oscillations also occur due to the distorted output currents. These oscillations are going to be suppressed by virtual impedance concept.

B. VIRTUAL IMPEDANCE EFFECT IN STEADY STATE CONDITION

The results for steady state condition experiment are displayed in Fig. 16. The experiment gives the same trend in virtual impedance performance as the simulation, that is the low harmonic oscillation in SRF can be suppressed. The effect of low harmonic suppression can be clearly seen in abc frame, where the peak values of each phase are getting equal and the current waveform in abc frame is almost sinusoidal.

The unbalance factor decreases significantly by using the proposed method. FFT analysis is performed to observe the suppression of each frequency components, shown in Fig. 17. These results are in accordance with the simulation results in the previous section. Higher impedance value gives higher suppression at 2nd harmonic. Different virtual impedance type also gives different suppression level, as exhibited by the simulation results, with virtual resistor in series with virtual inductor gives the best suppression performance. However, in Fig. 16 and Fig. 17, higher frequency contents appear to be

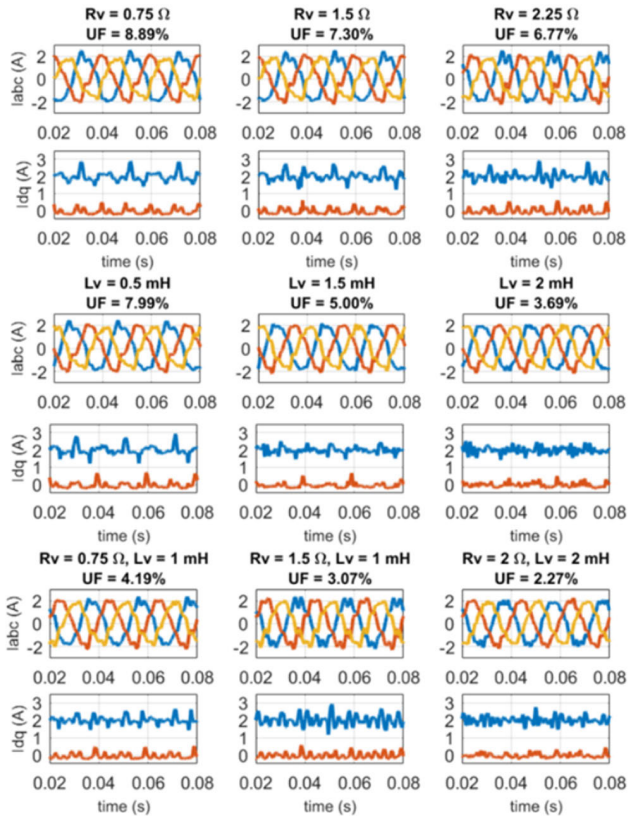

FIGURE 16. Experiment results of output currents in abc and SRF after addition of virtual impedances.

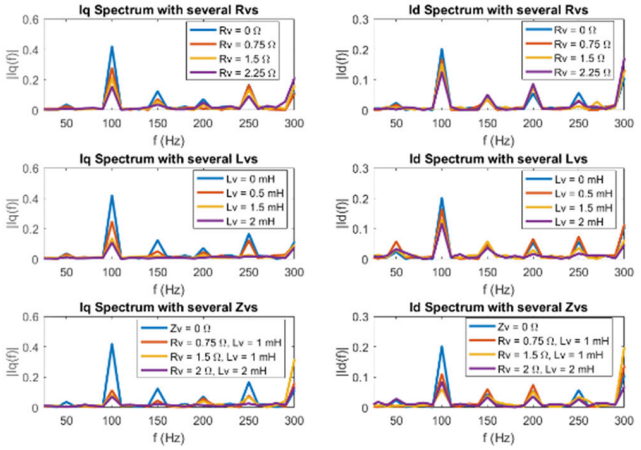

FIGURE 17. Frequency spectrum of i_q and i_d.

increasing when virtual inductor is used. This phenomenon does not appear in simulation results because of ideal conditions. This phenomenon is due to the differentiator characteristic of the virtual inductance that amplifies higher order harmonics. This implies that the trade-off between harmonic suppression and noise amplification should be considered carefully in order to choose the optimum virtual inductance. This also indicates the sensitivity of the proposed method in some frequency regions.

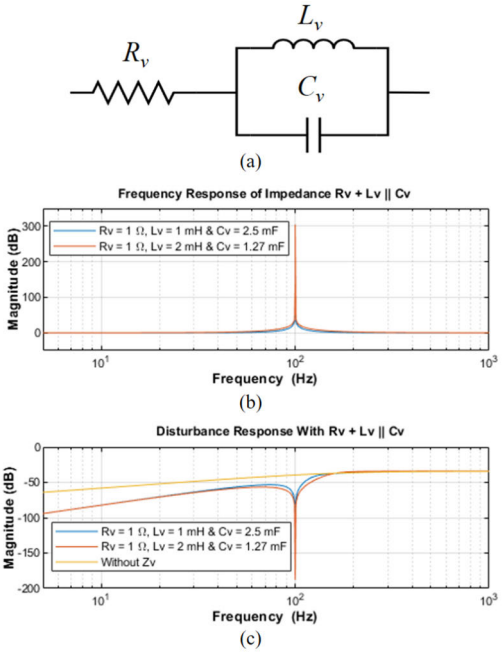

FIGURE 18. (a) Combination of virtual resistor, capacitor, and inductor to avoid high frequencies amplification, (b) virtual impedance frequency response, (c) disturbance response.

Another type of virtual impedance such as combination of resistor, inductor, and capacitor can be applied to suppress unbalanced currents, shown in Fig. 18a. Tuning the combination of those three components will allow the virtual impedance to have very high value in the 2nd harmonic (100 Hz), due to the resonance characteristic of L and C [31]. The impedance frequency response is depicted in Fig. 18b. If virtual inductor or virtual resistor in series with virtual inductor are used, their impedance response in high frequencies will become inductive, thus higher order frequencies will be amplified due to the differentiator characteristic. Note that the impedance response in Fig. 18b is resistive in high frequencies, so that the high frequency components or noise will not be amplified by the virtual inductor. By the high value of impedance in the 2nd harmonic, unbalanced currents can be suppressed much higher in the SRF, as shown in Fig. 18c. Comparing this figure to the previously mentioned bode plot in Fig. 7, the 2nd harmonic is suppressed much higher. However, this virtual impedance configuration can only suppress one harmonic component, leaving the other components unsuppressed. Selectivity of harmonic suppression is also an issue when this combination is used.

C. VIRTUAL IMPEDANCE EFFECT IN TRANSIENT CONDITION

Transient response is done by choosing virtual impedance that gives highest suppression in steady state condition, which is virtual resistor (2 Ω) in series with virtual inductor (2 mH). The experimental transient response result in shown in Fig. 19.

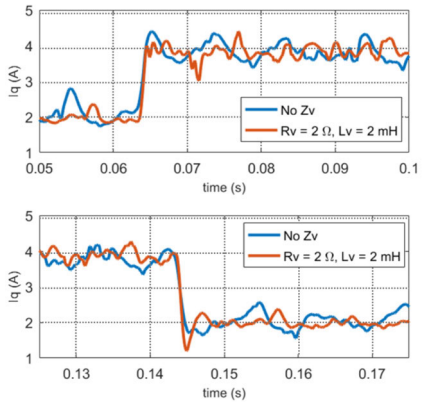

FIGURE 19. Experiment results of output currents transient response without and with virtual impedance in SRF.

The transient response without and with virtual impedance are compared and it is proven that this method does not change the transient response significantly. The proposed method does not change the settling time and overshoot. A little overshoot occurs when the reference is stepped down due to existence of disturbance in that point. As it is experiment, disturbance is not only unbalances, but also unwanted noise. This is proven by no overshoot appears when the reference current is stepped up. So, this little overshoot is due to disturbance, not the failure of the proposed method.

VII. CONCLUSION

This paper proposes a virtual impedance concept to suppress the effect of unbalance on the output currents of a three-phase inverter. Due to unbalanced grid voltage and line impedance, output current of three-phase inverter becomes unbalance as well. In SRF, unbalanced output currents produce low frequency components that cannot be suppressed by conventional methods.

Virtual impedance is a control technique that makes the system feels the effect of additional impedance without its existence in the system. The proposed method in this paper does not need sequence components decomposition, so it only needs two control signals instead of four like a conventional dual-reference controller does. Its characteristics can be chosen as any type and combination of impedances. In this paper, the chosen behaviours are resistive, inductive, and a combination of resistive and inductive. The results show that virtual impedance concept is effective to reduce oscillation in SRF and suppress the unbalanced output currents from 12.13% to only 2.27%. The best suppression is obtained when using the combination of virtual resistor in series with virtual inductor. Compared to the conventional dual-reference frame control, this method does not add overshoot and can maintain fast settling time. However, the conventional dual-reference method may strongly nullify current unbalance, whilst the proposed method may only suppress it, leaving a small value of unbalance factor. Other than that, the proposed method is also sensitive to noise amplification due to the differentiator effect, but it can be mitigated by using low pass filter.

For future development, the same method can be applied for the combination of RLC virtual impedance. By using combination of those three components, very high impedance value can be tuned in 2nd harmonic. This allows very high suppression of unbalanced current in SRF without amplifying the high frequencies components and noise.

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