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A Cost-Effective Antenna-in-Package Design With a 4 \times 4 Dual-Polarized High Isolation Patch Array for 5G mmWave Applications

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ABSTRACT A cost-effective antenna-in-package design based on a 4×4 dual-polarized high isolation patch array for 5G mmWave applications is proposed in this paper. To obtain a cost-effective design, we devised a four-layer metal stack-up structure with dielectric materials consisting of one TLY-5 polytetrafluoroethylene (PTFE) and two FR-4 epoxies. The devised stack-up exhibits a simple and compact geometry due to the small number of layers, which allows the design to be manufactured using a low-priced standard printed-circuit-board process. Additionally, the employed material combination in the stack-up design possesses a high-end PTFE only in the region with the antenna radiators, which enables good antenna radiation performance at an affordable price. In addition, to design a high-isolation patch array for dual-polarized applications using the low-layer stack-up structure, we employed capacitive probes, defected ground structures, and the rotated-fed method in the proposed array design. With these techniques, the designed array exhibited excellent performance with respect to both port-to-port isolation and crosspolarization isolation. The mechanism of improvement in port-to-port isolation was clearly described using the established equivalent circuit model of the proposed structure. As a result, the fabricated antenna-inpackage has the reflection coefficients of less than -10 dB in the targeted frequency range of 26.5–29.5 GHz and has a peak gain of 17.37 dBi at 28 GHz. The measured port-to-port isolations and cross-polarization isolations are higher than 22.63 and 30 dB in the targeted frequency band, respectively.

INDEX TERMS 5G mm-Wave, antenna in package (AiP), capacitive probe, defected ground structure (DGS), dual-polarized patch antennas.

I. INTRODUCTION

With the growing need for higher data rate services, millimeter-wave (mmWave) communications have received great attention in both industry and academia [1]. In mmWave communications, multiple-input multiple-output (MIMO) antennas with electrical beamforming capabilities are essentially used to mitigate severe propagation losses and to accommodate multiple users [2], [3]. Modern mmWave MIMO antennas are usually designed based on the antennain-package (AiP) interface approach, in which integrated chips are packaged on the antenna surface or inside the cavity

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built into antennas to offer low interconnection losses [4]. Orthogonal dual-polarized diversity is widely supported in mmWave communications to increase the channel capacity and to reduce the additional losses attributed to the polarization mismatch [5], [6].

Several works have been conducted to design dualpolarized AiPs for mmWave communications. The dualpolarized AiPs implemented using low-temperature co-fired ceramic (LTCC) technology were reported in the literatures [7]–[9]. They provide superior performance in terms of efficiency, loss, and gain and offer a high degree of integration with the aid of the LTCC process [10]. However, the LTCC process is too expensive for many consumer electronics applications. In [11] and [12], the dual-polarized AiPs fabricated using the high-definition interconnect (HDI) process with an FR-4 epoxy laminate material were presented. They have the main advantage of being ultralow cost, but their antennas suffer from gain and efficiency reductions due to the high material loss, especially in mmWave bands. As an alternative, in [13]–[18], multilayer organic (MLO) materials such as Megtron-6, liquid crystal polymer (LCP), and polytetrafluoroethylene (PTFE) were employed instead of FR-4 epoxy. The AiPs based on MLO materials provide better efficiency and gain performance at a lower price than the LTCC based AiPs, but the materials are still expensive in nature compared to FR4 epoxy, which is a major obstacle for commercialization [16], [19].

Further efforts have been made to reduce the manufacturing cost of the MLO based AiPs by decreasing the number of layers in their stack-up design and using the standard PCB process [20]–[24]. These efforts can be an effective solution for low-integration small-scale AiP applications. Unfortunately, the literatures in [20]–[23] do not consider the dualpolarized diversity, and the work in [24] does not satisfy the required isolation for dual-polarization despite supporting the diversity. Note that the minimum required isolation in mmWave systems is as high as 24 dB when the 256-QAM modulation scheme is used [25]. To overcome this drawback, a design technology on the dual-polarized AiPs that is cost-effective and achieves better performance need to be studied.

In this paper, we propose a cost-effective AiP design with a dual-polarized high isolation patch array for 5G mmWave applications. First, we devised a four-layered AiP stack-up design which consists of a single TLY-5 PTFE for the radiating elements and two FR-4 epoxies for the feeding networks to provide good performance at an affordable price. We then presented the patch array with high port-to-port isolation by using the defected ground structure (DGS) and capacitive probe feeding. Lastly, the rotated-fed method was adopted in the designed patch array to further improve the polarization isolation.

This manuscript is divided into five sections. The single element design of the proposed AiP is given in Section II, and the array design is introduced in Section III. Section IV presents experimental verifications and the concluding remarks are given in Section V.

II. ANTENNA ELEMENT DESIGN

A. DESIGN CONCEPT AND GEOMETRY

The concept of the stack-up design of the proposed AiP is illustrated in Fig. 1, in which two different core materials, an FR-4 prepreg, and four metal layers from M1 to M4 are included. The core materials consist of TLY-5 PTFE and FR-4 epoxy. Over the layers of M1–M4, the patch element and RF feeding lines including the capacitive probes and quasi-coaxial via transition are arranged. The antenna ground plane is located on the M2 layer, which isolates the patch element on the M1 layer from other components under the M2 layer to avoid undesired spurious modes and crosstalk [26]. The

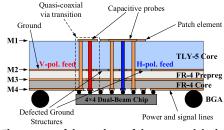


FIGURE 1. The concept of the stack-up of the proposed dual-polarized AiP.

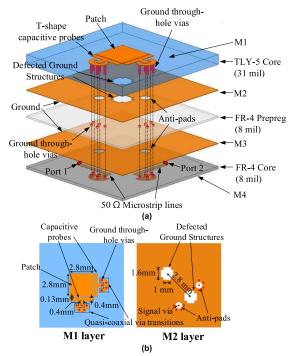


FIGURE 2. Configuration of the single element in the proposed dual-polarized AiP: (a) 3-D expanded view and (b) top view on the M1 and M2 layers.

RFIC is attached to the bottom of the M4 layer by the flipchip technology using the ball grid array (BGA) interconnect.

The larger BGAs on the side are for interconnection with motherboards. Additionally, the power and signal lines are positioned on the M4 layer for the chip integration. Here, the antenna design over the layers of M1–M4 is based on literature [20] except for the chip and board interconnections.

Fig. 2 shows the configuration of the single element of the proposed AiP. One square patch and two T-shaped capacitive probes are positioned on the M1 layer, and the gap between them is 0.13 mm. On the M2 layer, the antenna ground plane, on which two cross shaped DGSs and two anti-pads are inserted, is placed. The DGSs are separated diagonally and placed symmetrically to the square patch, and the optimized dimensions can be referred to in Fig. 2(b). Between M1 and M2, the TLY-5 core material with a relative dielectric permittivity (ε_r) of 2.2, a loss tangent (tan δ) of 0.0009, and a thickness of 31 mil is employed. This low-loss thick core enables the antenna to achieve wideband characteristics and to have good antenna efficiency and gain [27]. On the

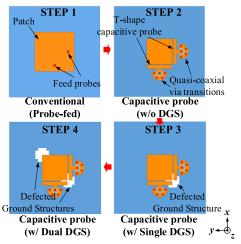
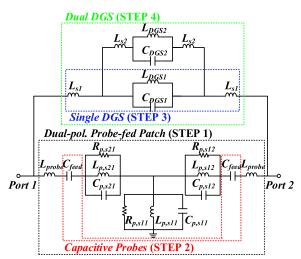
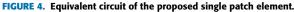


FIGURE 3. Design steps of the single patch element in the proposed AiP.





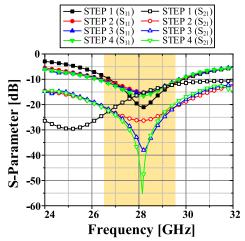


FIGURE 5. The simulated S-parameter results for each design step.

other hand, the ultralow-cost FR-4 core and prepreg with $\varepsilon_r = 4.0$ and tan $\delta = 0.02$ are placed between the M2 and M4 layers. The dielectric constant of the FR-4 material at 28 GHz is determined based on [19]. These cores are chosen to reduce the whole material cost while maintaining the antenna

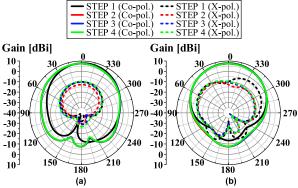


FIGURE 6. The simulated gain pattern results at 28 GHz for each design step: (a) *E*- and (b) *H*-planes.

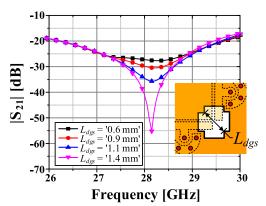


FIGURE 7. Parametric study on the simulated port-to-port isolations of the single element by different DGS dimensions of L_{dgs} .

performance by positioning the radiating elements in the lowloss TLY-5 core material. The quasi-coaxial via transitions with five through-hole vias are routed over the layers from M1 to M4. Two $50-\Omega$ microstrip lines are attached to the terminals of the transitions. The lumped ports are placed at the end of the microstrip lines and are used in the electromagnetic (EM) simulation environment for simplicity. The EM simulation was performed using ANSYS/HFSS software [28].

B. PATCH ELEMENT DESIGN

The design steps of the single patch element of the proposed AiP are illustrated in Fig. 3. We first designed the conventional probe-fed patch antenna in STEP 1 [29], and the antenna was implemented on a thick substrate to meet the wideband characteristic in a cost-effective way. However, the use of a thick substrate leads to the degradation of the port-to-port isolation due to the increase of the feed probe inductance [30]. To alleviate the degradation caused by using a thick substrate, we replaced the feed probes with T-shaped capacitive probes with the quasi-coaxial via transitions in STEP 2. The probes were designed by modifying the rectangular capacitive probe [31] to have vertical transition using a quasi-coaxial structure [20]. To achieve higher port-to-port isolation to meet the required modulation schemes in mmWave systems (e.g., 256-, 512-, or 1024-QAM, etc.),

we additionally included a single DGS in STEP 3 and dual DGSs in STEP 4, each of which was inserted on the ground plane between the probes and acts as a band-stop filter [32]. We designed the fundamental structures of the proposed antenna based on existing literature, including the probe-fed patch in [29], capacitive probes in [31], quasi-coaxial via transition structure in [20], and defected ground structures in [33]. In the case of DGS, we chose a cross-shaped design to meet the tight PCB design rules related to via pads. By combining these well-known methods, we devised a new cost-effective dual-polarized mmWave patch antenna with high isolation. The dimensions of the proposed single patch element were optimized based on parameter studies using the full EM simulation software (ANSYS/HFSS), as seen in Fig. 2(b).

Fig. 4 depicts an equivalent circuit of the proposed single patch element. The dual-polarized probe-fed patch antenna in STEP 1 can be modelled as parallel R-L-C resonant circuits $(R_{p,s11}-L_{p,s11}-C_{p,s11}, R_{p,s21}-L_{p,s21}-C_{p,s21}, \text{ and } R_{p,s21}-L_$ $C_{p,s21}$) and a series of inductance of probes (L_{probe}) (see the dotted black line in Fig. 4) [34]. Here, Lprobe at the left side and two parallel circuits $(R_{p,s21}-L_{p,s21}-C_{p,s21})$ and $R_{p,s11}$ - $L_{p,s11}$ - $C_{p,s11}$) are responsible for the input impedance of the patch antenna at port 1, and these are dominant enough to determine the resonant frequency in the reflection coefficient response $(f_{p,s11})$. Another two parallel circuits $(R_{p,s21}-L_{p,s21}-C_{p,s21} \text{ and } R_{p,s12}-L_{p,s12}-C_{p,s12})$ determine the resonant frequency of the port-to-port isolation reaction $(f_{p,s21})$, as described in [30]. These two resonant frequencies are almost the same in a typical thin substrate. However, in the case of a thick substrate (>0.02 λ_0) with feed probes, $f_{p,s11}$ shifts upward relative to $f_{p,s21}$ due to the increased L_{probe} , which leads to degradation of the port-to-port isolation. The capacitive probes in STEP 2 can be expressed as series capacitance (C_{feed}) , which is used to cancel the series L_{probe} (see the dotted red line in Fig. 4) [27]. After that, the single DGS in STEP 3 was modeled as a parallel L-C resonance circuit connected parallel with the equivalent circuit of the dual-polarized probe-fed patch in the previous step (see the dotted blue line in Fig. 4). The dual DGS in STEP 4 was similarly expressed as two parallel L-C resonance circuits between two input ports (see the dotted green line in Fig. 4) [33]. These L-C resonance circuits provide bandgap characteristics between the two ports, ensuring suppression of the surface waves flowing toward port 2 from port 1, and vice versa.

The simulated reflection coefficients and port-to-port isolation of the presented single elements for different design steps are given in Fig. 5. The S₂₁ values (i.e., port-to-port isolations) of the single element at 28.15 GHz for STEP 1, 2, 3, and 4 are -15.46, -26.35, -37.64, and -55.18 dB, respectively. The design of STEP 2 has the lowest S₂₁ value at the targeted frequency of 28.15 GHz with the aid of the T- shaped capacitive probes, while the design of STEP 1 has the lowest value at a shifted frequency of 25.1 GHz due to the increase in the feed probe inductance. The S₂₁ values of the designs of STEPs 3 and 4 are improved especially within

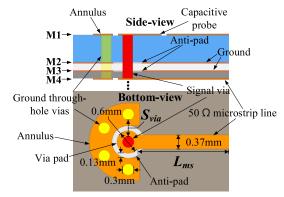


FIGURE 8. Geometry of the designed quasi-coaxial via transition.

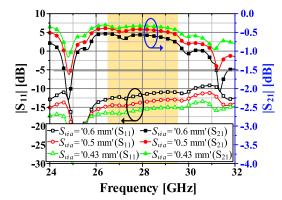


FIGURE 9. Simulated transmission and reflection characteristics of the designed quasi-coaxial via transition for different S_{via} values ($L_{ms} = 1.0$ mm).

the frequency range of 26.9 - 29.13 GHz by means of the added DGSs, and they are enhanced by 11.65 and 28.82 dB at 28.15 GHz, respectively, compared to the design of STEP 2. Consequently, the final single element design of STEP 4 has higher than 20 dB of port-to-port isolation from 26.22 to 29.5 GHz, higher than 25 dB from 27.12 to 28.93 GHz, and greater than 30 dB from 27.57 to 28.59 GHz. All designs described in Fig. 3 have reflection coefficients (i.e., S₁₁ and S₂₂) of less than -10 dB from 26.5 to 29.55 GHz.

The simulated gain patterns of the presented single element for different design steps at 28 GHz are given in Fig. 6. It is worth noting that there are few changes in the patterns in Fig. 6, depending on the design steps. The maximum gain of the single element in STEP 4 is 7.44 dBi, and the radiation efficiency is 89.79%. The half-power beamwidths (HPBWs) in the *xz*- and *yz*-planes (i.e., *E*- and *H*-planes) are 80° and 82°, respectively. The cross-polarization isolation (XPI) of the presented single element is 17.9 dB and this value is not enough for dual-polarized MIMO applications [25]. The method to improve the XPI will be covered in Section III.

The simulated results of the parametric study on the cross- shaped DGS depending on the dimension of L_{dgs} are presented in Fig. 7. As the value L_{dgs} increases, the port-to-port isolation improves at a targeted frequency of 28.15 GHz. If the value L_{dgs} exceeds 1.7 mm, the designed DGS is in contact with vias of the quasi-coaxial transitions, which leads

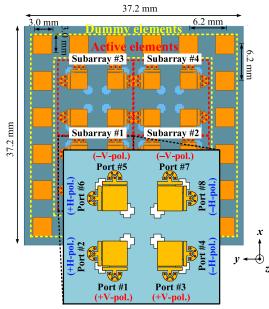


FIGURE 10. Configuration of the 4 \times 4 patch array with the rotated-fed method in the proposed AiP.

to an invalid design. Considering the minimum region of via pads required in the standard PCB process, the optimized value of L_{dgs} was determined to be 1.4 mm.

C. VERTICAL TRANSITION DESIGN

Fig. 8 shows the configuration of the employed quasi-coaxial via transition in the single element design. The transition is designed to convert the $50-\Omega$ microstrip line to the capacitive probe by using signal and ground through-hole vias. The signal via is surrounded by four ground vias connected to the annulus pads to form a coaxial-like transmission structure. In this design, the blind and buried vias were not contained, considering the fabrication complexity and cost issues [22]. The diameters of the vias and via pad are 0.3 mm and 0.6 mm, respectively, and the gap between the via pad and the annulus is 0.13 mm, which were determined to comply with the minimum design specifications in our PCB process.

We analyzed the transmission and reflection characteristics of the designed quasi-coaxial via transition for several signalto-ground via spacings (S_{via}) in Fig. 9. When $S_{via} = 0.6$ mm, $S_{via} = 0.5$ mm, and $S_{via} = 0.43$ mm, the reflection coefficients ($|S_{11}|s$) of the designed transition are -11.47, -13.53, and -15.50 dB, respectively. The transmission coefficients ($|S_{21}|s$) for those S_{via} values are -0.57, -0.42, and -0.33 dB, respectively. These results indicate that the performance of the transition improves, as the S_{via} values decreases. Considering the available PCB design specifications, the optimal value of the parameter S_{via} was chosen to be 0.43 mm.

III. ANTENNA ARRAY DESIGN

In this section, the antenna array design is introduced in detail, and its performances are evaluated. In order to verify and to compare the antenna in an array configuration to precedent AiP researches [9], [21], we chose the array size

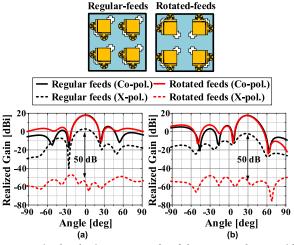


FIGURE 11. Simulated gain pattern results of the 4×4 patch array with and without the rotated-fed method in the E-plane for the scan angles of (a) 0° and (b) 30° (@28 GHz).

as 4×4 . In addition, dummies were employed for maintaining uniformity of the radiation patterns of the active elements located on the outer edges, as described in [14]. As for the distance between the elements, it should be carefully decided for grating lobe-free scanning as described in the literature [35], [36]. The theoretical inter-element spacing of the array can be calculated as

$$d = \frac{\lambda_0}{1 + \sin \theta_{\max}} \tag{1}$$

where *d* is the distance between the elements; λ_0 is the freespace wavelength of 28 GHz, and θ_{max} is the maximum scan angle [37], [38]. According to this equation, to provide a scanning capability of $\pm 30^{\circ}$ with grating lobe-free scanning, the inter-element spacing of the proposed antenna should be less than 0.67 λ_0 (i.e., 7.1mm at 28 GHz). In addition, the distance between elements should be determined considering the minimum region of the capacitive probes with quasicoaxial via transitions in the array design. Based on these conditions, the inter-element spacing of the proposed array was set to 6.2 mm (=0.58 λ_0). In the case of an array feeding method, to obtain higher XPI performance, each element was arranged based on the rotated-fed method introduced in [15].

The configuration of the designed 4×4 patch array in the proposed dual-polarized AiP is illustrated in Fig. 10. The designed array has four identical subarrays in the inner region and 20 dummies with the dimensions of 3 mm × 3 mm in the periphery of these subarrays. In each subarray, four single elements are paced by rotating a single element by 0°, 90°, 180°, and 270° in turn in either the clockwise or counterclockwise direction to realize the rotated-fed method (see the enlarged view for subarray #1 in Fig. 10). Under this condition, the phases of the excited signals between the ports flipped each other (e.g., between Port #1 and #5, Port #2 and #4, and so on) and are set to have 180° difference. The overall dimensions of the designed 4×4 patch array are $37.2 \text{ mm} \times 37.2 \text{ mm} \times 1.2 \text{ mm}$.

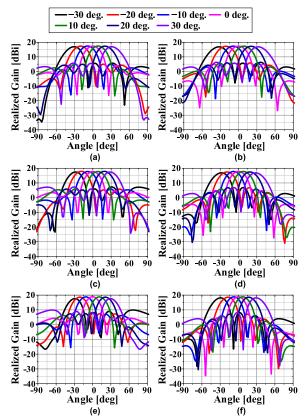


FIGURE 12. Simulated gain pattern results of the 4×4 patch array at different scan angles. (a) *E*- and (b) *H*-planes at 26.5 GHz. (c) *E*- and (d) *H*-planes at 28 GHz. (e) *E*- and (f) *H*-planes at 29.5 GHz.

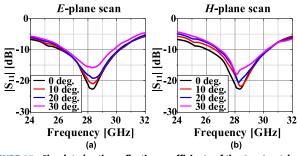


FIGURE 13. Simulated active reflection coefficients of the 4×4 patch array at different scan angles. (a) *E*- and (b) *H*-planes.

The simulated gain patterns of the designed 4×4 patch array with and without the rotated-fed method in the *xz*-plane (i.e., *E*-plane) for the scan angles of 0° and 30° are given in Fig. 11. To consider only a vertical polarization mode for convenience, ports #1, #3, #5, and #7 in each subarray were set to be on in this case (see Fig. 10). As a result, the XPI values of the proposed array with the rotated-fed method at 0° and 30° scan angles are calculated at 72.53 dB and 71.5 dB, respectively. The XPI values are improved by 51.72 dB and 51.52 dB, respectively, compared to the case using the conventional regular-fed method. The peak gain, radiation efficiency, HPBW, and side-lobe level (SLL) of the proposed array at a 0° scan angle are 17.71 dBi, 86.79%, 21.9°, and -13.14 dB, respectively, while at a 30° scan angle they are 17.37 dBi, 85.95%, 21.7°, and -11.44 dB,

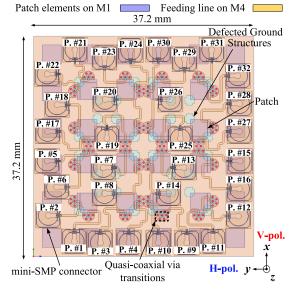
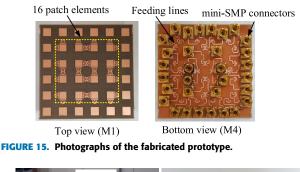


FIGURE 14. Layout of the fabricated 4 × 4 patch array prototype equipped with mini-SMP connectors for direct measurement.



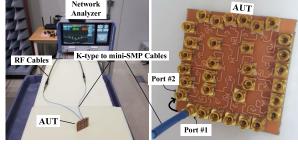


FIGURE 16. Photographs of the experiment setup for measuring the S-parameters of the fabricated prototype.

respectively, which are similar to those values for the conventional regular-fed method. From these results, the use of the rotated-fed method in the proposed array is effective to enhance the XPI values while maintaining other performance values such as gain, HPBW, and SLL.

To assess the beam-steering characteristic of the proposed patch array, the simulated gain patterns in the *xz*- and *yz*-planes for different beam scan angles at several frequencies are presented in Fig. 12. The beam was steered over the angular range of $-30^{\circ} \sim +30^{\circ}$ with a 10° interval by properly adjusting the linear progressive phase shifts among the input ports. As a result, the proposed patch array provides a good beam steering ability over the angular range

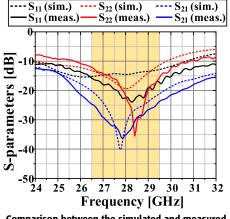


FIGURE 17. Comparison between the simulated and measured S-parameter results of the fabricated prototype.

at several frequencies. The proposed array covers 102°, 94°, and 92° with a gain of 10 dBi in the *E*-plane at 26.5, 28, and 29.5 GHz, respectively, and covers 106°, 98°, and 95° in the *H*-plane. The maximum beam scan angles that satisfy an SLL of -10 dB at 26.5, 28, and 29.5 GHz in the E-plane are calculated at $\pm 34^{\circ}$, $\pm 30^{\circ}$, and $\pm 23^{\circ}$, respectively, and in the *H*-plane at $\pm 36^{\circ}$, $\pm 31^{\circ}$, and $\pm 25^{\circ}$, respectively. The reason for offering the widest beam scan angle at 26.5 GHz is that the separation distance between the adjacent elements in the designed array is set to 6.2 mm which is 0.55 λ_0 , 0.58 λ_0 , and 0.61 λ_0 at 26.5, 28, and 29.5 GHz, respectively. For the additional beam-steering evaluation of the proposed patch array, we analyzed the simulated active reflection coefficients at different scan angles in the E- and H-planes in Fig. 13. The proposed patch array has fractional impedance bandwidths $(|S_{11}| < -10 \text{ dB})$ of 14.56% at a 0° scan angle, and 11.93%, and 11.89% at the 30° scan angle in the E- and H-planes, respectively, and show a well-behaved performance from 26.5 to 29.5 GHz except for the small deviation at the maximum scan angles.

IV. EXPERIMENTAL VERIFICATIONS

To verify the simulation results, we fabricated a prototype of the proposed AiP and performed the measurements. The fabricated prototype was implemented as a connectorized model in which the RF connectors and their pads are included to enable direct measurement using RF cables [14]. Chip integration and over-the-air (OTA) measurement were not dealt with in this experimental verification due to the cost issue.

The illustration of the layout of the connectorized prototype is presented in Fig. 14. The overall dimensions of the prototype are 37.2 mm \times 37.2 mm \times 1.2 mm, which is the same as the simulation model introduced in Section III. The main difference from the simulation model is that thirtytwo miniaturized surface-mount package (mini-SMP) type connectors, connector pads, and additional microstrip lines are contained on the bottom of the M4 layer. The added microstrip lines extend the original ones to the connector pads while generating the 180° phase reversal between the flipped

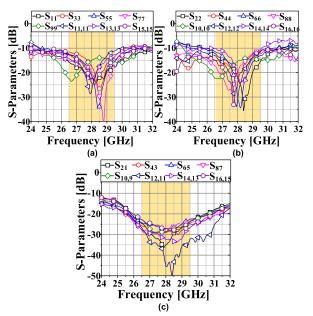


FIGURE 18. Measured reflection coefficients for (a) V-pol. ports and (b) H-pol. port and (c) port-to-port isolation of the fabricated prototype.

ports for the implementation of the rotated-fed method. The photographs of the top and bottom views of the fabricated prototype are given in Fig. 15. The prototype was built using a standard PCB process, and the connectors were mounted on the bottom of the prototype using surface mount technology (SMT).

The measurement setup for assessing the S-parameters of the fabricated prototype is shown in Fig. 16. The Keysight's E8362B two-port vector network analyzer (VNA), the K-type cable, and the K to mini-SMP-type cables were used for the measurements. Using the VNA, one-port and two-port measurements were conducted for each element of the prototype. The remaining ports were kept open during the measurements, considering the complexity of the direct measurement in the antenna array [11], [26]. This approach can give readers a guideline that is able to assess the simulated results of the presented antenna element design.

Fig. 17 shows the comparison between the simulated and measured S-parameter results for element #1 of the array prototype. The resonant frequencies of the reflection coefficients $(S_{11} \text{ and } S_{22})$ and port-to-port isolation (S_{21}) in the measured results are shifted upward relative to the simulated ones. The major reasons for this discrepancy are due to the differences in thickness and dielectric constant of the employed substrate between simulation and measurement, which can result in an upshifted frequency response of the fabricated antenna, as described in [20], [22]. Another difference between the measured and simulated results is a discrepancy in the magnitudes. This may be due to the surface roughness, fabrication errors, and connector arrangements, which are not included in the simulation [21]. Even with the deviations, both the measured and simulated $S_{11}s$ and $S_{22}s$ satisfy the desired level of -10 dB in the frequency range from 25.7 to 29.83 GHz, which completely covers the target 5G NR's n257

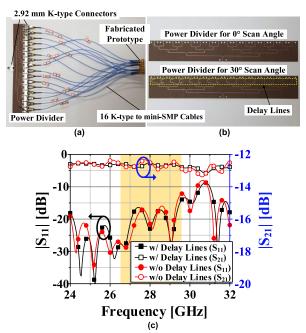


FIGURE 19. Photographs of the fabricated prototype connected with the feeding network and (b) the power dividers for 0° and 30° scan angles using fixed delay lines. (c) Simulated S-parameter results of the power dividers with and without delay lines.

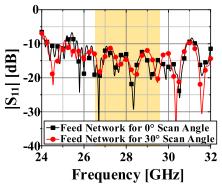


FIGURE 20. Measured reflection coefficients of the fabricated prototype connected with the feeding networks.

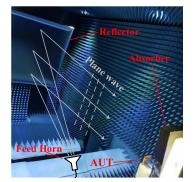


FIGURE 21. Photographs of the experiment setup for measuring the gain patterns.

band ranging from 26.5 to 29.5 GHz. Besides, the measured and simulated $S_{21}s$ meet -20 dB in the targeted frequency band, which is consistent with the prior result in Fig. 5.

The detailed measurement results for the S-parameters of the fabricated prototype are presented in Fig. 18.

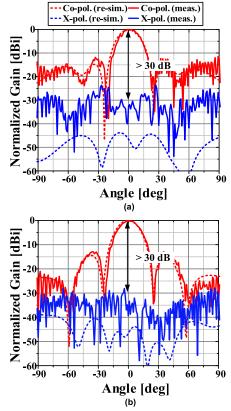


FIGURE 22. Comparison between the simulated and measured gain patterns of the fabricated prototype at 28 GHz. (a) *E*- and (b) *H*-planes.

The reflection coefficients at the ports responsible for the vertical and horizontal polarizations are illustrated in Figs. 18(a) and (b), respectively. It can be seen in Figs. 18(a) and (b) that all measured reflection coefficients from S_{11} to $S_{16,16}$ satisfy -10 dB within the frequency range of 26.26 - 29.58 GHz. The measured port-to-port isolation results are illustrated in Fig. 18(c). All measured port-to-port isolations at frequencies within the targeted frequency band are higher than 22.63 dB. It was also confirmed that the measured mutual couplings between elements are less than -16.28 dB over the targeted frequency range.

The feed network for assessing the reflection coefficients and beam patterns of the fabricated prototype is shown in Fig. 19. To form the synthesized beam patterns, two 16-way T-junction power dividers and the 16 K-to-mini SMP type cables with an equal length of 300 mm were additionally used for the feed networks. One provides equal phase splitting to form a synthesized beam at the 0° scan angle, and the other supplies linear progressive phase shifts with the use of delay lines to generate a beam at the 30° scan angle (see Fig. 19(b)). The simulated S-parameter results of the power dividers with and without delay lines are plotted in Fig. 19(c). The $S_{11}s$ and $S_{21}s$ of both power dividers satisfy -12.62 dB and -12.79 dB in the frequency range of 26.5-29.5 GHz, respectively. We also confirmed that the designed feed networks have reflection coefficients of less than -10 dB and an average insertion loss of 16.24 dB over the same

20

18

16

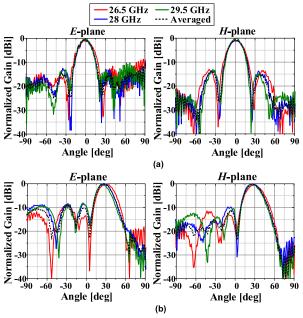
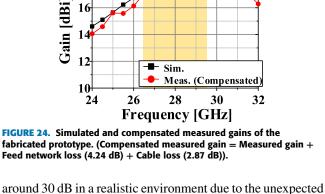


FIGURE 23. Measured gain patterns of the fabricated prototype at 26.5, 28, and 29.5 GHz in the E-and H-plane at (a) 0° and (d) 30° scan angles.

frequency range of 26.5 – 29.5 GHz. Here, a connector loss of 3 dB and a manufacturing loss of 1.24 dB were included, excluding an ideal power division loss of 12 dB. In addition to the feed network, each cable loss was 2.87 dB. To evaluate the array prototype, the measured reflection coefficients of the fabricated prototype equipped with the feed networks are shown in Fig. 20. It is shown that the fabricated prototype with feed networks for 0° and 30° scan angles also satisfies the desired level of -10 dB in the targeted frequency range.

Fig 21 shows the measurement environment for evaluating the gain patterns of the fabricated prototype. The measurements were conducted inside a far-field anechoic chamber where a standard feed horn, a reflector, and an antenna-undertest (AUT) were installed.

Fig. 22 shows the comparison between the measured and simulated gain patterns of the designed array in the E- and H-planes at 28 GHz. For a fair comparison between the simulated and measured results, the measured pattern was compensated for the feed network and cable losses, which were not considered in the simulation model. Here, the simulated results were replaced with the re-simulated results for the connectorized model illustrated in Fig. 14 (see the term re-sim in Fig. 22). The vertical polarization beams were activated in this measurement, with the unused horizontal polarization beams shut off. The measured peak gain of the designed array is 17.37 dBi, which is 0.15 dB lower than the simulated one. The measured and simulated gain patterns show good agreement in the co-polarized component. On the other hand, they show a recognizable difference between the patterns in the cross-polarized component. The simulated one was calculated at 45 dB, whereas the measured XPI value was limited at 30 dB. In this regard, it was reported from the literature [15] that it is hard to achieve better XPIs of



side effects such as measurement misalignment. Even with this limitation, the measured XPI value is sufficient for the dual-polarized mmWave 5G systems. The detailed measurement results for the beam steering patterns of the fabricated prototype are presented in Fig. 23. The gain patterns for beam scan angles, of 0° and 30° are illustrated in Figs. 23(a) and (b), respectively. The measured peak gains of the proposed array for the 0° scan angle at 26.5, 28, and 29.5 GHz are 17.04, 17.37, and 18.07 dBi, respectively, identically in the E- and *H*-planes, and for the 30° scan angle those frequencies are 16.78, 16.91, and 16.44 dBi in the *E*-plane, respectively, and are 16.44, 17.06, and 16.65 dBi in the H- plane, respectively. The measured patterns are well-formed at 0° and 30° scan angles. We also present the simulated and compensated measured gains of the fabricated prototype in Fig. 24. The maximum compensated measured gain in the targeted frequency range is 18.07 dBi. Although the compensated measured gains are slightly higher than those of the simulation at several frequencies, these two results show a good correlation.

Sim.

28

Meas. (Compensated)

30

32

Table 1 summarizes the performance comparison between this work and recent mmWave AiP studies. As for the cost comparison, since it is difficult to define the absolute price of state-of-the-art AiPs, we instead roughly compared previous AiPs with our work in terms of cost using five distinct classes (i.e., High, Medium, Low, Very-low, and Ultra-low). These scorings were determined based on several cost comparisons as given in the literature [10], [19], [26], [39]. Considering [10], the LTCC-based AiP has the highest process cost compared to the other AiP processes. According to [39], the cost of HDI PCB-based MLO AiPs is lower than the LTCC-based AiP, but higher than that of standard PCB-based MLO AiPs. Here, our proposed AiP has the fourth highest cost because it uses the smallest number of high-end substrates compared to other MLO AiPs. Finally, we considered the FR-4 PCB-based AiP to have the lowest cost based on having the cheapest material cost for the FR-4 epoxies, as described in [19] and [26], even with the use of an HDI process. Otherwise, in the bandwidth comparisons, the previous antennas using additional techniques such as ME dipoles [9] and stack patches [15], [21] show wider

Ref.	Pol.	Ant. Type	Center Freq. [GHz]	Array Size	-10 dB Reflection Coefficient BW	# of Layers	Gain [dBi] (Single/ Array)	Port-to- Port Isol. [dB]	XPI [dB]	Process (Materials)	Fab. Cost
[26]	Single	Stack patch (probe-fed)	60	2×4	14.63% (57–66 GHz)	12	3.5~5.5 / 12.7	N/A	17	HDI PCB (FR-4)	Ultra- low
[16]		Bow-tie patch (cavity-backed)	79	2×4	9.25% (76.3–83.7 GHz)	8	5.65~7.9 / 11.6	N/A	30	HDI PCB (Megtron-6)	Medium
[21]		Stack patch (aperture coupled)	60	4×4	20% (54–66 GHz)	6	8.9 / 16.3	N/A	35 (sim.)	Standard PCB (PTFE)	Low
[23]		Single Patch (proximity coupled)	28	2×2	14.4% (25.8–29.8 GHz)	4	5.5~7.5 / N/A	N/A	N/A	Standard PCB (RO4000 [*])	Low
[9]		ME dipole	28	4×4	42.5% (26.5–40.8 GHz)	12	6.9(sim.) / 16.1	>24	15	LTCC (Ceramic)	High
[11]	Dual	Mesh-grid patch	60	1×8	7.87% (61–66 GHz)	12	4.1 / 13.2	>25	N/A	HDI PCB (FR-4)	Ultra- low
[15]		Stack patch (probe-fed)	28	8×8	15.13% (27.5–32 GHz)	12	5.5 / 22.5	>18	30	HDI PCB (Megtron-6)	Medium
[24]		Stack patch (aperture coupled)	94	1×8	7.91% (85–92 GHz)	6	7.3~8.2(sim.) / N/A	>17.8	20	Standard PCB (LCP)	Low
This work	Dual	Single Patch (capacitive probe)	28	4 × 4	11.89% (26.26–29.58 GHz)	4	7.4(sim.) / 17.37	>22.63	30	Standard PCB (PTFE/FR-4 Hybrid)	Very- low

TABLE 1. Comparison between mmWave AiP studies and this work.

* The RO4000 refers to the glass-reinforced hydrocarbon–ceramic substrate.

bandwidth characteristics compared to our proposed antenna. Unlike our proposed AiP, these antennas with additional techniques have more than two resonance frequencies, resulting in a widening of their bandwidths. Although the proposed AiP has a relatively narrow bandwidth, it uses a simple structure that employs the lowest number of substrate layers among the compared radiator designs while also covering the entire target 5G NR n257 band of 26.5–29.5 GHz. In addition, the proposed AiP supports dual-polarization with marked performance in terms of both the port-to-port isolation and the XPI. At the same time, the proposed design offers excellent gain performance as compared to the other AiPs described in [9], [21] with the same array size of 4×4 , while using a highly cost-effective material laminated stack-up and the standard PCB process.

V. CONCLUSION

In this paper, we propose a cost-effective AiP design of a 4×4 dual-polarized high isolation patch array for 5G mmWave applications. To reduce the material cost while mitigating performance degradation, a combined substrate comprised of a low-loss TLY-5 layer and two ultralow-cost FR-4 layers is devised. The antenna elements in the proposed patch array is placed over 16-unit cells of the cross-shaped DGS and are fed by 32 capacitive probes to offer high port-toport isolation between two input ports for dual-polarization. Moreover, the antenna elements are arranged based on the rotated-fed method to further enhance the XPI. We fabricated a prototype for measurement by using the standard PCB process. As a result, the fabricated prototype offers -10 dBreflection coefficient bandwidth in the targeted frequency range of 26.5 – 29.5 GHz and provides peak gains of 17.04, 17.37, and 18.07 dBi at 26.5, 28, and 29.5 GHz, respectively. The measured port-to-port isolations and XPIs are higher than 22.63 and 30 dB in the targeted frequency band, respectively. The proposed AiP is a good candidate for 5G mmWave small-cell communication applications.

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