IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received November 12, 2021, accepted December 1, 2021, date of publication December 3, 2021, date of current version December 17, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3132667

Building Blocks for GaN Power Integration

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This work was supported in part by the European Commission (H2020 Program) within the Project ''GaNonCMOS'' under Grant 721107.

ABSTRACT GaN technology is on the advance for the use in power ICs thanks to space-saving integrated circuit components and the increasing number of integrated devices. This work experimentally investigates a number of key building blocks for GaN power integration. First, an overview of the active and passives devices of the technology is given with focus on area-efficient layouts for power transistors and limitations of on-chip capacitors and inductors with comparison to other IC technologies. Digital and analog basic circuits as part of device libraries are examined and optimized with regard to area-efficiency. The NOT gates have active areas as low as 56.7 μm^2 and max. static currents of 0.12 mA with high noise margins. Further digital gates are presented. For the analog circuits, differential amplifiers and voltage reference concepts are presented and compared. Finally, GaN power integration is discussed, and integration levels are defined and described. The GaN technology is compared with other IC technologies, and future challenges and perspectives are shown. GaN power integration based on building blocks aims to exploit the full potential of the lateral GaN technology in order to compete with Si-based IC technologies in the future.

INDEX TERMS Gallium nitride, integrated circuit technology, power integrated circuits, logic circuits, analog circuits.

I. INTRODUCTION

GaN wide bandgap performance together with monolithic integration is rapidly evolving new generation of power electronics, which progressively lower size, losses and cost of these systems and its applications. In this manner, first GaN power ICs on cost-effective Si-substrates have successfully entered the market and combine the superior figure-of-merits compared to Si [1]. The lateral structure of the GaN-on-Si technology allows monolithic integration of several devices on a single chip [2], which improves performance due to lower parasitics and reduced assembly effort. A major challenge is the lack of p-type devices, as well as the large structure size compared with Si CMOS [3] or Si BCD (Bipolar-CMOS-DMOS) technologies.

There are already several GaN-on-Si technologies based on the AlGaN/GaN high electron mobility transistor (HEMT) with p-GaN or MIS gate [4]–[13] for GaN power integration. In addition, technologies with Silicon-on-Insulator (SOI) substrates are available as multi-project wafer [14].

The associate editor coordinating the review of this manuscript and approving it for publication was Chi-Seng Lam.

The integration of power devices and peripheral components enables an increase in function and power density in combination with a reliability improvement driven by a continuous further development of the technology. The peripheral components consist of driving, sensing, protection, control, interface [8], and auxiliary power supply. Many different circuits have already been realized in such GaN power platforms to increase and investigate the circuit integration of GaN ICs. These includes digital circuits like logic gates in nMOS logic or direct coupled FET logic (DCFL) [15]–[19] and analog circuits like amplifiers, comparators or references [17], [20]–[24]. Combined or cascaded circuits such as gate drivers [25]–[30], and protection functions [31], [32] can be implemented using digital and analog circuits. The development of these buildings or function blocks allows the realization of more complex circuits consisting of power device(s), driver, control [33] in combination with protection [6] as well as power supply [34]. Furthermore, GaN power ICs consisting of power device(s) and driver(s) are already commercially available from companies such as EPC or Navitas Semiconductor and many more are in the development phase of such ICs [35]. Thus, the integration of

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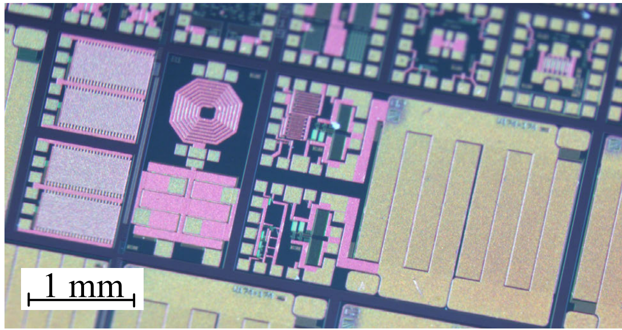

FIGURE 1. Multi-project wafer with monolithically integrated GaN power circuits consisting of power devices and additional periphery in a GaN-on-Si technology.

GaN devices has become an obvious technology trend in the GaN power industry.

This work experimentally investigates a number of key building blocks for GaN power integration. Section II shows and describes a typical GaN power IC technology, shown in Fig. 1. This technology is similar to the technologies from [4], [7], [10], [12], [13]. The technology is the basis for the development of the active and passive devices, shown in the section III. Active devices in such technologies have already been intensively investigated. Therefore, only a small overview is given and layout approaches for power transistors are presented. However, passive components are still in the early research phase in these GaN power technologies based on p-GaN gate. For this reason, the on-chip passives are investigated in more detail; their limitations are shown and compared with similar technologies. In section IV, the digital and analog circuits are analyzed and compared with similar work. The circuits include logic gates, amplifiers or comparators. To compete with Si-based BCD IC technologies, these circuits must be fabricated on a small chip area and have low current consumption. The level of integration and a comparison of IC technologies as well as the future challenges and perspectives are discussed in Section V. Section VI concludes this article.

II. GAN POWER IC TECHNOLOGY

The epitaxial structures of this typical GaN-on-Si technology starts with a low resistive 4-inch Si substrate with a thickness of $\sim$700 μm. A step-graded AlGaN/GaN buffer and an AlGaN barrier are grown above [2], [36]. A p-GaN layer with Mg concentration of $\sim$3-4$\times 10^{19}$ cm^{-3} and a thickness of 50 nm covers the epi-stack and is structured to realize the p-GaN gates. The vertical breakdown of the graded buffer is $>$750 V and has a linear dependence with the buffer thickness of $\sim$150 V/μm determined at a leakage current of 1 μA [2]. The AlGaN/GaN heterojunction establishes a highly conductive two-dimensional electron gas (2DEG), which yields in a sheet resistance of $\sim$800 $\Omega/\square$. The 2DEG is connected with ohmic contacts (OHM). The active devices can be separated by an isolation. A Schottky metal (METFP) is used to form a gate contact of the HEMT or an anode contact for the Schottky barrier diode (SBD). The threshold voltage is shifted into the positive range by the p-GaN layer and enhancement-mode (e-mode) or depletion-mode (d-mode) devices can thus be fabricated in the same technology. By increasing the depletion length, a higher breakdown voltage can be achieved. Therefore high-voltage (HV) and low-voltage (LV) devices can fabricated in the same IC. A further increase in the breakdown voltage can be achieved by using multiple field plates. In this technology, the gate field plate is realized with METFP and the source-connected field plate with the interconnection metal (MET1). The field shaping has already been studied in [37]. An lateral field-effect-rectifier (LFER) can be formed from the e-mode HEMT by a gate-to-source connection [38]. A galvanic metallization (METG) realizes a low-resistive connection. A final passivation protects the structures and is opened at the bond pads. The passivation between the AlGaN barrier and METFP is 100 nm and between METFP and MET1 as well as MET and METG is 300 nm. A breakdown voltage of $\sim$200 V is achieved for the passivation between MET and METG, which corresponds to a dielectric strength of $\sim$0.67 V/nm. Passive devices such as resistors, capacitors and inductors can be realized using the metal layers. A simplified cross-section of this technology is shown in Fig. 2 with the active and passive devices. Further devices can be integrated in this technology like GaN HEMTs with integrated freewheeling diode [39], [40] or multi-stage cascodes [41].

III. DEVICES

A. ACTIVE DEVICES

The HEMT can be divided into three channel sections: Gate-source length l_{GS}, gate length l_{G} and gate-drain length l_{GD}. The sum corresponds to the channel or drift length given by: $l_{\mathrm{CH}} = l_{\mathrm{GS}} + l_{\mathrm{G}} + l_{\mathrm{GD}}$, whereas l_{GD} corresponds at the same time to the depletion length. The gate head is a T-gate with an overhang of 0.3-0.5 μm towards the source l_{GFP} and an overhang of 0.5-2 μm towards the drain depending on the voltage. The source-connected field-plate has a length l_{SFP} of 0.8-4 μm, dimensioned from the gate foot edge to the drain.

Fig. 3 (a) shows the transfer characteristic of e/d-mode devices, measured at $V_{\mathrm{DS}} = 10$ V. The average value of the threshold-voltage V_{TH} is 1.0 V and -1.3 V for each of the 37 devices and has a standard deviation of 0.07 V and 0.26 V. The histogram is shown in Fig. 3 (b). The threshold voltages can be shifted via the barrier thickness, Al-content and p-GaN layer according to [42] to a typical threshold voltage of about 2 V. The additional p-GaN layer reduces the max. saturation current and max. transconductance.

The min. theoretical on-resistance is determined by the drift zone, gate width, and the 2DEG sheet resistance, and given by $R_{\mathrm{ON}} = (l_{\mathrm{CH}}/W_{\mathrm{G}}) \cdot R_{\square,2DEG}$. Fig. 4 (a) shows the on-resistance as function of the channel length for different HEMT structures with different field-plate configurations measured at $V_{\mathrm{DS}} = 0.5$ V. The parameter of the devices

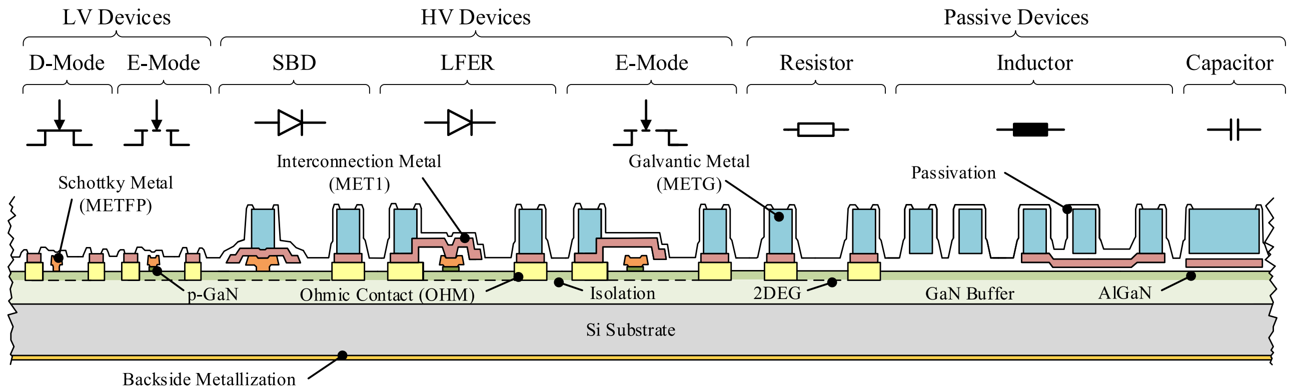

FIGURE 2. Simplified cross-section of the GaN-on-Si technology as GaN power IC platform. In the platform, there are different active devices, e-/d-mode HEMTs, Schottky barrier diodes (SBD), and lateral field-effect rectifiers (LFER) as low-voltage (LV) or high-voltage (HV) devices. In addition, there are passive components such as resistors, inductors, and capacitors.

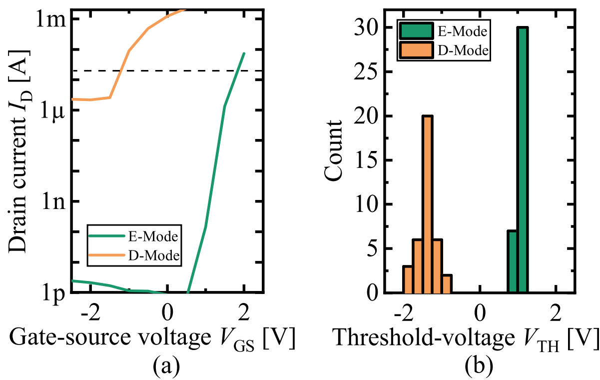

FIGURE 3. (a) Transfer characteristic at V_{DS} = 10 V and (b) histogram of the threshold-voltage distribution for 37 e-mode and d-mode GaN HEMT devices each. The gate-width is 100 μm.

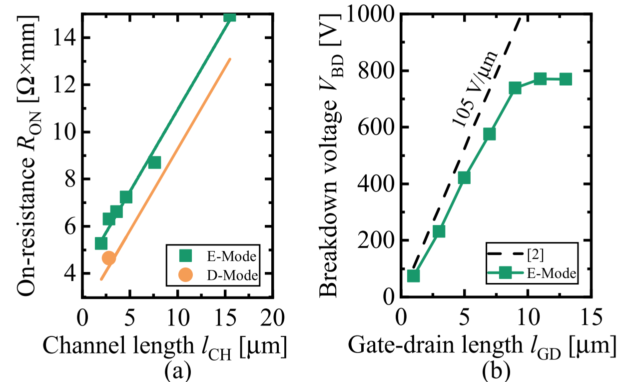

FIGURE 4. (a) On-resistance as function of the channel length for both type of devices with linear interpolation and (b) breakdown-voltage as function of the gate-drain length determined at I_{DS} = 10 μA for e-mode devices.

(all with the same gate width of 1 mm) are listed in Table 1 without field-plate configuration. A linear interpolation of the e-mode devices is also shown. For the d-mode devices, the straight line was only shifted. The breakdown voltage is depend on the depletion zone. Fig. 4 (b) shows the breakdown voltage as function of the gate-drain length determined at $I_D = 10\ \mu$A for devices with small gate-width of 50 μm and without source-connected field-plate. The increment value is 2 μm. The dashed line shows the same determined values in a similar technology, resulting in a linear dependence of 105 V/μm [2].

A typical output characteristic of an e-/d-mode device of the 12 V-class is shown in Fig. 5 (a). Fig. 5 (b) shows the forward characteristic of the two low-voltage diodes LFER and SBD. The characteristic curve can be linearized by using a turn-on voltage and a differential resistance, which corresponds to the on-resistance: $V_F = V_{T0} + R_{ON} \cdot I_F$. The device parameter are listed in Table 1. For the diodes, the channel is divided into anode length l_A and anode-cathode length l_{AC}. The turn-on voltage of the LFER is lower than with the SBD. However, the on-resistance of the LFER is higher compared with the SBD due to the asymmetrical structure and the

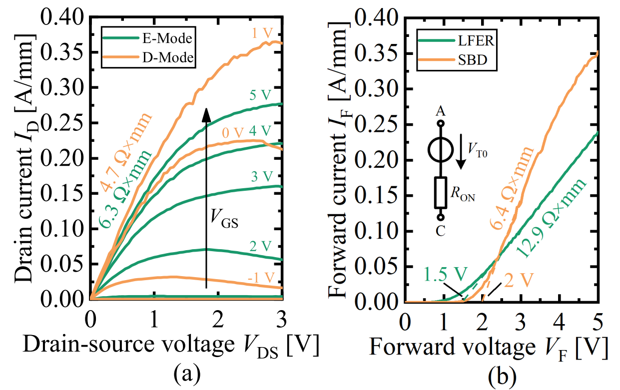

FIGURE 5. (a) Output characteristic of an e-/d-mode 12 V-class HEMT and (b) forward characteristic of a LFER and SBD with inset of the equivalent circuit.

resulting different transconductances in forward and reverse direction [38], [40]. The LFER was realized by an e-mode HEMT with short-circuited gate-source terminal, therefore the drift zone is increased by the l_{GS}-section.

TABLE 1. Active devices.

		E-Mode				D-Mode	SBD	LFER[3]
Class	V	650	300	100	12	12	-	-
l_{GD} (l_{AC})	µm	12.5	6	3	1.5	1.5	2.6	2
l_G (l_A)	µm	1	1	0.6	0.6	0.6	1	0.6
l_{GS}	µm	2	1	1	1	1	-	1
R_{ON}' [1]	Ω×mm	14.9	8.7	7.2	6.3	4.7	6.4	12.9
V_{T0}	V	-	-	-	-	-	2	1.5
V_{BD} [2]	V	776	-	182	54	-	-	-
$g_{m,MAX}$	mS	-	-	-	58.3	155.4		

[1] at V_{DS} = 0.5 V (ΔV_F = 0.5 V)
[2] at I_D = 10 µA
[3] E-mode HEMT with gate-source short circuit

The layout of the devices plays an important role for power transistors. With the scaling of the gate width using, a reduction of the on-resistance and a higher current carrying capability can be achieved. The theoretical min. area specific on-resistance $R_{ON} \times A_{MIN}$ of an active device is limited by:

$$R_{ON} \times A_{MIN} = R_{\square,2DEG} \cdot l_{CH}^2 \tag{1}$$

the gate width is reduced in the equation and without the area for the ohmic contacts and contact pads. The typical layout is the comb structure. However, this structure has its limits in low-voltage applications due to minimum dimensions and clearance of the uppermost low-resistive metallization layer. The layer METG is used in combination with MET1 and OHM to form the fingers of the parallel HEMT segments, shown in Fig. 2 and Fig. 6 (a). Therefore, the drift and/or depletion zone cannot be chosen arbitrary small in large-area devices, but the term goes quadratically into $R_{ON} \times A_{MIN}$ using (1). An alternative layout is the matrix structure for LV applications. In this structure, only the lower metal layers MET1 and OHM are used for the finger structures. These layers allow a smaller resolution and clearance compared to METG, which allows to shrink the channel. The currents of the finger structures are collected via a 90° rotated bus track, which is realized with METG. The drain and source bus tracks are visible in Fig. 6 (b). A detailed analysis of the two layout structures is presented in [37], [43]. Two large-area e-mode HEMTs were realized on the same chip area (2×2 mm^2) with different layout structure. The device parameter are listed in Table 2. The gate width of the matrix layout is more than twice as large as that of the comb layout, realized on the same area. Furthermore, the depletion length can be halved. Fig. 6 (a) and (b) shows schematic 3D illustration. The measured output characteristic of both transistors are shown in Fig. 6 (c). The on-resistance R_{ON}, measured at V_{DS} = 0.35 V, and the area-specific on-resistance $R_{ON} \times A$ is reduced by 37.5% with the matrix layout. However, the comb structure achieves a higher breakdown voltage and at the same time lower drain leakage currents, and therefore the voltage class for the matrix structure is significantly lower.

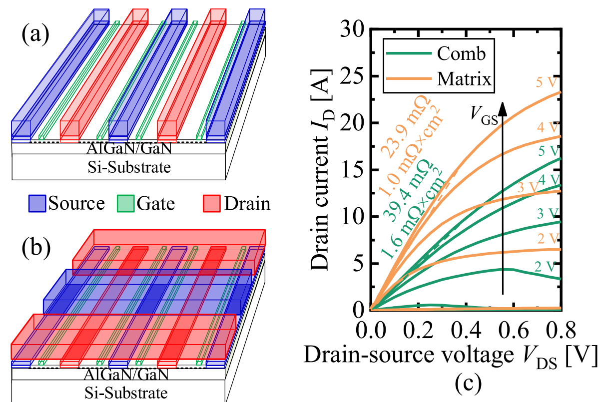

FIGURE 6. Schematic 3D illustration of the metallization for source, gate and drain with (a) comb structure, (b) matrix structure and (c) measured output characteristic for e-mode power transistors with the same chip area of 2 × 2 mm^2 and different layouts.

TABLE 2. Layout comparison.

		Comb	Matrix
Class	V	>100	>25
W_G	mm	151	353
$l_{GD}/l_G/l_{GS}$	µm	3/0.6/1	1.5/0.6/0.7
A	mm²	4	4
R_{ON} [1]	mΩ	39.4	23.9
$R_{ON}\times A$	mΩ×cm²	1.6	1.0

[1] at V_{DS} = 0.35 V

TABLE 3. Resistors.

		Metal				Epi.
Layer		OHM	METFP	MET1	METG	2DEG
Sheet resistance $R_\square$	Ω/□	~2	~0.1	~0.1	~0.001	~800
Min. length l_{MIN}	µm	2	0.5	1	5	2

B. PASSIVE COMPONENTS

There are two types of resistors available in the GaN power IC technology, metal and epitaxial resistors. The parameter of the resistors are listed in Table 3. In comparison, there are additionally diffused and poly resistors in Si BCD technologies. The resistance is similar to the on-resistance given by: $R = l/W \cdot R_\square$, whereas $R_\square$ is the sheet resistance of the used layer. However, it is difficult to realize high-resistive resistors in this technology. In this case, 2DEG meander structures must be used, which are not linear and have a saturation current.

In addition to resistors, capacitors can also be integrated. There are the two types, MIM capacitors (shown in Fig. 2) and p-GaN gate capacitors in this technology. The p-GaN gate capacitors offer the counterpart to MOS capacitors from Si-based IC technologies in this technology. The capacitance C of the MIM capacitors can be calculated by the well-known formula $C = \varepsilon_0 \cdot \varepsilon_r \cdot (A/t)$, whereas the relative permittivity ε_r and thickness t of the SiN passivation are process-specific parameters. The thickness of the passivation has been mentioned in section II. The relative permittivity for

TABLE 4. Capacitors.

		MIM	MIM	Stacked MIM	Stacked MIM	p-GaN gate
No.		C1	C2	C3	C4	C5
Layer		OHM METFP	MET1 METG	METFP MET1 METG	OHM METFP MET1 METG	GaN AlGaN p-GaN METFP
C [1]	pF	6.89	2.17	4.64	11.55	11.89
C/A	fF/µm^2	0.689	0.217	0.464	1.155	1.189
ESR	Ω	2.60	5.44	3.66	1.73	3.29
Q_{PEAK}		208	213	66	83	46
V_{MAX} [2]	V	50	>150	150	50	2-6.5

[1] at 4 V

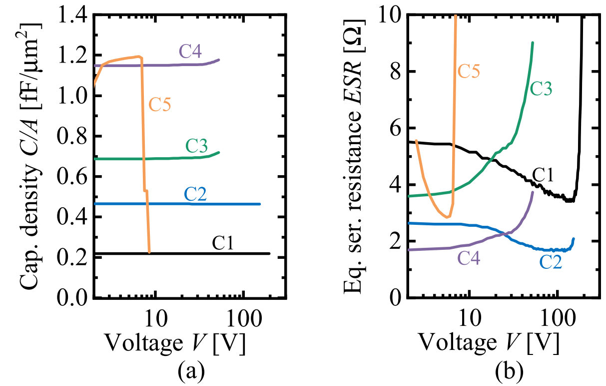

FIGURE 7. On-chip capacitors C1-C5 from Table 4 (a) area-normalized capacitance density as a function of the voltage and (b) determined ESR as function of the voltage.

the amorphous SiN is ~5.4-6.7. Its area is a design parameter. By stacking serval MIM capacitors, a higher capacitance density can be achieved. Table 4 lists five different on-chip capacitors, realized on the same chip area of 0.1×0.1 mm^2. The plate capacitor structures were characterized with a LCR meter at a frequency at 1 MHz with different operating voltages, which measures the capacitance C and the dissipation factor $tan\delta$. The reciprocal of the dissipation factor is the quality factor Q. A typical lumped capacitor model includes an ideal capacitor and a resistor called equivalent series resistance ESR. The ESR can be calculated using the loss factor as follows: $ESR = 1/(\omega \cdot C) \cdot tan\delta$. Fig. 7 (a) shows the area-normalized capacitance density C/A as function of the voltage V. The capacitance and capacitance density are determined at 4 V. The calculated ESR as function of the voltage is shown in Fig. 7 (b). The stacking technique allows a significantly higher capacitance density. By stacking three MIM capacitors (C4), a capacitance density of 1.155 fF/μm^2 is achieved. At the same time, all MIM and stacked MIM capacitors have an operating voltage of ≥50 V at room temperature. The ESR is very low for the capacitors with the low-resistive metal layer METG. A MOS capacitor in the GaN power IC technology can be realized by additional process steps with extra costs [44]. Another way is to use the gate structure (metal/p-GaN/AlGaN/GaN) as a capacitor to provide a high capacitance density. The explanation and modeling of the capacitance is described in [44] using the energy band diagram. However, the performance can be affected by increased leakage currents, threshold voltage instability and gate-stress degradation. The capacitance density of all MIM capacitors is exceeded by the p-GaN gate capacitor C5. A more than 5 times higher capacitance density is achieved with the p-GaN gate capacitor compared with the simple MIM capacitor C1. Above the threshold voltage, the capacitance is almost constant until a max. operating voltage. The ESR, on the other hand, depends strongly on the voltage, but is in the same order of magnitude as the MIM capacitors. The operating voltages ranges from the threshold voltage to a voltage of 6.5 V. The leakage current at 6.5 V is 32.6 μA/mm^2. In comparison to the MIM capacitors, this leakage current is very high, which is reflected in a lower peak quality factor. As a comparison, in a 0.25 μm-BiCMOS technology, for example, capacitance densities of 1.1/2.1 fF/μm^2 are achieved [45]. The further development of the MIM capacitors leads to the replacement of conventional insulator materials such as SiN and SiO by materials with a high dielectric constant. With these materials capacitance densities of ~3-13 fF/μm^2 are possible [46].

In addition to the capacitors, inductors and transformers can also be integrated. There are various examples of on-chip inductor types, such as spiral, toroid, stripline with or without magnet core material. The most commonly used on-chip inductor type is the spiral inductor without core material [47], shown in Fig. 2. In order to calculate the design parameter of a spiral inductor in this technology, a design flow [48] is introduced with simple expression [47], which describes the electrical behavior of the inductor in the relevant working range with sufficiently accuracy. The basis for this design flow is the common lumped inductor model with inductance L, equivalent series resistance ESR and parallel capacitance C_P. Not included in the model are skin effects and eddy currents. Circular and hexagonal spirals are selected due to their improved current distribution compared to rectangle spirals. Two metals are required for a spiral: one for the spiral itself and one for the return wire from inside the spiral. With the inductance and capacitance the self-resonance frequency can be calculated according to $SRF = 1/(2\cdot(\sqrt{L \cdot C_P}))$. The rated current can be calculated by the power loss that can be dissipated through the substrate. The calculation and thermal considerations are carried out in detail in [48]. Table 5 listed the geometry data and extracted inductor parameters, which corresponds to the analytically calculated parameters. Additionally the parameters were verified with EM simulations. The extracted inductor parameters are shown in Fig. 8. These parameters are based on on-wafer two port measurements starting from 100 kHz. All inductances are <24 nH, but L1 and L3 have only a small ESR of <2 Ω, due to the realization with METG. The quality factor is given by $Q = (\omega \cdot L)/ESR$. In comparison with other on-chip inductors form [49], the peak quality factor of the spiral inductors L1 and L3 are in the same range than other technologies.

TABLE 5. Inductors.

		Circular Spiral		Hexagonal Spiral
No.		L1	L2	L3
Layer *Spiral*		METG	MET1	METFP
Return wire		MET1	METFP	MET1
Inner diameter d_{IN}	µm	88.6	27.3	115.0
Outer diameter d_{OUT}	µm	415.0	160.8	610.0
Turns n		8.5	16	7.5
Space S	µm	8.6	1.93	10
Width W	µm	10.6	1.93	24
Area A	mm²	0.135	0.002	0.412
Inductance L	nH	12.6	~20.0	19.0
Inductance density L/A	nH/mm²	99.3	10000.0	46.1
Eq. ser. resistance ESR	Ω	1.6	115.2	1.1
Self-resonant frequency SRF	GHz	2.0	>3.0	1.9
Peak quality factor Q		5.34	1.63	4.43
Rated current I [1]	A	0.98	0.037	2.103

[1] at a temperature rise of 40°C

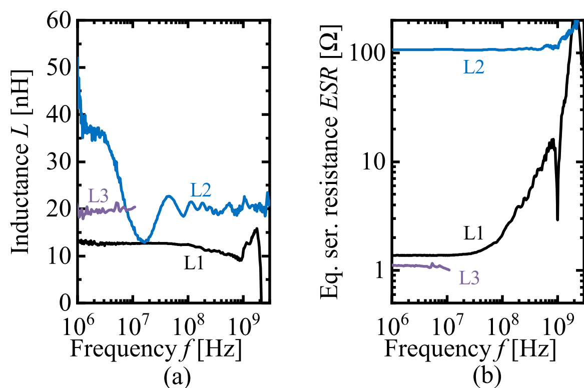

FIGURE 8. On-chip spiral inductors L1-L3 from Table 5 (a) inductance as a function of the frequency and (b) ESR as function of frequency.

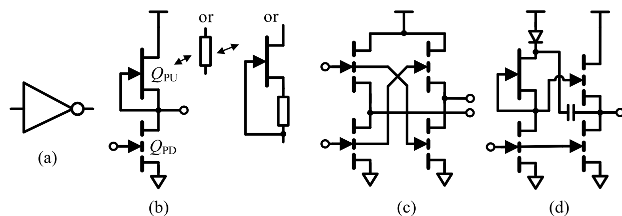

FIGURE 9. DCFL inverter as (a) symbol, (b) inverter with different load configurations: active d-mode load, resistive load, V_{TH}-shifted d-mode load, (c) PCFL inverter, and (d) bootstrapped push-pull stage with DCFL inverter.

IV. DIGITAL AND ANALOG CIRCUITS

A. DIGITAL CIRCUITS

Digital or logic circuits are essential building blocks for gate driver or other functional sub-circuits. Power consumption is of decisive importance in digital circuits. In Si-based CMOS technologies n- and p-channel transistor are available, which can be used for the same named CMOS logic. However, in the most GaN technologies only n-channel d-/e-mode transistors are available. Thus, no CMOS logic can be realized and the change to NMOS logic or direct-coupled FET logic (DCFL) for HEMTs is inevitable. Generally, the logic inverter (see Fig. 9) consists of a pull-down (PD) and up (PU) device.

TABLE 6. Not gates.

		DL	DRL	RL	DL	DRL
No.		INV1	INV2	INV3	INV4	INV5
W_{PD}	µm	18	3	30	30	30
L_{PD}	µm	2.7	2.7	2.7	2.7	2.7
W_{PU}	µm	3	3+80 [1]	5	5	5+5 [1]
L_{PU}	µm	2.7	2.7+3 [1]	20	2.7	2.7+20 [1]
β		6		44.4	6	
A_{ACTIVE}	µm²	56.7	256.2	181	94.5	194.5

[1] first d-mode device, second resistor device

Usually the DCFL inverter uses an n-channel e-mode HEMT as PD device and a d-mode transistor with short-circuited gate-source path as PU device. The PU devices acts as an active load and is called d-mode load (DL), as shown in Fig. 9 (b). There are three different load configurations: passive or resistive load (RL), the standard active d-mode load (DL) and V_{TH}-shifted active d-mode load (DRL). If a resistor is added between gate and source short circuit, the negative threshold voltage of the d-mode transistor is shifted further into positive and the current flow through the transistor is reduced. The DC characteristic of the DCFL inverter is called voltage transfer characteristic (VTC). For an input voltage lower than the threshold voltage of the PD device $V_{IN} < V_{TH,PU}$ the transistor turns off and high-level output voltage V_{OH} corresponds to the supply voltage V_{DD}. However, if the input voltage is $V_{IN} > V_{TH,PU}$ the transistor turns on and a voltage divider is formed between the PD and PU device. The low-level output voltage can be described by the on-resistance of the two transistors as follows: $V_{OL} = R_{PD}/(R_{PD} + R_{PU})$. With the gate width and length of the PU and PD device, the resistance ratio is given by $\beta = (W_{PD}/L_{PD})/(W_{PU}/L_{PU})$. A larger value of β results in a sharper transition, a higher V_{OL} and a higher noise margin. For high performance logics, the ratio must be as large as possible and $V_{TH,PD}$ must be close to $V_{DD}/2$. The low-level input V_{IL} and the high-level input voltage V_{IH} is defined at $dV_{OUT}/dV_{IN} = -1$. The robustness is defined by two noise margins: low-input noise margin ($NM_L = V_{IL}$- V_{OL}) and high-input noise margin ($NM_H = V_{IH}$ - V_{OH}) [19]. Table 6 lists different realized and miniaturized logic inverters in the GaN power IC technology. INV1 and INV2 are critically designed. The active area A_{ACTIVE} is the area without wiring and ohmic contacts. Fig. 10 (a) shows the VTC at $V_{DD} = 5$ V of the logic inverter INV4. In the low output state, it applies: $I_{STAT} = 1.9$ mA, $V_{OL} = 0.28$. The low-level input voltage is 1.7 V and the high-level input voltage 2.9 V. The transition region has a width of 1.2 V due to a small resistance ratio of 6. The noise margins are $NM_L = 1.42$ V, $NM_H = 2.1$ V. Furthermore, supply voltages above 12 V are possible, whereby the transition regions expands. Fig. 10 (b) shows the static current as function of the input voltage. In the low-input region only the leakage current of the PU device is visible, which is <0.4 μA for all NOT gates. In the transition region, the static current increases exponential until it reaches

TABLE 7. Comparison of DCFL NOT gates with DL.

		INV4	[15]	[16]	[17]	[19]
Technology		p-GaN	MIS	p-GaN	MIS	MIS
$V_{TH,E}/V_{TH,D}$	V	1/-1.3	2/-2.9	1.6/-1.33	1.5/-8.5	2.5/-
W_{PD}/L_{PD}	µm	30/2.7	200/17	27/3.5	2000/10	160/8
W_{PU}/L_{PU}	µm	5/2.7	5/17	6/3.5	50/18	10/32
β		6	40	4.5	72	54
V_{DD}	V	5	10	5	10	5
V_{OL}/V_{OH}	V	0.28/5	0.2/10	0.33/4.99	0.11/10	0.07/5
	%	94.4/100	98/100	93.4/99.8	98.9/100	98.6/100
V_{IL}/V_{IH}	V	1.7/2.9	-/-	2.03/2.99	3.33/4.61	2.2/2.8
V_{TR}	V	1.2	1.1	0.96	1.28	0.6
	%	24	11	19.2	12.8	12
NM_L/NM_H	V	1.42/2.1	1.7/7.2	1.58/2	3.22/5.39	2.2/2.13
	%	56.8/84	34/144	63.5/80	64.4/107.8	88/85.2
I_{STAT}	mA	1.42	-	2.1[1]	-	-
A_{ACTIVE}	µm²	94.5	3465	181	36900	1600

[1] from output characteristic curve

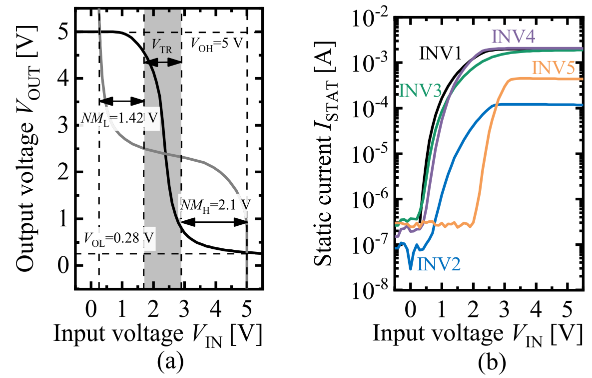

FIGURE 10. Measurement of logic inverters with V_{DD} = 5 V from Table 6: (a) VTC of INV4 and (b) Supply current as function of the input voltage.

the final value in the high-input region. INV2 has the lowest static current of 0.12 mA followed by INV5 with 0.44 mA. The remaining gates have a current of <2.1 mA. The overall dissipation per gate is the sum of the static and dynamic parts. The static current also plays a role for the propagation delay. Thus, there is a trade-off between speed and losses [12]. A RL NOT gate has an increased rise time and area compared to a DL NOT gate with the same power losses [3].

Table 7 compares different DCFL NOT gates with active d-mode load (DL) configuration in the GaN-on-Si technology at room temperature found in the literature [15]–[17], [19]. The logic inverter from [19] shows the best values for the noise margins, but requires a large area compared to INV4. The NOT gates from [15], [17] need the largest area. The DCFL inverter from [16] has a similar area as INV4, but requires a higher static current due to a lower resistance ratio of 4.5. A smaller area reduces the input capacitance of the next stage. For this reason, the power-delay-product *PDP* decreases with a smaller area. Another way to improve the *PDP* is to reduce the supply voltage. The V_{DD} reduction is accompanied by the reduction of $V_{TH,E}$. This makes the use in GaN power ICs impossible, because a high e-mode threshold voltage of power transistors is desired. The V_{DD} reduction can therefore only be used for pure logic technologies.

The lack of a p-type device results in a static current flow, which results in a high power dissipation and consequently a higher *PDP* compared to CMOS. Complementary signals are used to replace the lack of complementary transistors, which mimics the CMOS behavior. This leads to the pseudo-complementary FET logic (PCFL), which is based only on n-channel e-mode transistors in the GaN technology [50]. Fig. 9 (c) shows a PCFL inverter with four transistors a complementary input as well as output signals. It can be seen that the PCFL inverter consists of two identical paths with PD and PU device. These paths are often referred to a push-pull or totem-pole stage in TTL circuits. The advantage of PCFL gates is the reduction of the static power dissipation. However, the disadvantages of PCFL gates or push-pull stages is the voltage drop in the high-level output voltage. It follows V_{OH} = V_{DD} - $V_{TH,E}$. This voltage drop will significantly increase the low-to-high propagation time. In addition, a certain over-drive of the next stage must be guaranteed, which means that V_{DD} must be $>2\times V_{TH,E}$. The work in [51] shows a comparison between DCFL and PCFL inverter in a similar p-GaN power IC technology with a low threshold voltage of 0.5 V, that the maximum static current could be reduced by factor $\sim 10^3$. A further possibility to reduce the voltage drop of the PCFL inverter is the extension with a bootstrap circuit. Fig. 9 (d) shows a push-pull stage with DCFL inverter extended by a bootstrapped circuitry. This stage has the advantage compared to a PCFL inverter that the voltage drop can be reduced. The static current should be similar to the PCFL inverter.

The realization of further logic gates based on the DCFL are possible. The NOR and NAND gates can be derived from DCFL NOT gates. AND and OR in turn must be connected together from NOR or NAND and NOT. Fig. 11 (a) and (b) shows the symbol and schematic of the NOR gate. The NOR gate consists of two e-mode PD and an active d-mode load as PU device. Other load configurations are also possible. The gate widths and lengths for PD and PU devices are identical to the NOT gate. Fig. 12 (a) shows the measured VTC of the NOR gate with V_{DD} = 5 V with four input voltages: $V_A = 0$, $V_A = 1$, $V_A = V_B$, $V_A = \neg V_B$. The insets show the corresponding truth table with the colored marking of the associated input voltage. For the case $V_A = 1$, it can be seen that if one input transistor is turned on, $V_{OL} = 0.37$ V. However, if two input transistor are turned on, the output low-level is 0.16 V due to the changed voltage divider of the PD and PU devices. Fig. 11 (c) and (d) shows the symbol and schematic of the NAND gate with dual gate e-mode HEMT. The d-mode load is identical to the NOT gate. The input transistor has the same gate width as INV4 with 30 μm, but the channel lengths differ due to the dual gate. The length increases from 2.7 μm to 4.2 μm with each 0.5 μm wide gate lengths. In comparison to two input transistors arranged on above the other [19], a considerable amount of chip area can be reduced due to the elimination of further ohmic contacts. Fig. 12 (b) shows the measured VTC of the NAND gate with V_{DD} = 5 V and four input voltages: $V_A = 0$, $V_A = 1$, $V_A = V_B$, $V_A = \neg V_B$. The insets show the corresponding

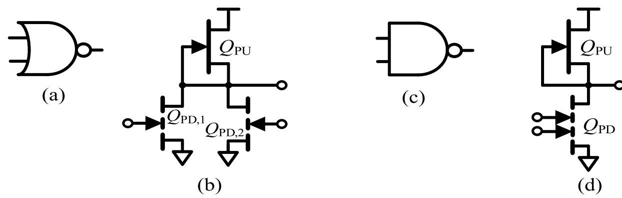

FIGURE 11. (a) Symbol and (b) schematic of a NOR gate and (c) symbol and (d) schematic of a NAND gate with dual gate e-mode HEMT.

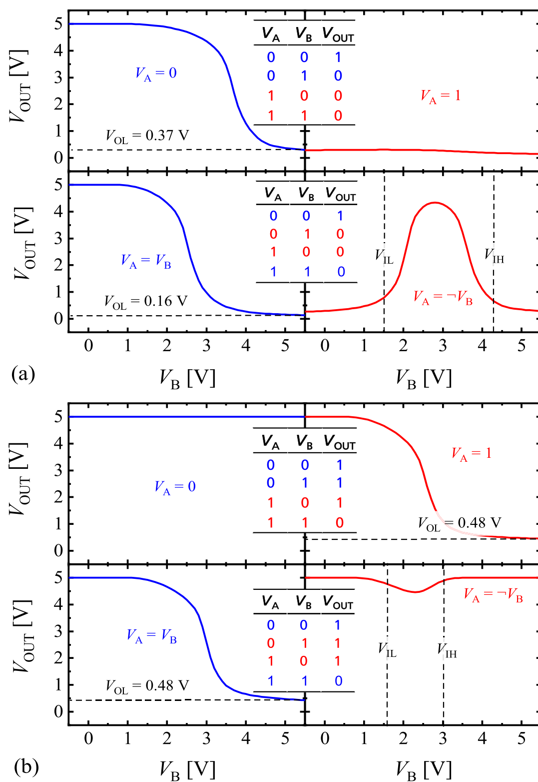

FIGURE 12. VTC of the (a) NOR and (b) NAND gate with $V_{DD} = 5$ V and four input voltages: $V_A = 0$, $V_A = 1$, $V_A = V_B$, $V_A = \neg V_B$. Insets with the corresponding truth table.

truth table with the colored marking of the associated input voltage. With this NAND gate the V_{OL} is always 0.48 V even if both inputs are high in contrast to the NOT gate.

B. ANALOG CIRCUITS

In addition to the digital circuits in the GaN power IC technology, the analog circuits are important building blocks for signal conditioning for e.g. analog controls or amplification of sensor signals. These blocks include amplifiers and voltage references. The differential amplifier (illustrated in Fig. 13 (a)) is the basic circuit of more complex amplifiers like opamps and comparators. There are also some works based on the p-GaN technology. The differential amplifier basically consists of a differential pair Q_1/Q_2, two loads Q_3/Q_4 and a current source Q_5, shown in Fig. 13 (b). A d-mode differential pair can be used for comparing lower voltages, while an e-mode differential pair is used for higher voltages [22]. The loads can be realized as active d-mode

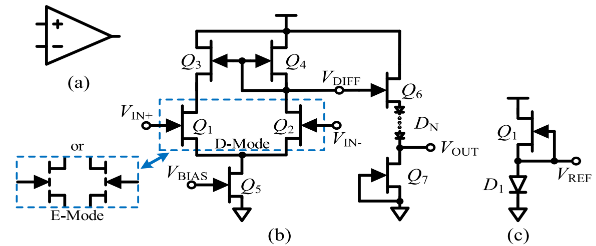

FIGURE 13. (a) Symbol and (b) schematic of two-stage amplifier consisting of a differential amplifier and source follower and (c) schematic of a voltage reference.

loads without feedback (so called current-source load) or as in this case with feedback (so called current mirror load). The advantage of implementing as an active load is the reduced chip area and the lower influence on process variations. At the same time, the voltage gain can be increased by the current mirror load [22]. A transistor (in this case a d-mode transistor) can realize the current source. The differential output voltages are limited at the maximum by the supply voltage V_{DD} and at the minimum by $V_{DD} - R_1 \cdot I_{BIAS} = V_{DD} - R_{ON,Q3} \cdot I_{D,Q5}$. For use as a comparator, the output voltage range must be shifted down to drive subsequent function or logic circuits. This is realized by an additional stage, e.g. a source follower. Fig. 13 (b) shows a source follower with d-mode transistor Q_3 and N SBDs connected in series to the source to increase the threshold voltage of transistor Q_6 [20], [23]. The load is implemented as an active d-mode load. All transistors and diodes in the design belong to the 12 V-class and have following gate widths: $W_{Q1/Q2/Q6/DN} = 50\ \mu$m, $W_{Q3/Q4/Q7} = 5\ \mu$m, $W_{Q5} = 10\ \mu$m. In the comparator with d-mode differential pair, 4 diodes ($N = 4$) are used and with e-mode differential pair 3. Fig. 14 (a) shows the transfer characteristic of the two-stage comparator for e-mode and d-mode differential pair at $V_{DD} = 12$ V and three different non-inverted input voltage V_{IN+} (3/4/5 V for e-mode and -1/0/1 V for d-mode differential pair). The bias voltage of both variants is 0 V and the step size of the inverted input voltage V_{IN-} is 0.1 V. The transition voltage is not symmetrical for the three non-inverted input voltages due to the same bias voltage in all operating points. However, the different input voltage ranges and the low-level output voltage of 0 V can be seen. Fig. 14 (b) shows the determined voltage gain from the transfer characteristic. The peak gain value is -6.2 for e-mode and -10.1 for d-mode differential pair. The difference in the peak gain is due to the higher transconductance of d-mode transistors. The gain is low due to the large step size of V_{IN-}.

There are already comparators based on a single differential amplifier (diff. amp.) stage with current-source (CS) load [18], [19] and current-mirror (CM) load [17], [20], [22], [23], [53]. An additional stage is needed to adapt the output levels of the differential amplifiers [17], [20], [23], [53], for example with source follower (SF). In [34] a comparator is realized with three stages consisting of a differential amplifier with cross-coupled latch and two logic inverters.

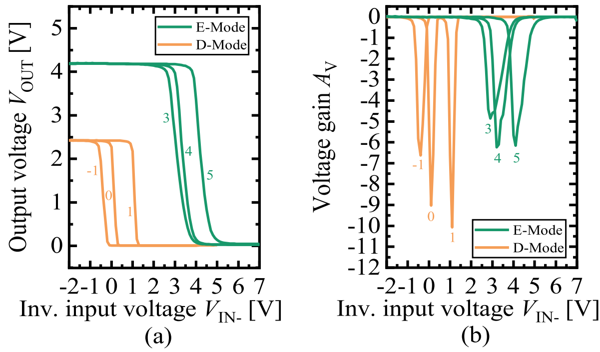

FIGURE 14. (a) Transfer characteristic of the amplifier and (b) determined voltage gain for e-mode and d-mode differential pair at V_{DD} = 12 V and three different non-inverted input voltage V_{IN+}.

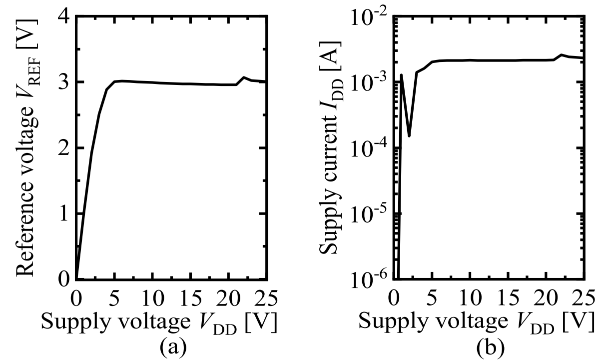

FIGURE 15. (a) Reference voltage and (b) supply current as function of the supply voltage of a diode-based voltage reference.

TABLE 8. Comparison of amplifiers with E-mode differential pair.

		This work	[23]	[22]	[21]	[34]
Technology		p-GaN		F-GaN[1]	F-GaN[1]	p-GaN
Topology		Diff. Amp. w/ SF		Diff. Amp.	Diff. Amp	Diff. Amp w/ latch + 2× inv.
Load		CM		CM	CM	CS
Stages		2		1	1	3
$V_{TH,E}/V_{TH,D}$	V	1/-1.3	0.5/-0.5	0.5/-2.0	0.8/-1.6	-[4]
V_{DD}	V	12	12	10	10	-
V_{OL}/V_{OH}	V	0/2.5	0/7.3	>1/10	>1/10	-/-
A_V		6.2[2]	20	78.5[3]	56.2	-
	dB	20[2]	26	37.9[3]	35.0	-
I_{STAT}	mA	15.3	15.0	-	-	-
A	µm²	15300	28000	-	426600	-

[1] By applying a fluorine plasma implantation technique
[2] From DC-characteristics
[3] With adjusted bias voltage
[4] Only e-mode devices in this technology

The amplifier from [23] is realized in the same technology but with different process parameters. Table 8 lists different amplifiers with e-mode differential pair at room temperature. The amplifier or comparator without second stage have a high low-level output voltage, but a high voltage gain. However, this work and [23] need a small chip area to realize a comparator, which can also be cascaded. A higher load resistance can reduce the high static current I_{STAT}. The active load can be further increased by a longer and narrower channel. The highest gain solution seems to be a three stage approach with cross-coupled latch [34], but no information on voltage gain etc. could be found.

For the realization of a bias voltage, needed in analog integrated circuits, there are two possibilities: Using a reference voltage or via a current mirror based on a diode. A current mirror for biasing has advantages in superior insensitivity to circuit properties and variation of power supply and temperature. At the same time, less chip area is required compared to passive voltage dividers. Fig. 13 (c) shows a voltage reference with a SBD and an active d-mode load. This circuit can also be used to realize a current mirror consisting of an e-mode transistor with a short-circuited gate-drain connection instead of a SBD. This circuit was realized in the GaN power IC technology. Both devices belong to the 12 V-class. The gate-widths are $W_{Q1} = 5\ \mu m$ and $W_{D1} = 50\ \mu m$. The measurement of the voltage reference is shown in Fig. 15. From about 4.5 V supply voltage, the reference voltage remains stable. The line sensitivity is 0.35%/V for a range of V_{DD} from 5-25 V. The max. supply current is 2.42 mA.

Temperature compensated references have also been realized in GaN power IC technologies, although these are not linear with supply voltage changes. These circuits have a high temperature stability of 70 ppm/°C [54] and 150 ppm/°C [52] and generate proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) coefficients. In [24] a reference voltage is published with current loop and PTAT coefficient of e-mode GaN transistors. This reference achieves a line sensitivity of 0.32%/V for a range of V_{DD} from 3.9-25 V and a temperature compensation of 23.6 ppm/°C.

V. GAN POWER INTEGRATION

A. LEVELS OF INTEGRATION

Integration levels are first be defined to discuss the possibilities of function integration in GaN-based power electronics. There are different classifications of the integration levels into the GaN power IC platforms [3], [4]. This work modifies the classification from [3] and divides into 6 levels, as shown in Fig. 16. The components of GaN-based power converters are power device(s), driver(s), sensing, protection, control, and energy storage. These levels begin with a few active devices to realize a power stage, over a dozen devices to ensure the integration of the driver up to hundreds of active and passive devices for implementing a control system.

1) LEVEL 0: POWER STAGE

The integration of multiple power devices to form a power stage in one chip can dramatically reduce the power-loop size, eliminate interconnect parasitics and reduce packaging as well as assembly complexity. Examples include integrated monolithic half-bridges [55]–[57], H-bridge [58], multilevel inverter [59], 3-phase inverters [60], [61], buck/boost converters [62], [63], and diode multiplier [64]. There are also commercially available monolithic integrated low-voltage

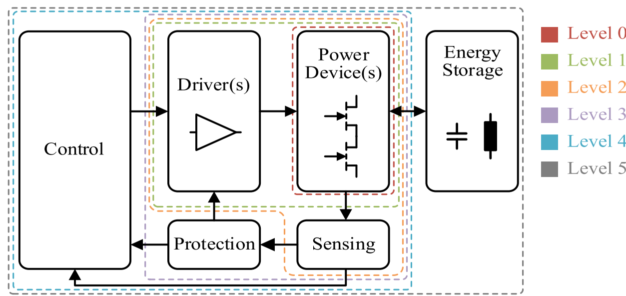

FIGURE 16. Levels of integration in power electronic converters with the components power device(s), driver(s), sensing, protection, control, and energy storage.

half-bridges up to an operating voltage of 80 V [65] with additionally synchronous bootstrap [66] from EPC. However, the power stages are influenced by the substrate-biasing effects, due to the shared conductive Si-substrate [56], [57], [67].

2) LEVEL 1: POWER STAGE WITH INTEGRATED DRIVER(S)

GaN power devices with integrated gate drivers can lead to an increase in switching frequency by reducing the gate loop inductance. Furthermore, critical ringing and overshoot can be reduced [2], [3]. A half-bridge with push-pull and DCFL inverter is published in [6]. Many other publications followed based on this driver concept [3], [6], [28], [30], [69]–[74]. Gate drivers based on boot-strapping techniques have also already been realized [34], [75], [76]. Commercial ICs with power HEMT and gate driver with voltage regulator as well as *dV/dt*-control called AllGaN^{TM} are fabricated by Navitas Semiconductor [77]. Also EPC manufactures single GaN HEMTs with gate driver, commercial half-bridges with driver, level shifter, under-voltage lockout (UVLO) and logic called ePower^{TM} Stage, and single GaN HEMTs with high-frequency laser driver called eToF^{TM} [66].

3) LEVEL 2: SENSING

The integration of sensing with driver and power devices allows fast protection circuits. Temperature sensors [78] and current sensors based on shunts [79] or sense-FETs [80]–[83] can be integrated. A readout circuit for current sensors has also been published [23].

4) LEVEL 3: PROTECTION

Protection circuits such as over-current protection (OCP) [31], [32], over-temperature protection (OTP) [52], [84], and UVLO [85] in combination with the power device(s) and partly the gate driver and sensing increases the functionality of the IC.

5) LEVEL 4: CONTROL

A closed-loop control in GaN with sensing and control is very complex and still faces some challenges. First works show the realization with power device(s), driver, sensing, control [33] in combination with protection [6] as well as power supply [34] and demonstrate the potential of an all-in-GaN solution.

6) LEVEL 5: ENERGY STORAGE

The energy storage elements are still missing for a complete power converter system. The limitations have already been examined in section III-B. The on-chip capacitors are limited by the available chip area, which is why integration is usually only useful for charge pumps and smoothing capacitors with small capacitance values. On-chip spiral inductors are mostly used in high frequency applications due to the low inductance. To use on-chip inductors in this technology for power applications, the switching frequency must be increased to the very high frequency range (VHF) of 30-300 MHz [48]. This in turn can lead to an extreme reduction of volume.

With these levels of integration, GaN power ICs can be categorized for better comparability. In addition, other levels can be added like interface and auxiliary power supply. In digital technologies, only the number of transistors defines the integration levels: Small-scale integration (SCI) 1-10, medium-scale integration (MSI) 10-100, large-scale integration (LSI) 100-10^4, and very large-scale integration (VLSI) $>10^4$. However, this definition is not practical for power ICs, but shows the complexity of the circuit to a certain degree.

Fig. 17 (a) shows an investigation of the integration levels based on the approx. integrated devices as function of the year. The data points are divided into research and industry. It can be estimated that the levels of integration as well as the number of integrated devices have increased over the years. The state-of-the-art is in the MSI level between 10-100 integrated devices. A first work [34] can already be classified in the next level LSI. The state-of-the-art will exceed the MSI level in the next 3-5 years for GaN power integration if a forecast is attempted. This is achieved by continuous improvements of the PDKs of the GaN power IC platforms. However, the integration density is limited to the losses of the building blocks. Fig. 17 (b) and (c) shows the levels of integration based on research using the voltage as function of the current with the power (dashed line) and the frequency. Increasingly higher operating voltages and simultaneously higher currents are achieved in DC-DC conversions, leading to outputs of up to serval kilowatts. At the same time, higher switching frequencies area also achieved. This is supported on the one hand by new gate driver concepts and increased protection function in combination with sensing. The integration level 4 control can leads to an increase in switching frequency, but usually results in a smaller volume or chip area of the power electronics system.

An initial overview of GaN power integration is given in [86] with the integration for DC-DC conversion divided in integrated components and integrated DC-DC converters. In addition to the discussed GaN power integration, the co-integration with optical devices such as LEDs or lasers might be feasible [87], but is not considered in this paper because technological changes are required that could

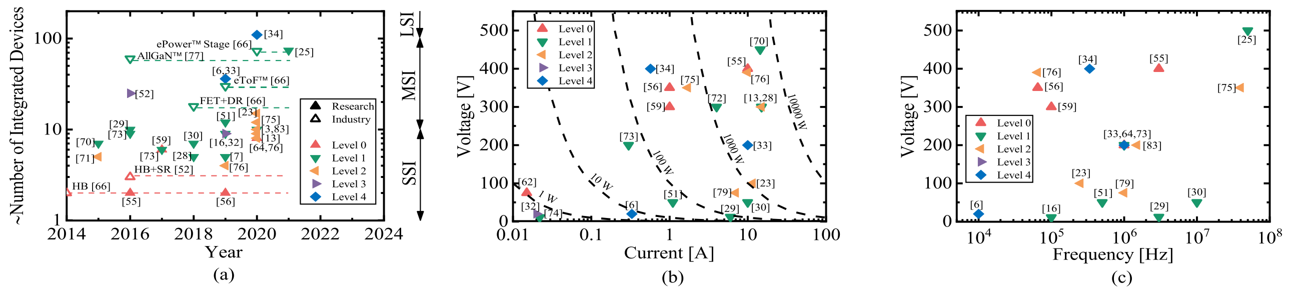

FIGURE 17. Investigation of integration level: (a) Approx. number of integrated devices as a function of the year divided into research and industry, (b) voltage as a function of the current, and (c) voltage as a function of the frequency based on research work.

degrade the power HEMT device performance. However, in this work, a further subdivision into the integration levels with the state-of-the-art is shown. In the future, GaN power integration with the lateral structure will be possible at higher and higher integration levels supported by the continuous development of the PDKs. On EPC's technology timeline, all new GaN devices are expected to have some level of integration starting in 2022 [66].

B. COMPARISON OF IC TECHNOLOGIES

Most power ICs for power management are based on BCD technologies. Thereby, a BCD technologies offer low-voltage logic CMOS transistors, high-voltage DMOS transistors, bipolar transistors, capacitors, diodes, and power lateral double-diffused MOS (LDMOS) in the same process. The typical feature size of BDC is 0.35 μm and 0.18 μm, which is relatively large compared to CMOS [88]. In this section, the GaN power IC technology (p-GaN gate 0.5 μm) will be compared with two similar technologies. On one hand with a GaN-on-SOI technology with a structure size of 1.3 μm (gate length) [14], [89] and on the other hand with a high-voltage BCD technology with a structure size of 0.35 μm [90]. Table 9 shows the comparison between the two GaN technologies and a comparable BCD technology. The BCD technology has a significantly larger number of active and passive components as well as a greater library of digital, I/O and analog function blocks. However, with increased maturity of GaN technologies, a higher number of devices will be possible. Table 9 also lists several active and passive devices for comparison. The difficulty is to find similar components. The advantage resulting from the physical properties is the >10 smaller area-specific on-resistance of the GaN HEMTs compared to an NDMOS transistors with similar voltage classes. However, the leakage currents of the HEMTs are somewhat higher than those of the NDMOS transistors. In this work, HEMTs are available in different voltage classes. In the GaN-on-SOI technology, there is at least a 200 V HEMT and a logic HEMT. There is also a GaN-on-SOI platform for 650 V HEMTs. The BCD technology has MOS transistors in the 5/20/40/400/700 V class. The Schottky diodes have similar parameters in all three technologies. The BCD technology has additional p-channel and bipolar transistors, which the GaN technologies does not have. The GaN technologies has only the 2DEG epitaxial resistor used as a high-ohmic resistor. The BCD, on the other hand, has several poly and diffusion resistors. All technologies can provide several metal resistors. The GaN-on-Si technology as well as the BCD technology, offers several MIM capacitors. In addition, the GaN-on-Si technology has a p-GaN gate capacitor, which is comparable to a MOS capacitor. A MOS capacitor provides almost 100 times higher capacitance density than a stacked MIM capacitor. Lastly, a price comparison in that the technologies are in the same order of magnitude. The prices are from Europractise IC service [91]. However, the price of GaN technology will probably decrease and/or the number of devices will increase at the same time [35].

C. FURTHER CHALLENGES AND FUTURE PROSPECTS

In addition to the integration opportunities presented here, there are still some challenges that have to be overcome and a wide horizon to further increase the potential of lateral GaN integration.

1) VERTICAL ISOLATION

One challenge is the vertical isolation, which is influenced by the dependence of the conductive substrate potential and leads to back gating effects. A possibility is to further increase the GaN buffer thickness or to replace the step-graded AlGaN/GaN buffer to a superlattice buffer [57]. Additionally, substrate biasing networks can be used to avoid these effects [55], [56]. Another approach is to use an SOI [14] or a Qromis substrate technology (QST®) [92] with a deep trench isolation and a local substrate contact. These approaches also avoid the back gating effects. A disadvantage compared to GaN-on-Si with improved buffer is the higher epitaxy cost. In addition, a possibility to avoid back gating effects could be Si-removal techniques. On wafer level, this is achieved by wafer transfer techniques to a second carrier substrate or selective Si-removal with mechanical stabilization by the remaining frame. At package level, a PCB carrier substrate with embedded GaN-on-Si IC can be used to remove the Si substrate [93].

2) GaN CMOS

The lack of complementary transistor types can be compensated to some extent by circuit approaches such as bootstrapping. Nevertheless, a p-type transistor is desirable. Fortunately, the GaN power IC technology provides a p-GaN

TABLE 9. Comparison of IC technologies.

			GaN-on-Si (This work)		GaN-on-SOI [14, 89]		BCD [90]	
Structure size		µm	0.5		1.3		0.35	
Device number	Transistors		≥9		≥2		30	
	Diodes		≥9		≥1		12	
	Resistors		5		≥2		14	
	Capacitors		5		≥1		6	
	Miscellaneous		Digital library, analog library, inductors		Logic gates, protection functions (UVLO, OTP, OCP)		Logic & I/O library, analog library	
HV/LV e-mode transistor	Type		HEMT		HEMT		NDMOS	
	Class		300	12	200		400	40
	On-resistance R_{ON}	Ω×mm	8.7	6.3	7.5		100	17.5
	Area specific on-resistance $R_{ON}\times A$	Ω×mm²	0.16	0.1	-		5	1.20
	Threshold-voltage V_{TH}	V	1.0		3.0		0.8	
	Leakage current I_{DSS}	µA/mm	<10		<1		0.108	0.21
Schottky diode	Forward voltage V_F	V	~1.5		~1.0		~0.21	
	Breakdown voltage V_{BD}	V	>20		-		>22	
High/low ohmic resistor	Type		2DEG	Metal	2DEG	Metal	Poly	Metal
	Sheet resistance $R_{\square}$	Ω/□	~800	~0.001-2	600	1.7	43-11000	0.03-1140
MIM capacitors	Capacitance density C/A	fF/µm²	0.22-1.16		0.3		1.25	
	Breakdown voltage V_{BD}	V	≥50		40		≥20	
Costs [1]		€/mm²	-		27.45		20.7 [2]	

[1] From Europractise IC service
[2] Price for similar technology

layer that can be used for a p-channel transistor. Already first works realize a p-channel FET and the combination of both transistor types in a GaN CMOS inverter was shown in [94], [95]. The current consumption can be massively reduced compared to DCFL inverter and enable a complementary transistor that allow higher energy-efficiency. The p-channel FET can be fabricated by a small number of process steps, but has a significantly lower hole mobility of $\sim 10^2$ compared to electron mobility in unipolar n-type GaN devices. However, more efficient gate drivers and additional peripherals are feasible through this extension.

3) COMBINATION OF LATERAL AND VERTICAL TECHNOLOGIES

GaN technology has been significantly improved over the last 20 years and is already delivering commercial transistors with operating voltages up to 1200 V. However, this lateral device structure sees an upper limit in voltage scaling and power handing typically limited by a few kW. Vertical GaN devices can extend this application range above 650 V and currents greater than 100 A. Vertical structures offer higher breakdown voltage capability and higher current levels without enlarging the chip area [96]. A combination of lateral and vertical structure with key focus of integration and at the same time higher performance combines the advantages of both technologies. A suitable structure for the combination offers the current aperture vertical electron transistor (CAVET) [97], shown in Fig. 18. The CAVET has a highly conductive 2DEG channel with the AlGaN/GaN heterostructure similar to the HEMT. However, the source region is separated from the drain region by a p-GaN current blocking layer (CBL), which includes a narrow current aperture region below the gate-contact [98]. Furthermore, the CAVET can be extended by the known e-mode techniques for the HEMT, e.g. with a p-GaN gate as shown in Fig. 18. Quasi-vertical CAVET structures on Sapphire [99] and Si [100] can be upgraded to a fully vertical structure [101]. The CBL serves as a potential barrier to suppress the drain-source leakage current and can be used as a protective well for the lateral HEMTs by connecting the CBL to the source with e.g. a VIA. This well allows to avoid static and dynamic influences of the drain potential to the lateral HEMTs [97]. Other approaches are also conceivable, such as a GaN/SiC hybrid FET based on a GaN-on-SiC epitaxial growth to combine the advantages of both material systems [102].

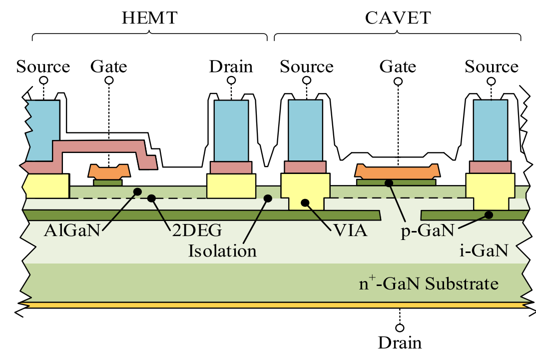

FIGURE 18. Simplified cross-section of novel GaN power IC technology consisting of a CAVET and HEMT structure as vertical and lateral devices.

VI. CONCLUSION

The GaN power IC platform combines wide-bandgap performance with advanced periphery and functionality. Device, digital and analog libraries are continuously enhanced and expanded to handle the pursuit for higher levels of integration. Therefore, a comprehensive overview of integrable key building blocks in common technology are experimentally investigated and optimized for area-efficiency as well

as compared with other GaN/- and/or Si-based technologies. Power devices with matrix instead of comb layout show a reduction of the area-specific on-resistance $R_{ON} \times A$ of 37.5%. In addition, passive components were investigated, such as on-chip capacitors with high capacitance density >1 fF/μm^2 realized by stacked MIM or p-GaN gate capacitors and spiral inductors with inductance densities >50 nH/mm^2. Digital gates were optimized for small chip area and low power consumption. NOT gates were realized in active areas as low as 56.7 μm^2 and with low max. static currents of 0.12 mA. NAND gates were realized with dual gate HEMTs for a smaller chip area. The analog building blocks included the investigation of differential amplifiers or comparators for e/d-mode differential pair and voltage references. The amplifiers from this work can be realized on an area of 15300 μm^2 with a gain of up to 20 dB. Furthermore, GaN power integration is classified into six integration levels based on a literature review. This work's GaN technology is compared with other GaN- and Si-based IC technologies. Finally, challenges and future perspectives such as vertical isolation, GaN CMOS and the combination of lateral and vertical technologies are identified and discussed to further increase the potential of the GaN Power IC platform.

ACKNOWLEDGMENT

The authors would like to thank the colleagues from the Fraunhofer IAF Epitaxy and Technology Department for their contributions during wafer growth, IC processing, and characterization.

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