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Novel Multiple-Layer Stack Capacitor and Its Application in the IRPFA Readout Circuit

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ABSTRACT In this paper, a kind of four-layer stack capacitor is proposed, which has realized the compatibility with the conventional standard 0.5μm CMOS technology. The effective capacitance per area of the proposed stack capacitor is about three times larger than that of the mono-layer MOS capacitor. The Simulation Program with Integrated Circuit Emphasis (SPICE) model of the presented four-layer stack capacitor has been also established with considering the fringe effect. The results show that the root mean square error of the proposed SPICE model is less than 2%. The model has been applied in the simulation design of the infrared focal plane array readout circuit (IRFPA ROIC) successfully. Based on the improved 0.5μm CMOS process with four-layer stack capacitor, an IRFPA ROIC with 640 $\times$ 512 array has been implemented and the dynamic range is improved from 73db to 78dB.

INDEX TERMS Four-layer stack capacitor, infrared focal plane array, readout circuit, dynamic range.

I. INTRODUCTION

Infrared focal plane arrays have a wide range of industrial, medical, and scientific applications. The infrared focal plane array readout circuit (IRFPA ROIC) [1]–[3], as the critical part of the dynamic range, can deal with the weak electrical signal sensed by the detector. Generally, the infrared detector can generate numerous carriers once it receives the photons, the generated carriers will be saved into the integrating capacitor and then transformed into the output voltage signal by the ROIC. Dynamic range is an important parameter in image sensors, and the large dynamic range requirement is the most challenging aspect in modern CMOS process [4]. Generally, methods of extending dynamic range can be divided into three categories. One uses logarithmic pixels response to extend dynamic range as in [5], one group accepts multiple exposure-times to expand the dynamic range as in [6], and the other one applies lateral overflow capacitors to improve operation range [4], [7], [8]. From aspect of device design, enhancing the capacitance of integrating capacitor is the most direct way. In addition, the ROIC's uses a capacitor along with active elements for signal integration and processing, the amount of charge collected is defined by the charge handling capacity and limited by the size of integrating capacitor. Capacitance with smaller size can reduce the overall chip area and promote the development of product miniaturization. Meanwhile, larger capacitance values can store more charge and electrical information in IRFPA ROIC, which provides more pixel information on image processing. In CMOS technology, improving the capacitance value per unit area by means of optimizing device structure design is a research of great engineering value. Therefore, enhancing the capacitance of integrating capacitor at the limited pixel cell area is the most effective way to improve the performance of the dynamic range.

In this paper, a kind of stack capacitor is proposed, which has realized the compatibility with the conventional standard 0.5um CMOS technology process. Compared with mono-layer MOS capacitor [9], [10], it can largely enhance the capacity of integrating capacitor at the limited pixel cell area. Obviously, this four-layer stack capacitor is more competitive to balance the relationship between the capacitance of integrating capacitor and the occupying space.

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Moreover, it is noted that the Simulation Program with Integrated Circuit Emphasis (SPICE) model is the link between the physical world and the design world of the semiconductor industry. But until now, no any SPICE model is established to describe the electrical characteristics of the stack capacitor. In this paper, the SPICE model of the four-layer stack capacitor has been established, the considerable accuracy and general applicability of the proposed SPICE model have guaranteed the successful simulation design of the IRFPA ROIC. Finally, based on the improved 0.5μm CMOS process, a kind of IRFPA ROIC with 640×512 array has been implemented, and the test results show that the enhanced capacity of the integrating capacitor has improved the performance of the dynamic range effectively.

II. THE STRUCTURE AND SPICE MODEL OF CAPACITOR

A. THE STRUCTURE OF CAPACITOR

The conventional 0.5μm CMOS technology platform [11] owns a full suite of devices, including industry compatible 5V CMOS, free bipolar, precision resistors and capacitors. Based on the 0.5μm CMOS technology platform, we have implemented a kind of four-layer stack capacitor by only adding two MCT layers, as shown in Fig.1. The schematic cross section of the presented four-layer stack capacitor has been shown in Fig.2. It is noted that MOS capacitor is formed by an NMOS device, Poly-Insulator-Poly (PIP) capacitor is fabricated between two poly layers, MIM (Metal-Insulator-Metal) cap.1 is between Aluminum layer 2 (A2) and Aluminum layer 3 (A3), MIM cap.2 is between Aluminum layer 3 and Aluminum layer 4 (A4). All of them are connected in parallel.

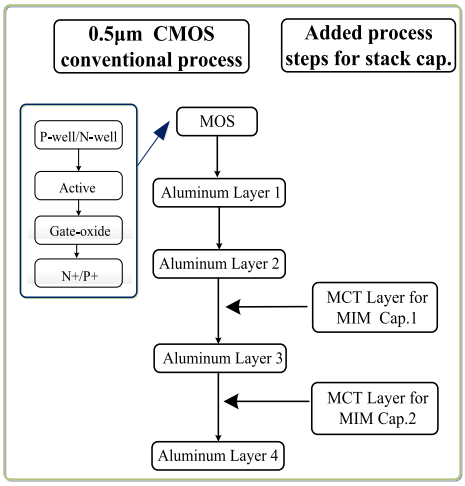

FIGURE 1. Stack capacitor process flow based on 0.5μm CMOS.

As shown in Fig.3, when the MOS capacitor part of four-layer stack capacitor is under accumulation region, the total capacitance of stack capacitor is 7.6pF, which is larger than that under-inversion region (5.5pF). This is because, the MOS capacitor under accumulation region mainly contains the gate oxide layer capacitor, while the MOS capacitor under inversion region is formed by the gate oxide layer capacitor

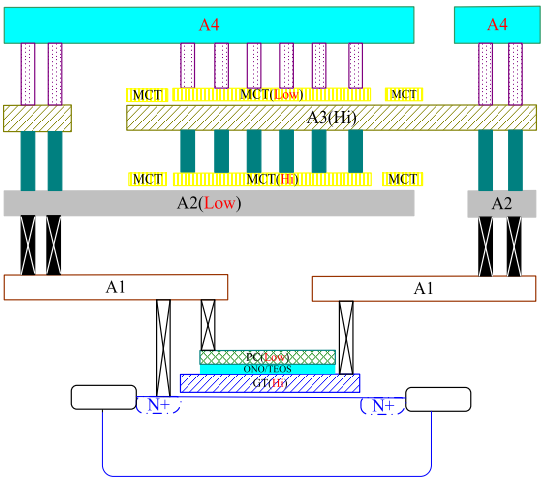

FIGURE 2. The cross section of four-layer stack capacitor.

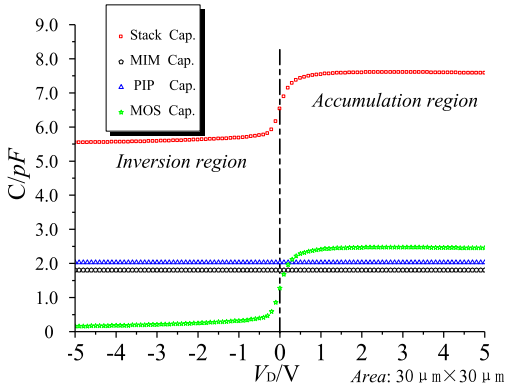

FIGURE 3. The measuring curves of four-layer stack capacitor and other mono-layer capacitors.

and semiconductor layer capacitor in series. Therefore, in the practical application, the stack capacitor is normally set on the state that its own MOS capacitor works in accumulation region, so as to acquire more larger capacitance value.

In addition, other measurement results can be also shown in Fig.3. In the same area (30μm$\times30\mu$m), the four-layer stack capacitor is 7.6pF, while only 2.5pF for mono-layer MOS capacitor, 2.1pF for mono-layer PIP capacitor and 1.8pF for mono-layer MIM capacitor. The effective capacity of the stack capacitor is more than 3 times larger than that of any other mono-layer capacitor. This can prove that the stack capacitor owns larger capacitance in less occupying space, which verifies great advantage in the charge storage capability and the occupying space comparing with the mono-layer MOS capacitor, MIM capacitor and PIP capacitor.

B. THE SPICE MODEL OF MOS CAPACITOR

The idea of the four-layer stack capacitor SPICE model has been shown in Fig.4. The SPICE models for the MOS capacitor, PIP capacitor and MIM capacitors will be established respectively.

In this paper, the charge-thickness model (CTM) [12], [13], as a classical charge-based model, has been established to

describe the characteristics of MOS capacitor, as shown in Fig.5.

The MOS capacitor has been regarded as C_{ox} and C_{cen} in series, which can be expressed by

$$C_{MOS}=\frac{C_{ox}C_{cen}}{C_{ox}+C_{cen}} \tag{1}$$

where C_{ox} is unit-area capacitance of gate-oxide capacitor, C_{cen} is unit-area capacitance of charge-thickness capacitor. Respectively, C_{ox} and C_{cen} can be expressed by

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{2}$$

$$C_{cen} = \frac{\varepsilon_{si}}{X_{DC}} \tag{3}$$

where ε_{ox} is permittivity of gate oxide and ε_{Si} is permittivity of silicon, T_{ox} is the gate-oxide thickness and X_{DC} is the DC charge thickness.

It is observed that C_{ox} and ε_{Si} are both constant, and we just analyze the only variable of them, X_{DC}. Based on numerical self-consistent solution of Schrodinger, Poisson and Fermi-Dirac equations, the universal and analytical X_{DC} model has been discussed.

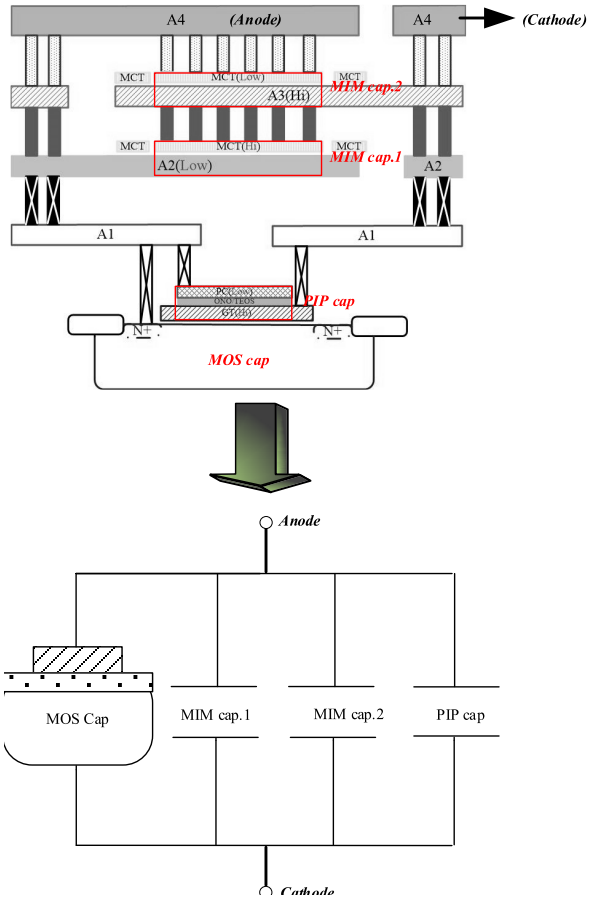

FIGURE 4. The modeling idea of stack capacitor.

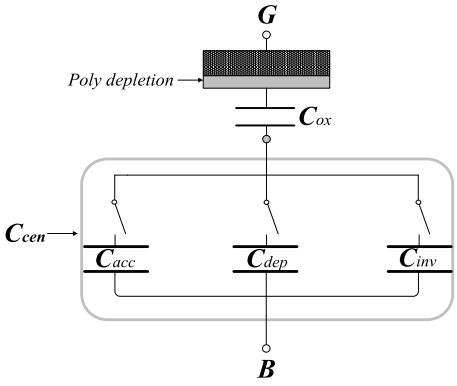

FIGURE 5. The schematic of charge-thickness model.

The DC charge thickness in the accumulation and depletion regions can be expressed by

$$X_{DC}=\frac{1}{3}L_{debye}exp[acde(\frac{N_{sub}}{2\times10^{16}})^{-0.25}\frac{V_{gb}-V_{fb}}{T_{ox}}] \tag{4}$$

where X_{DC} is in the unit of cm, (V_{gb}- V_{fb}) / T_{ox} has a unit of MV/cm, *acde* is exponential coefficient for the charge thickness in accumulation and depletion regions, N_{sub} is the channel doping concentration, and V_{fb} is the flat-band voltage. Respectively, the Debye length L_{debye} and the flat-band voltage V_{fb} can be expressed by

$$L_{debye} = \sqrt{\frac{\varepsilon_{si}v\tau_0}{qN_{sub}}} \tag{5}$$

$$V_{fb} = V_{th}-\varphi_s-K_{1ox}\sqrt{\varphi_s-V_{bseff}} \tag{6}$$

where $V_{\tau0}$ is the thermal voltage at test temperature, K_{1ox} is the first-order parameter for the body effect coefficient, φ_s is surface potential, V_{bseff} is the effective body bias. But for numerical stability, Equation (4) is replaced by Equation (7)

$$X_{DCeff}=X_{max}-\frac{1}{2}(X_0+\sqrt{X_0^2+4\delta_x X_{max}}) \tag{7}$$

where

$$X_0=X_{max}-X_{DC}-\delta_x \tag{8}$$

and

$$X_{max}=\frac{1}{3}L_{debye},\delta_x=10^{-3}T_{ox} \tag{9}$$

The inversion charge layer thickness can be formulated as

$$X_{DC}=\frac{1.9\times10^{-7}}{1+[\frac{V_{gsteff}+4(V_{th}-V_{fb}-2\varphi_B)}{2T_{ox}}]^{0.7}} \tag{10}$$

where V_{gsteff} is effective gate voltage, V_{th} is the threshold voltage, and φ_B is the effective interface contact potential.

C. THE SPICE MODELS OF MIM CAPACITOR AND PIP CAPACITOR

Both MIM capacitor and PIP capacitor are parallel-plate capacitors. Thus, we can establish one kind of model for both.

The surface field lines those are in the interior of parallel-plate capacitor are uniformly distributed, which are shown as

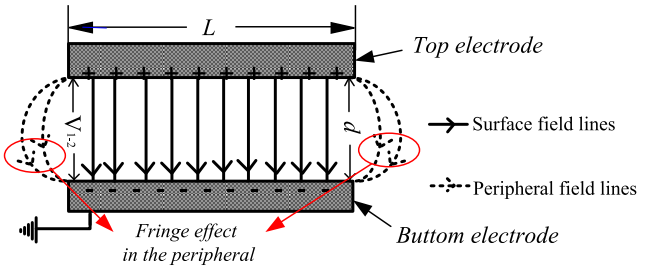

FIGURE 6. The schematic of parallel-plate capacitor.

the solid lines in Fig.6. Thus, we can express the unit-area capacitance for this part by

$$C_{un}=\frac{\varepsilon_r}{4\pi kd} \tag{11}$$

where ε_r is the dielectric constant of the parallel-plate capacitor, k is the electrostatic constant and d is the distance between the two electrodes.

However, when the distance d is small, the shapes of electric field lines in peripheral parts vary from parallel to outward arc [14], [15], as shown in Fig.6. Therefore, the fringe effect will not be negligible and the traditional result (Eq. (11)) is not applicable for the peripheral capacitor. Equation (12) is the expression for the peripheral capacitor and Equation (13) is the expression for v_{fac} in Equation (12).

$$C_{edgeff} = C_{edg} * P_{ER} * v_{fac} \tag{12}$$

$$v_{fac} = 1+p_{vc1} * V_{1-2}+p_{vc2} * V_{1-2}^2 \tag{13}$$

where C_{edg} is the unit-length capacitance of the peripheral capacitor, P_{ER} is the perimeter of the parallel-plate capacitor, V_{fac} is the voltage impact factor for fringe effect, p_{vc1} is the first-order voltage fitting parameter, p_{vc2} is the second-order voltage fitting parameter and V_{1-2} is the effective voltage between the two electrodes.

The temperature parameter of the parallel-plate capacitor can be expressed by

$$d_{temp} = temp - 25 \tag{14}$$

$$t_{fac} = 1+p_{tc1} * d_{temp}+p_{tc2} * d_{temp}^2 \tag{15}$$

where t_{emp} is test temperature and in the unit of °C, d_{temp} is the temperature difference between test temperature and room temperature and in the unit of °C, p_{tc1} is the first-order temperature parameter, p_{tc2} is the second-order temperature parameter, t_{fac} is the temperature impact factor for the parallel-plate capacitor.

In conclusion, the formula model of the parallel-plate capacitor including fringe effect and temperature impact factor can be expressed by:

$$C_0 = C_{un} * \boldsymbol{Area} * t_{fac} \tag{16}$$

$$C_1 = C_{edgeff} * t_{fac} \tag{17}$$

$$C_{MET} = C_0+C_1 \tag{18}$$

where C_0 is the capacitance for the interior part of the capacitor, Area is the area of the parallel-plate capacitor, C_1 is the capacitance for the peripheral part of capacitor and C_{MET} is the total capacitance of the parallel-plate capacitor.

TABLE 1. The structure parameters of the four-layer stack capacitors (unit: μm).

		Stack Cap. A	Stack Cap. B	Stack Cap. C
MOS Cap.	Width	30	12	30
	Length	30	12	30
MIM Cap.1	Width	30	30	30
	Length	30	30	30
MIM Cap.2	Width	30	30	30
	Length	30	30	30
PIP Cap.	Width	30	12	30
	Length	30	12	30
Number of parallel stack capacitors		1	1	10

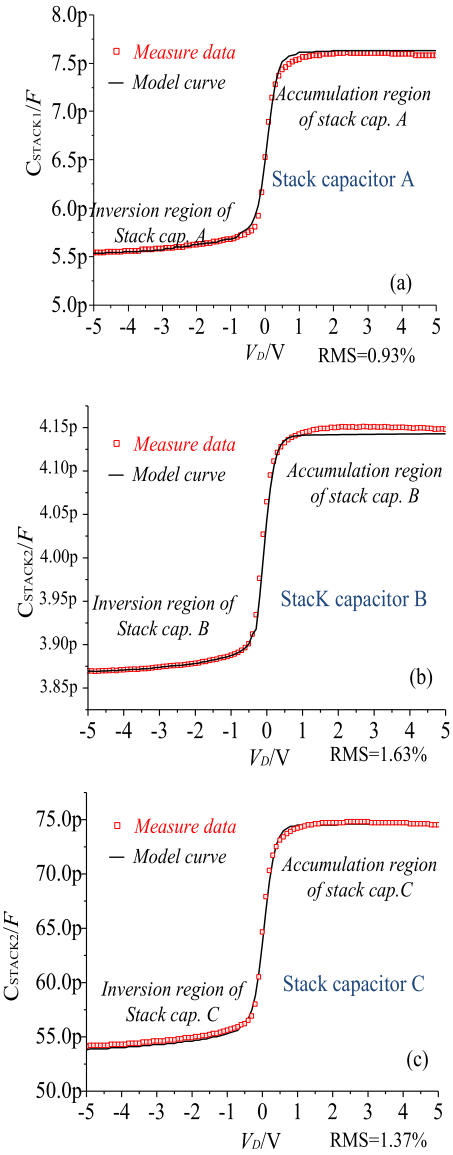

FIGURE 7. (a)-(c). The curves of the measured data and the model fitting results for the different stack capacitors (test temperature: 25°, test frequency: 100 kHz).

D. THE VERIFICATION OF SPICE MODELS

Three completely different stack capacitors have been selected to verify the accuracy and applicability of stack capacitor SPICE model. The structure parameters of the three stack capacitors can been seen in Table 1.

In order to evaluate the accuracy of the proposed model, the root mean square (RMS) is calculated by:

$$RMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{mea_i - sim_i}{max\{|mea|_{max}, |sim_i|\}}\right)} \quad (19)$$

where the mea_i is the measured data per point, the sim_i is the model prediction data per point, and the N is the total numbers of all points. As shown in Fig.7, the RMS values of the three capacitors are 0.93%, 1.53%, and 1.37% respectively, so we can confirm the RMS based on the proposed stack capacitor model are all less than 2%, which confirm the considerable accuracy and general applicability of the stack capacitor SPICE model.

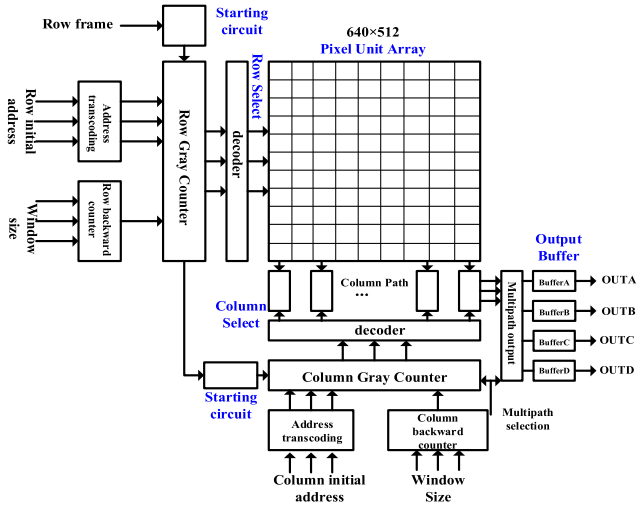

FIGURE 8. Block diagram of the readout structure.

III. APPLICATION OF MULTIPLE-LAYER STACKED CAPACITOR IN INFRARED READOUT CIRCUIT

A. THE STRUCTURE OF INFRARED READOUT CIRCUIT

In this section, a high performance, 640 × 512 pixels, readout integrated circuit (ROIC) with snapshot mode integration is proposed and described. Typically, the ROIC consists of charge integration, charge to voltage conversion, pixel voltage multiplexing, signal transfer and amplification stage [16-18]. In our work, the block diagram of the readout structure consists of the block diagram of the readout structure plotted in Fig.8 including logic circuit, row select circuit, column select circuit, pixel unit array, column path, output buffer, and all parts are marked in Fig.8.

B. THE STRUCTURE AND OF PIXEL UNIT CIRCUIT

Pixel cell design is one of the most important designs of ROIC. In this paper, proposed novel multiple-layer stack

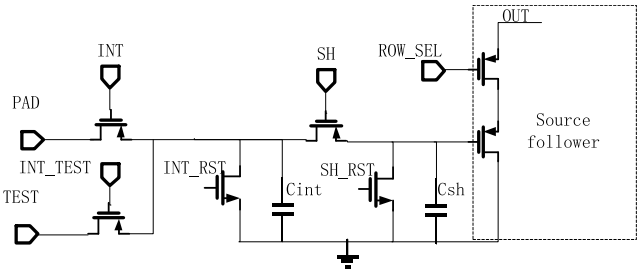

FIGURE 9. Block diagram of pixel unit circuit.

capacitors are used in pixel unit and the pixel unit uses direct injection (D_I) structure. The D_I structure has the characteristics of small occupied area, simple circuit structure and containing large integral capacitance. When the ROIC operates in the I_{WR} readout mode, whenever the frame signal arrives, the pixel unit will sample the voltage from the C_{int} to the C_{sh}, then the C_{int} will be reset and integrating next frame signal. However, when the ROIC operates in the I_{TR} readout mode, sampling tube is in constant Open state so that C_{int} and C_{sh} will be integrated together. As a result, the integral capacitor becomes larger in this mode so that greater charge handling ability can be obtained.Fig.9 shows the block diagram of pixel unit circuit.

The dynamic range can be defined as the ratio of the maximum unsaturated input signal (i_{max}) to the minimum measurable input signal (i_{min}), the minimum measurable input signal is usually defined as the noise equivalent current without illumination. It is shown in Formula (20), id represents the sum of dark current and background current. Q_{noise} is the sum of equivalent noise charges of IRFPA, and Q_{max} is the maximum charge storage capacity.

$$DR = 20log_{10}\left(\frac{i_{max}}{i_{min}}\right) = 20log_{10}\left(\frac{Q_{max} - i_d t_{int}}{Q_{noise}}\right) \quad (20)$$

Therefore, when the structure of the detector and pixel unit is relatively fixed, increasing the charge storage capacity of the integral capacitor is the most effective solution to increase the dynamic range. Increasing the charge storage capacity means increasing the integral capacitance. So in this design, we use the multiple-layer stacked capacitor as the integral

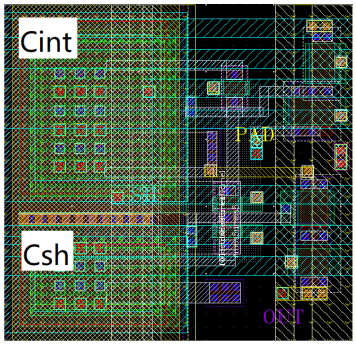

FIGURE 10. The layout of pixel cells.

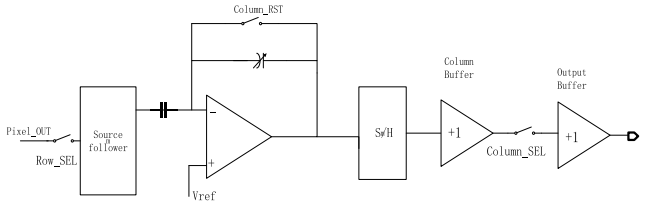

FIGURE 11. Block diagram of column path.

capacitance of the pixel unit. Fig.10 shows the layout of pixel cells.

Since there are only 6 layers of metal, the 4 and 5 layers of metal need to be used as control signal wiring, and the top layer of metal is used to connect the detector interface. Therefore, only one MIM capacitor is stacked on the integral capacitor. The integral capacitance of this design is about 0.9pf ($C_{\text{in}}+ C_{\text{sh}}$).

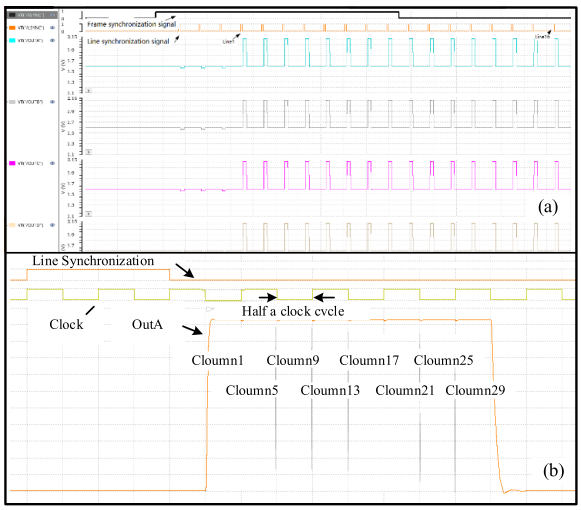

FIGURE 12. (a)-(b). The simulation results of the whole circuit.

C. THE STRUCTURE OF COLUMN PATH

Fig.11 shows the simplified architecture of the column path [19], [20]. The column path starts with source follower, composed of charge amplifier, a sample-and-hold circuit, column buffer and output buffer. Row and column address are controlled by the row select circuit and column select circuit. Whenever all the pixels of the row have been readout, the column path will be reset.

IV. SIMULATION RESULT AND TEST RESULT

A. SIMULATION RESULTS OF THE WHOLE CIRCUIT

Fig.12 shows the simulation results of the whole circuit. The simulation window is 32 × 16 arrays, 4 outputs, using integrating while read-out mode. When the line synchronization signal comes, it means that the output of the line begins. Because four output channels are used, OUTA outputs column 1, 5, 9, 13, 17, 21, 25 and 29 respectively, and the output time of each column takes up half a clock cycle.

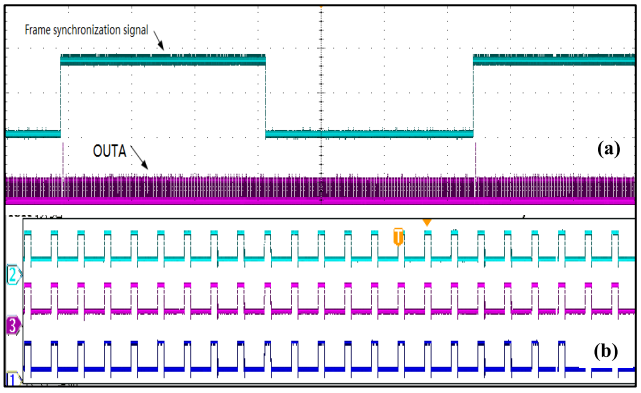

FIGURE 13. (a)-(b). The waveform of the full window and another three output.

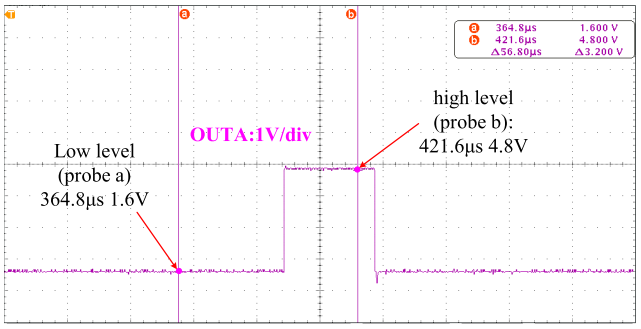

FIGURE 14. The output swing.

FIGURE 15. The sample of the chip and the imaging results of readout circuit with detector.

B. TEST RESULT

Fig.13 shows the waveform of the full window and four output at the clock frequency of 5MHz. As showed by Fig.14, the output reference voltage is 1.6V, the maximum output voltage is 4.8V. The output noise is about 400uV, thus the dynamic range is 78dB.

This ROIC is fabricated using CSMC 0.5um double poly, six metal process that utilized high-speed CMOS transistors and the whole chip area is $17.5 \times 16.5\text{mm}^2$. Fig.15 shows the sample of the chip and the imaging results of readout circuit with detector.

Table 2 shows the main performance parameter of the ROIC. Compared with the reported work [21] and the previous design using mono-layer MOS capacitor. The dynamic range is increased from 73db to 78dB by using multiple-layer stacked capacitor as integral capacitor.

TABLE 2. The main performance parameter of the ROIC.

Items	Reference [21]	Previous work (Using mono-layer MOS capacitor)	This work (Using multiple-layer stack capacitor)
Process Technology	0.35um 2P3M CIS	standard 0.5um CMOS technology process	standard 0.5um CMOS technology process
Array size	320×240	320×256	640×512
Pixel Size	5.6um×5.6um	25um×25um	25um×25um
Supply Voltage	3.3V	5.5V	5.5V
Number of Analog Outputs	10 bit digital	Programmable as 1 ,2 or 4 outputs	Programmable as 1 ,2 or 4 outputs
Output Swing	-	>3V	>3V
Dynamic Range	60dB	73dB	78dB
Input charge-handling capacity	18500e^-	11Me^-	18Me^-
Frame Rate	72Hz	60 Hz	60 Hz

V. CONCLUSION

In this paper, a kind of four-layer stack capacitor is proposed, which has realized the compatibility with the conventional standard 0.5μm CMOS technology. The Simulation Program with Integrated Circuit Emphasis (SPICE) model of the presented four-layer stack capacitor has been also established with considering the fringe effect. The results show that the root mean square error of the proposed SPICE model is less than 2%. The model has been applied in the simulation design of the infrared focal plane array readout circuit (IRFPA ROIC) successfully. Based on the improved 0.5μm CMOS process with four-layer stack capacitor, an IRFPA ROIC with 640 × 512 array has been implemented. Compared with the previous chip, the dynamic range is improved from 73dB to 78dB. At the same time, the chip and detector are packaged together, and the infrared imaging is successful.

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