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Parametric Analysis of CSDG MOSFET With La_2O_3 Gate Oxide: Based on Electrical Field Estimation

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ABSTRACT Cylindrical Surrounding Double-Gate (CSDG) MOSFETs have been designed for a suitable CMOS replacement to diminish the power and area tradeoff. With these MOSFETs below *70 nm* node for Semiconductor Industry Association (SIA) roadmap, the CMOS technology has excellent immunity to the Short Channel Effects (SCE) and better scalability. To reduce the SCE, the device was analyzed by improving the gate oxide thickness between the gate terminal and channel material and replacing the conventional Silicon dioxide layer with numerous high-ƙ dielectric materials. The gate oxide thickness is scalable so that it should have the same thickness as that of the Equivalent Oxide Thickness (EOT). This kind of novel structure shows improvement in the ON-state current and OFF-state current. The usage of the cylindrical surrounding double-gate and the high-ƙ dielectric in the oxide layer makes the MOSFET with improved stability and controllability. In this paper, the high-ƙ material is chosen in a way that it has been applied in the CSDG environment and the electrical field, electron densities have been analyzed. The semiconductor can exhibit various energy bands at the Fermi level, commonly referred to as valley. These kinds of valley semiconductors, which have several valleys are called multi-valley semiconductors. The current value in valley-1 is *2.41 mA/μm*; it also drops to *62.14 %* than valley-4, which has *6.38 mA/μm*. However, valley-2 and valley-3 have intermediate values. The energy in the sub-band for the operating region of the source has been observed to be *19.12 %* to the drain side which has the value of *0.041 eV* at the terminal end. This shows the modeled CSDG MOSFET works well with the operating electric field created by the cylindrical capacitors constituted by the two different gate materials surrounding the substrate.

INDEX TERMS Cylindrical surrounding double-gate (CSDG) MOSFET, cylindrical structure, double-gate (DG) MOSFET, high-speed devices, high-ƙ dielectric, microelectronics, nanotechnology, VLSI.

I. INTRODUCTION

Nowadays, the dimensions of the transistors are shrinking below *10 nm* and research works are carried out dominantly in the nanometer region. According to Moore's Law, this makes the transistor work downsized and further scalable to pack millions of transistors [1]. The essential limitations of the MOSFET are the Short Channel Effects (SCEs) [2]. The IRDS showcased the effect of the transistor technology in nanometer regime and low power applications with high-speed switching with increased performance [3]. It also uses various dielectrics. These dielectrics have negligible gate oxide current leakage and improved threshold voltages for both the semiconductor material and channel mobility at par with the conventional SiO_2 layer but they lack in fabrication process with the existing technologies such as Atomic Layer Deposition. High-ƙ dielectric materials tend to *1 nm* because their EOT is equivalent to this thickness. The potential high-ƙ dielectric materials are Al_2O_3 (ƙ∼10), HfO_2 (ƙ∼25), ZrO_2 (ƙ∼24.8), and La_2O_3 (ƙ∼30) which has better performance than the conventional material. Also, these high-ƙ materials provide minimum tunneling leakage and better physical thickness [4].

Sen *et al.* [5] have introduced a nano-gap in the gate oxide region which acts as a cavity for trapping the bio-particles or bimolecular applications. Also, the sensitivity of the biosensor has been taken under consideration by incorporating the dielectric modulation method. Hence, the complete performance of the device has been evaluated in their research by introducing the nano-gap filling factor and temperature variation. Villa *et al.* [6] have proposed Intermediate Band Solar Cells (IBSCs) to increase the efficiency by absorbing

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below-bandgap energy photons while preserving the output voltage. Experimental IBSCs based on Quantum Dots (QDs) have demonstrated that both below-bandgap photon absorption and output voltage preservation are possible. However, their experimental work has also revealed that the below-bandgap absorption of light is weak and insufficient to boost the efficiency of the solar cells. Allaei *et al.* [7] have proposed an explicit and analytic charge-based model for estimating SCEs in GaN High-Electron-Mobility Transistor (HEMT) devices. This model is derived from the physical charge-based core of the Ecole Polytechnique Federale de Lausanne (EPFL) HEMT model, which treats HEMT as a generalized MOSFET. Liu and Shur [8] came with a Technology Computer-Aided Design (TCAD) model for AlGaAs/InGaAs & AlGaN/GaN, and Silicon-On-Insulator (SOI) TeraFETs are in good agreement with the measured current-voltage characteristics and the response to the sub-THz radiation in their research. By activating or deactivating different physical mechanisms in the TCAD models, they show that the response saturation is caused by the gate leakage for AlGaAs/InGaAs Heterostructures Field-Effect Transistors (HFETs) and AlGaN/GaN HFETs and by the avalanche effect for SOI MOSFETs.

The author's previous research work [9] designed an analytical model of the lightly doped Cylindrical Surrounding Double-Gate (CSDG) MOSFET. The capacitance modeling was performed for this cylindrical structure. This modeling was analyzed for all operating regions of the transistors, capacitance estimation, and electrical field dependence on the capacitance. The results were compared with the previous research and tabulated. It was observed that the transconductance (G_m) values had been raised to $0.0106\ S/\mu m$ from $0.000645\ S/\mu m$ with the inclusion of 2D electron gas in the core of CSDG MOSFET. Also, the author's previous work [10] designed a novel Double-Gate (DG) MOSFET design. The parasitic capacitance has to be taken care of while designing a device using this material since the capacitance affects much in the AlGaAs based devices. The average velocity of the electrons has been observed to increased by 14.63 % in the Au-gate (gate-1) and Pt-gate (gate-2) material-based DG MOSFET compared to the Silicon-based DG MOSFET. These works are the fundamental works carried out for the present research work. The DG MOSFET with arbitrary alloys and the high-ƙ dielectric make the potential motivation for the development of this work. The energy band potential has been calculated from the previous research carried out by the same authors.

In this present research work, a CSDG MOSFET has been designed using Lanthanum Oxide (La_2O_3) as a prominent gate oxide dielectric material. The La_2O_3 outperforms all the high-ƙ dielectric materials in the linear region of operation. Also, the authors have carried out recent research to support the usage of La_2O_3 in the MOSFET design. The high-ƙ dielectric material has been used to subsidize the effect of short channel while in the working region of the MOSFET. The Lanthanum Oxide properties have been analyzed using an electronic simulator. The designed CSDG MOSFET structure has been simulated with various channel lengths and thickness of gate-oxide to analyze the effects on the device's electrical parameters. The selected dielectric has been introduced in the CSDG platform to analyze the results. This paper has been organized as follows. Section II analyzes the design of CSDG MOSFET for electrical field with high-k dielectric. Section III realizes the electron density profiles for the CSDG MOSFET using the capacitive model. Section IV has the results and its discussions belong to the proposed energy model. Finally, Section V concludes the work and recommends the future aspects.

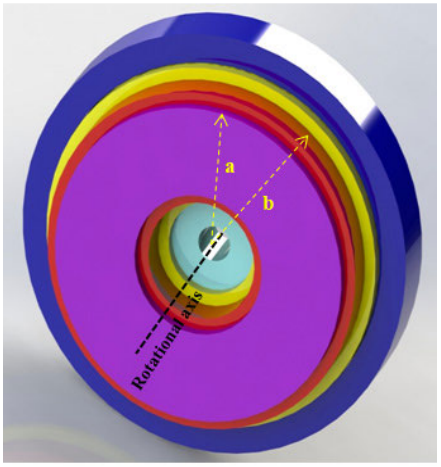
II. CSDG MOSFET WITH HIGH-ƙ DIELECTRIC

In this research work, all the Short Channel Effects (SCEs) have been discussed to reduce its effects so that the MOSFET operates with high efficacy. The SCEs considered are the ON-current, OFF-current, subthreshold swing, and Drain Induced Barrier Lowering (DIBL). In this analysis, the various materials have been analyzed and its characteristics have been compared. This yields that the La_2O_3 outperforms by providing greater immunity from the SCEs and make the MOSFET works well in low power RF devices. The CSDG MOSFET has been the most successful structure, which has good controllability and is highly influential with the electrical behavior of the conventional MOSFETs [11], [12]. In recent years, numerous approaches which utilize the CSDG MOSFET have been developed with diverse switching applications [13]–[16].

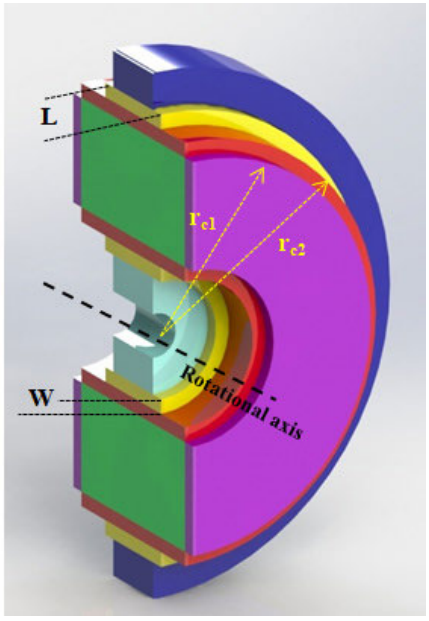
The voltage required to change the slope of the drain current during switching mode (subthreshold swing) and relates to the faster switching performance when the transistor operates in the sub-threshold region of operation at minimum voltage application [17]. The desirable carrier injection module has been introduced in the CSDG MOSFET design to obtain a lower subthreshold swing. Therefore, CSDG MOSFET with thermal stability has been designed with low gate voltages. The desired carrier injection mechanism has been utilized [18]–[20] to achieve a low subthreshold swing. Therefore, the CSDG MOSFETs have been introduced as a substitution for conventional MOSFETs in the technology nodes. This device gained more popularity since the band-to-band leakage in CSDG MOSFET could give a *55 mV/decade* subthreshold slope valu *e* at threshold voltage below *1 V*. Fig. 1 shows the architecture and cross-sectional views of the proposed CSDG MOSFET in the technology node. Cylindrical capacitance can be given as [9], [11], [14]:

$$C_{ox\_cyl} = k\varepsilon_0 \frac{A}{d} = k\varepsilon_0 \frac{2\pi\left[\left(r_{cl}^2 - r_{c2}^2\right) + h\left(r_{cl} - r_{c2}\right)\right]}{d} = \frac{2\pi k\varepsilon_0}{d}\left[\left(r_{cl}^2 - r_{c2}^2\right) + h\left(r_{cl} - r_{c2}\right)\right] \quad (1)$$

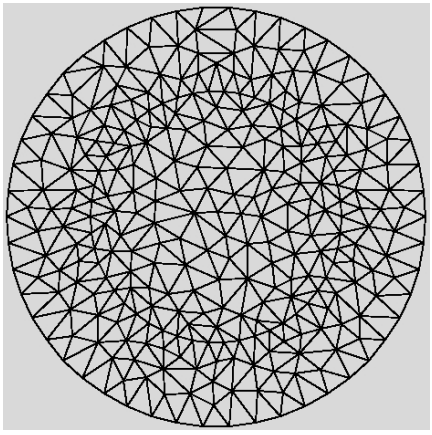
where C_{ox_cyl} is the capacitance in the concentric walls, A and d is the area of the cylinder and length of the cylindrical structure, ƙ and ε_0 is the dielectric constant and permittivity, respectively (Table 5). The capacitance present in the



(a) The isometric view of the proposed CSDG MOSFET



(b) Cross-Sectional view of the CSDG MOSFET



(c) Mesh structure in the CSDG MOSFET

FIGURE 1. The proposed CSDG MOSFET structure with a high-k̂ dielectric material.

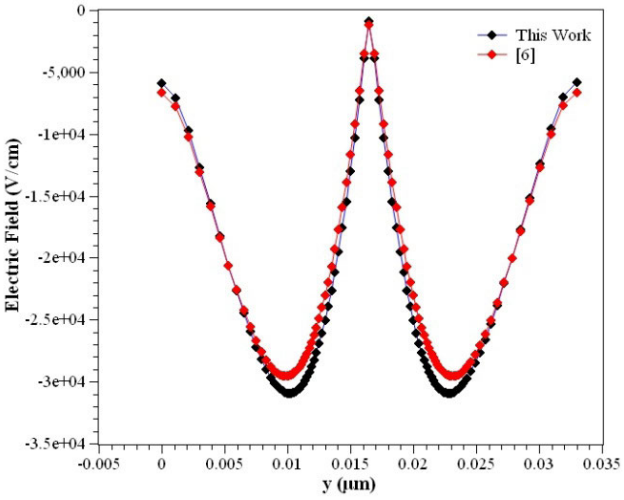


FIGURE 2. Electrical field along the length of channel of proposed CSDG MOSFET compared with previous research.

cylindrical structure is the function of the radii of the inner '*a*' and the outer '*b*' cylinders. Eq. (1) shows the capacitance between the gate and the channel materials due to the oxide layer. The proposed design is compatible with improving the ON-current to OFF-current ratio, thereby makes the device most suitable for RF applications such as amplifiers, mixers, and filters of the nanoscale regime [21]–[24].

An electric field in this cylindrical capacitor within the cylinder is expressed as [14], [17]:

$$\left.\begin{aligned} E = \frac{V}{d} = \frac{\mu_0}{2\pi R^2} \cdot \frac{\mu_n \pi k \varepsilon_0}{\ln\left(\frac{b}{a}\right)} \\ \cdot \frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \\ E = -\frac{\mu_0 \mu_n k \varepsilon_0}{2R^2} \cdot \ln\left(\frac{a}{b}\right) \\ \cdot \frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \end{aligned}\right\} \quad (2)$$

The electrical field is directly proportional to the radius of the CSDG MOSFET, which has been proposed in this section. As shown in Fig. 2, the electrical field in the proposed CSDG MOSFET has been more submissive with the conventional method of using SiO_2 in the dielectric material. The electron characteristics of the entire device are shown in Fig. 3. This shows the distribution of electrons in the conduction band, doping concentration, and the electron density profile when the device has been switched on. Plane views along the dimensions of the device in x- and y-axis have been represented in Fig. 3.

The presence of an electrical field states that the high-k̂ dielectric material in the CSDG MOSFET regime has more controllability over the device [25]–[29]. The Lanthanum Oxide (La_2O_3) shows a considerable improvement in the electrical characteristics of the CSDG MOSFETs. This high-k̂ dielectric material has the potential

to be used shortly in almost all the transistor designs because of the stability improvement and immunity towards SCEs [30].

III. ELECTRON DENSITY PROFILE OF CSDG MOSFETs

The electrical characteristics of the CSDG MOSFET have been analyzed and the optimum condition is derived. The device behaves in the operating region with high immunity to the SCE developed in the bulk and gate contacts. The simulation observed the drain current to be *2.41 mA/μm* ($V_d = 0.4\ V$) at the edge of the terminal towards gate contact and *2.39 mA/μm* ($V_d = 0.7\ V$) at the edge of the device. The drain current plays a major role in determining the I_{ON}/I_{OFF} ratio. The current observed from the simulation near the gate terminal is *62.14 %* less than the edge of the device for $V_d = 0.4\ V$.

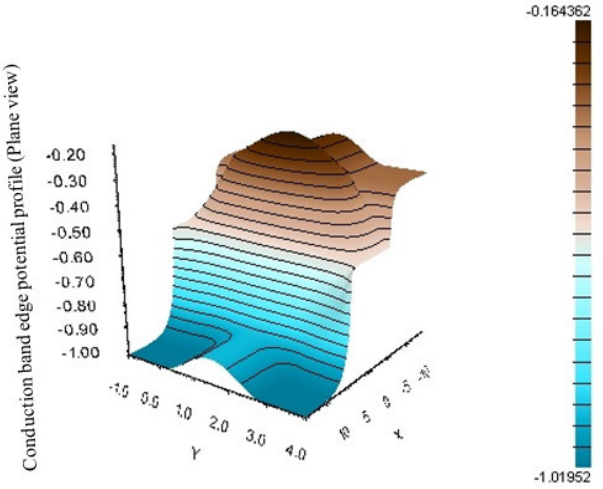
Also, the current measured at the place proximity to the gate has been 49.5 % less than the edge for $V_d = 0.7\ V$. The current at the edge of the device is measured and it has to be maintained high to ensure high electron mobility in the CSDG MOSFET structure [31]–[33]. The energy stored in the cylindrical capacitor inside the CSDG MOSFET, as shown in (3), constitutes the most significant factor for the mobility of electrons in the channel [15], [21]. The high-k̂ dielectric has been maintained between the gate and the channel to protect the device from the injection of the electrons from the gate terminal when an external supply is given.

A. ENERGY DENSITY ANALYSIS

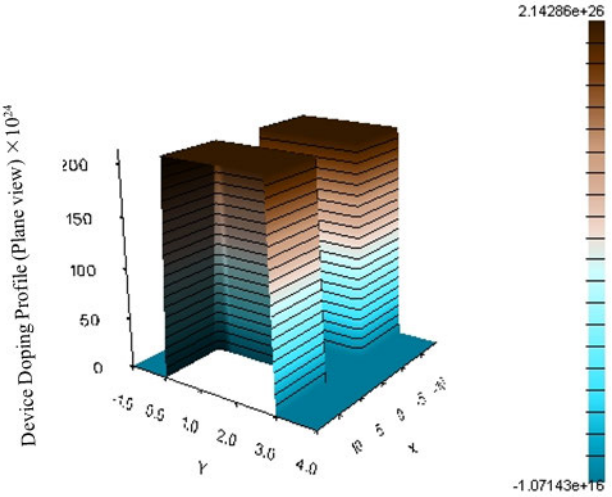
The electron density inside the device changes with the applied electrical field among the terminals [23]. The expression for the electric field in the oxide layer (E_{ox}) of CSDG MOSFET is given as [9], [14], [17], [32]:

$$\left.\begin{aligned} E_{ox} &= E_{imer} + E_{outer} \\ E_{ox} &= \left\{ -\frac{\mu_0 \mu_n k \varepsilon_0}{2r} \cdot \ln\left(\frac{b}{a}\right) \right. \\ &\quad \left. \cdot \frac{W}{L} \left[2\,(V_{GS} - V_T)\, V_{DS} - V_{DS}^2 \right] \right\} \\ &+ \left\{ \frac{\mu_0 \mu_n k \varepsilon_0}{r} \cdot \ln\left(\frac{a}{b}\right) \cdot \frac{W}{L} \left[2\,(V_{GS} - V_T)\, V_{DS} - V_{DS}^2 \right] \right\} \\ E_{ox} &= \frac{1}{2r} \mu_0 \mu_n k \varepsilon_0 \cdot \ln\left(\frac{a}{b}\right) \\ &\quad \cdot \frac{W}{L} \left[2\,(V_{GS} - V_T)\, V_{DS} - V_{DS}^2 \right] \end{aligned}\right\} \quad (3)$$

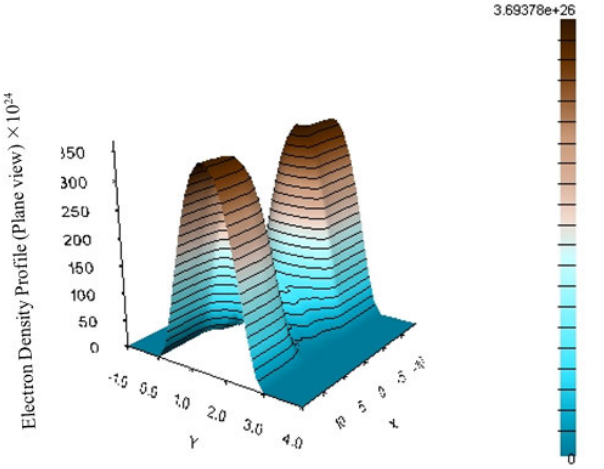
This (3) needs further modification for the cylindrical structure and also to provide energy storage condition, it has been rewritten as (4). By considering the Eq. (16) of Ref. [9], the inner structure of the cylindrical capacitor is mainly dependable on the '*a*' and not on the '*b*'. Hence the (3) can



(a) The conduction band potential profile.



(b) Doping profile in the operating condition of CSDG.



(c) Electron density profile of the device.

FIGURE 3. Electron characteristics of the proposed CSDG MOSFET with high-k̂ dielectric material between gate and substrate (A Plane view representation in working mode).

be rewritten as:

$$\left.\begin{aligned} E_{ox} &= \left\{-\frac{\mu_0\mu_n k\varepsilon_0}{2r}\frac{aW}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]\right\} \\ &+\left\{\frac{\mu_0\mu_n k\varepsilon_0}{r}\cdot\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]\right\} \\ E_{ox} &= \frac{1}{2r}\mu_0\mu_n k\varepsilon_0\cdot\left\{\left[\ln\left(\frac{a}{b}\right)\right]-a\right\} \\ &\cdot\frac{W}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right] \end{aligned}\right\} \quad (4)$$

This derivation has been further divided into the following sections:

a. For CSDG MOSFET, $a = r_{c1}; b = r_{c2}$ in (4), the E_{ox} becomes,

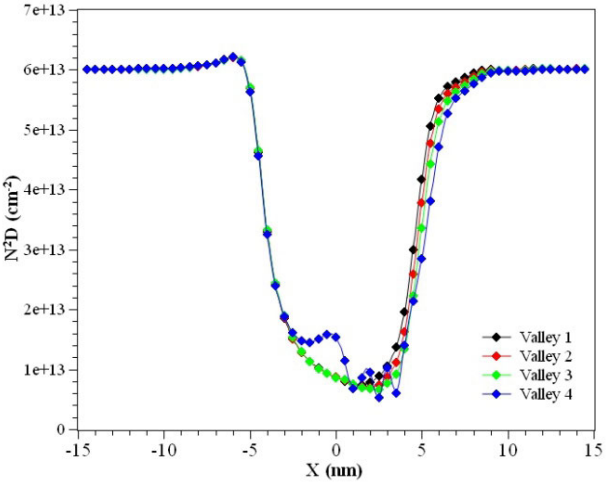
$$\begin{aligned} E_{os} &= \frac{1}{2r}\mu_0\mu_n k\varepsilon_0 \\ &\cdot\left\{\left[\ln\left(\frac{r_{cl}}{r_{c2}}\right)\right]-r_{cl}\right\} \\ &\cdot\frac{W}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]\Bigg\} \end{aligned} \quad (5)$$

b. For $r_{c1} = r_{c2} = r$:

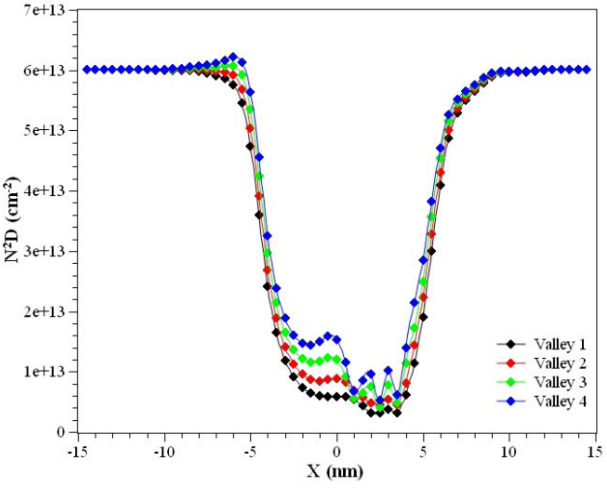
$$\begin{aligned} E_{0\,s} &= \frac{1}{2r}\mu_0\mu_n k\varepsilon_0\cdot\{[\ln(1)]-r\} \\ &\cdot\frac{W}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right] \\ E_{oss} &= \frac{1}{2r}\mu_0\mu_n k\varepsilon_0\cdot\{-r\} \\ &\cdot\frac{W}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]\Bigg\} \\ E_{os} &= -\frac{1}{2}\mu_0\mu_n k\varepsilon_0\frac{W}{L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right] \end{aligned} \quad (6)$$

The energy stored in this condition exists in a negative form and is independent of the radial geometry. Whereas in ref. [9] the boundary condition provides no energy. In (16) of ref. [9], the boundary condition gives $E_{ox} = 0$. To overcome this issue, (3) has been modified for the inner cylindrical structure as (4).

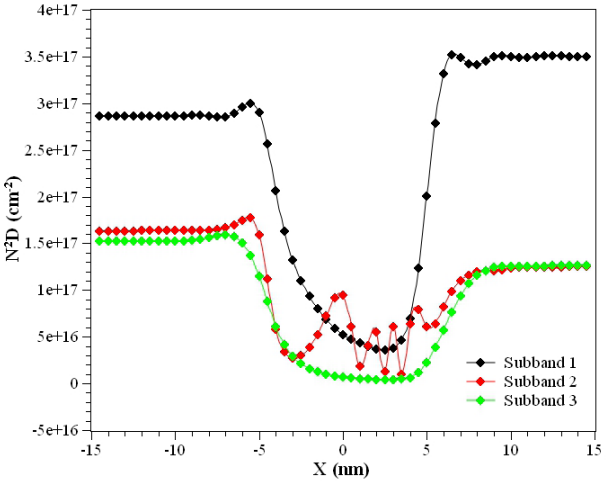
Fig. 4 shows the electron density in the CSDG MOSFET when the terminal voltage is applied. The complete electron density profile shows the exact representation of the electrons flow as per the device doping and hardware setups. Fig. 4(a) illustrates the electron density profile at the terminal with a different V_d that has the same effect on the electron concentration for all the valley degeneracy values. The same number of electrons passes by until the gate terminal edge [27], [34]–[36]. But in Fig. 4(b), it has been clearly shown with various electron concentrations along the device's channel. Fig. 4(c) portrays the electron density along with the sub-bands along the length of the channel. The sub-bands along the length of the device have been illustrated in Fig. 5. The sub-bands play a significant role in accumulating the electrons for fast transfers across the channel of the CSDG MOSFET [37].



(a) 2D Energy density along the channel at different V_d

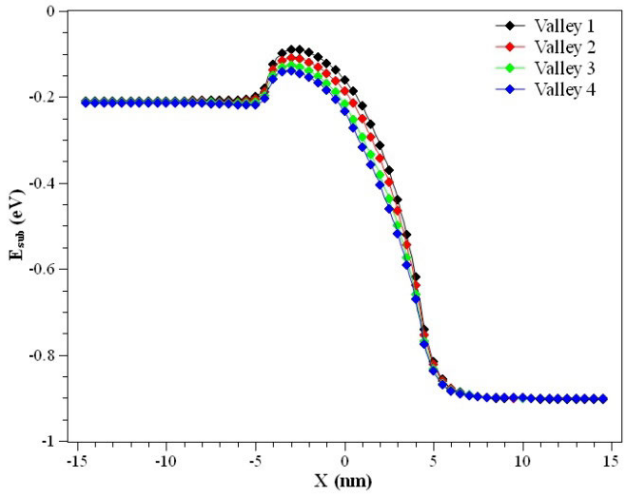


(b) 2D Energy density along the channel

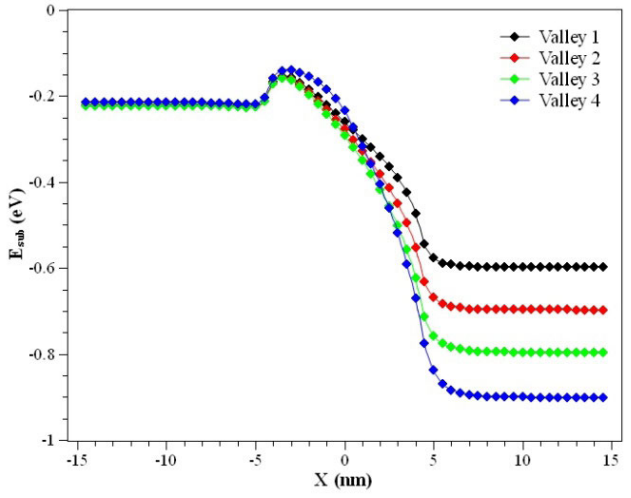


(c) 2D Energy density of sub-bands along the channel

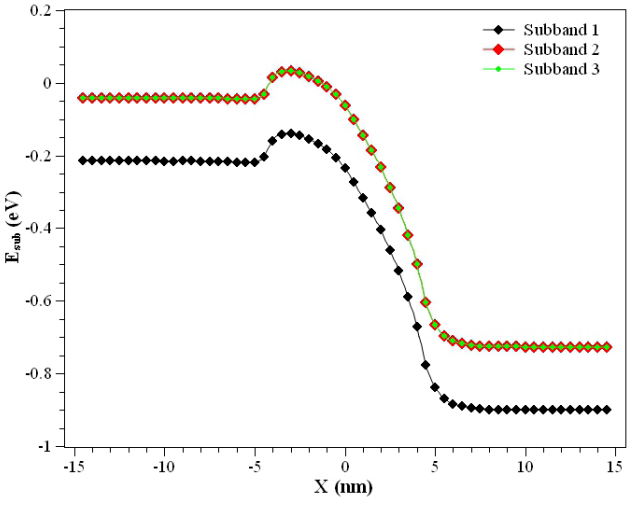
FIGURE 4. 2D Energy density profile in the CSDG MOSFET paradigm.



(a) First sub-bands along the channel at different V_d.

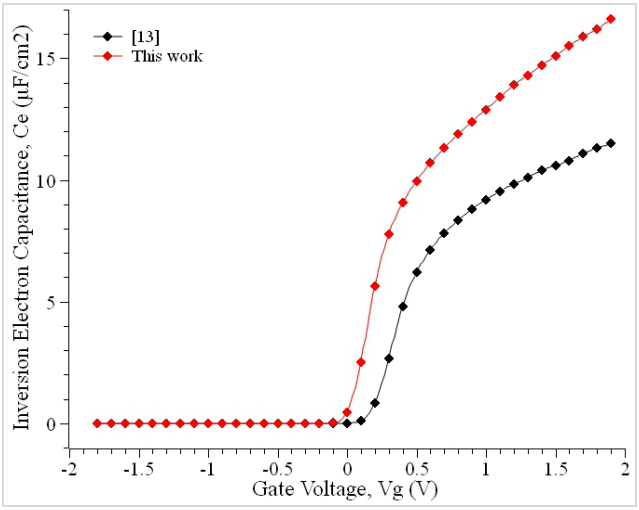


(b) First sub-bands along the channel.

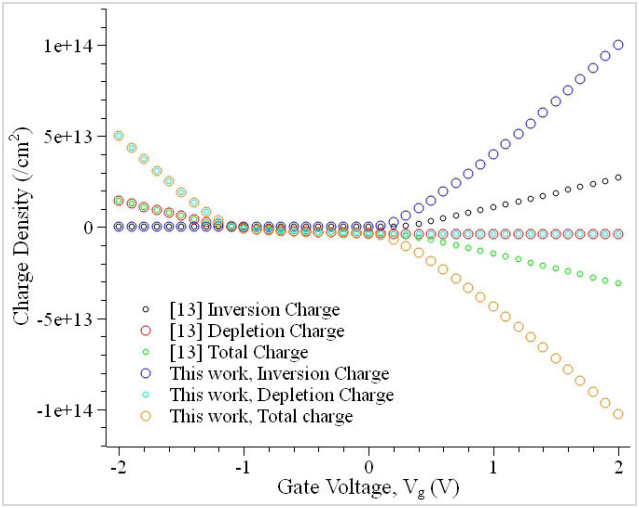


(c) Sub-band energy potential along the channel.

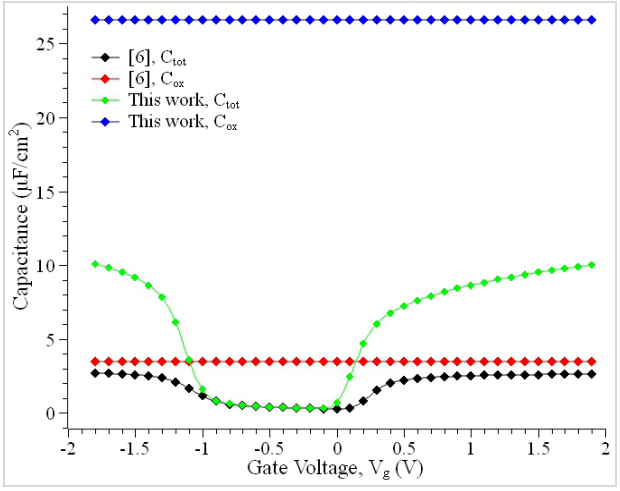
FIGURE 5. Sub-bands along the channel in the CSDG MOSFETs.



(a) C_e-V_g for a gate length of L_g = 70 nm and t_{ox} = 5 nm.



(b) Charge distribution along the channel in the CSDG MOSFET.



(c) Capacitance (oxide and total) versus Gate Voltage, Vg

FIGURE 6. Effect of capacitances w.r.t. gate voltage (V_g) in the CSDG paradigm.

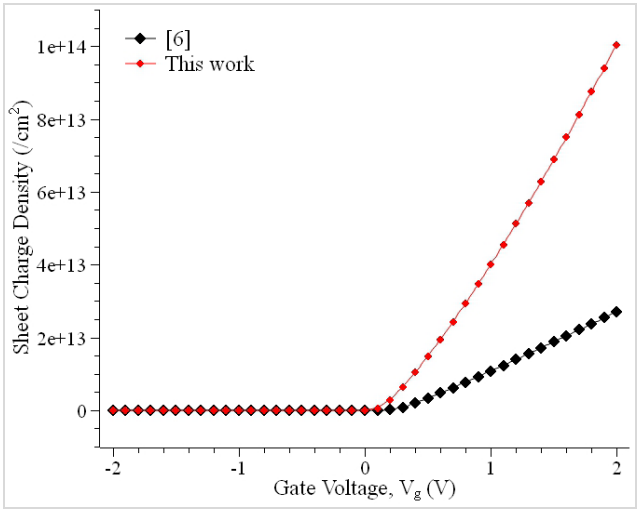


FIGURE 7. Sheet charge density versus gate voltage, (V_g).

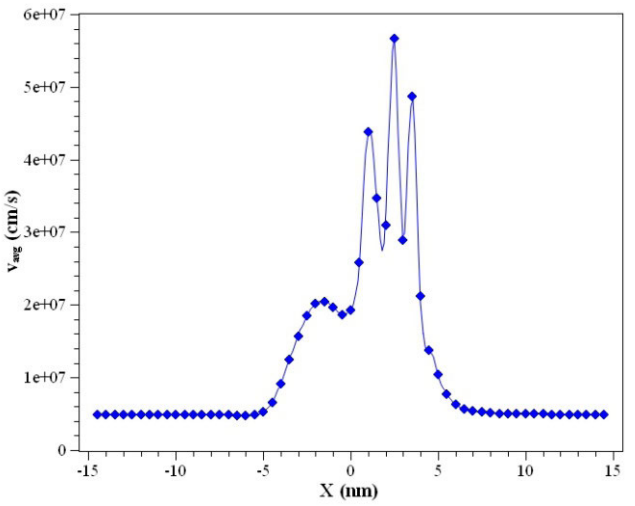


FIGURE 9. Average velocity of the electrons in the channel.

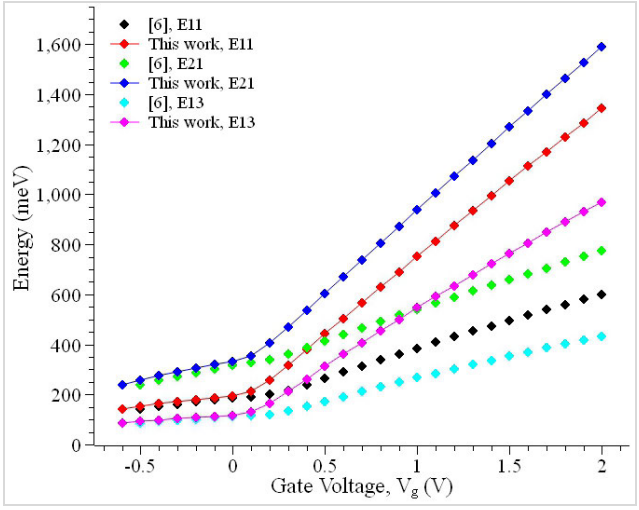


FIGURE 8. Energy levels of E11, E21, and E13 for various types of configurations in CSDG MOSFET.

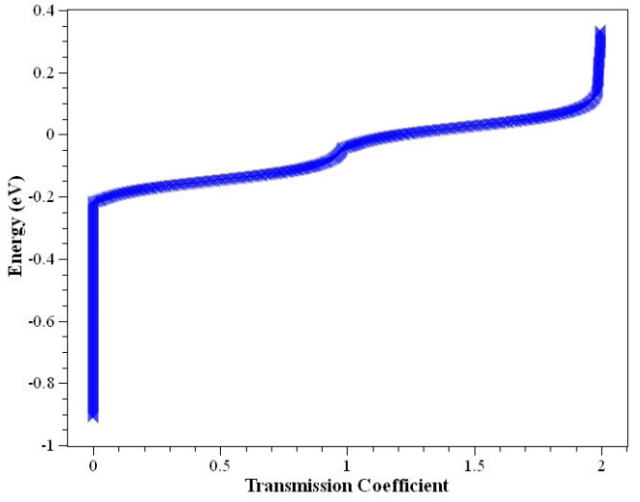


FIGURE 10. Energy versus transmission coefficient.

The end of the device along the source, center of the gate terminal, and the end of the device along the drain have become potential spots for the measurement of the energy in the sub-bands. The *0.220 eV* difference has been observed at the source terminal with a drop of *12.4 %* than the *0.260 eV* along the center of the gate and *0.598 eV* at the end of the device along with the drain terminal. The drain has more eV to be supplied to the electrons for mobility [38]–[40]. The sub-bands energy has been extensively shown in Fig. 5. The figures (a) along the different V_d, (b) along the channel, and (c) sub-bands along the channel in CSDG MOSFETs clearly show the difference in eV to be supplied as a result of gate terminal supply. This represents the electron mobility along the length of the channel.

B. CAPACITANCES IN THE CSDG

The CSDG MOSFETs are governed by the energy and electrostatic potential produced by the gates and the terminals. This capacitance modeling efficiently creates an understanding concept for the SCEs and the device dimensions [9], [10]. The energy stored in this capacitor is responsible for the channel potential, which in turn switch-ON the transistor for RF applications. The parabolic approximation of the SCEs in the CSDG MOSFET regime has been made for the energy density profile [41]–[46].

The charge accumulation due to various capacitances in the CSDG MOSFET with different configurations has been illustrated in Fig. 6. The results of the proposed device had been submissive to the conventional MOSFET. The charges discussed here are inversion charge, depletion charge, and the total charge per square centimeter. The drain current gradually rises by increasing the gate voltage (V_g) in the device with gate length *70 nm*. The proposed CSDG MOSFET is submissive to the conventional MOSFET.

The capacitance characteristics (C-V_g) and sheet charge density of the CSDG MOSFET device had been analyzed,

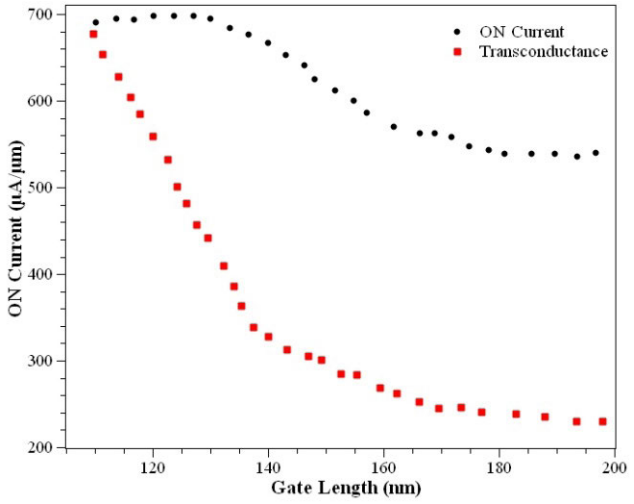


FIGURE 11. ON-current vs transconductance.

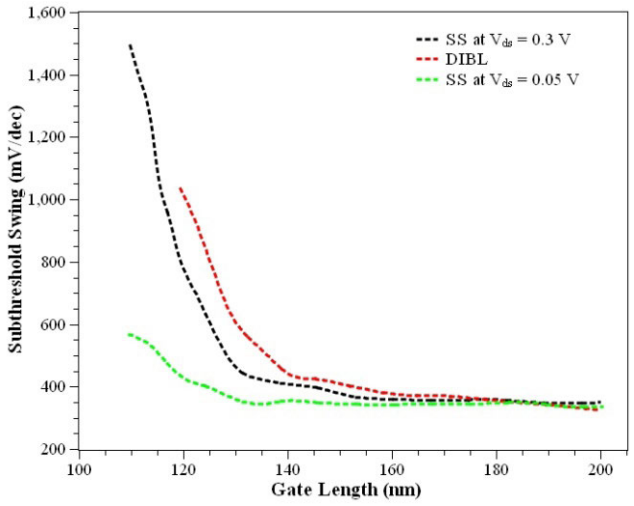


FIGURE 12. Subthreshold swing vs DIBL in CSDG paradigm.

which is obtained at fixed gate length ($L_g = 70\ nm$) and oxide thickness ($t_{ox} = 5\ nm$). The results of the extracted parameters for the device with La_2O_3 gate oxide for various gate length and oxide thickness shows submissive results compared to the conventional MOSFET device. The proposed model showing the improvements in I_{ON}/I_{OFF} ratio of 3.1×10^7 at $V_d = 0.05\ V$ for $L_g = 100\ nm$; $t_{ox} = 5\ nm$ with La_2O_3 oxide layer and I_{ON}/I_{OFF} ratio of 1.2×10^7 at $V_d = 0.05\ V$ for $L_g = 100\ nm$; $t_{ox} = 5\ nm$ with conventional SiO_2 oxide layer. Hence, the proposed CSDG MOSFET is best suited for the RF hybrid applications and also in consumer electronics.

IV. RESULTS AND DISCUSSIONS

The characteristics of the CSDG MOSFET with high-ƙ dielectric are obtained as results of the simulation of the device. Capacitance, energy stored in the MOSFET, and sheet charge density measure different devices' performance [22]–[24], [47]. Fig. 6 shows the comparison of inversion electron capacitances of the work carried out in [6], [13] and this proposed work with diversified gate oxide materials. The result shows that the highest C_e difference achieved in the simulation design with La_2O_3 based CSDG MOSFET is the order of $17.24\ \mu F/cm^2$.

For analyzing the device performance capacitance, sheet charge density, and the energy levels of various configurations (as in Fig. 7 and Fig. 8.) and their parameters have been extracted from the characteristics of the proposed CSDG MOSFET device. The sheet charge density has been calculated for the proposed CSDG MOSFET and it has been observed to accumulate a large number of electrons in terms of charge density. The charge density plays a significant role in electron mobility across the device [29], [48]–[51]. This makes the device faster than the conventional MOSFETs. The variation of the sheet charge density across the applied gate voltage has been portrayed in Fig. 7. The energy level such as E12, E21, and E13 has been discussed concerning gate voltage applied to the device. Fig. 8 shows the energy levels in the CSDG MOSFET device with the gate voltage. The sub-bands along the length of the channel are tabulated in Table 1.

The CSDG MOSFET shows good improvement when used with La_2O_3 as a high-ƙ dielectric material. The average velocity of the electrons in the device across the dimension has been shown in Fig. 9. Energy stored in the capacitor has been converted into an electric field, thereby influencing electrons' movement inside the device [7], [52]–[55]. The energy concerning the transmission coefficient has been illustrated in Fig. 10. Table 2 shows the simulation results with the La_2O_3 material for various oxide thickness.

TABLE 1. Sub bands for the CSDG MOSFET along the device length.

Length of the device (nm)	Energy Distribution (eV)		
	Valley-1	Valley-2	Valley-3
-14.5 (Source)	-0.2148	-0.04108	-0.04108
-10	-0.215	-0.04127	-0.04127
-5	-0.218	-0.04393	-0.04393
0 (Gate)	-0.23429	-0.06183	-0.06183
5	-0.83765	-0.66571	-0.66571
10	-0.90009	-0.7265	-0.7265
14.5 (Drain)	-0.90095	-0.72731	-0.72731

TABLE 2. Simulation results of CSDG MOSFET with La_2O_3 at $L_g = 100$ nm.

t_{ox} (nm)	V_g (V)	Subthreshold Swing (mV/decade)	I_{ON}/I_{OFF} At $V_d = 0.05$ V	I_{ON}/I_{OFF} At $V_d = 1$ V
3	0.601	20.015	1.32×10^7	7.66×10^9
5	0.957	21.764	3.35×10^7	6.72×10^9
7	1.350	23.481	2.89×10^7	5.20×10^9

TABLE 3. Average velocity and first sub bands.

Length of the device (nm)	Average Velocity (cm/s)	First Sub Bands (eV)		
		Valley-1	Valley-2	Valley-3
-14	4,924,460	-0.214798	-0.041078	-0.041078
-13	4,925,220	-0.214823	-0.0411024	-0.0411024
-12	4,923,870	-0.214833	-0.0411106	-0.0411106
-11	4,921,500	-0.214877	-0.0411521	-0.0411521
-10	4,922,360	-0.214997	-0.0412656	-0.0412656
-9	4,908,260	-0.214967	-0.0412130	-0.0412130
-8	4,877,890	-0.215143	-0.0413397	-0.0413397
-7	4,840,820	-0.216217	-0.0423193	-0.0423193
-6	4,761,590	-0.218188	-0.0441226	-0.0441226
-5	5,251,450	-0.217998	-0.0439277	-0.0439277
-4	9,112,640	-0.158655	0.0148478	0.0148478
-3	15,709,900	-0.139217	0.0337587	0.0337587
-2	20,108,700	-0.154305	0.0184226	0.0184226
-1	19,686,600	-0.183308	-0.0106754	-0.0106754
0	19,272,000	-0.234293	-0.0618277	-0.0618277
1	43,810,900	-0.315852	-0.1437200	-0.1437200
2	31,002,100	-0.404699	-0.2326950	-0.2326950
3	28,867,900	-0.517784	-0.3458730	-0.3458730
4	21,190,900	-0.670797	-0.4989110	-0.4989110
5	10,409,200	-0.837646	-0.6657120	-0.6657120
6	6,285,870	-0.883303	-0.7109110	-0.7109110
7	5,362,510	-0.894543	-0.7215610	-0.7215610
8	5,138,340	-0.898959	-0.7256340	-0.7256340
9	4,976,750	-0.899408	-0.7258920	-0.7258920
10	4,949,610	-0.900089	-0.7265000	-0.7265000
11	4,949,010	-0.900789	-0.7271760	-0.7271760
12	4,927,110	-0.900754	-0.7271220	-0.7271220
13	4,926,260	-0.900823	-0.7271850	-0.7271850
14	4,929,320	-0.900952	-0.7273140	-0.7273140

The results obtained so far constitute the submissive operating of the CSDG MOSFET. The ON-current versus the gate length has been shown in Fig. 11. The comparison shows that the gate length affects the ON-current. The ON-current reduces with the increase in the gate length. The transconductance value also drops down when increasing the gate length. The drain-induced barrier lowering has been recorded against the subthreshold swing in the CSDG MOSFET in Fig. 12. The threshold voltage comparison has tabulated in the Table 4. The DIBL has been compared with the subthreshold swing at the various drain to source voltages; such as *0.3 V* and *0.05 V*. The SS at the $V_{ds} = 0.3\ V$ has controllable than the DIBL in the active region compared to the $V_{ds} = 0.05\ V$. The research work pulled out parameter DIBL for La_2O_3 *~5.78 mV/V* (for SiO_2 *~16.13 mV/V*), and subthreshold swing (SS) for La_2O_3 *~18.29 mV/decade* (for SiO_2 *~91.5 mV/decade*). The average velocity and the first sub-bands were shown in the Table 3 for further representation.

TABLE 4. Comparison of threshold voltage.

Ref	Material Analyzed	0.05	1
[6, 32]	$InAs/HfO_2$	0.455	0.389
[13]	$Silicon/SiO_2$	0.464	0.334
[21]	$GaAs/HfO_2$	0.458	0.393
[45]	InP/HfO_2	0.458	0.394
This Work	$Al_{0.3}Ga_{0.7}As/La_2O_3$	0.459	0.397

TABLE 5. Parameters used for capacitance modeling.

Symbol	Description of the parameters used
a	The inner radius of the cylindrical capacitor
b	The outer radius of the cylindrical capacitor
C_{ox}	The specific capacitance of the gate oxide
C_{ox_cyl}	The cylindrical capacitance (CSDG)
E_{cap}	Energy stored in the capacitor
E_{cap_cyl}	Energy stored in the cylindrical capacitor (CSDG)
E_{inner}	Energy stored in the inner cylinder
E_{outer}	Energy stored in the outer cylinder
h	Height of the cylindrical capacitor (CSDG)
L	The gate length of the transistor
L_c	Unit length of the capacitor
r	The radius of the cylindrical capacitor (General)
r_{c1}	The inner radius of the cylindrical capacitor (CSDG)
r_{c2}	The outer radius of the cylindrical capacitor (CSDG)
V_{GS}	Gate to Source voltage
V_{DS}	Drain to Source voltage
V_T	Threshold voltage
W	The width of the transistor
ε_0	The permittivity of free space
ε_{ox}	The relative permittivity of the gate oxide
k	Dielectric constant
π	Pi (≈ 3.1416), constant
μ_n	The electron mobility of the transistor substrate (n-type)

V. CONCLUSION AND FUTURE ASPECTS

With the increase in the kappa ($\hat{k}$) for the oxide materials, the equivalent thickness of the oxide layer decreases drastically. Due to this, the channel gets isolated from the high-$\hat{k}$ oxide material, resulting in narrower oxide in the CSDG MOSFET. Hence, the effect of the gate terminal has a better impact on the channel and experiences improved controllability. The selection of high-k dielectric improves the performance of the proposed device in the nanometer regime. It makes the CSDG MOSFET suitable for applications in RF hybrid and low power switching circuits. The current value in valley-1 is *2.41 mA/μm*; it also drops to *62.14 %* than valley-4, which has *6.38 mA/μm*. The energy in the sub-band for the operating region of the source has been observed to be *19.12 %* to the drain side which has the value of *0.041 eV* at the terminal end. This makes the proposed device has immune to SCEs and also have great scalability parameter. This also have greater performance in low power RF regime.

The effect of gate overlap distance from the source and drain terminal in the La_2O_3 gate oxide device can be analyzed as the future scope of this work. Future nano-CMOS device structures are constructed using non-silicon materials to over-

come the existing MOSFETs' basic limitations. This work can be extended in developing the Cylindrical Surrounding Double-Gate (CSDG) MOSFETs with inert semiconductors materials and various other arbitrary semiconductor materials.

APPENDIX

See tables 3–5.

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