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Research on Synchronous Rectification Driver Technology of High-Frequency DC-DC Resonant Converter Based on GaN Devices

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ABSTRACT With the increase of switching frequency to tens of MHz, the synchronous rectification faces many new challenges, among which a significant one is the design of the driver circuit for the synchronous rectification with wide bandgap gallium nitride (GaN) devices. According to the self-resonant driving theory, an in-phase feedback synchronous rectification driver circuit (SRDC) based on GaN devices and the driver chip is proposed in this paper. In this SRDC, the nonlinear parasitic capacitors are replaced with external capacitors, and the synchronous driving signal is in-phase with the excitation source. The new scheme can provide precise driving timing, stable driving amplitude and flexible phase-shifting characteristics for the synchronous rectification of a high-frequency DC-DC resonant converter (HFDRC) based on GaN devices. In this paper, a detailed parameter design method is introduced by analyzing the characteristics of the feedback network. The feasibility and effectiveness of the proposed SRDC are verified on a 20 MHz prototype with 18 V input and 5 V/2 A output.

INDEX TERMS External capacitor, gallium nitride (GaN), high frequency, synchronous rectification driver circuit (SRDC).

I. INTRODUCTION

Increasing switching frequency of converters can significantly reduce the volume and weight of passive components, increase the power density and the dynamic response [1]–[4]. Recently, the application of wide bandgap devices [5], [6] has enabled the operating frequency of DC-DC power converters to tens of MHz. Among them, the high-frequency DC-DC resonant converter (HFDRC) has received much attention.

The HFDRC generally includes three parts: the inverter, the matching link, and the rectifier. At present, diodes are usually adopted in the rectifier of the HFDRC at dozens of MHz, causing significant power loss [7]. To solve this problem, synchronous rectification technology can be utilized.

The biggest challenge to introduce synchronous rectification technology into the HFDRC is the driving control of the synchronous rectifier (Q_{SR}). When synchronous rectification based on Si MOSFET is adopted, the driving modes mainly include square wave driving mode and resonant driving mode [8]. The loss of square wave driving mode is directly proportional to the operating frequency. As the operating frequency increases to tens of MHz, the loss of driver circuit will rises rapidly, making it difficult to apply in such a high frequency region. To reduce the driving loss, the Q_{SR} can be driven by a resonant driver circuit. There are two main types of resonant driver circuits: external resonant driver circuit and self-resonant driver circuit. Reference [9] introduced a two-way complementary external resonant driving mode for push-pull circuit. In a resonant converter operating at tens of MHz, the timing relationship between the main switch (Q_{main}) and Q_{SR} is not necessarily complementary; and it depends on the circuit parameters. Therefore, the resonant driving mode mentioned in [9] is not appropriate for synchronous rectification at high-frequency region.

To overcome the difficulty of controlling the timing between the Q_{main} and Q_{SR}, some scholars have proposed two

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self-resonant schemes for synchronous rectification driver circuit (SRDC) based on Si MOSFET. Reference [10] mentioned a self-resonant SRDC, whose excitation source is from the auxiliary winding of transformer. The auxiliary winding can realize electrical isolation and achieve a satisfactory driving effect. Nevertheless, this method requires additional auxiliary winding, increasing the volume and design difficulty. Reference [11] illustrated a self-resonant SRDC in which the excitation source is the drain-source voltage of Q_{SR}. The parasitic capacitor of Q_{SR} is applied to transmit the signal, whereas the amplitude and phase of the driving signal is adjusted by changing the parameters of other components in the feedback network. Due to the non-linearity of the parasitic capacitor of the Q_{SR}, the driving signal is unstable. If the gate source or drain source of Q_{SR} was paralleled with capacitors to obtain a stable driving signal, the working state of Q_{SR} would be affected. Thus, this self-resonant SRDC greatly limits the stability of the driving signal and the freedom in the feedback network design.

All the aforementioned researches mainly focus on the SRDC with Si MOSFET. Compared with Si MOSFET, gallium nitride (GaN) devices possess the advantages of low on-resistance, small gate charge, excellent switching performance, high current density, and high power density [12], [13]. Therefore, GaN devices are suitable for high-frequency applications at ten MHz and above [14]–[16].

As for power converters based on GaN devices, a reliable GaN driver is critical for maintaining stable operation [17], [18]. In recent years, many scholars have proposed new ideas or designs in response to the challenges of GaN drivers, such as the stringent gate-source voltage limit, fast dv/dt behavior and high voltage drop during reverse conducting. Reference [19] introduced a synchronous gate driver with an adaptive detection function to ensure that the circuit achieves zero-voltage-switching (ZVS). Reference [20] proposed a high-voltage-level shifter with differential-mode noise blanking scheme, which can effectively improve the driving reliability of the converter in high-voltage and high-frequency occasions. Besides, reference [21] introduced a bipolar and a three-level gate drive voltage scheme, achieving a robust switching as well as low power losses during reverse conduction of the GaN device.

Currently, GaN devices are rarely used in MHz-level synchronous rectification circuits. However, with the advancement of wide bandgap devices and the increase in frequency and capacity, research in this area is urgently needed. Literature [22] reported an SRDC that combines the driver chip LM5114 with the second-order RC filter feedback network. A special phase shift is required in the feedback network to compensate for the long delays in the driver chip (typically 14 ns) and the comparator (9 ns). This not only limits the switching frequency, but also increases the design complexity and reduces the flexibility of the feedback network design.

In this paper, an in-phase feedback SRDC with external capacitors for GaN devices is proposed. Compared with the previous works, the proposed SRDC shows several advantages. Firstly, the sampling capacitors are separated from Q_{SR}, so that driving performance of the rectifier stage will not be affected when adjusting the amplitude-frequency characteristics of the feedback network. Secondly, the SRDC keeps the excitation source signal and the synchronous driving signal, v_S, in-phase, which greatly improves the flexibility of the feedback network design to adjust the amplitude-frequency characteristics of v_S. Thirdly, the SRDC drives GaN devices efficiently and makes the on-resistance low. According to the data sheet of the GaN device we use, the gate-source voltage needs to be controlled between 4.5 V and 5.5 V during the on-time to ensure extremely low on-resistance [23]. While the proposed SRDC can output a square wave signal stabilized above 4.5 V by comparing v_S with the threshold voltage.

This paper is structured as follows. In Section II, the control method of the HFRDC and the applied rectifier are introduced; and the traditional SRDC is presented. The proposed SRDC is detailed in Section III. Section IV shows the experimental results based on the SRDC. Finally, the conclusion is presented in Section V.

II. HFDRC

A. CONTROL METHOD OF HFDRC

For general power converters, the closed-loop control of the system is usually realized through pulse width modulation (PWM) [24] or pulse frequency modulation (PFM) [25], but neither of them is suitable for the HFDRC working at tens of MHz. The soft switch of the HFDRC is achieved with a certain duty cycle. Under the PWM control method, the duty cycle of the switch is variable, causing the deterioration of the soft switch and greatly increasing the switching loss. For the PFM control method, the frequency change of the system at high frequency requires an extremely fast response of the control system, which can be hardly fulfilled. Therefore, these two control methods are not suitable for the HFDRC.

The common control method for the HFDRC is hysteresis (ON-OFF) control [26], [27], which controls the enablement of the high-frequency driving signal through a low-frequency signal. Fig. 1 illustrates the operating principle block diagram of the HFDRC used in this paper, and Fig. 2 shows the main waveforms of ON-OFF control.

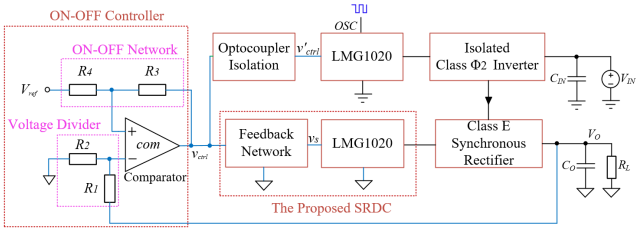

FIGURE 1. Operating principle block diagram of the HFDRC.

Its operating principle can be described as follows: the voltage dividing network samples the output voltage V_O, and then compares V_O with the reference voltage V_{ref} with the

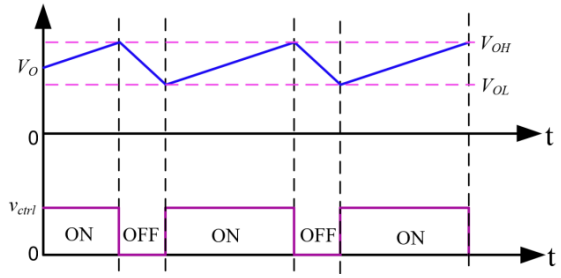

FIGURE 2. Main waveforms of the ON-OFF control.

high-speed comparator. When V_O reaches the upper limit voltage V_{OH} set by ON-OFF control, the control signal v_{ctrl} output by the comparator flips from high to low. On the one hand, v_{ctrl} can control the driver chip of Q_{main} with the high-speed optocoupler to prohibit the inverter from working. On the other hand, v_{ctrl} makes Q_{SR} turn off synchronously by controlling the SRDC. When V_O decreases to the lower limit voltage V_{OL}, v_{ctrl} changes from low to high. Then, the inverter and rectifier are re-enabled to work normally at 20 MHz and the converter works in the optimal resonant state, which is the prominent advantage of the ON-OFF control.

B. RECTIFIER OF HFDRC

In the HFDRC, the rectifier is designed to work in a resonant state to achieve ZVS conditions for Q_{SR}. The rectifier in this paper adopts the current-source Class E rectifier [28], as shown in Fig. 3. Here, I_{ac} is the input current source; L_R is the resonant inductor; C_R is the resonant capacitor, which absorbs the parasitic capacitor of Q_{SR}; C_O is the output capacitor; and R_L is the load resistor.

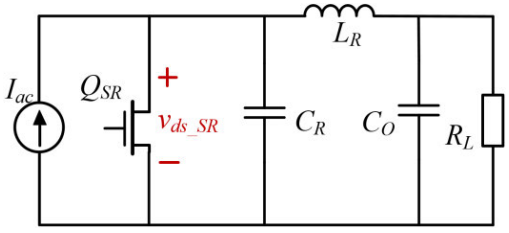

FIGURE 3. Current-source Class E rectifier.

The operating mode of the rectifier can be divided into two different parts. When Q_{SR} is on, all other components in the rectifier stage can be treated as short-circuited, so the equivalent impedance of the rectifier stage (Z_{rec}) can be seen as zero. When Q_{SR} is off, the load and the filter capacitor are regarded as a constant voltage source, which can be regarded as short-circuited when analyzing Z_{rec}. At this time, Z_{rec} can be considered as a branch that L_R and C_R connected in parallel [29].

C. TRADITIONAL SRDC

The traditional SRDC based on Si MOSFET devices is shown in Fig. 4. The excitation source utilizes the drain-source

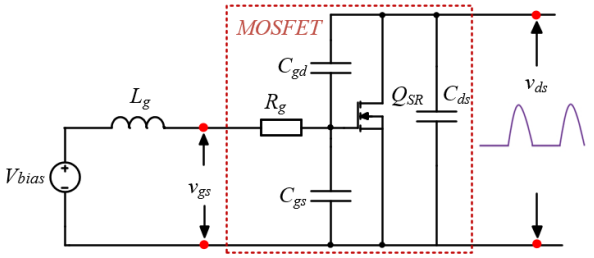

FIGURE 4. Feedback network of the traditional SRDC.

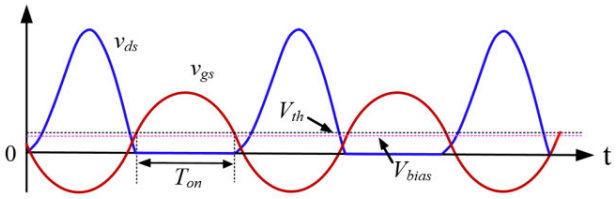

FIGURE 5. Main waveforms of the traditional SRDC.

voltage (v_{ds}) of Q_{SR}, and the way to sample v_{ds} uses the parasitic capacitors C_{gd} and C_{gs} of the corresponding Q_{SR} directly. Fig. 5 presents the time-domain relationship between v_{ds} and the gate-source voltage (v_{gs}) of the traditional SRDC, and v_{ds} is in opposite phase with v_{gs}. Besides, the duty cycle of Q_{SR} can be flexibly changed by adjusting the DC bias voltage (V_{bias}).

The transfer function of the traditional SRDC can be summarized as the following equation:

$$\frac{v_{gs}(s)}{v_{ds}(s)} = \frac{s^2 L_g C_{gd}}{s^2 L_g (C_{gd} + C_{gs}) + s R_g (C_{gd} + C_{gs}) + 1} \tag{1}$$

By substituting the designed parameters in [30] into (1), the bode diagram can be plotted, as shown in Fig. 6.

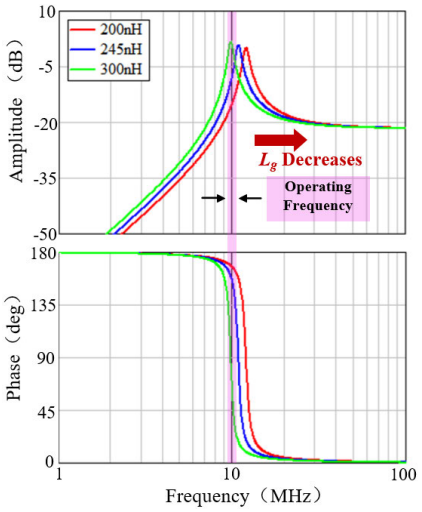

FIGURE 6. Bode diagram of feedback network with different L_g.

According to the transfer function and bode diagram, it can be seen that v_{gs} and v_{ds} exhibit opposite phases so that the

operating frequency of the circuit is set before the resonant point. Moreover, v_{gs} needs to be maintained at a large amplitude to ensure low on-resistance for Q_{SR}.

For Si MOSFET operating at MHz level, C_{gd} is usually not large. For example, Q_{SR} SI7454DP used in [30] holds $C_{gd} =$ 72 pF. If paralleling capacitor is added to the gate drain of Q_{SR} to improve the driving capability, the gate-drain impedance will be reduced. Thus, the risk of coupling v_{ds} to v_{gs} will increase when Q_{SR} turns on, resulting in a large loss in the driver circuit, unstable v_{gs}, and decreased switching speed. In addition, C_{gd} and C_{gs} vary non-linearly with the change of v_{ds}. As v_{ds} resonates, the unstable C_{gd} and C_{gs} will bring instability to the feedback network. Therefore, the best choice would be adjusting the gain and phase shift of the feedback network by changing L_g. Nevertheless, a small difference of L_g will lead to a drastic change in the amplitude and phase of v_{gs} before the resonant point. To obtain the required phase of v_{gs} by adjusting L_g will likely cause drastic changes in the amplitude of the v_{gs}, which is not allowed for GaN devices. Moreover, driving GaN with a sinusoidal signal will not only increase the risk of breakdown, but also fail to keep the device in a low on-resistance state during the on-time.

III. ANALYSIS ON PROPOSED SRDC

In the HFDRC, the switching timing of Q_{SR} needs to be strictly matched with the resonant state of the rectifier to achieve ZVS. The accurate switching timing of Q_{SR} is obtained through careful design of the feedback network.

A. OPERATING PRINCIPLE OF PROPOSED SRDC

Aiming at the problem that the design flexibility of the feedback network in the traditional SRDC is limited by the parasitic parameters of Q_{SR}, an in-phase feedback SRDC with external capacitors is proposed in this paper. The circuit structure is demonstrated in Fig. 7. It consists of a driver chip LMG1020 and a feedback network that is composed of external capacitors C_{S1} and C_{S2}, inductor L_S, resistor R_S, and DC bias voltage V_{bias}, where no additional comparator is required. Fig. 8 presents the time-domain relationship among the drain-source voltage of Q_{SR} (v_{ds_SR}), v_S, and the gate-source voltage of Q_{SR} (v_{gs_SR}). Among them, t_{on_delay} and t_{off_delay} represent the turn-on delay and turn-off delay of the driver chip (typical 2.5 ns), respectively; and V_L and V_H are the low-level threshold and high-level threshold of the driver chip, respectively.

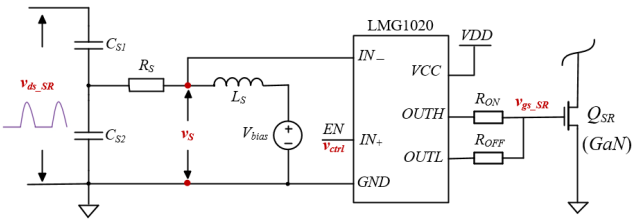

FIGURE 7. In-phase feedback SRDC with external capacitors.

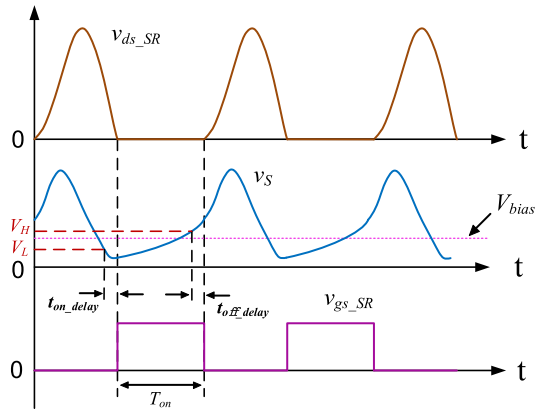

FIGURE 8. v_{ds_SR}, v_S, and v_{gs_SR} of proposed SRDC.

The operating principle of the proposed SRDC is described as follows: the excitation source v_{ds_SR} generates v_S through the function of the feedback network. And v_S goes to the inverting input of the driver chip, making v_S in-phase with v_{ds_SR}, so that the operating frequency band is located after the resonant point. Meanwhile, the noninverting input of the driver chip is enabled by the control signal v_{ctrl} of the ON-OFF control system. The driving timing of Q_{SR} is determined by v_S. As v_S decreases from high to V_L, Q_{SR} turns on after t_{on_delay}; and as v_S rises from low to V_H, Q_{SR} turns off after t_{off_delay}. The driver chip's output, v_{gs_SR} is close to a square wave, which ensures the low on-resistance of the GaN devices during the on-time.

In this work, V_{bias} is generated by the voltage regulator chip LP3878MR-ADJ, which provides DC bias voltage for v_S to realize a flexible duty-cycle adjustment. The part-to-part variation of the driver chip can be compensated via fine-tuning V_{bias}. It is important that the amplitude of the V_{bias} must be higher than V_L. Otherwise, v_S will always be lower than V_L, making Q_{SR} straight on.

B. FEEDBACK NETWORK OF PROPOSED SRDC

The feedback network controls the switching timing and duty cycle of Q_{SR} by adjusting the amplitude and phase of v_S. $v_S(t)$ includes the DC part, V_{bias} and the AC part, $v_{S\_ac}(t)$, as shown in (2):

$$v_S(t) = V_{bias} + v_{S\_ac}(t) \tag{2}$$

To get the transfer function of v_{ds_SR} and v_S, V_{bias} is set to zero in Fig. 7 to get the AC signal feedback network shown in Fig. 9.

The transfer function of v_{ds_SR} and v_S in Fig.9 can be derived as:

$$\frac{v_S}{v_{ds\_SR}} = \frac{s^2 L_S C_{S1}}{s^2 L_S (C_{S1} + C_{S2}) + s R_S (C_{S1} + C_{S2}) + 1} \tag{3}$$

The phase of the transfer function given in (3) can be expressed as:

$$\theta = \pi - \arctan\left[\frac{\omega R_S (C_{S1} + C_{S2})}{1 - \omega^2 L_S (C_{S1} + C_{S2})}\right] \tag{4}$$

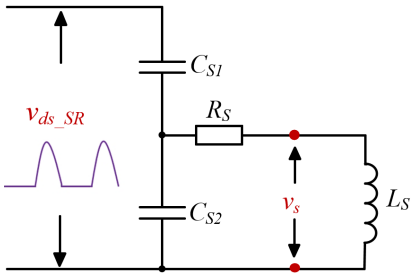

FIGURE 9. Feedback network when $V_{bias} = 0$.

It can be seen from (3) and (4) that L_S, C_{S1}, C_{S2}, and R_S influence the characteristics of the feedback network. The following is the analysis of the detailed effect of these parameters.

Fig. 10 shows the bode diagram of the feedback network with different L_S. v_{ds_SR} and v_S have an in-phase feedback relationship. The operating frequency band locates after the resonant point. And the advantage is that the amplitude of v_S is not oversensitive to the changes in L_S. As can be seen from Fig. 10, v_S can maintain a high and steady amplitude, whereas the phase shift becomes obvious as L_S changes in a relatively large range. By adjusting L_S, the phase of v_S can be flexibly adjusted without causing drastic changes in amplitude.

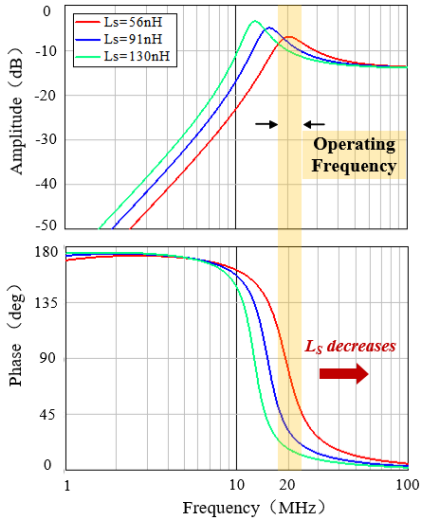

FIGURE 10. Bode diagram of feedback network with different L_S.

Fig. 11 presents the bode diagram of the feedback network with different C_{S1}. It can be found that the amplitude of v_S increases with the growth of C_{S1}, but the phase is almost unchanged. Therefore, we can fine-tune C_{S1} to adjust the amplitude of v_S in a small range without changing the phase shift.

Fig. 12 provides the bode diagram of the feedback network with different C_{S2}. Obviously, C_{S2} has a vital impact on the amplitude of v_S. The larger the C_{S2}, the lower the amplitude and the smaller the phase shift.

Fig. 13 plots the bode diagram of the feedback network with different R_S. It shows that R_S has a great impact on the

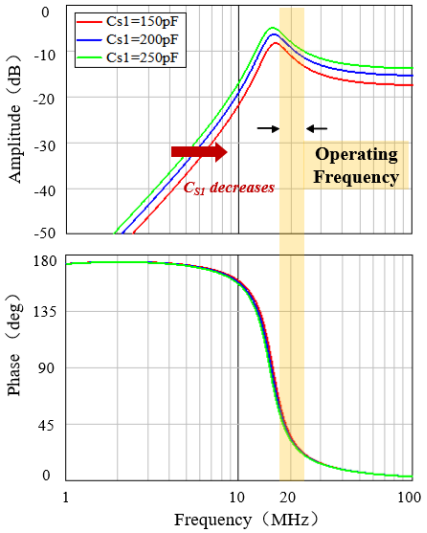

FIGURE 11. Bode diagram of feedback network with different C_{S1}.

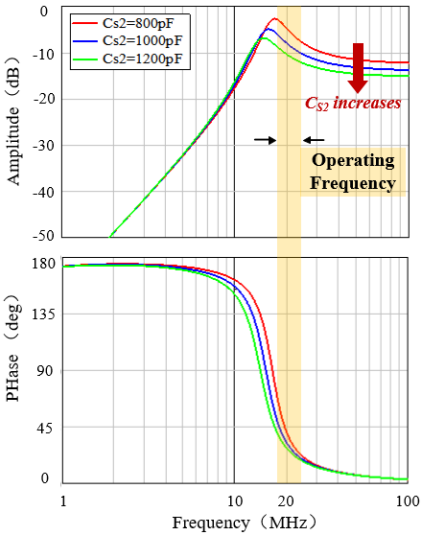

FIGURE 12. Bode diagram of feedback network with different C_{S2}.

phase shift. The greater the R_S, the more obvious the phase shift.

Theoretically, the proper phase can be obtained by adjusting R_S. But the growth of R_S also increases the driving loss. Hence, R_S in series should not be too large.

From the above analysis, it can be seen that compared with the traditional SRDC, the sensitivity of v_S to the components of the feedback network is greatly reduced. Proper amplitude and phase of v_S can be realized by adjusting L_S, C_{S1}, C_{S2}, and R_S. This makes circuit calibration much easier.

C. PARAMETER DESIGN METHOD

The transmission gain of the feedback network can be obtained by substituting $s = j\omega$ into (3):

$$\left|\frac{v_S}{v_{ds\_SR}}\right| = \left|\frac{-\omega^2 L_S C_{S1}}{1-\omega^2 L_S(C_{S1}+C_{S2})+j\omega R_S(C_{S1}+C_{S2})}\right| \quad (5)$$

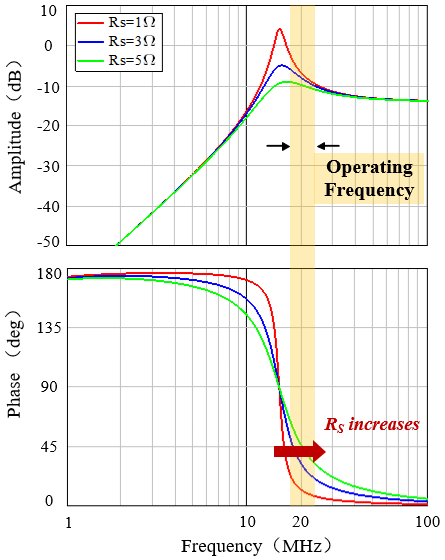

FIGURE 13. Bode diagram of feedback network with different R_S.

By sorting out (4), the identity can be derived as follows:

$$\omega R_S(C_{s1}+C_{s2})=\left[1-\omega^2 L_S(C_{s1}+C_{s2})\right]\tan(\pi-\theta) \quad (6)$$

The expression of L_S can be derived by substituting (6) into (5):

$$L_S=\frac{K}{\omega^2\left[K(C_{s1}+C_{s2})-C_{s1}\right]} \quad (7)$$

where

$$K=\left|\frac{V_s}{V_{ds}}\right|\sqrt{1+\tan^2(\pi-\theta)} \quad (8)$$

Combining (6) and (7), the expression of R_S becomes as follows:

$$R_S=-\frac{C_{s1}\tan(\pi-\theta)}{\omega(C_{s1}+C_{s2})\left[K(C_{s1}+C_{s2})-C_{s1}\right]} \quad (9)$$

From (6) and (7), it becomes obvious that for the determined gain and phase shift, L_S and R_S can be calculated when C_{S1} and C_{S2} are given.

At tens of MHz frequency, the capacitance and inductance are as low as pF and nH level, respectively. The parasitic parameters of traces and devices are in the same or close orders of magnitude. Therefore, it is important to minimize the loop area of the gate driver and pay attention to the grounding in PCB layout. For this reason, circuit debugging requires precise theoretical design guidance.

In addition, the chip used in the design has extremely low latency; and the comparator is eliminated. As the result, the converter can operate at very high frequency, while the chip delay can be compensated by fine-tuning the component parameters, which ensures the flexibility and convenience of the design.

IV. EXPERIMENTS

To verify the theoretical analysis, a 20 MHz prototype with 18 V input and 5 V / 2 A output is built. As shown in Fig. 14, the converter topology [31] contains an isolated Class Φ_2 inverter and a current-source Class E rectifier, where GaN devices are used at both Q_{main} and Q_{SR}. The air-core planar transformer [32] and the air-core inductor are also introduced. Q_{main} chooses the external driving mode, and Q_{SR} adopts the in-phase feedback SRDC with external capacitors. The experimental prototype is shown in Fig. 15.

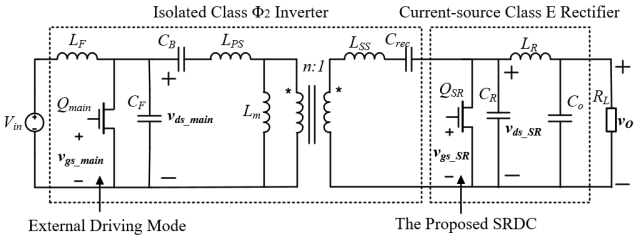

FIGURE 14. Isolated HFDRC.

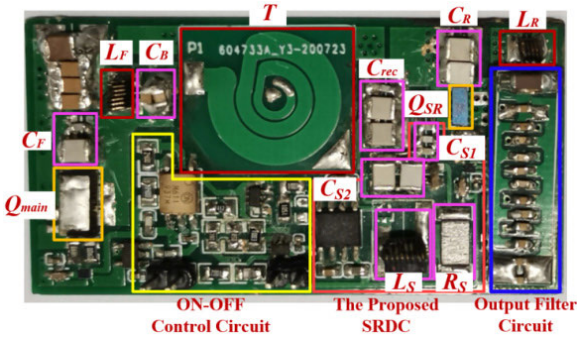

FIGURE 15. Experimental prototype.

The parameters of the SRDC are calculated with the proposed method in Section III C. The result is presented in Table 1. Table 2 exhibits the part numbers of Q_{main} and Q_{SR}. And the values of the main circuit components are shown in Table 3. Among them, L_{11}, L_{22}, and k are the parameters of the transformer equivalent to T model, which are obtained by finite element simulation. C_{ds} is the parasitic capacitor of Q_{main}.

TABLE 1. Parameters of proposed SRDC.

Parameter	Value
C_{S1}	227pF
C_{S2}	1047pF
L_S	82nH
R_S	3Ω

Fig. 16 shows the drain-source voltage of Q_{main}(v_{ds_main}), the gate-drain voltage of Q_{main} (v_{gs_main}), and the control signal output by optocoupler (v'_{ctrl}) under ON-OFF control

TABLE 2. Part numbers of Q_{main} and Q_{SR}.

Component	Part number
Q_{main}	GS61008T
Q_{SR}	EPC2015C

TABLE 3. Parameters of main circuit.

Parameter	Value
L_F	33nH
C_{ds}	250pF
C_F	810pF
C_B	0.6uF
C_{rec}	630pF
L_{11}	40.36nH
L_{22}	85.03nH
k	0.816
C_R	540pF
L_R	27nH
C_O	(20+0.1*12)uF

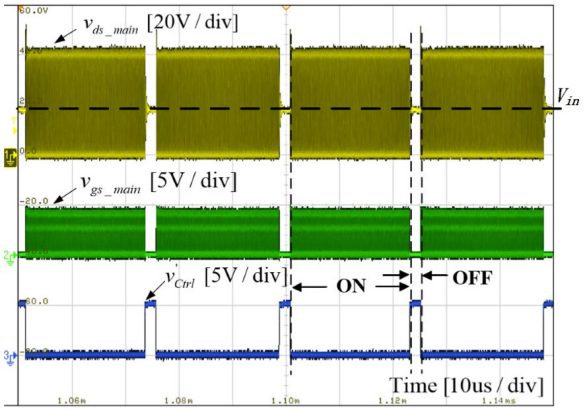

FIGURE 16. v_{ds_main}, v_{gs_main}, and v'_{ctrl} under ON-OFF control cycle.

cycle at full load. Fig. 17 shows v_{ds_SR}, v_{gs_SR}, and v_S under ON-OFF control cycle at full load. The ON-OFF control frequency of Q_{main} and Q_{SR} in these figures are both about 41 kHz, which means that Q_{main} and Q_{SR} cooperate well.

The noninverting input of the driver chip is enabled by v_{ctrl}. And v'_{ctrl} is in opposite phase with v_{ctrl}. When v'_{ctrl} is high, the driver chip no longer drives Q_{SR}; and the converter turns off. Meanwhile, v_{ds_SR} gradually reaches the output voltage (5V). When v'_{ctrl} is low, the driver chip is re-enabled and Q_{SR} continues to work at 20 MHz. Then, the converter turns on and quickly enters a steady state.

Fig. 18 shows v_{ds_SR}, v_{gs_SR}, and v_S within switching cycle. It can be seen that the delay of the driver chip is compensated by the feedback network. v_S is well-matched with the phase of v_{ds_SR} to control the driving timing, making Q_{SR} turn on and turn off accurately and maintain soft switch.

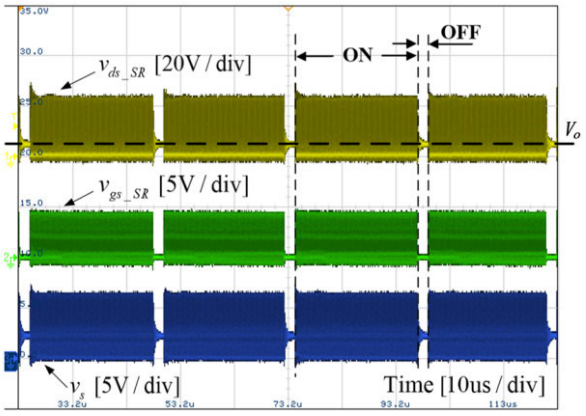

FIGURE 17. v_{ds_SR}, v_{gs_SR}, and v_S under ON-OFF control cycle.

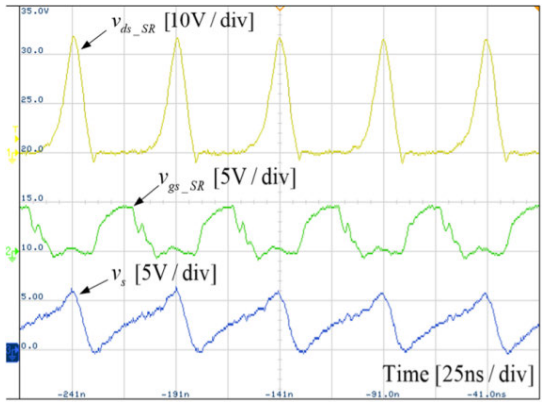

FIGURE 18. v_{ds_SR}, v_{gs_SR}, and v_S within several switching cycle.

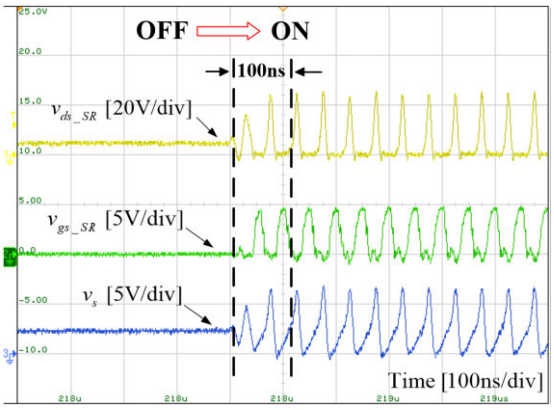

FIGURE 19. v_{ds_SR}, v_{gs_SR}, and v_S when converter starts up.

The switching of Q_{SR} under ON-OFF control requires fast dynamic response to establish a normal driving timing of soft switch. Fig. 19 and 20 show the waveforms of v_{ds_SR}, v_{gs_SR}, and v_S when the converter starts up and shuts down, respectively.

It can be seen that the time from the resonant working state to the steady-state working state is about 100 ns during the start-up process of the converter. When the converter shuts

TABLE 4. Properties comparisons of some typical high frequency topologies.

Topology	f_s	Input/output voltage	Output power	Isolation	Voltage stress	Efficiency
Proposed	**20MHz**	**18V/5V**	**10W**	**Yes**	**2.3**	**78.4%**
Synchronous Class Φ_2	10MHz	12V/5V	10W	No	3	79.5%
Isolated Class Φ_2	20MHz	12V/5V	10W	Yes	2.6	80%
Class E [33]	20MHz	36~54V/12V	24W	Yes	2.8	77.5%
Push-Pull	30MHz	30~36V/24V	50W	Yes	2.8	73.3%
SEPIC [34]	30MHz	15V/28V	25W	No	3.5	82.5%

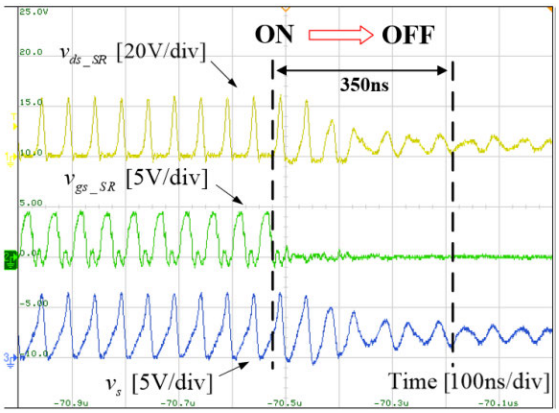

FIGURE 20. v_{ds_SR}, v_{gs_SR}, and v_S when converter shuts down.

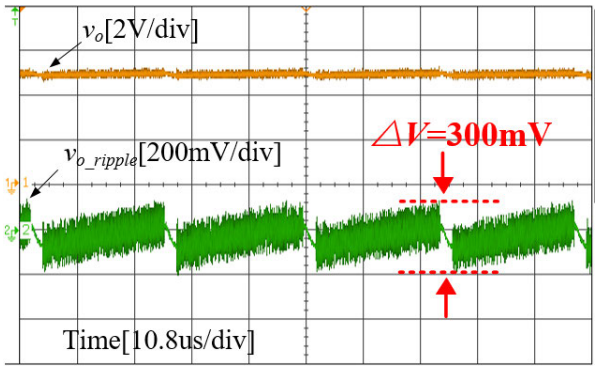

FIGURE 21. Output voltage of experimental prototype.

down, the whole process takes about 350 ns. After entering the steady state, the driving timing sequence is accurate to keep an efficient and reliable operation of the rectifier.

In the construction of an isolated power converter operating at MHz, the design of the inverter is based on the feasibility of the rectifier. Only when the rectifier and its driver circuit are reasonable and effective, the inverter and the whole prototype can work normally. Fig. 21 shows the output voltage waveform of the prototype at full load. The output voltage of the prototype is stable at 5 V. The ripple peak-to-peak is approximately 300 mV. The prototype can work steadily under ON-OFF control.

Table 4 depicts the property comparisons of some typical high frequency topologies. It can be seen that the proposed converter has the lowest switch drain-source voltage stress. Even working at such a high frequency and at such a large input-to-output voltage ratio, the converter still possesses a satisfactory efficiency.

V. CONCLUSION

Due to the shortcomings of oversensitive parameter adjustment and unstable feedback network, the traditional SRDC is not suitable for synchronous rectification based on GaN devices at tens of MHz. In this paper, a novel in-phase feedback SRDC with external capacitors which is suitable for GaN devices is proposed. The SRDC uses the external capacitors to sample the excitation source, and provides a stable and reliable driving signal by combining the self-resonant feedback network with the driver chip. Meanwhile, the operating frequency band is set behind the resonant point, which gives the feedback network plenty of gain margin and phase margin.

This paper thoroughly analyzes the operating principle and characteristics of the feedback network, and provides the detailed parameter design method. The experiment is carried out on a 20 MHz prototype with 18 V input, and 5 V/2 A output. The experimental result demonstrates that the proposed scheme can provide reliable and stable driving signal for synchronous rectification based on GaN at 20 MHz; and the prototype can work stably, which verifies the feasibility and effectiveness of the designed SRDC.

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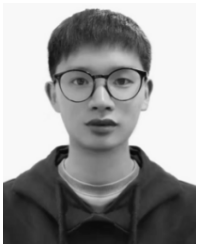

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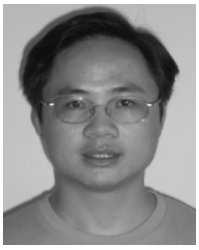

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