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A PWM Nie-Tan Type-Reducer Circuit for a Low-Power Interval Type-2 Fuzzy Controller

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ABSTRACT A novel Type-Reduction/Defuzzification circuit architecture for an analog interval type-2 fuzzy inference system is proposed. Based on the Nie-Tan type-reduction method, the circuit operates with current-mode inputs, representing the firing intervals of the rules created by the inference engine, and generating a PWM output. It is demonstrated that by selecting an appropriate number of consequents it is possible to create the PWM output directly, without the need for analog multiplier/divider circuits. This feature makes the circuit very simple, aiding in the design process, while the PWM output makes it suitable for controlling DC-DC converters, maximum power point trackers (MPPT) for energy generators, or other switching applications. It is designed to achieve very low power consumption, allowing its use in power restrained environments, such as energy harvesting systems. The circuit was designed using TSMC 0.18μm technology, in CADENCE Virtuoso software, and simulated for different combinations of input values, demonstrating its capabilities. It was also simulated as part of a type-2 fuzzy inference system with two inputs, nine rules, and firing intervals represented by currents within 0 and 10μA. The circuit was prototyped, and the experimental average power consumption was only 53.8μW, validating its low power consumption characteristic.

INDEX TERMS Analog integrated circuits, fuzzy hardware, interval type-2 fuzzy logic, low-power.

I. INTRODUCTION

Many low-power applications require non-linear control systems with enough robustness to work in the presence of uncertainties. Those applications can rely on fuzzy logic for a compact and relatively simple representation of complex relations. Several fuzzy inference systems have been proposed to control DC-AC inverters [1], DC-DC converters [2]–[5], active power filters [6], maximum power point trackers (MPPT) for wind energy conversion [7], solar photovoltaic generators[8]–[10], and energy harvesting systems [11], for example.

Depending on the application, however, a hardware implementation of such controllers must present a very low power consumption, especially in the case of the MPPT for energy harvesting, in which the efficiency of the whole system can be directly affected by the power consumption of the control circuit. One type of implementation that can fulfill this role, presenting great tolerance to uncertainties and the potential for low power consumption, is an analog interval type-2 fuzzy controller. An interval type-2 fuzzy inference system usually consists of five blocks: The Fuzzifier, the Inference Engine, the Rule Base, the Type-Reducer, and the Defuzzifier [12].

Previous studies demonstrated the potential of this kind of controller, presenting greater robustness to uncertainty [13] and being capable of representing systems with a smaller number of membership functions and rules when compared with an equivalent type-1 fuzzy inference system [12]. This is especially important to reduce total power in an analog implementation, given that fewer membership functions and rules mean fewer hardware components required to generate those functions [14]. This could mean a significant advantage for type-2 hardware implementations in terms of power. The use of analog hardware also presents the benefit of not requiring A/D and D/A converters, as would be the case in a digital implementation, further assisting in the reduction of power

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consumption. There is, however, the difficulty of an increased computational cost associated with the type-reduction/output processing, that can spoil any obtained power gain, preventing practical implementations.

A method of type-reduction for interval type-2 inference systems, proposed as a closed-form alternative to the iterative algorithms (such as the Karnik-Mendel [15] and Wu-Mendel methods [16]), is called the Nie-Tan method (NT) [17] and is particularly well suited for analog hardware implementations. The accuracy of the NT method has been demonstrated [18], and while some analog controllers have already employed it using current-mode multiplier/divider circuits [19]–[21], the design process of multiplier/dividers must deal with several non-linear effects, such as mismatch and channel-length modulation, that can degrade the performance of the circuit.

Given the need for low-power controllers in switching applications, such as energy harvesting systems, the circuit proposed in this work aims to demonstrate that it is possible to conceive a simple analog architecture capable of implementing the complete expression that represents the NT type-reduction with current-mode inputs (representing the firing levels from the inference engine), directly creating a PWM output without multiplier/divider circuits or other additional components.

The paper is organized as follows: Section II presents the Type-Reducer analog hardware considerations and the proposed architecture is discussed. Section III presents the simulation results under different conditions, including the results as part of a complete type-2 fuzzy inference system. The experimental results which were obtained with the prototyped IC are shown in Section IV, followed by the conclusion in Section V.

II. TYPE-REDUCTION PWM ARCHITECTURE

The standard type-reduction method, known as the Karnik-Mendel method (KM) is an iterative algorithm that aims to obtain both the smallest and the largest centroids of the embedded type-1 fuzzy sets and considers the average of both values as the crisp, defuzzified output [15].

Other methods have been proposed to improve the algorithm's performance, such as the Wu-Mendel (Extended Karnik-Mendel) method [16] and the Uncertainty bounds method [22], but the main issue remains that real-time and embedded systems may not have enough speed to depend on an iterative or mathematically complex process to decide the output value [23]. Also, very low-power applications need an implementation that is accurate enough to operate properly, but as simple as possible to minimize power consumption. One possible approach to achieving this goal is through analog hardware. The representation of fuzzy values by analog variables is a natural choice, since they are continuous, by definition. The inherent ambiguity of fuzzy logic offsets the accuracy limitations of an analog implementation [24].

Analog computations, however, are only feasible if in a closed form, i.e. not an iterative process. For that, the NT method is especially well-suited, since it provides a simple, closed-form expression, dependent only on the rules' activation levels and the consequents' centroids. The Nie-Tan method consists of taking the average of the upper and lower firing levels associated with each consequent before performing a center of sets or zero-order TSK defuzzification [17]. Mathematically, this corresponds to applying (1) to each firing interval obtained by the inference engine and then performing the operation in (2).

$$\mu^*(x) = \frac{\bar{\mu}(x) + \underline{\mu}(x)}{2} \tag{1}$$

$$u(x) = \frac{\sum_{i=1}^{N} \mu_i^*(x) \cdot y_i}{\sum_{i=1}^{N} \mu_i^*(x)} \tag{2}$$

The variable $u(x)$ represents the crisp output of the system, while $\bar{\mu}(x)$ and $\underline{\mu}(x)$ represent the upper and lower firing levels associated with each consequent, in a system with N consequents with values y_i. The variable $\mu^*(x)$ stands for the average of upper and lower firing levels. Combining (1) and (2), a single expression for type-reduction/defuzzification can be obtained, as shown in (3).

$$u(x) = \frac{\sum_{i=1}^{N} \left(\bar{\mu}_i(x) + \underline{\mu}_i(x)\right) \cdot y_i}{\sum_{i=1}^{N} \bar{\mu}_i(x) + \underline{\mu}_i(x)} \tag{3}$$

Analog type-2 fuzzy controllers found in the literature generally implement the expression in (3) with multiplier/divider circuits operating in current-mode [19], [20]. Equation (3) is very similar to a Center-of-Sets defuzzification, and most type-1 analog defuzzifiers also operate with multiplier/divider circuits in current-mode [25], [26], voltage mode [27], and some with current-input and voltage-output circuits [28]–[30]. The current-mode implementation has the advantages of a higher dynamic range and simpler implementation of the addition operation. Multiplier/divider circuits operating in current-mode and with MOS transistors in the saturation region depend on the geometric-mean/squarer circuits to generate the result, which can be very susceptible to mismatch, channel length modulation, and other effects that disturb/modify the quadratic model, thus complicating the design process. Multiplier/divider circuits that operate in weak-inversion have been proposed [31], and though they have low-power consumption, they are even more prone to suffer from mismatch and also tend to present lower speeds [32]. A different approach could be useful to facilitate the use of fuzzy inference systems in practical power-constrained systems.

Many applications, such as the MPPT and DC-DC converter examples cited in the Introduction, use a PWM signal to control the system. In order to use existing analog type-reducer/defuzzifier architectures in fuzzy controllers for this kind of system (in which the output of the fuzzy inference system represents the duty cycle of the PWM signal), additional circuits would be necessary to convert a current/voltage into a PWM equivalent. By making the output processing stage of the fuzzy system generate a PWM signal directly, without the need for additional components, both a power

reduction and a circuit simplification can be achieved. The idea of using PWM signals directly during the fuzzy inference process has been applied by Tombs *et al.* [33] in an architecture where the membership values of type-1 fuzzy sets, represented by currents, are converted to PWM signals by comparing the integrated voltage with a fixed reference ramp. The inference engine in that architecture is significantly simplified, being performed only by AND gates that effectively implement the minimum operation. The main disadvantage in doing this is that defuzzification becomes too complex. A transconductance amplifier and an integrator are used for multiplication, and a successive approximation logic circuit and D/A converter are used for division, in a strategy that is not suitable for low-power implementations. Also using PWM signals, the work by Alarcon *et al.* [34] creates a PWM output for a type-1 defuzzifier by implementing the division between two currents, and it assumes the multiplications between the currents that represent the firing levels and the consequents are performed by a previous multiplier circuit.

In this context, the architecture for the type-reducer/defuzzifier stage of a type-2 fuzzy controller proposed in this work receives the firing intervals coming from the inference engine in current-mode and makes the conversion directly into a PWM output signal. It is demonstrated that, for a given number of consequents, a simple structure can implement the complete equation in (3) without any multiplier/divider circuits. This is a reasonable design choice, given that controllers with a small rule-base are easier to design, entail simpler hardware (low power), and also present good performance, sometimes even better than systems with a larger rule-base [12], [35], [36].

The operating principle of the proposed architecture is based, as in [34], on the implicit division present in the PWM conversion process. Section A explains this process while Section B shows how, under certain conditions, it can be used to yield the complete type-reduction/defuzzification expression. Section C details the circuit designed to implement the proposed strategy.

A. PWM DIVISION

Usually, a PWM signal is generated by comparing the variable with a fixed reference ramp. If this reference is also dependent on a second variable, the PWM signal can represent the result of the division operation between these two variables, coded in the fraction of the total cycle time spent on the high level. The variables of interest in this implementation are assumed to be currents representing the firing intervals associated with each consequent of the type-2 fuzzy inference system. Therefore, a division between two analog currents is necessary and can be performed by integrating the two currents in sequence and comparing the voltages as illustrated in Fig. 1.

Assuming that the currents change little during each period, i.e. they remain approximately constant, the expression for crossover voltage v can be written as a function of two currents i_1 and i_2, as shown in (4) and (5).

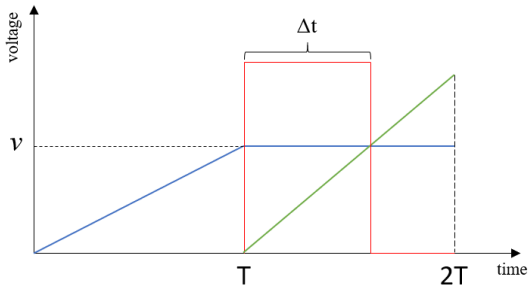


FIGURE 1. PWM division of two currents by integration and comparison of voltages.

$$v = i_1 \cdot T / C \tag{4}$$

$$v = i_2 \cdot \Delta t / C \tag{5}$$

The capacitance for both integrators is C, the period is T and the time between the beginning of the second current integration and the voltage crossover is Δt. Combining (4) and (5) into (6), the division between i_1 and i_2 is encoded in the time fraction $\Delta t/T$.

$$\Delta t = \frac{i_1}{i_2} \cdot T \tag{6}$$

The fact that this result is available for half of the total time required to obtain it is used in favor of the architecture, as explained in Section B.

B. TYPE-REDUCER/DEFUZZIFIER

If one makes the assumption that three consequents are used in the system (aiming at an inference process with a nine-rule MacVicar-Wheelan rule-base[36]) and named N, Z, and P, then the complete NT Type-reduction/defuzzification expression in (3) can be written as in (7).

$$u = \frac{\left(\bar{\mu}_N + \underline{\mu}_N\right) \cdot y_N + \left(\bar{\mu}_Z + \underline{\mu}_Z\right) \cdot y_Z + \left(\bar{\mu}_P + \underline{\mu}_P\right) \cdot y_P}{\bar{\mu}_N + \underline{\mu}_N + \bar{\mu}_Z + \underline{\mu}_Z + \bar{\mu}_P + \underline{\mu}_P} \tag{7}$$

Rewriting the term corresponding to the consequent Z and grouping upper and lower consequents, as in (2), an equivalent expression is obtained, as shown in (8).

$$u = y_Z + \frac{\mu_N^* \cdot y_N + \left(-\mu_N^* - \mu_P^*\right) \cdot y_Z + \mu_P^* \cdot y_P}{\mu_N^* + \mu_Z^* + \mu_P^*} \tag{8}$$

If the consequents' values y_N, y_Z, and y_P are chosen to be 0, 0.5, and 1, to reflect the full range of possible duty cycle values, then the output becomes (9).

$$u = 0.5 + \frac{\left(-0.5\left(\bar{\mu}_N + \underline{\mu}_N\right) + 0.5\left(\bar{\mu}_P + \underline{\mu}_P\right)\right)}{\bar{\mu}_N + \underline{\mu}_N + \bar{\mu}_Z + \underline{\mu}_Z + \bar{\mu}_P + \underline{\mu}_P} \tag{9}$$

Expression (9) can be implemented as a PWM signal by combining two waveforms in sequence, as in Fig. 2. It corresponds to the division associated with the N consequent, from 0 to T, and with the P consequent from T to $2T$.

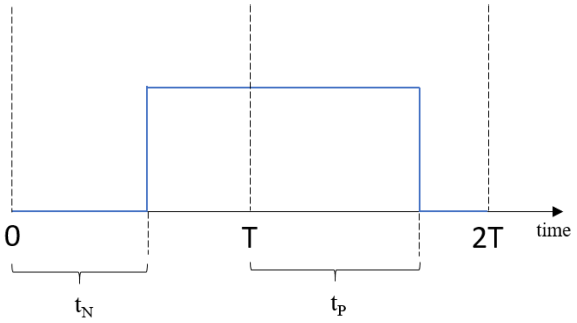


FIGURE 2. PWM output signal, formed by two periods, each corresponding to the N and P terms of the full NT type-reduction/defuzzification expression.

The duty cycle associated with Fig. 2 is described in (10).

$$u = \frac{T - t_N + t_P}{2T} \tag{10}$$

Time intervals t_N and t_P are obtained by PWM division, as described in Section A, and therefore have the values described by (11) and (12), respectively.

$$t_N = \frac{i_N}{i_N + i_Z + i_P} \cdot T \tag{11}$$

$$t_P = \frac{i_P}{i_N + i_Z + i_P} \cdot T \tag{12}$$

At each period T, individual currents i_N and i_P are compared to the sum of all currents representing the firing intervals, and the results are intercalated at the output, with an inverted signal for the N portion of the signal. Combining (10)-(12) results in (13).

$$u = 0.5 + \frac{(-0.5 \cdot i_N + 0.5 \cdot i_P)}{i_N + i_Z + i_P} \tag{13}$$

The expression obtained in (13) is equivalent to (9), given that currents i_N, i_Z and i_P represent the sum of upper and lower firing levels of each consequent as determined by the inference engine. To form the desired PWM output, with the two periods associated with consequents N and P, the division process detailed in Section A is performed as shown in Fig. 3.

Voltages V_N, V_P, and V_S are obtained respectively by the integration of the currents i_N, i_P, and of the sum of all currents $(i_N + i_Z + i_P)$. The control signals required to set the period T (EN) and to reset each of the capacitors at the appropriate time (RST, RN, and RP) are also shown in Fig. 3.

C. CIRCUIT ARCHITECTURE

The proposed architecture requires three independent capacitors to integrate each current. Wide-swing current mirrors are used to feed the integrators, and transmission gates control which currents are injected during each part of the cycle. Simple voltage comparators are used to implement the division corresponding to each half of the period, and transmission gates switch between them to create the output signal. Fig. 4 illustrates the proposed circuit architecture. Signals EN and

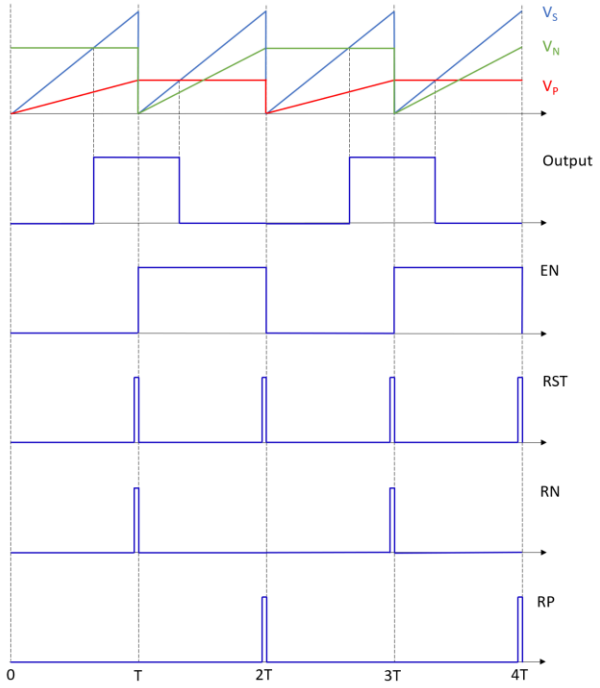


FIGURE 3. The waveform of all signals involved in the generation of the PWM output in the proposed method.

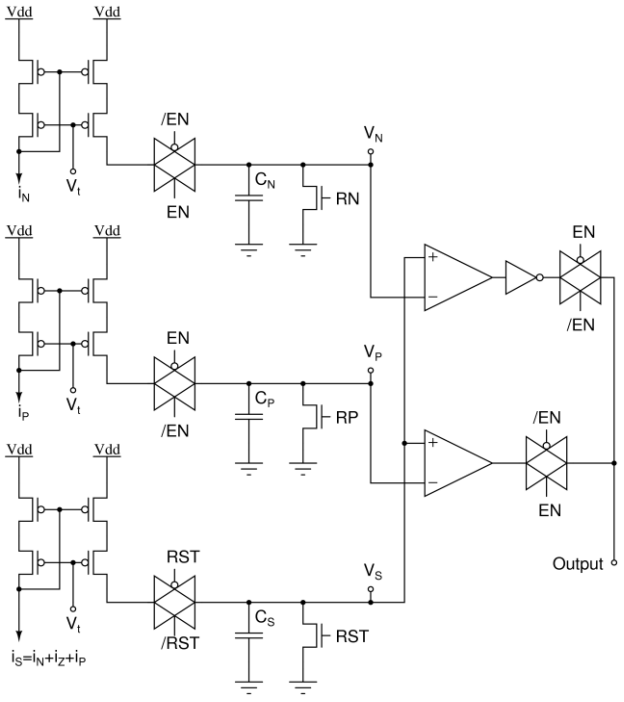


FIGURE 4. Proposed output processing circuit architecture.

RST are control inputs, and signals RN and RP are generated internally as /EN&&RST and EN&&RST, respectively. While EN is in the HIGH state, the capacitors CN and CS are charging, whereas the capacitor CP is not. Its voltage VP is held constant and is compared with the voltage VS to generate

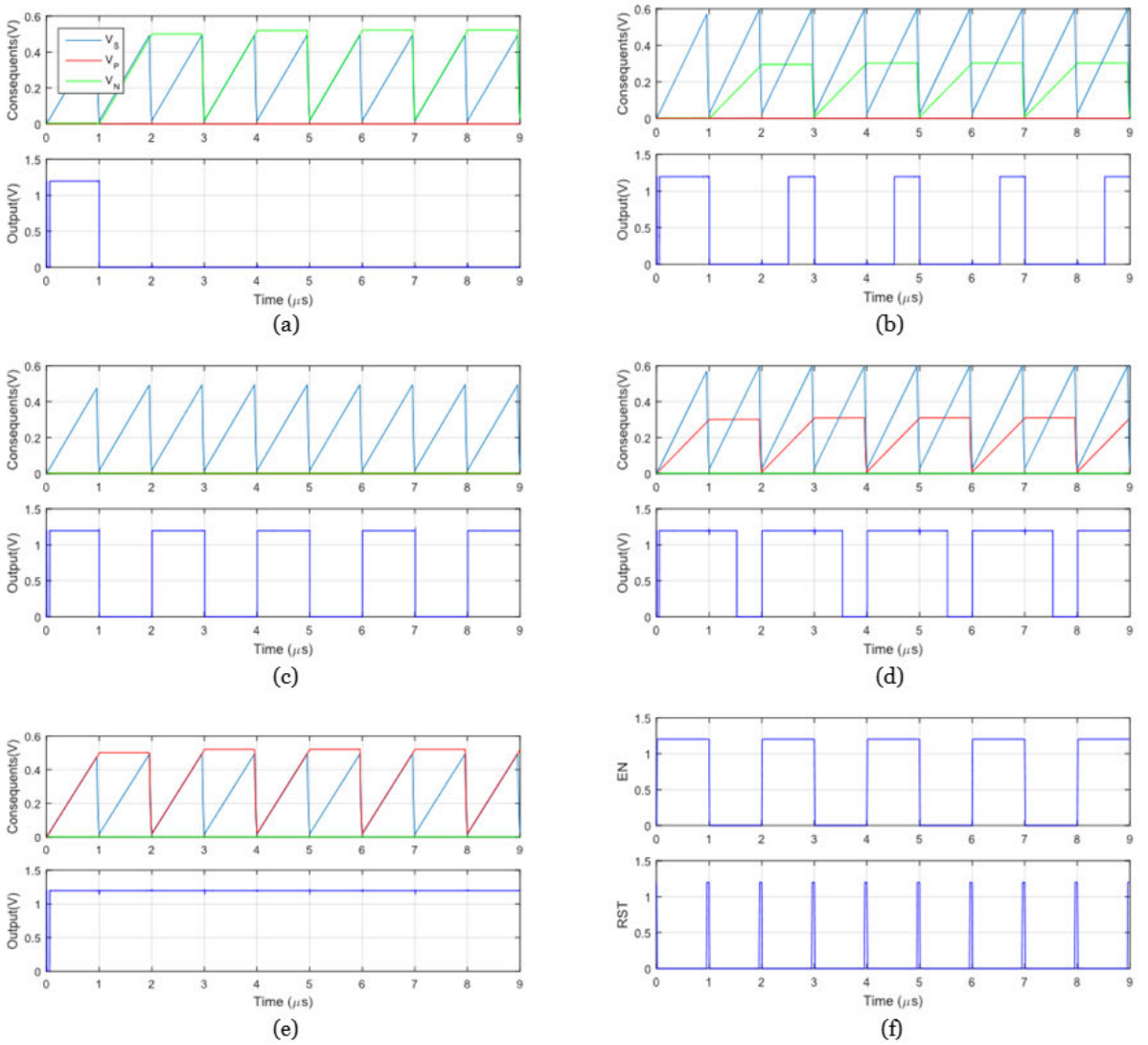


FIGURE 5. Simulation results for different combinations of input currents, as defined in Table 2. (a) Output with 0% Duty cycle. (b) Output with 25% duty cycle. (c) Output with 50% duty cycle. (d) Output with 75% duty cycle. (e) Output with 100% duty cycle. (f) Control signals EN and RST.

the part of the output signal associated with consequent P. When EN switches to the LOW state, capacitors CP and CS reset and start charging again, while capacitor CN maintains its voltage VN constant, to be compared with VS, generating the other part of the output, associated with consequent N. When EN switches back to HIGH, capacitors CN and CS reset, and the cycle restarts. The voltage comparators are high-gain differential amplifiers, designed to work with low voltage and low bias current in order to achieve low power consumption.

TABLE 1. Parameters defined for all simulations.

Parameter	Value
T	1μs
μ^*_{MAX}	10μA
C	20pF
RST	70ns
V_{DD}	1.2V

III. SIMULATION RESULTS

The proposed circuit architecture was designed with TSMC 0.18μm technology and simulated using Cadence Virtuoso software. The parameters common to all tests are specified in Table 1.

To verify the operation in the range of possible duty cycles, from 0 to 100%, different combinations of input currents were tested, as described in Table 2. The average power consumption obtained for each case is also displayed in Table 2 and the simulation results are as shown in Fig. 5. For each input

TABLE 2. Input currents combinations and corresponding duty cycle and power consumption.

i_N (μA)	i_Z (μA)	i_P (μA)	i_S (μA)	Duty Cycle	Power (μW)
10	0	0	10	0%	48.35
6	6	0	12	25%	45.05
0	10	0	10	50%	30.05
0	6	6	12	75%	44.33
0	0	10	10	100%	46.91

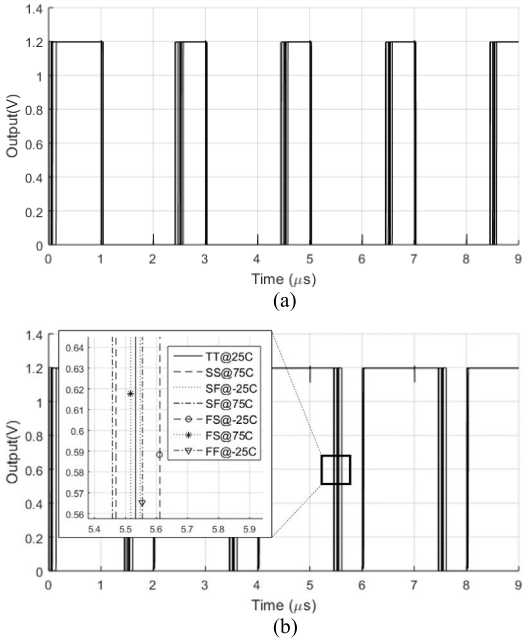


FIGURE 6. Corner analysis. (a) Duty cycle equal to 25%. (b) Duty cycle equal to 75% and detail identifying corner/temperature combinations tested.

combination, the voltage integration signals V_N, V_P, and V_S are also shown. The waveforms are according to the designed behavior explained in Section II and illustrated in Fig. 3. Importantly, as shown by the simulation results, the charge injection effect could be neglected in this implementation due to the fact that the load capacitances are much larger than the gate to drain capacitances of the devices used in the switches.

To guarantee the robustness of the circuit against process variations, a corner analysis was performed for different corners under different temperature conditions. The output results for the cases with duty-cycle equal to 25% and 75% are shown in Fig. 6. These two cases present the largest error, up to 3.5%, which is certainly small enough for practical fuzzy implementations, where this and other sources of uncertainty can be treated by adjusting the input membership functions accordingly.

Fig. 7 also shows the histogram of the Monte Carlo simulation results, performed for each case in Table 2. The plot groups the error to the nominal case in bins with a size

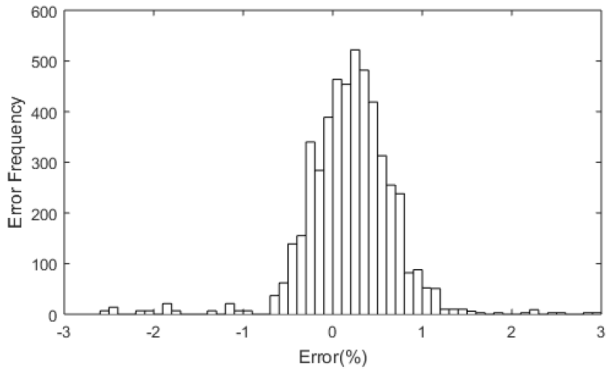


FIGURE 7. Histogram of the monte carlo analysis.

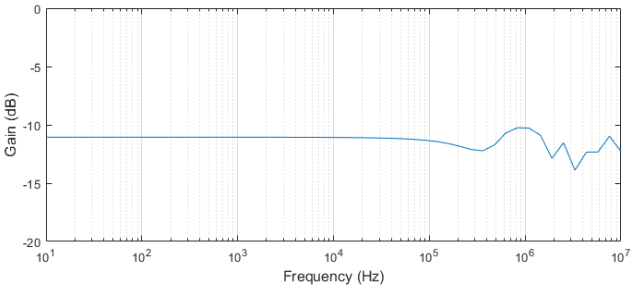


FIGURE 8. Power supply noise rejection at the output (10Hz to 10MHz).

equal to 0.1%. The average error is 0.22% and the standard deviation is equal to 0.51%. Both Corner and Monte Carlo results reflect the robustness of the circuit against process variations.

In order to verify the circuit's immunity to power supply noise, a simulation was performed to obtain the gain at the output for different frequencies (ranging from 10Hz to 10MHz).

Fig. 8 shows that the power supply noise is attenuated by about 10dB with respect to the output terminal, demonstrating that the circuit is capable of dealing with power supply noise.

Another simulation was conducted, this time taking into consideration a complete type-2 fuzzy inference system. It was implemented in order to test the proposed output stage operating in a system with a MacVicar-Wheelan Rule Base. Assuming a system with two inputs, each one associated with the proposed type-2 membership functions shown in Fig. 9, and with the rule-base described in Table 3 (with antecedents N1, Z1, P1, N2, Z2, and P2, and consequents N, Z, and P), it is possible to mathematically find the ideal output of an NT type-reducer/defuzzifier.

The inference process uses MIN/MAX operators as t-norm and t-conorm, respectively. Fig. 10 shows the ideal output in terms of the duty cycle as a function of the two inputs.

Considering an inference engine that outputs the firing intervals of the consequents in current-mode, in the range [0,10μA], such as in [14], [19], [37], it is possible to simulate the response of the proposed circuit and similarly plot its output as a function of the two inputs of the system. The result

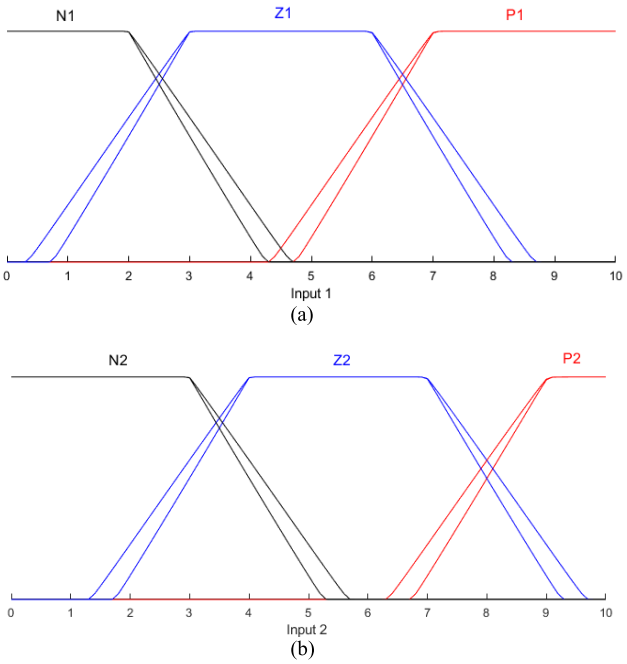


FIGURE 9. Input membership functions of a type-2 fuzzy inference system with two inputs, labeled (a) Input 1 and (b) Input 2.

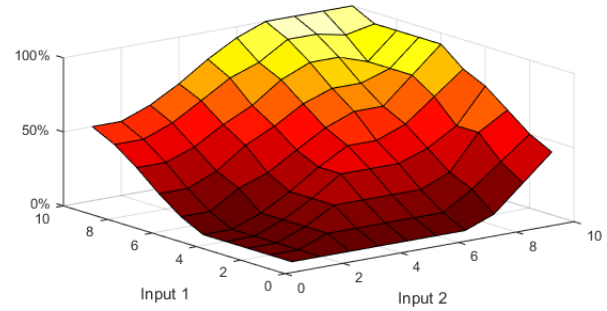


FIGURE 10. Duty cycle of the PWM output of an ideal type-2 fuzzy inference system.

TABLE 3. Fuzzy rule base with two inputs, nine rules, and three output consequents.

		Input 2		
		N2	Z2	P2
Input 1	N1	N	N	Z
	Z1	N	Z	P
	P1	Z	P	P

is shown in Fig.11, as well as the error when compared to the ideal case.

The power consumption corresponding to the output surface was simulated as well, and the result was plotted in Fig.12. The average power consumption was equal to 51.4μW, the comparator circuits are responsible for about 10% of that value (5.5μW), while the current mirrors feeding the capacitors during the charging process are responsible for

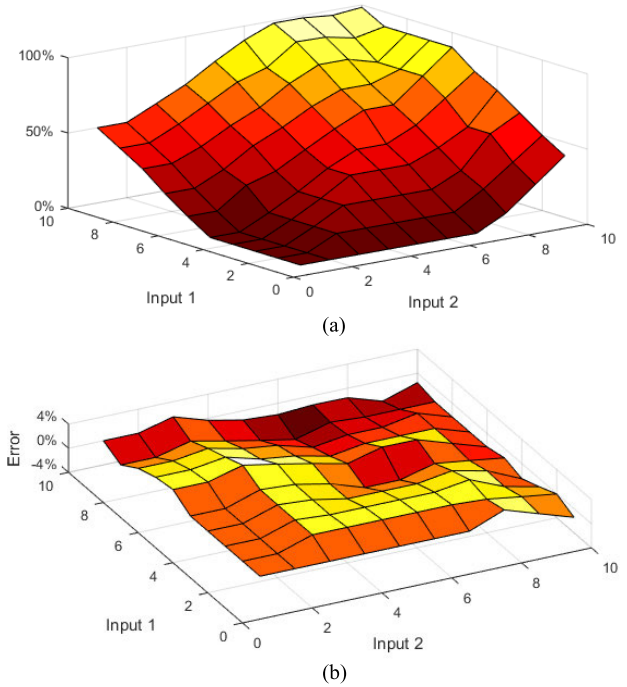


FIGURE 11. Simulation result of the example type-2 fuzzy inference system using the proposed NT Type-reducer/defuzzifier circuit. (a) Duty cycle of the PWM output. (b) Error in comparison to the ideal output.

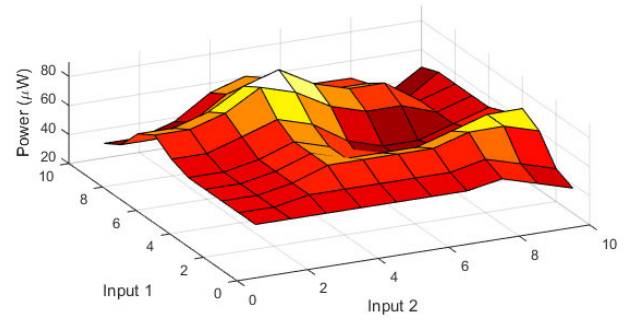


FIGURE 12. Simulation results of the power consumption surface as a function of the system's inputs.

the remaining 90%. In the worst case, the maximum power was equal to 81.6μW.

IV. EXPERIMENTAL RESULTS

The type-reduction/defuzzifier circuit with PWM output, as described in Section II and simulated in Section III, was manufactured using TSMC 0.18μm technology, in cooperation with IMEC, in a multi-project wafer (MPW) run, which is part of the mini@sic program of Europractice-IC. The layout of the proposed circuit and the micrograph of the testing chip are shown in Fig.13. Common analog layout techniques (such as interdigitation in the current mirrors and comparators) were employed to prevent mismatch and other non-ideal effects [38]. Measurements were performed with input current values as in Table 2. The output results have

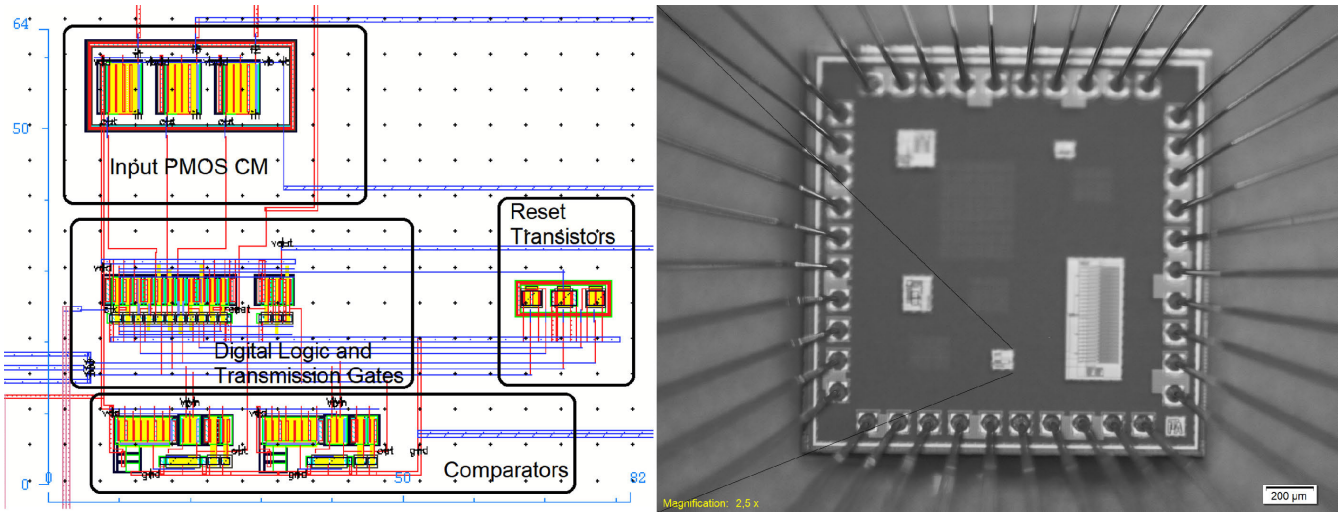


FIGURE 13. The layout of the proposed output processing circuit with an area of 64 μm × 82 μm and the micrograph of the testing chip.

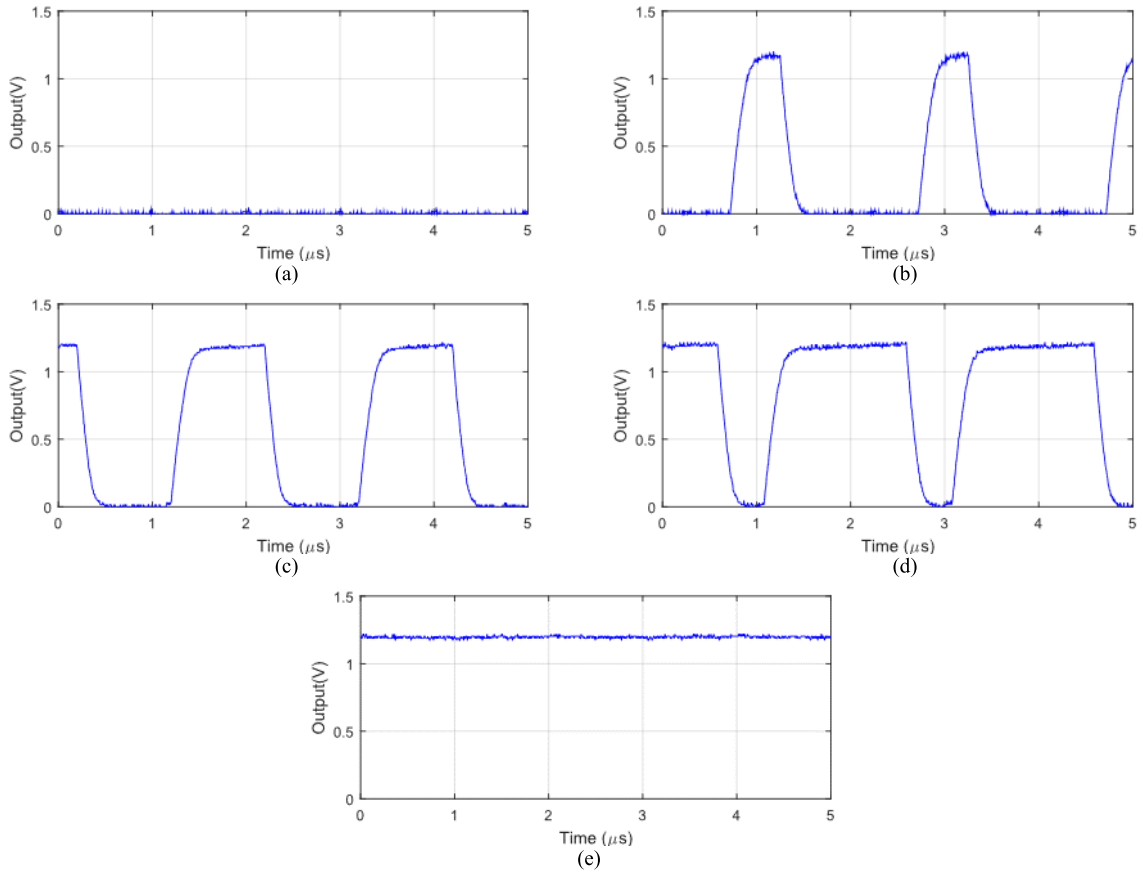


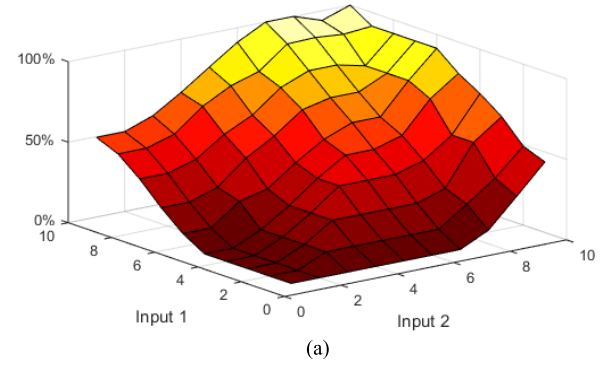
FIGURE 14. Experimental results for different combinations of input currents, as defined in Table 2. (a) Output with 0% duty cycle. (b) Output with 25% duty cycle. (c) Output with 50% duty cycle. (d) Output with 75% duty cycle. (e) Output with 100% duty cycle.

duty cycles as shown in Fig. 14, which are consistent with the values expected from Table 2.

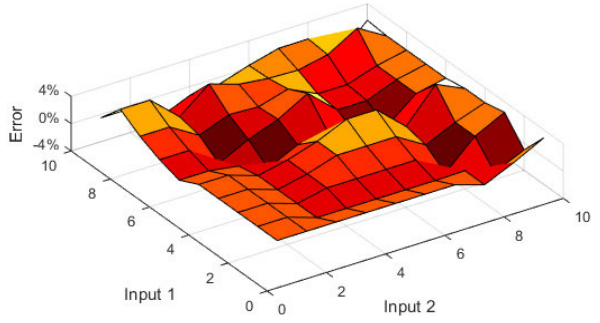
The duty cycle was also measured considering a complete type-2 fuzzy inference system (i.e. the output duty cycle for each combination of the input pair of the complete system), by feeding the firing intervals of the inference engine as described in Section IV to the output processing circuit. Those results were plotted in Fig. 15. The experimental error

TABLE 4. Comparison between possible type-reduction/defuzzification strategies in hardware.

	This Work	[39]	[40]	[41]	[19]	[20]	[42]	[25]	[26]
Technology	0.18µm	0.5µm	0.18µm	0.18µm	0.18µm	0.18µm	0.35µm	0.18µm	0.35µm
Area	64µm x 82µm	150µm x 140µm	600µm^2	625µm^2	0.028mm^2	0.32mm^2	350µm x 300µm	84µm x 36µm	0.1mm^2
Supply Voltage	1.2V	1.5V	1.2V	1.4V	1.8V	3.3V	-	2V	-
Speed/ Frequency	0.5MHz	18MHz	79.6MHz	173MHz	6.37MHz	20MHz	41.3MHz	20MHz	16.6MHz
Error	1.4%	-	0.75%	0.63%	-	-	-	1.08%	-
Power	53.8µW	120µW	60µW	340 µW	4.64mW	20mW	3.2mW	626µW	13.4mW
Purpose	Type-Reducer/ Defuzzifier	Multiplier/ Divider	Multiplier/ Divider	Multiplier/ Divider	Type-2 Analog Fuzzy Controller	Type-2 Analog Fuzzy Controller	Type-1 Mixed-Mode Fuzzy Controller	Type-1 Defuzzifier (Multiplier/ Divider)	Type-1 Analog Fuzzy Controller
Sim./Exp.	Exp.	Exp.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.



(a)



(b)

FIGURE 15. Experimental result of the example type-2 fuzzy inference system using the proposed NT Type-reducer/defuzzifier circuit. (a) Duty cycle of the PWM output. (b) Error in comparison to the simulated output.

is also plotted in Fig. 15(b), showing that the corresponding root mean square error is equal to 1.4%, and in the worst case the error is smaller than 4%, which is within the expected margin and certainly acceptable in a practical implementation of a fuzzy system.

The power consumption corresponding to the output surface was also measured, and the result was plotted in Fig.16. The measured average power consumption was equal to 53.8μW, and the maximum power was equal to 86.5μW. The experimental power was about 3μW larger than the simulated values due to a larger output capacitance.

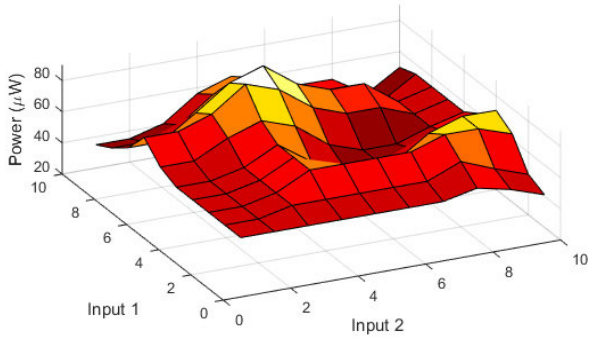


FIGURE 16. Experimental results of the power consumption surface as a function of the system's inputs.

The results demonstrate the proposed circuit's capability to operate as an NT Type-reducer/defuzzifier for PWM applications with a simpler architecture and with small power consumption, even smaller than the individual power consumption of analog multiplier/divider circuits, such as [39] with 120μW and [40] with 60μW, as shown by the comparison in Table 4.

This comparison must also take into account the fact that at least two current-mode multiplier/divider circuits and a PWM generator circuit would be needed to create an output equivalent to the one generated by the proposed architecture. Table 4 also includes the analog type-2 fuzzy controllers in the literature that implement the Nie-Tan type-reduction method, as well as three type-1 analog fuzzy circuits, emphasizing the low power feature of the proposed architecture.

V. CONCLUSION

A novel architecture for a type-reduction/defuzzifier circuit was proposed that generates a PWM output from current-mode inputs and does not depend on analog multiplier/divider circuits, thus greatly simplifying the design process and facilitating the use of analog type-2 fuzzy inference systems in real applications.

The type-reduction stage of a type-2 fuzzy inference system is usually a computationally-intensive process, presenting many challenges for an analog implementation. The Nie-Tan method presents a simple, closed-formed expression, that facilitates its realization in analog hardware. It was demonstrated that appropriately choosing the number of consequents allows the creation of a circuit that produces the output of the fuzzy system directly as a PWM signal. The circuit was tested as part of a complete interval type-2 fuzzy inference system, presenting an output error smaller than 4%. The fact that the proposed architecture does not require multiplier/divider circuits also reduces power consumption, as is demonstrated by the simulated and experimental results. The circuit was prototyped, presenting a measured power consumption of 53.8 μW with a power supply of 1.2V. The consumption is even smaller than that of a single analog multiplier/divider, of which at least two would be required, along with a PWM generator, to produce an equivalent output.

The PWM output makes the integration with DC-DC converters and other switching applications quite simple, and the low power consumption presented makes it suitable for small, embedded applications such as an energy harvester's MPPT system.

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