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Design and Analysis of InP/InAs/AlGaAs Based Cylindrical Surrounding Double-Gate (CSDG) MOSFETs With La_2O_3 for 5-nm Technology

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ABSTRACT The structural improvement and rapid production of InP, InAs (III-V, binary), and AlGaAs (III-V, ternary) compound semiconductor materials have invariably enabled its utilization in typical high-speed device applications. Using the electronic simulator tool, the ON- and OFF-state drain current (I_{ON}/I_{OFF}) performance of InP/InAs/AlGaAs High Electron Mobility Transistors (HEMTs) with Lanthanum Oxide (La_2O_3) as a dielectric material has been analyzed. Thereafter, a design of cylindrical surrounding gate MOSFET has been planned with this novel heterostructures. The InAs spacer (primary) layer is placed as per requirement below the source and drains the terminal to improve mobility. A heavily doped AlGaAs channel layer is employed beneath the primary layer, followed by the required layers. The given device gate length of $L_G = 5\ nm$, source-drain device length $L_{SD} = 0.15\ \mu m$ and $V_{GS} = V_{DS} = 1\ V$ of InP/InAs/$Al_{0.53}Ga_{0.47}As$ HEMT having Equivalent Oxide Thickness (EOT) of La_2O_3 as *2 nm* (gate dielectric oxide), the measured values of maximum drain current ($I_{D,max}$), transconductance (G_m), Charge carrier density (ρ), and leakage current (I_{leak}) are $10\ mA/\mu m$, $12\ mS/\mu m$, $1.5\ C/cm^3$, and 0.03 $\mu A/\mu m$, respectively. The electrostatic potential (φ) and electric field (E) are $2.58\ V$ and $-47.12\ V/\mu m$ are obtained when $V_{DS} = 1\ V$. This proposed design enhances the heterostructures immune to all the Short Channel Effects (SCEs) in the RF range that can be used in low power circuits design. Furthermore, the rotational cylindrical structure paves the way for a lesser board area to be occupied to reduce heat generation.

INDEX TERMS Charge carrier density, composite channel, CSDG MOSFET, electrostatic potential, high-ⱪ dielectric, nanotechnology, VLSI.

I. INTRODUCTION

Over the last few decades, the InP and AlGaAs semiconductor materials have excellent electron transport characteristics, making them promising options for future nanoscale CMOS. Indium Phosphide (InP) is a direct band-gap III-V compound semiconductor material with a short carrier time. It is primarily employed for lasers, sensitive photo-detectors, and modulators at *1550 nm* wavelength, which is widely used in media communications. Due to its operation with GHz frequency range and excellent intrinsic properties, InP-based transistors are widely used in high-speed applications [1], [2]. Their applications include aerospace industries, high-speed fiber optics, and microwave communications [2]–[4]. Recent High Electron Mobility Transistors (HEMTs) are made with compound semiconductor (AlInN/AlGaN/GaN) materials that are extensively utilized for high-speed applications operating in the Ka-band between *26.5 GHz - 40 GHz* and in high power applications at the X-band frequencies between the *8 GHz* to *12 GHz*. The GaN is a semiconductor material with a wide band-gap (*3.6 eV*) similar to SiC and diamond, whose band-gap energy is *3.3 eV* and *5.5 eV*, respectively. These materials exhibit low intrinsic carrier concentrations at high temperatures of above *500* °. The sheet charge density, high carrier density, and mobility were considered for high power operations of AlInN/GaN Heterostructure FETs [3].

Feng *et. al.* [4] and Wong *et. al.* [5] have proposed two different structures for GaN HEMTs and named them Vertical Polarity Inversion Heterostructures (VPIH) and

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Ga polar Metal Insulator Semiconductor (MIS) HEMT, respectively. The VPIH structure predominantly utilizes an insulator interlayer to reduce gate interference. In E-mode devices, the N-polar GaN, with a reverse polarization field, is beneficial compared to Ga-polar GaN devices, which are at a disadvantage due to their low access resistance. The AlGaAs grown on the InP layer-base have aided in creating heterostructures and have been extensively researched and widely considered to be the best in matching the semiconductor's lattice constants. The original mobility enhancement methods and heterostructures were not remarkable at ambient temperature, but these structures exhibited promising results at a minimal temperature [6], [7]. To achieve ultra-high frequency applications, Kim *et. al.* [8] have focused on device structures and scaling methods. To enhance high-frequency operations, reduction in the gate length (L_g $<$ *50 nm*), improvement in the transportation of charge carriers either by applied electric field or concentration gradient, upgradation of Electrostatic Integrity Factor (EIF), reduction in the resistance and parasitic capacitance must be taken into consideration.

Fiegna *et. al.* [9] have analyzed that the SCEs can be controlled by considering various factors like device geometry, increased channel doping, fabricating a device with gate length (L_G) $<$ *100 nm,* and a thin channel to hold constricted coupling of gate potential with the channel potential. This makes it essential to analyze the effects of Single-Gate (SG) HEMT along with L_G parameter, the source to drain device length (L_{SD}), the material of the channel layer, the oxide layer, and its altered thickness. For the last few decades, amphoteric doping has been prominent in most III–V compound semiconductors. At temperatures between *700 °C - 900 °C*, the Silicon atoms act as the acceptors and donors after combining GaAs semiconductors with Arsenic and Gallium layers. Hence, the concentration of Silicon is an essential aspect of amphoteric doping. The surface driving force is powerful at critical doping concentration, such that the dopants drift to the surface faster than the rate of development and are not extended into the semiconductor. Hence, the high impurity concentrations are not permitted to reach an epitaxial growth limit. The n-type and p-type dopants of GaAs, InP semiconductors are Se, Sn, Ge, C, and Zn, respectively [8], [9].

Garcia *et. al.* [10] have analyzed the inertia, memory effects, and diffusion by doping Tellurium (Te) in the GaInP semiconductor. All these parameters depend upon doping profile and the surface growth of Te in the semiconductor. The doping profile matches δ-doping Dirac's delta functions when doped with III–V semiconductors. The δ-doping technique has several advantages such as the increase in the carrier concentration, vicinity between the channel and the gate conductor, a large gate Breakdown Voltage (BV), reduction of effects due to short channel, and increase in transconductance (G_m). The investigation of the doping profile with a thickness of few angstroms and a limited temperature below *550* °C had been carried out in previous years [11]–[14]. As a result of heavy doping, the narrow band-gap occurs in bipolar devices. Thus, the additional amount of doping strongly changes the Fermi level crossing bands at the forward bias junction of the Heterojunction Bipolar Transistor (HBT). This, in turn, changes the accumulation of charges in the devices and varies the thermionic and tunneling currents [15], [16]. The direct tunneling current depends upon the physical thickness and barrier height (h). Hence, the tunneling current is expressed as:

$$I \alpha V \,.\, \exp\left[-\frac{4\pi d\sqrt{2m.\phi_b}}{h}\right] \tag{1}$$

Since 2011, authors have designed Cylindrical Surrounding Double-Gate (CSDG) MOSFET [17], [18] and realized its various parametric analysis. An extension of these, the author's recent research [19] utilizes the La_2O_3, which is mainly suitable for high-frequency applications. The capacitance effect in 2D structures was estimated. The gate insulator of the high-ꝁ dielectric material (La_2O_3) layer plays a vital role. This distinctive material offers greater control over the applied gate voltage. The La_2O_3 layer oxide in the CSDG MOSFET improves the transistor sub-threshold controllability, and the simulation results clearly illustrate the parametric evaluation, the quantity of energy stored in the cylindrical MOSFET, and the associated electrical field in it.

To extend the author's recent research work of [19], this present research work has been enabled for HEMT design in low power applications. The stacking of several layers of nearby band-gap can enable the resultant heterostructures immune to SCEs and benefit with low power consumption with high-speed switching. This research work has been organized as follows: Section II discusses the basics of MOSFET based on high-ꝁ dielectric material between the gate and the channel. Section III elaborates the compound semiconductor materials used in the design of HEMTs and heterostructures. Section IV proposes the novel CSDG MOSFET using HEMT technology based on the high-ꝁ dielectric oxide. Section V has the qualitative analysis followed by the discussions. Finally, Section VI concludes the work and recommends the future aspect.

II. BASICS OF MOSFETs AND ITS DEVELOPMENTS BASED ON InP SEMICONDUCTORS

Several researchers proposed Al_2O_3 as the gate dielectric preferably in InGaAs III–V group semiconductor MOSFETs. Kim *et. al.* [20] illustrated that the channel in the InP quantum-well MOSFET is purely intrinsic and acts as a barrier between the channel and the dielectric gate layer. There are two types of InP-based MOSFETs, surface channel and buried channel MOSFETs. In these two devices, the movement of charge carriers is faster in buried channel MOSFETs than surface channel MOSFETs. This buried channel type MOSFET is considered as one of the notable MOSFET in next-generation CMOS technologies. The prevalence of high mobility in the buried channel MOSFETs is due to its thick InAs layer. Whereas the surface channel MOSFETs,

whose surface layer is rough due to the dielectric oxide layer, developed between the boundaries of the channel. The major drawback in the buried channel MOSFET is that the thickness of the InAs layer reduces the surface scattering and improves channel mobility. Therefore, the buried channel MOSFET shows superior transfer characteristics, resulting in better performance [21]–[23]. The charge density 'ρ' and state performance are superior in InGaAs MOSFETs than GaAs MOSFETs. There may be production losses when the gate dielectric interface is of poor quality and has high access resistance at the source and drain connections. Thus, the production can be improved by utilizing a low-impact self-aligned approach by introducing high-quality Aluminum Gallium Arsenide (AlGaAs) channels in InGaAs (MOSFETs). This approach has been used as a shadow mask on top of the T-gate for source and drain deposition. Excellent results are attained when considering the head size of the gate and the separation of *300 nm* between source and drain in *0.05-µm* technology. The fringing capacitance formed by the T-overlap gates with the source/drain areas acts as a drawback, and hence, this solution is not suitable for Very/Ultra Large Scale Integration (VLSI/ULSI) [24]–[27].

III. COMPOUND SEMICONDUCTOR WITH HIGH-κ DIELECTRIC OXIDE MATERIALS

Aluminium Gallium Arsenide (also known as Gallium Aluminum Arsenide) ($Al_xGa_{1-x}As$) is a semiconductor material with a higher band-gap than GaAs and a nearly identical one lattice constant. The energy band-gap depends upon the value of aluminum content 'x'. The band-gap energy of $E_g = 2\ eV$ and a gap wavelength of $\lambda_g = 620\ nm$ is obtained by adding *53 %* aluminum content and *47 %* Ga content into the AlGaAs semiconductor. The material properties of AlGaAs compared to the attributes of InP are tabulated in Table 1 (appendix). In the manufacturing of InP HEMTs, Si deactivation plays an important role. It primarily deactivates Si impurities in InAs layers. The complete system output degrades when carrier concentration reduces [28], [29]. AlGaAs is a wide band-gap semiconductor material that outperforms other compound materials in the HEMT design. Unfortunately, the materials with a higher band-gap than the AlGaAs exhibit unstable properties in the HEMT construction, as shown in Fig. 1. Thus, AlGaAs act as an appropriate material for design purposes.

Zhao *et al.* [30] and Kim *et al.* [31] have analyzed the inversion-mode surface channel III–V MOSFETs through several dielectric oxides like Al_2O_3 and HfO_2, HfAlO and ZrO_2 or La_2O_3 dielectrics. Ga_2O_3 dielectrics from Molecular Beam Epitaxy (MBE), Interfacial Passivation Layer (IPL) using Si, Ge, Si_xN_y, Ge_xN_y, or Al_xN_y and high-κ gate stack and HfLaO are chosen to exhibit properties with high dielectric constant (ε), low OFF current (I_{OFF}) good thermal strength, insignificant dispersion, high breakdown voltage, and good consistency. The comparison among each oxide led to achieving the desired results [32]–[35]. The Hafnium-Lanthanum gate insulator has amorphous

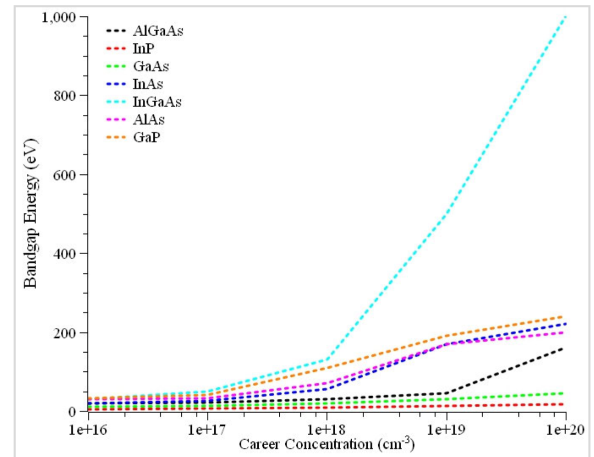


FIGURE 1. Band-gap in III-V semiconductors.

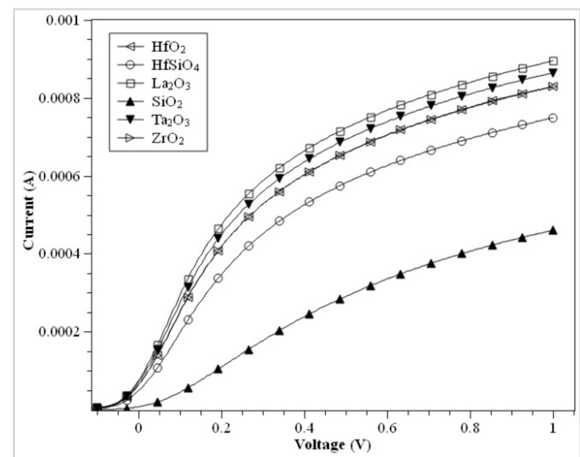


FIGURE 2. Drain characteristics of E- mode AlGaAs MOSFETs with various oxide concentrations.

properties processed with thin-film oxide for high stable performances while operating at low voltage. The mixture of Hf and La exhibits excellent dielectric properties and high crystallization temperature (up to *900 °C*), reduces the leakage current, and improves the high dielectric constant, which is more suitable for future device technologies.

A novel gate stack for III–V QW-MOSFETs was created using a bilayer dielectric consisting of Beryllium Oxide (BeO) and hafnium dioxide (HfO_2). The BeO exhibits a significant energy band gap (*10.6 eV*), a wide conduction band offset (E_c), and a trapping interface layer when compared to Al_2O_3. This layer improves the retention properties of MOSFET output by reducing leakage trapped charges [12], [36]. Largely, the drain current is proportional to the thickness of the oxide (t_{ox}) layer. To attain the desired output, Lanthanide Oxide is chosen for its characteristic features. In the Lanthanum Oxide layer, the drain current increases with reduced thickness and its resistive property. Thus, the drain current (I_D) variations concerning changes in drain-source voltage (V_{DS}) with various oxide concentrations are depicted in Fig. 2. The dielectric constant ε and leakage currents I_{LEAK} usually have a trade-off relationship in a

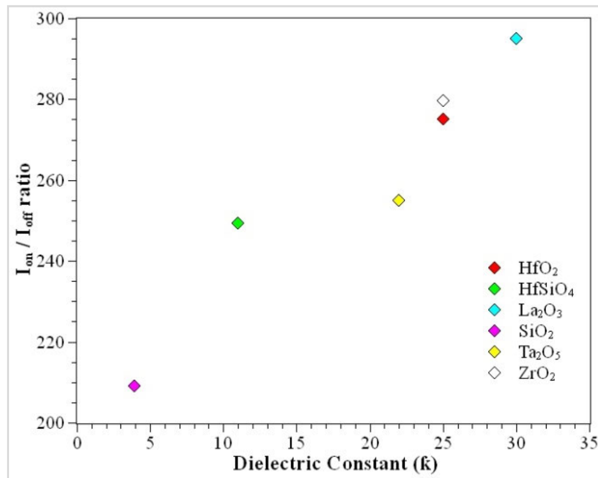


FIGURE 3. I_{ON}/I_{OFF} ratio in SG MOSFET.

high-ƙ dielectric system. To overcome this severe trade-off, an appropriate amount of impurities added into HfO_2 using the Atomic Layer Decomposition (ALD) technique is a promising solution. However, ε values of most dielectric materials and the gate leakage current of SG-MOSFET are shown in Table 2 (appendix). It has been observed from Table 3 (appendix) the dielectric constant ε is inversely proportional to the band-gap. The leakage current proportionality depends upon dielectric constant ε of dielectric oxide, the thickness of the oxide layer or gate thickness (t_{ox}), gate length (L_G), and the cross-sectional area (A) of the SG MOSFET. The discussions and comparison of the properties of HfO_2 with basic MOSFET by doping with different elements such as N, Si, Al, Ti, and Ta have been carried out [17], [23], [30]. The leakage current densities of both n-MOSFET and p-MOSFET were measured as 9.8×10^{-13} and 9.2×10^{-12} $nA/\mu m^2$ under an electric field of $+0.75$ and -0.75 mV/cm, respectively. The change in ON-current (I_{ON}) and OFF-current (I_{OFF}) current ratio of E-mode $Al_{0.53}Ga_{0.47}As$ surface channel SG MOSFET varies differently as compared to the dielectric oxide materials, as shown in Fig. 3. In the associated results of I_{ON}/I_{OFF} with high-ƙ dielectric constant illustrates, the lanthanum oxide provides OFF-current of 2.41×10^{-4} $A/\mu m$.

The I_{ON}/I_{OFF} ratio is expected to be increased by introducing several EOTs as in conventional MOSFETs. The ON-current is the current that passes through the device, while OFF-current is the current that passes through the insulator or high-ƙ dielectric material. The oxide capacitance (C_{ox}) between the gate metal and the semiconductor determines the ON-current I_{ON}. In contrast, sub-threshold leakage, Gate-Induced Drain Leakage (GIDL), and gate leakage determine the off current I_{OFF} in any compound semiconductor MOSFET [37]–[39]. In contrast to gate leakage, sub-threshold leakage makes it impossible to reduce off-state current. The reduction can be possible only when high threshold voltage V_{TH} transistors are employed. A Sandwich Tunnel Barrier kind of FET (STBFET) with a *2 nm* tunneling distance into it had been effective with the conventional design of MOSFETs. The non-local band investigates the device specifications for tunneling, mainly determined by the band-edge profile located around the tunneled cross-sectional area [40], [41].

Accordingly, the electric field at each tunneled location changes dynamically. The result of STBFETs using advanced method standardization with Monte Carlo implantation determines the increase in ON-current ($I_{ON} > 1$ mA/m) and OFF-current (I_{OFF} at 0.1 mA/m) with a sub-threshold fluctuate less than *40 mV/dec*. The high I_{ON} current is accomplished by tunneling in the gate region rather than the gate width specified; however, the value of I_{OFF} is low, and it mainly depends on spacer thickness. The investigations that the spacer length thickness in any compound semiconductor technology must be within the optimal limit were performed [42]–[45]. Exceeding the limit leads to an increase in source and drain resistances and causes an overall degradation by a decrease in on-state current I_{ON}. Compared to SiN and SiO_2, Lanthanum oxide La_2O_3 is used as a passivation layer due to its resistivity, lowest lattice energy among the rare earth oxides, and dielectric constant property ($\varepsilon = 27$) is *4 - 6* times greater than that of SiO_2.

The relationship between on-resistance R_{ON} and the gate length L_g is proportional to each other. Thus, R_{ON} decreases as gate length (L_G) decreases. By observing the result, choosing an $L_G < 50$ nm to achieve high current I_{ON} and maximum transconductance (G_m) can be inferred. With decreasing L_G, the device sub-threshold voltage and drain to source voltage (V_{DS}) also increase. It is also evident that the high subthreshold swing and reduced gate length are the major reasons for severe short-channel effects. The InGaAs/InAs/InGaAs composite channel MOSFETs using *1 nm* Al_2O_3/ZrO_2 as a dielectric with dielectric constant $\varepsilon = 25$ is suitable for high-frequency applications. When compared ZrO_2 with Al_2O_3 and HfO_2, the drain current obtained using ZrO_2 as a dielectric is greater as 520 $\mu A/\mu m$ than Al_2O_3 and HfO_2, whose value is 290 $\mu A/\mu m$ and 400 $\mu A/\mu m$ for the same EOT $= 1.2$ nm [46]–[50]. The I_{ON}/I_{OFF} ratio and I_{ON} current for $L_g = 200$ nm are 220×10^2 and $220 \times 10^2 \mu A/\mu m$. Hence, it is concluded that an increase in drain current of 700 $\mu A/\mu m$ is achieved with an increase in gate length L_g of *100 nm*. With the effect of an increase in gate length L_g, the I_{ON}/I_{OFF} ratio also increases.

The mobility of the charge carriers increases concerning the gate voltage. The carrier mobility increases when the channel charge density is less than 2.6×10^{12} cm^{-2}. Thus, mobility drops when carrier density is increased further. The increase in gate length of *100 nm* leads to the rise in drain current of 700 $\mu A/\mu m$. The I_{ON}/I_{OFF} ratio increases because of an increase in L_G. Also, the mobility of the charge carriers increases concerning gate voltage. Under investigation, the carrier mobility increases when the channel charge density is less than 2.6×10^{12} cm^{-2}. Thus, mobility drops when there is a further increase in carrier density [51]–[53].

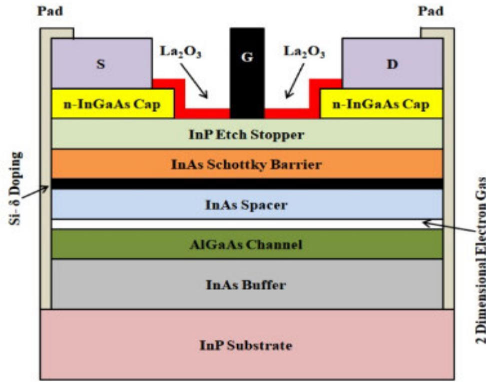


FIGURE 4. Structure of InAs/AlGaAs/InAs HEMT.

IV. PROPOSED InP/InAs/AlGaAs HEMTs IN CSDG REGIME

Several researchers proposed HEMTs with various compound materials like InP & AlGaN/GaN to improve high frequency, breakdown voltage, transconductance, and noise characteristics. The gate structure has been fabricated to adjust gate recess length (L_{gr}) and gate length (L_G). The condition to improve transconductance (G_m), drain current (I_D), and Breakdown Voltage (BV) can be achieved by adjusting with L_{gr} and L_G. The drain current in HEMT can be controlled by setting up the L_{gr} with constantV_{DS} and varying the etch time. Persistent etch time may alter surface hardness and roughness, resulting in decreasing drain current. The frequency response of the HEMT can be increased by reducing the $L_G < 50\,nm$ [19], [29]. Poor channel modulation and low breakdown voltage exist due to reduced gate length.

Scaling L_G and distance from the gate to the channel L_{GS} must be examined to achieve excellent performance. Recommended improved results can be achieved by keeping the value of gate-source length concerning drain L_{GS}/d as maximum. In general, the band-gap energy of InP HEMTs with AlGaAs channel layers (Aluminium content can be up to *30 %* depending on the application) increases. The electronic device simulator has been used to create a *5 nm* gate-length $Al_{0.53}Ga_{0.47}As$/InP based HEMT to demonstrate the features of HEMTs. Fig. 4 shows the cross-sectional structure of the InAs/AlGaAs/InAs HEMT. The arrangement includes a *15 nm* InP substrate layer, a *5 nm* InAs buffer layer, a *10 nm* $Al_{0.53}Ga_{0.47}As$ channel layer, and a thin layer of undoped InAs is utilized as a spacer layer. To reduce columbic scattering, the undoped InAs have been proposed in this work. The InAs Schottky barrier layer and an InP etching layer are consecutively placed above the channel with a separation of *3 nm* thickness.

Hence, adding up indium content in the substrate has been limited to reducing the gate leakage current in the MOSFET regime. The impact ionization in the high indium content material may lead to more gate leakage current. To address these issues, a dielectric layer of La_2O_3 is sandwiched between the metal gate and the InAs Schottky barrier layer to provide a high-energy barrier layer. The proposed HEMT has been revolved around the axis outside the substrate to form a cylindrical structure suitable for the design of CSDG MOSFETs with HEMTs.

The addition of aluminum content in the Schottky layer is practiced to avoid leakage current issues, reducing breakdown voltage. The capacitance can be given as:

$$C = \frac{Q}{V} \tag{2}$$

where Q and V are charge and voltage, respectively. It has been substituted with the author's previous work [18, 19]. The voltage is the potential difference between the layers of the cylindrical capacitor between r_{c1} and r_{c2} is given as:

$$V = -\int_{r_{c2}}^{r_{c1}} \frac{Q}{2\pi\varepsilon_0 rl} \tag{3}$$

$$V = \frac{Q}{2\pi\varepsilon_0 h}\int_{r_{c1}}^{r_{c2}} \frac{dr}{r} \tag{4}$$

$$V = \frac{Q}{2\pi\varepsilon_0 h}\ln\left(r\left|\frac{r_{c2}}{r_{c1}}\right.\right) \tag{5a}$$

$$V = \frac{Q}{2\pi\varepsilon_0 h}\ln\frac{r_{c2}}{r_{c1}} \tag{5b}$$

The r_{c1} and r_{c2} are shown in Fig. 5(a). The final equation of the voltage across the imaginary capacitance has been given in (5(b)). The flux density along the capacitor has been given as:

$$\phi = \frac{Q_{cap}}{\varepsilon_0} \tag{6}$$

where Q_{cap} can be substituted with the (7) in (6) to get (9).

$$Q_{cap} = \frac{Q_h}{L} \tag{7}$$

In (6) with the electrical field along with the small distance ds changes to:

$$\phi = \int \vec{E}.\vec{ds} = E.A = E.2\pi rh \tag{8}$$

The voltage differences in the cylindrical structure can be given as the potential difference between the r_{c1} and r_{c2}:

$$V_{c1} - V_{c2} = -\int_{r_{c2}}^{r_{c1}} \vec{E}.\vec{dr} \tag{9}$$

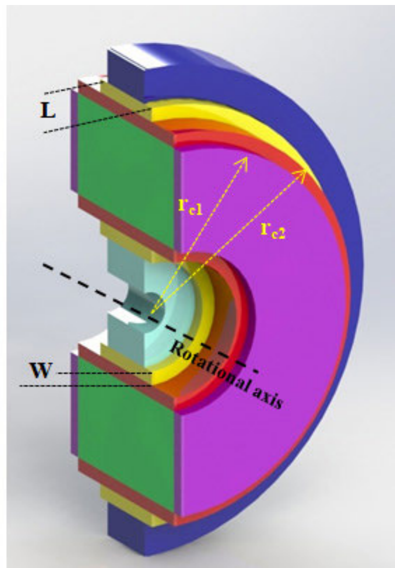
The flux has been substituted with the general expressions for the Q_{cap} and can be rewritten as (10) for the insight of the CSDG regime.

$$\phi = \frac{Q_{cap}}{\varepsilon_0} = \frac{k\varepsilon_0\frac{A}{d}}{\varepsilon_0} = k\frac{A}{d} \tag{10}$$

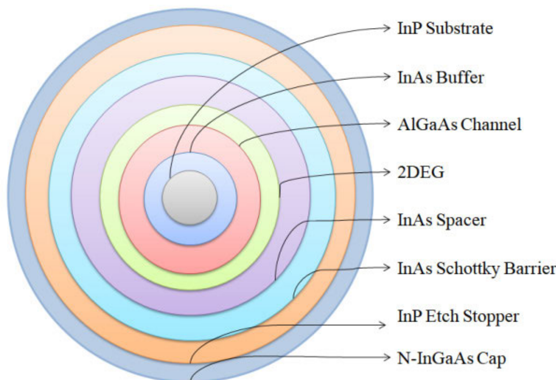
On further reduction, it becomes:

$$\phi = \frac{k\varepsilon_0\frac{2\pi\left[\left(r_{c1}^2-r_{c2}^2\right)+h(r_{c1}-r_{c2})\right]}{d}}{\varepsilon_0}$$

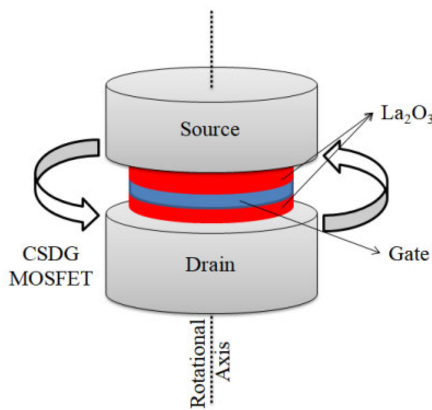
$$\phi = \frac{2\pi k}{d}\left[\left(r_{c1}^2 - r_{c2}^2\right) + h\left(r_{c1} - r_{c2}\right)\right] \tag{11}$$



(a) Basic CSDG MOSFET [19]



(b) Proposed CSDG after rotating the HEMT as in Fig. 4



(c) Isometric view of InP/InAs/AlGaAs based CSDG MOSFET

FIGURE 5. Improvement in the basic CSDG MOSFET using InP/InAs/AlGaAs.

It can be used for analysis in the CSDG MOSFET design.

$$\frac{Q_h}{L} = k\varepsilon_0 \frac{2\pi \left[\left(r_{c1}^2 - r_{c2}^2\right) + h\left(r_{c1} - r_{c2}\right)\right]}{d} \tag{12a}$$

$$Q_h = \frac{2\pi k\varepsilon_0 L}{d}\left[\left(r_{c1}^2 - r_{c2}^2\right) + h\left(r_{c1} - r_{c2}\right)\right] \tag{12b}$$

$$E_{ox} = \frac{1}{2r}\mu_0\mu_n k\varepsilon_0 . \left\{\left[\ln\left(\frac{a}{b}\right)\right] - a\right\} . \frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \tag{13}$$

The charge along the height of the capacitor has been derived in (12) and has been used to determine the electrical field of the oxide as in (13). The proposed design can be used to create an extensive structure that abides the cylindrical structural characteristics of the HEMTs.

V. RESULTS AND DISCUSSIONS

To stream charge carriers towards source/drain contact regions and reduce resistance at source and drain-Si-δ doping concentration (20×10^{11} cm^{-2}) of *2 nm* thickness is sandwiched between the InAs Schottky Barrier (SB) and a spacer layer. Introducing a thick InAs SB layer with a thickness of *3 nm* reduces gate leakage, eliminates surface scattering, and aids in confining and improving electron mobility in the channel. The difference between EOT and physical thickness is expressed as:

$$C_{ox} = C_{La_2O_3} = \frac{\varepsilon_0 . k_{La_2O_3} . L . W}{t_{La_2O_3}} = \frac{\varepsilon_{La_2O_3} . A}{t_{La_2O_3}}$$

$$EOT = t_{La_2O_3}\left(\frac{k_{SiO_2}}{k_{La_2O_3}}\right) \tag{14}$$

where L and W are the length and width of the channel; A is the area of the channel; ƙ of La_2O_3 is *21*; ƙ high ≫*12 - 25*. In the proposed research work, the direct high-ƙ /Si-sub contact becomes a significant concern when the EOT of the high-ƙ dielectric decreases.

The strongly doped n-$In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ MOSFET with the multi-level arrangement in the source and drain terminal significantly reduces its terminal resistances R_S and R_D. In addition, the $In_{0.53}Ga_{0.47}As$ multi-cap layer minimizes the potential barrier in the source/drain access region via the InAs spacer layer, and thus, the channel carrier concentration increases. The higher permittivity of high-ƙ Lanthanum oxide material improvises the accessibility of nanoscale CMOS MOSFETs and also regulates the charge carrier current based on oxide capacitance and gate leakage. The channel behavior of E-mode Ga-polar GaN Metal Insulator Semiconductor (MIS) HEMT has been demonstrated. With a gate length $L_G = 0.62\ \mu m$ and a threshold voltage $V_{TH} = 1\ V$, a high ON-state current I_{ON} of *0.74 A/mm* is obtained. Due to shorter gate length, the reduction in threshold-voltage roll-off caused DIBL. Feng *et al.* [28] have proposed GaN-based MIS-HEMT devices composed of nitride stacks with varying polarities that may provide numerous channels via flexible gate(s) control. Thus, a high ON-state current I_{ON} of *4 A/mm* is achieved by fixing the same $L_G = 0.62\ \mu m$ and $V_{TH} < 2\ V$.

Table 4 (appendix) shows the effect of gate length $L_g = 5\ nm$ on maximum drain current ($I_{D,max}$) and maximum transconductance (G_m) of E-mode $Al_{0.57}Ga_{0.43}As$ channel

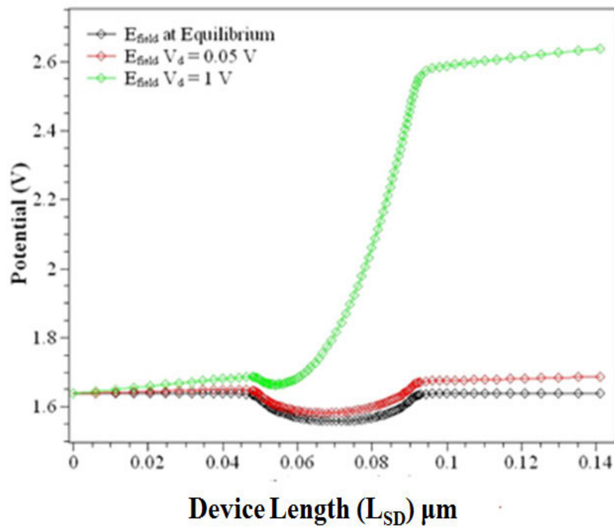


FIGURE 6. Device length Vs. Electro static potential.

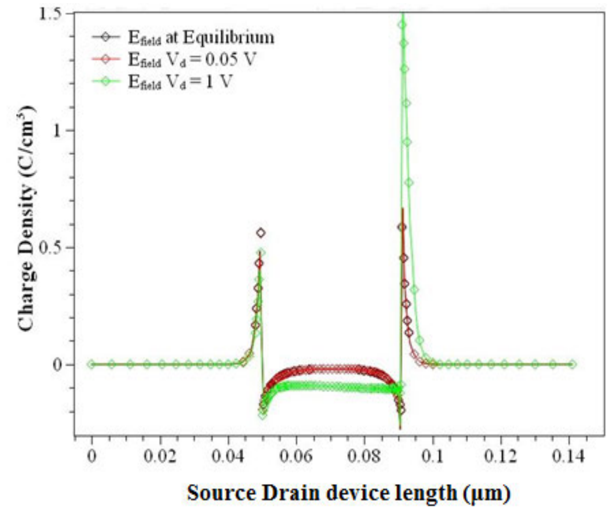


FIGURE 7. Source drain Length (L_{SD}) Vs. Charge density (ρ).

MOSFETs with varying drain-source voltages. When V_{DS} and V_{GD} are held at $0.78\ V$ and $0.16\ V$, respectively, the maximum transconductance of $11.4\ mS/\mu m$ is attained. Table 5 (appendix) compares the proposed InP/InAs/AlGaAs HEMT with standard HEMT. According to the results, the maximum drain current ($I_{D,max}$) of $5.4\ mA/\mu m$ is reached when $V_{DS} = 0.5\ V$ and $V_{GS} = 1\ V$. The leakage current I_{leak} is given by considering two cases:

Case 1: Drain: ON; Gate: OFF condition (I_G, OFF)

Case 2: Gate: ON; Drain: OFF condition (I_D, OFF)

$$I_{leak} = [(I_G, OFF) + (I_D, OFF)] \tag{15}$$

where (I_G, OFF) as when the drain is ON and (I_D, OFF) as when the gate is ON. Hence, the considered OFF-current depends on V_{GS}, $V_{TH,}$ and supply voltages (V_{DD}) of $0.5\ V$ and $0.05\ V$, respectively. The I_{ON}/I_{leak} ratio obtained for the 5 nm enhancement device is of value 1.8×10^3. Thus, it is observed and concluded that the I_{ON}/I_{leak} ratio decreases when a thin insulator is used in enhancement-mode devices. The E-mode nFETs of $L_G = 30\ nm$ and SiO_2 of $0.1\ nm$ thickness whose I_D current is measured to be $1.4\ mA/\mu m$ and transconductance of $2.3\ mS/\mu m$ when (V_{GS}-V_{TH}) is positive and is equal to the value of $0.83\ V$.

Fig. 6 shows the plot of electrostatic potential varied with device length measured between $50\ nm - 100\ nm$. In the absence of drain voltage or equilibrium, the potential variation along the channel has been examined. A potential emerges at the edges (source/drain) in the absence of drain-to-source voltage (V_{DS}). The lower potential of $1.5\ V$ occurs close to the middle of the device length, where the channel is placed when drain voltage $V_{DS} = 0\ V$ and $0.5\ V$ is applied. Between the device lengths of $0.05\ \mu m$ and $0.09\ \mu m$, an exponential increase in the potential from $1.682\ V$ to $2.639\ V$ arises when $V_{DS} = 1\ V$. Besides, the potential remains constant when $L_{SD} \geq 0.1\ \mu m$.

Fig. 7 illustrates the charge carrier density with variations in the structural device length. Here the charge carriers and their mobility in the channel are determined by V_{GS} and V_{DS}. However, when $V_{GS} > V_{TH}$ and V_{DS} is in equilibrium state at a voltage of $0.05\ V$, the more accumulation of charge carriers is expected in the device length L_{SD} of $90\ nm$ from source and drain per unit area defined as charge density 'ρ', which is equal to $0.5830\ C/cm^3$ and $0.5905\ C/cm^3$. Further, increase in drain voltage of $V_{DS} = 1\ V$, the charge carrier density 'ρ' increases at the peak of $1.4493\ C/cm^3$ whose value is $75\ \%$ increase when compared with variation in the drain voltage of $0\ V$ and $0.5\ V$. Thus, carrier transport efficiency improves in the constant electric field along the channel. This, in turn, provides advantages to measure low-frequency noise measurements on the drain current source.

The graph of Fig. 8 between device length vs. electric field along X-and Y-axis, respectively, depict the rapid variations in channel lengths between $50\ nm$ and $100\ nm$ for electric field values at equilibrium, $0.05\ V$ and $1.00\ V$. At equilibrium V_{DS}, the electric field increases to a peak value of $-\ 50\ mV/\mu m$. As indicated above, the proposed field value increases to a peak value of $-\ 93\ mV/\mu m$ for $V_{DS} = 0.05\ V$. The rise of the vertical electric field 'E' and the shortening of channel length cause carrier dispersion at the surface. As a result, there is less mobility near the surface. Similarly, at L_{SD} of $90\ nm$, when $V_{DS} = 1\ V$, the electric field rapidly reduces to $-\ 47.1259\ V/m$. When $V_{DS} = 1\ V$, the lateral electric field in short channel MOSFETs is very high, causing electron injection (hot carrier injection) into the oxide layer and an increase in V_{TH}, as seen in Fig. 8. The lateral electric field diminishes over the length of the channel as the V_{DS} increases. When the V_{DS} is low and the V_{GS} is high, the channel potential decays linearly, resulting in a constant electric field. When the drain and gate-source biases are substantial, the electric field created in the channel is strong and fluctuates non-linearly with the position. The electric field is low at the source (at the top of the barrier), but it rises near the drain, reducing the hot carrier effect. In the

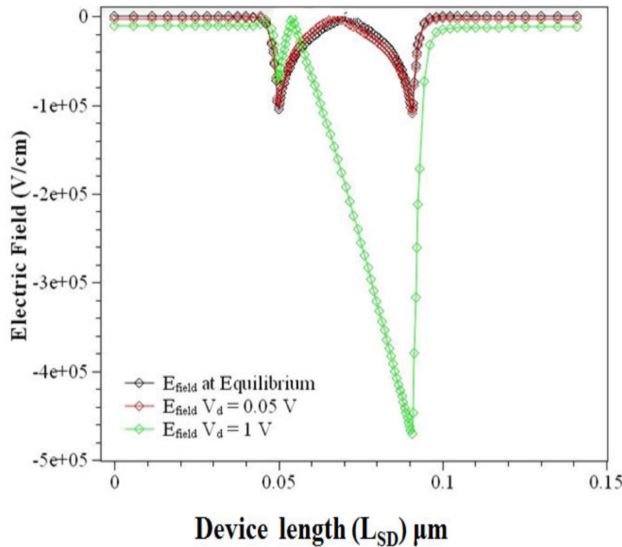


FIGURE 8. Device length vs electric field.

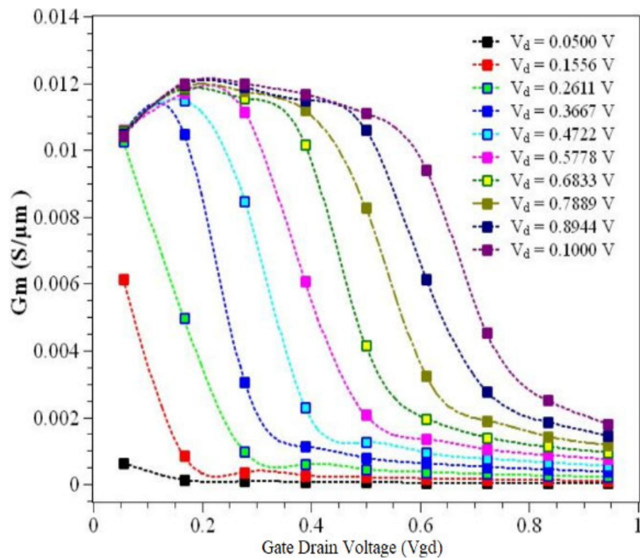


FIGURE 9. The transconductance of E-mode Al 0.53Ga 0.47As surface channel.

saturation region, the increase in V_{DS} would cause a large potential drop in the channel. Thus, the top of the barrier remains unchanged when DIBL is small.

Asymmetric $In_{0.53}Ga_{0.47}As$/InP MOSFETs through different sources and drain have been analyzed. $In_{0.53}Ga_{0.47}As$ compound semiconductor is currently grown at the source and drain, whereas InP is grown distinctly at the drain. The G_m and I_D are proportional to L_G when monitored (Fig. 9). From the result, it can be inferred that when InGaAs is used as the drain, an increase in drain current and transconductance occurs when the gate length is lowered to $L_G = 50\ nm$ rather than $L_G = 100\ nm$. The comparison between InGaAs and InP concludes that InGaAs have superior growth on drain than InP. The properties of lower doping and a wide band-gap of *1.34 eV* in InP MOSFET achieve reduced Band-To-Band Tunneling (BTBT) effect at drain substrate junction, immune to higher impact ionization at the drain. The same BTBT becomes inconvenient when the thickness of the oxide t_{ox} and electric field 'E' increases. The reduction of space length from *8 nm* to *3 nm* with the supply voltage of $V_{DS} = 0.5\ V$ and $V_{GS} = 0.3\ V$ decreases the leakage current I_{leak} in the ratio of *5:1*. The spacer length reduces at low drain voltage, thereby causing more degradation in the analog performance.

TABLE 1. Parameters used for capacitance modeling.

Symbol	Description of the parameters used
a	The inner radius of the cylindrical capacitor
b	The outer radius of the cylindrical capacitor
C_{ox}	The specific capacitance of the gate oxide
C_{ox_cyl}	The cylindrical capacitance (CSDG)
E_{cap}	Energy stored in the capacitor
E_{cap_cyl}	Energy stored in the cylindrical capacitor (CSDG)
E_{inner}	Energy stored in the inner cylinder
E_{outer}	Energy stored in the outer cylinder
h	Height of the cylindrical capacitor (CSDG)
L	The gate length of the transistor
L_c	Unit length of the capacitor
r	The radius of the cylindrical capacitor (General)
r_{c1}	The inner radius of the cylindrical capacitor (CSDG)
r_{c2}	The outer radius of the cylindrical capacitor (CSDG)
V_{GS}	Gate to Source voltage
V_{DS}	Drain to Source voltage
V_T	Threshold voltage
W	The width of the transistor
ε_0	The permittivity of free space
ε_{ox}	The relative permittivity of the gate oxide
ƙ	High Dielectric constant (kappa)
π	Pi (≈ 3.1416), constant
μ_n	The electron mobility of the transistor substrate (n-type)
μ_0	The electron mobility of the transistor substrate (free space)

TABLE 2. Properties of III-V binary and ternary compound semiconductors [19].

S.No	Properties	InP	AlGaAs
1	Lattice constant(A∘)	5.869	5.6351
2	Electron Effective Mass	0.077	0.067
3	Electron Mobility μ_n (cm^2/Vs)	4600	10^7
4	Hole mobility μ_p(cm^2/Vs)	150	400
5	Velocity Saturation at low field ($\times 10^7$ cm/S)	2.5	2.3
6	Band-gap (eV)	1.35	1.93
7	N_C ($\times 10^{17} cm^{-3}$)	5.7	4.82
8	N_V ($\times 10^{18} cm^{-3}$)	9.0	4.82

TABLE 3. Dielectric oxides vs leakage current for SG-MOSFET.

Dielectric Oxide	Dielectric constant (ε)	Band-gap (eV)	Leakage Current (I_{OFF}) (μA/μm)
La_2O_3	27	6	2.91
HfO_2	22-25	5.5-6	2.85
ZrO_2	25	5.8	2.90
$HfSiO_4$	11	6.7 -7.3	2.8
SiO_2	4	9	1.9
Ta_2O_3	22	4.4	3.23

TABLE 4. Parametric measurement with variation in V_{DS}.

Parameter	V_{DS}= 0.05 V	V_{DS}= 0.5 V	V_{DS} = 1 V
$I_{D,max}$ (mA/μm)	0.64	5.4	10
G_m (mS/μm)	0.644	11.4	12
Electrostatic Potential (V)	1.6361	1.6739	2.58
Charge Density (C/cm^3)	0.5830	0.5905	1.5
Electric Field (V/μm)	-5.07×10^2	-9.29×10^2	-47.12

TABLE 5. Comparison of various HEMTs with conventional HEMTs.

MOSFETs	Dielectric oxide	T_{ox}(nm)	L_g(nm)	ID_{max} (mA/μm)	G_m (mS/μm)	I_{ON}/I_{OFF}	I_{OFF} (μA/μm)
[4]	GaN	5	22	0.950	0.45	100	7.4
[13]	Al_2O_3/InAlAs gate stack	5	90	0.001	1.32	1.8×10^3	5.5×10^{-4}
[15]	Al2O3, HfO_2 and HfAlO	8	60	1.8	2.4	1000	1.8
[19]	HfSiON	2.3	15	2.57	0.60	7.73×10^7	0.01
[21]	Al_2O_3/ZrO_2	1	30	1	2	7×10^4	0.01
[30]	Al_2O_3	5	500	0.813	0.25	8.13×10^8	10×10^{-8}
[37]	Al_2O_3/InAlAs gate stack	4.6	50	1.327	1.7	1.7×10^4	0.07
[41]	SiO_2	1	30	0.514	1.2	5140	0.1
[50]	SiO_2	2	10	1.4	2.3	600	1
This work	La_2O_3	2	5	5.4	8.4	290	0.03

The deterioration occurs when spacer length increases with a less maximum operating voltage than a high driving voltage.

The mechanism of gate leakage in $Al_2O_3/Al_{0.55}Ga_{0.45}$ N/GaN HEMTs $L_g = 500\ nm$ and Al_2O_3 of *5 nm* thickness whose I_D current, leakage currents, and G_m have been measured to be *8.13 mA/μm*, $10 \times 10^{-8}\ \mu A/\mu m$, and *2.57 mS/μm*, respectively at $V_{DS} = 1\ V\ and\ 0.05\ V$. The findings suggest that structural improvement is required to increase the FinFET's driving current and prevent degradation of analog performance. The on/off ratio of 7.73×10^7 is achieved when the spacer length increases to *80 nm*. The OFF- and ON-current decreases from 10^{-8} to 10^{-13} A and 10^{-4} to $10^{-5}A$, when spacer length varies from *30 nm* to *110 nm*. Heterostructures often vary the characteristics based on the calculated gate voltage at the gate to drain terminals. The V_{GD} has been analyzed over G_m values with an L_G of *5 nm* for fixed V_{DS}. As an alternative for the gate to source connection, mutual conductance occurs between the gate to drain terminals. It has been observed that the Gm value remains peak in the linear region and exponentially decreases at high V_{GD}.

VI. CONCLUSION AND FUTURE RECOMMENDATIONS

In this research work, the analog parameters required to build the structure of novel InP/InAs/AlGaAs HEMT with a gate length of $L_g = 5\ nm$ were investigated. The quantum wave MOSFETs with high-ƙ gate dielectrics promise to enhance Moore's law by scaling gate length to *5 nm* is considered. Thus, a strong electric field is induced in the channel and fluctuates non-linearly with position when the drain and gate-source biases are kept large. A *10 nm* E-mode $Al_{0.53}Ga_{0.47}As$ MOSFET on InP substrates featuring La_2O_3/ InGaAs gate stack obtain a high-level transconductance of *11.4 mS/μm* and a drain current (ID) of *5.4 mA/μm*.

The InP technology is favored over other technologies due to its characteristics such as strong intrinsic transconductance, maximum extrinsic transconductance, high drain current, practical breakdown voltage, a high-ƙ dielectric layer, low leakage current, and high I_{ON}/I_{OFF} current. These characteristics play a vital role in millimeter-wave LNA applications and high-speed applications in the THz frequency range.

To achieve high-speed applications in future microelectronics technology, high-ƙ metal oxide film ZrO_2 is to be chosen as the best oxide layer due to its properties, such as high dielectric constant and low leakage current density. The fabrication involves challenges constrained to the cylindrical environment, but it has potential advantages. The HEMT, after making into the cylindrical surrounding structure, consumes lesser area onboard, making way for other components to be placed.

APPENDIX

See Tables 1–5.

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