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General Analytical Method for Heat Dissipation of N-Layer High-Power LED Systems

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ABSTRACT Although the light-emitting diode (LED) has been developed into relative maturity, thermal management remains an important problem for high-power LEDs. To obtain the temperature distribution and improve the heat dissipation of high-power LED systems, an *N*-layer model which is flexibly applied to different LED packaging structures is proposed, where the equivalent method of heatsinks is also included. The corresponding analytical solutions to temperature field and thermal resistance are generalized to *Nth* to adapt to the model. The method is proved to be accurate and time-saving in comparison with finite element method (FEM) simulations. In particular, it has obvious advantages in dealing with the thin layer analysis where the target region is much smaller than the entire model. By calculating the junction temperature and thermal resistance of an example LED module, the method is demonstrated in detail. Effects of printed circuit board (PCB) composition and heatsink on heat dissipation are analyzed, and the related thermo-mechanisms are revealed in terms of thermal resistance. This work may have significance for the design work of high-power LED systems.

INDEX TERMS Analytical method, thermal management, high power-LED system, N-layer model, thermal resistance.

I. INTRODUCTION

As the most widely used lighting device nowadays, light-emitting diodes (LEDs) have shown advantages of low-voltage operation, high brightness, good reliability, and long lifetime in competition against other traditional lighting sources. Further, people have been committed to improving the efficiency of LEDs [1], [2], the phosphor-converted LED has the potential to improve the luminous efficiency from 160 lm/W to 255 lm/W, and the color-mixed LED may realize 330 lm/W shortly [3]. However, with the increase of power, it must be vigilant that overhigh junction temperature will lead to frequency offset, shorter lifetime, efficiency droop, and even irreversible damages to high-power LEDs [4]–[7]. Consequently, good thermal management is beneficial for improving stability and electro-optic conversion efficiency. An important issue is to determine the junction temperature and the thermal resistance [8]–[10] and then to realize better heat dissipation [11], [12].

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The 1-D thermal resistance circuit is used to obtain junction temperature and thermal resistance [13]–[15]. However, it seems over-simplified compared to practical cases. For example, it cannot be used to analyze the impact of chip distribution on junction temperature. The finite element method (FEM) is often used to deal with the heat transfer problem of LED systems. Hsu *et al.* [16] made simulations with thermal under current loading conditions. Tsai *et al.* [17] analyzed the influence of natural and forced convective conditions on thermal resistance. Similarly, Abdelmlek *et al.* [18], [19] discussed the influence of LED quantity and distribution on junction temperature. In these studies, the temperature field can be easily obtained by the powerful FEM simulation. However, it may require a lot of time and computer memory. At the same time, model discretization and meshing have always been difficult problems. Thus, the analytical method is of great concern when the model is not necessary to be fully discretized and only the temperature distribution of target regions is needed. Yovanovich *et al.* used the analytical method to solve heat conduction problems earlier. However, the study was not applied to a specific LED application [20], [21]. Ha and Graham [22] made use of the

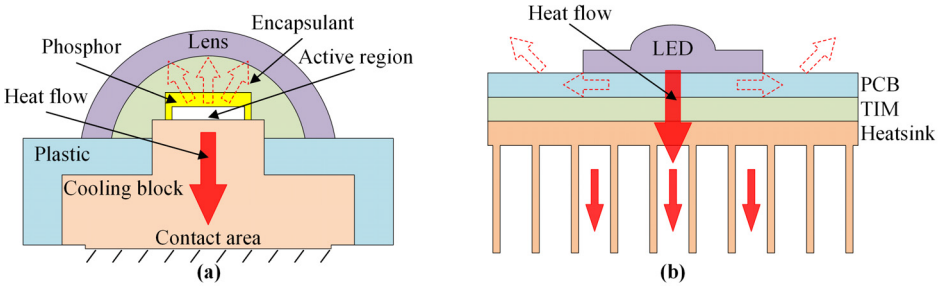

FIGURE 1. Schematics of pathways to heat dissipation of LEDs at (a) chip-level and (b) system-level.

empirical formula in the solving process, which may weaken the accuracy, and the algorithm is only adapted to a particular model of four layers. Zhou *et al.* [23] discussed mainly the influence of thermal conductivity of the printed circuit board (PCB). Cheng *et al.* [24] presented analysis and optimization of multiple LED packaging based on an analytical solution, their work can be further improved by considering the contribution of PCBs.

In this paper, heat dissipation processes and heat pathways of LEDs at both chip level and system level are introduced. Based on that, an N-layer model of LED systems is proposed. The packaging structure of LED systems can be divided into different layers to discuss their effects on thermal management separately. The N-layer model has the generality to adapt to different LED systems to a certain extent because there is no limitation on the number of layers. According to the model, the analytical method is employed to calculate the temperature field, junction temperature, and thermal resistance, and the corresponding solutions are generalized to Nth. The result from the layered model and analytical calculation is compared to that of the complete model and FEM simulation. Through the comparison, the work is verified to be valid, and it is especially suitable for the "thin layer" problem. When the target layer is much smaller than the entire model, the analytical method shows its advantage in a direct calculation of the junction temperature instead of the whole temperature distribution. Furthermore, the dependences of cooling performance on PCB and heatsink are presented. It can be concluded that optimizations of PCB and heatsink can effectively reduce the spreading and the convective thermal resistances respectively, and then has a significant effect on lowing the junction temperature.

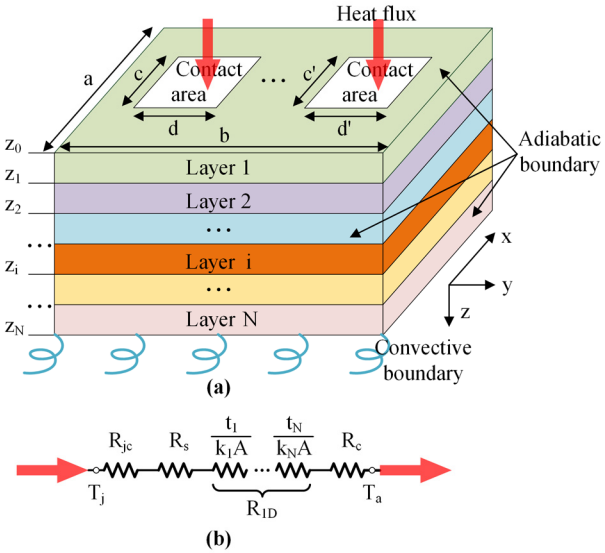

FIGURE 2. Schematic of (a) the N-layer LED system model and (b) equivalent thermal resistance circuit.

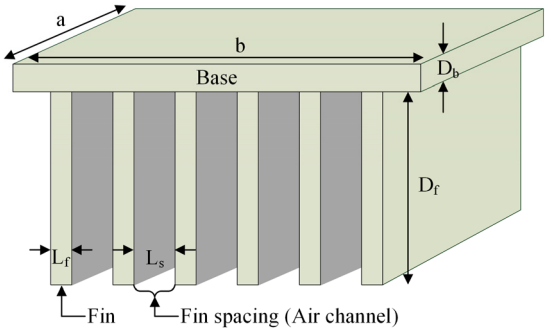

FIGURE 3. Schematic of the fins heatsink.

II. MODELING METHOD

When an LED device starts to work, heat is generated in the active region accompanied by the emission of photons. As shown in Fig. 1(a), the thermal conductivities of phosphor, encapsulant, and lens are small, whereas that of the cooling block is much higher. It is reasonable to assume that all heat is conducted through the contact area to the PCB below (the solid red arrows represent the heat flow, while the dashed arrows represent the heat flow that is ignored). The metal cooling block has a certain thickness and is much larger than the active region, which contributes to the uniform diffusion of heat flow. So, the contact area is set to the uniform heat flux boundary condition. As shown in Fig. 1(b), when the heat is transferred into PCB, the lateral conduction is limited by the thin PCB and the second lens limits the airflow near the PCB surface [22], [23]. Therefore, nearly all the heat is conducted downward through PCB, thermal interface material

(TIM), and heatsink, and finally convected to the surrounding environment.

An N-layer model of the LED system is proposed in Fig. 2(a). Based on the heat pathway analysis, LED chips are simplified as heat sources, components beneath the LED chip are divided into different layers. The contact areas of chips and the top layer are set to uniform heat flux conditions, and the rest region of the top surface is set to the adiabatic boundary. The lateral surface of each layer is also set to the adiabatic boundary. Because it is far less than the cross-sectional area, only a very small amount of heat is convected through these regions. The heatsink is always a necessity for high-power LED systems, which contributes to improving the heat dissipation by enhancing convection. It can be simplified into a plate and taken as the last layer of the model. Therefore, the bottom surface of the last layer is set to the convective boundary.

Taking a regular fins heatsink as an example, the equivalent method of the fins heatsink is illustrated (for other heatsinks of special shapes, they can also be transformed to the layered structure in the same way). As shown in Fig. 3, to assume that the heatsink has n fins, and the equivalent convective heat transfer area provided by a single fin (A_f) is [25]:

$$\begin{aligned} A_f &= 2\eta a f \\ \eta &= \frac{\tanh Mf}{Mf} \\ M &= \sqrt{2h(a+L_f)/kaL_f} \\ f &= D_f + 0.5L_f \end{aligned} \tag{1}$$

where a, b, D_b are the width, length, and depth of the heatsink base. a, L_f, D_f are the width, length, and depth of a single fin. L_s is the fins spacing, η is the fin efficiency coefficient, h is the convective heat transfer coefficient, and k is the thermal conductivity.

The total equivalent convective heat transfer area (A_t) is provided by all fins (nA_f) and heatsink base (A_b):

$$\begin{aligned} A_t &= nA_f + A_b \\ A_b &= (b - nL_f)a + 2D_b(a+b) \end{aligned} \tag{2}$$

The heatsink contributes to providing a wider area for heat convection, which is the equivalent of increasing the heat transfer coefficient:

$$\begin{aligned} hA_t &= h'A_0 \\ A_0 &= ab \end{aligned} \tag{3}$$

where h' is equivalent heat transfer coefficient, A_0 is the surface area of the bottom layer.

III. SOLUTIONS TO TEMPERATURE FIELD AND THERMAL RESISTANCES

The system model is defaulted to expose to room temperature and natural air convective conditions, there is no extra heat source except LED chips, and all materials are homogeneous, isotropic, and temperature-independent. Based on these assumptions, the temperature governing equation is the Laplace form under the steady-state:

$$\nabla^2 T = \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0 \tag{4}$$

According to the governing equation and boundary conditions, the method of variable separation is used to solve the temperature function of each layer. Based on [22], [26], and [27], the temperature solution to plate structures is further improved. (i) The heatsink is transformed to a plate structure and taken as the last layer of the model. (ii) Thermal resistance of chips (from junction to case, R_jc) is taken into account. (iii) The expression in Cartesian coordinates is given, which is suitable for the multi-chip case and does not need the Stokes approximation. (iv) The final expression is generalized to *Nth* to adapt to the N-layer model. The temperature solution of each layer is:

$$\begin{aligned} &T_i(x,y,z) \\ &= T_a + C_0 P\Big(1 + \sum_{m=i}^{N-1} \frac{k_N}{k_m} \frac{B_N z_m}{1 + z_N B_N} \\ &\quad - \sum_{m=i+1}^{N} \frac{k_N}{k_m} \frac{B_N z_{m-1}}{1 + z_N B_N} - \frac{k_N}{k_i} \frac{B_N z}{1 + z_N B_N}\Big) \\ &\quad + \sum_{k=1}^{\infty} \cos(\lambda_k x) C_1 P \left[\theta_{i,i+1\lambda} \sinh(\lambda_k z) - \xi_{i,i+1\lambda} \cosh(\lambda_k z)\right] \\ &\quad + \sum_{j=1}^{\infty} \cos(\beta_j y) C_2 P \left[\theta_{i,i+1\beta} \sinh(\beta_j z) - \xi_{i,i+1\beta} \cosh(\beta_j z)\right] \\ &\quad + \sum_{k=1}^{\infty}\sum_{j=1}^{\infty} \cos(\lambda_k x)\cos(\beta_j y) C_3 P \left[\theta_{i,i+1\delta} \sinh(\delta_{jk} z)\right. \\ &\quad \left. - \xi_{i,i+1\delta} \cosh(\delta_{jk} z)\right] \end{aligned} \tag{5}$$

where T_a is the ambient temperature, P is the heat power, subscript i refers to the index of each layer.

The expression for the last layer is slightly different from others:

$$\begin{aligned} &T_N(x,y,z) \\ &= T_a + C_0 P\Big(1 - \frac{B_N z}{1 + z_N B_N}\Big) \\ &\quad + \sum_{k=1}^{\infty} \cos(\lambda_k x) C_1 P \left[\sinh(\lambda_k z) - \xi_{N\lambda} \cosh(\lambda_k z)\right] \\ &\quad + \sum_{j=1}^{\infty} \cos(\beta_j y) C_2 P \left[\sinh(\beta_j z) - \xi_{N\beta} \cosh(\beta_j z)\right] \\ &\quad + \sum_{k=1}^{\infty}\sum_{j=1}^{\infty} \cos(\lambda_k x)\cos(\beta_j y) C_3 P \left[\sinh(\delta_{jk} z)\right. \\ &\quad \left. - \xi_{N\delta} \cosh(\delta_{jk} z)\right] \end{aligned} \tag{6}$$

TABLE 1. Geometric parameters and material properties.

	Layer	Material		Thickness/Depth (mm)	Size (mm × mm)	Thermal conductivity ($W \cdot m^{-1}K^{-1}$)
	LED chip	-		-	2 × 2	-
1	Conductor	Copper		0.07	40 × 40	398
2	Insulator	Dielectric		0.2	40 × 40	0.3
3	Metal	Aluminum		1	40 × 40	237
4	TIM	Grease		0.05	40 × 40	5
5	Heatsink	Al356T6	Base	1.6	40 × 40	150
	(Fin spacing 3mm)		Fin	25	1 × 40	

where

$$
\begin{aligned}
B_N &= h'/k_N \\
\lambda_k &= \frac{k\pi}{a}, \quad \beta_j = \frac{j\pi}{b}, \ \delta_{kj} = \sqrt{\lambda_k^2 + \beta_j^2}k, \ j = 0, 1, 2 \ldots \\
C_0 &= \frac{1 + z_N B_N}{abh}, \quad C_1 = -\frac{4\cos(\lambda_k x_0)\sin(0.5\lambda_k c)}{abck_1\lambda_k^2\theta_{1,2\lambda}} \\
C_2 &= -\frac{4\cos(\beta_j y_0)\sin(0.5\beta_j d)}{abdk_1\beta_j^2\theta_{1,2\beta}} \\
C_3 &= -\frac{16\cos(\lambda_k x_0)\sin(0.5\lambda_k c)\cos(\beta_j y_0)\sin(0.5\beta_j d)}{abcdk_1\lambda_k\beta_j\delta_{jk}\theta_{1,2\delta}}
\end{aligned} \tag{7}
$$

where c, d are the width, length of the heat source, and (x_0, y_0) is the centroid coordinate of the heat source.

In particular, to generalize the final expression to *Nth*, the corresponding intermediate variable are developed as:

$$
\begin{aligned}
\theta_{1,2\tau} &= \theta_{2,3\tau} - \varphi_{1,2\tau} \\
\xi_{1,2\tau} &= \xi_{2,3\tau} - \tanh(\tau z_1)\varphi_{1,2\tau} \\
\theta_{i,i+1\tau} &= \theta_{i+1,i+2\tau} - \varphi_{i,i+1\tau} \\
\xi_{i,i+1\tau} &= \xi_{i+1,i+2\tau} - \tanh(\tau z_i)\varphi_{i,i+1\tau} \\
\theta_{N-1,N\tau} &= \theta_{N,N+1\tau} - \varphi_{N-1,N\tau} \\
\xi_{N-1,N\tau} &= \xi_{N,N+1\tau} - \tanh(\tau z_{N-1})\varphi_{N-1,N\tau} \\
\theta_{N,N+1\tau} &= 1 \\
\xi_{N,N+1\tau} &= \frac{\tau\cosh(\tau z_N) + B_N\sinh(\tau z_N)}{\tau\sinh(\tau z_N) + B_N\cosh(\tau z_N)} \\
\varphi_{i,i+1\tau} &= (1 - k_{i+1}/k_i)\cosh(\tau z_i)\left[\theta_{i+1,i+2\tau}\cosh(\tau z_i)\right. \\
&\quad \left. - \xi_{i+1,i+2\tau}\sinh(\tau z_i)\right]
\end{aligned} \tag{8}
$$

where z_i is the coordinate of the interface of each layer, the label τ is used for a concise statement, it can be replaced by λ, β, or δ in specific expressions.

The different kinds of thermal resistance shown in Fig. 2(b) can be given as:

$$
\begin{aligned}
R_t &= (T_j - T_a)/P \\
R_{1D} &= \sum_{i=1}^{N} t_i/(k_i A_i) \\
R_c &= 1/hA_t \\
R_s &= R_t - R_c - R_{1D} - R_{jc}
\end{aligned} \tag{9}
$$

where R_t is the total thermal resistance, R_{1D} is the sum of 1-D thermal resistance of each layer, R_c is the convective thermal resistance, and R_s is the spreading thermal resistance [28], [29]. t_i, k_i, and A_i are the thickness, thermal conductivity, and surface area of each layer.

Integrating (5) over the heat source region (A_s) and substituting the result into (9), the junction temperature (T_j) can be attained:

$$
T_j = R_{jc}P + \frac{1}{A_s}\iint_{A_s} T_1(x, y, 0)dxdy \tag{10}
$$

For multi-chip (source) cases, the solution can be obtained by the superposition of the contribution of each chip.

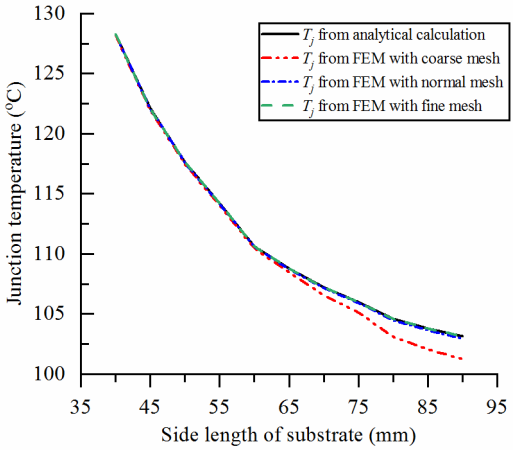

FIGURE 4. Junction temperature obtained by *N*-layer model with analytical calculation and complete model with FEM simulations.

IV. RESULTS AND DISCUSSION

Suppose there is such an LED system, a chip generates 3.5W heat under the steady-state operation, and it is located at the center of the insulated-metal-substrate (IMS) PCB which is attached to a regular fins heatsink with the thermal grease. This LED system is simplified to a model of five layers. The copper foil, dielectric, and metal base of PCB are taken as the 1st, 2nd, and 3rd layers respectively, and the thermal grease and heatsink are the 4th and 5th layers. The room temperature is 25 °C and the convective heat transfer coefficient is 5 W/(m^2·K). The other specific parameters of the model are shown in Table 1.

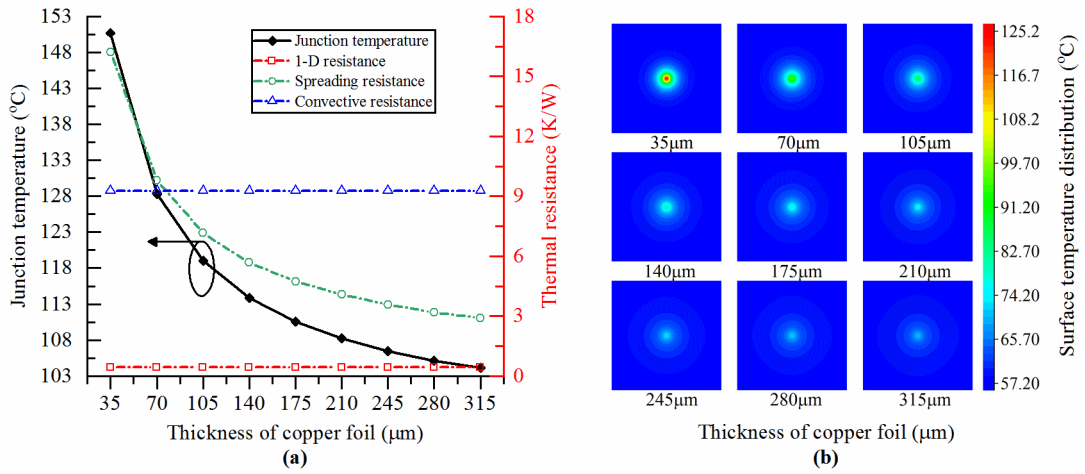

FIGURE 5. (a) Dependence of junction temperature (left y-axis) and thermal resistance (right y-axis) on the thickness of copper foil. (b) Surface temperature distribution of copper foil.

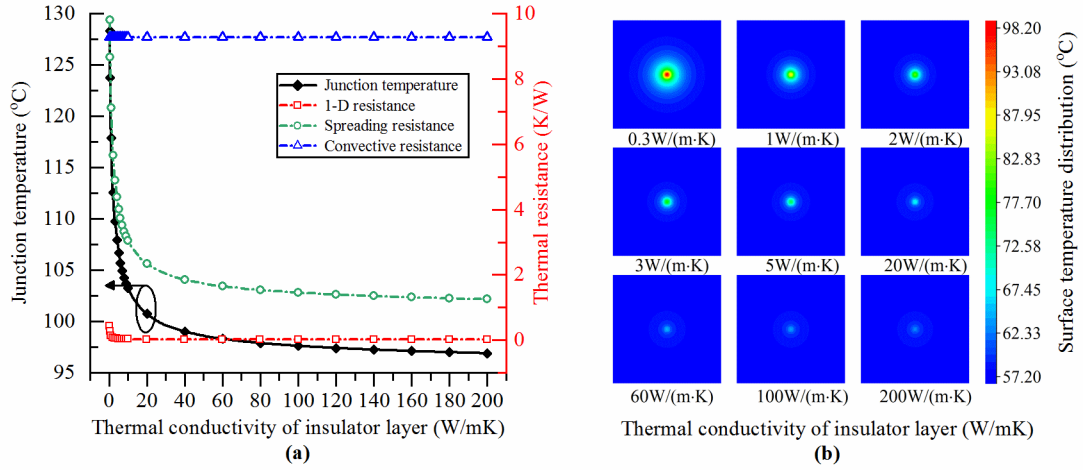

FIGURE 6. (a) Dependence of junction temperature (left y-axis) and thermal resistance (right y-axis) on the thermal conductivity of insulator layer. (b) Surface temperature distribution of copper foil.

A. VERIFICATION AND COMPARISON

To verify the N-layer model and corresponding analytical solutions, the junction temperature versus the side length of the substrate (''substrate'' is defined as the set of all layers) is obtained in different ways. The result from the layered model and the analytical calculation is compared to that of the complete model and the FEM simulation.

In the FEM simulation, three types of meshes are applied, namely, the coarse, normal, and fine meshes. It can be seen from Fig. 4, the result from the analytical calculation is very close to that of FEM simulations, the temperature curves are mostly overlapped with each other. It is worth noting that with the increase of the side length, there is a certain amount of error when the mesh quality is not fine enough. However, the analytical result is always consistent with that obtained by high-quality meshes. When the side length increases from 40 mm to 90 mm, the temperature difference between the analytical method and FEM (with coarse mesh) varies from 0.07 °C to 1.89 °C, varies from 0.01 °C to 0.19 °C (with normal mesh), and is always less than 0.01 °C (with fine mesh). The worse the mesh quality is or the larger the side length is, the greater the error will be. It is because the thinnest layer is only in the tens of micron range, however, the side length of substrate is in millimeters. The huge contrast has already required a large number of grids, the growth of the side length will cause a sharp increase in grid number, even by orders of magnitude. In this situation, it must be costly to maintain high precision, in terms of running time and computational memory. Meanwhile, it is easy to make the simulation difficult to converge and cause error accumulation. For example, when the mesh quality is fine and the side length is 90 mm, the model is discretized to 4,889,387 elements, the total number of degrees of freedom is 8,624,711, and it takes 271 seconds to run the simulation. Not just the time and memory, the model needs to be re-discretized and re-meshed when the side length value changes. However, the calculation

time of the analytical method is only in seconds. It is because the analytical method could realize a direct calculation of the junction temperature without solving the temperature distribution of the whole model. In addition, the increase in model size will not make the calculation more difficult. Therefore, the analytical method is more suitable to deal with the ''thin layer'' problem where the target area is much smaller than the entire model.

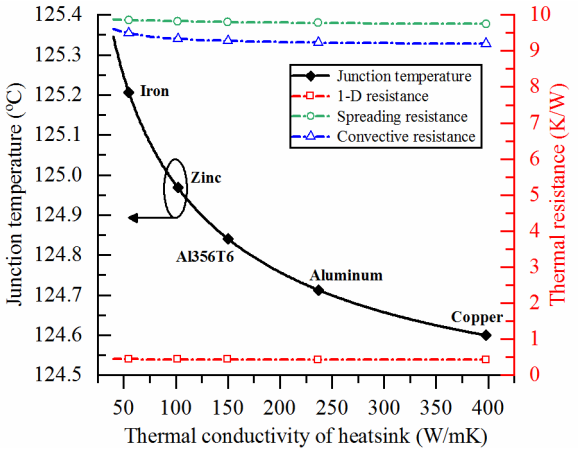

FIGURE 7. Dependence of junction temperature (left y-axis) and thermal resistance (right y-axis) on thermal conductivity of heatsink.

B. IMPACT OF PCB COMPOSITION ON SPREADING RESISTANCE

When the side length of the substrate is 40 mm, the junction temperature is 128.29 °C, and the 1-D, spreading, and convective thermal resistances are 0.43 K/W, 9.80 K/W, and 9.28 K/W, respectively. The high spreading and convective thermal resistances result in bad heat dissipation. Since the LED chip is relatively small to the PCB, heat is impeded when conducted away from the chip. It is easy to cause high spreading thermal resistance and to form an excessive temperature spot near the chip. Considering the direct contact between PCB and LED chip, copper-coating can improve the heat transfer for its high thermal conductivity. As shown in Fig. 5(a), when the thickness of copper foil increases from 35 μm to 315 μm, the junction temperature decreases by 46.65 °C. The 1-D resistance increases negligibly since the ratio of thickness to cross-section is still small. The convective resistance remains unchanged since the available area for convection maintains the same. The spreading resistance achieves a remarkable decline with the increase of copper thickness. It is because the thickened copper layer will improve the heat dissipation by providing wider heat access, and thus greatly reduce heat accumulation near the chip. It can be seen clearly from Fig. 5(b), there is a distinguishing hot spot when the thickness is 35 μm, and it gradually fades away with the increase of copper thickness. It is because the original copper layer is too thin, heat flow quickly reaches the dielectric layer and conducts inadequately to the lateral, which results in an undesirable heat concentration. As the copper layer thickens, the heat flow fully spreads around before it gets blocked.

The PCB contains dielectric material which works as the electrical insulation between the conductor layer and the metal base. The thermal conductivity of common dielectric material is only 0.3 W/(m·K) to 3 W/(m·K) approximately [12]. As a result, the PCB is often regarded as a poor thermal conductor. However, it can be contradicted that such a thin layer seems to make a negligible contribution to thermal resistance. As shown in Fig. 6(a), when the thermal conductivity is 0.3 W/(m·K), the junction temperature is 128.29 °C, and when it increases to 3 W/(m·K), the junction temperature is 109.80 °C. The junction temperature is significantly reduced and the downward trend is almost vertical. It indicates better heat management will be achieved by altering the dielectric material of even higher thermal conductivity. Therefore, traditional materials are no longer applicable, and composite or ceramic materials can be considered. When thermal conductivity varies from 3 W/(m·K) to 200 W/(m·K), the junction temperature decreases sharply at the beginning and changes a little in a considerable range. It is because of the great difference in thermal conductivity between metal and the sandwiched dielectric material, which will cause the discontinuity in heat conduction and high spreading thermal resistance. Therefore, increasing the thermal conductivity has a significant effect on reducing the spreading resistance when it is low. When the thermal conductivity is close to the order of magnitude of metals, the dielectric layer is no longer an obstacle to heat flow. The effect of continuing to increase thermal conductivity is no longer obvious. It can be seen from Fig. 6(b) when the thermal conductivity exceeds 20 W/(m·K), the hot spot has been quite weak and will not change much. It can be concluded that the conductor layer and the insulator layer both have evident impacts on thermal management. It is necessary to divide the PCB into different layers rather than to take it as a single component of low thermal conductivity. In this situation, the analytical method tends to be attractive because the temperature distribution of target regions can be directly calculated. It is especially suitable for the thin layer analysis in a comparatively large system model.

C. IMPACT OF HEATSINK ON CONVECTIVE RESISTANCE

According to (9), when the side length of the substrate is 40 mm, the convective thermal resistance is 9.28 K/W, and it contributes 47.6% of the total resistance. Using heatsinks is a common approach to promote convection. Although the use of high thermal conductivity materials is not directly related to the increase of available heat transfer area, it helps to improve the fin efficiency, and thereby reducing the convective thermal resistance. The candidate material for heatsinks is worth discussing. Several metal materials are selected as follows: iron 55 W/(m·K), zinc 102 W/(m·K), Al356T6 150 W/(m·K), aluminum 237 W/(m·K), and copper 398 W/(m·K). As shown in Fig. 7, the max difference in junction temperature occurs between iron and copper which

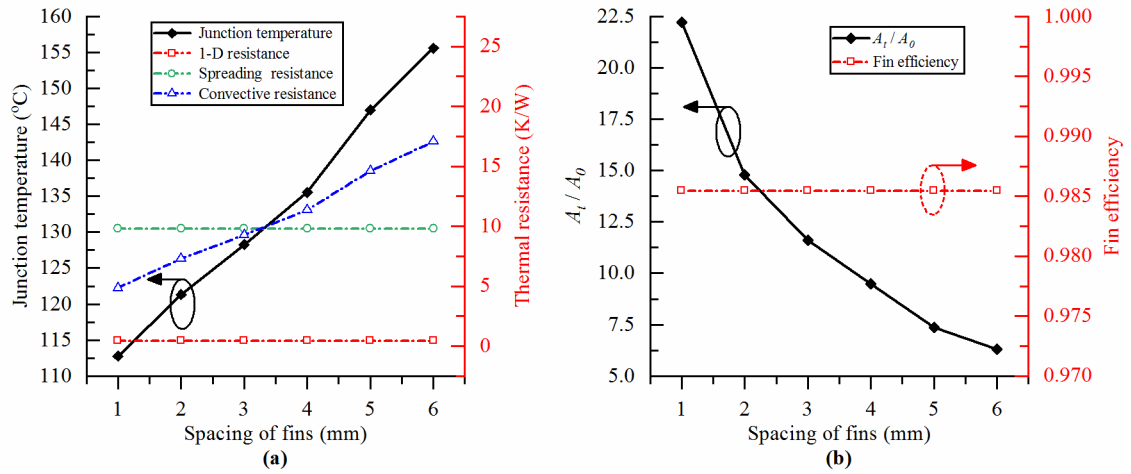

FIGURE 8. Dependence of (a) junction temperature (left y-axis) and thermal resistance (right y-axis); (b) ratio factor (left y-axis) and fin efficiency (right y-axis) on spacing of fins.

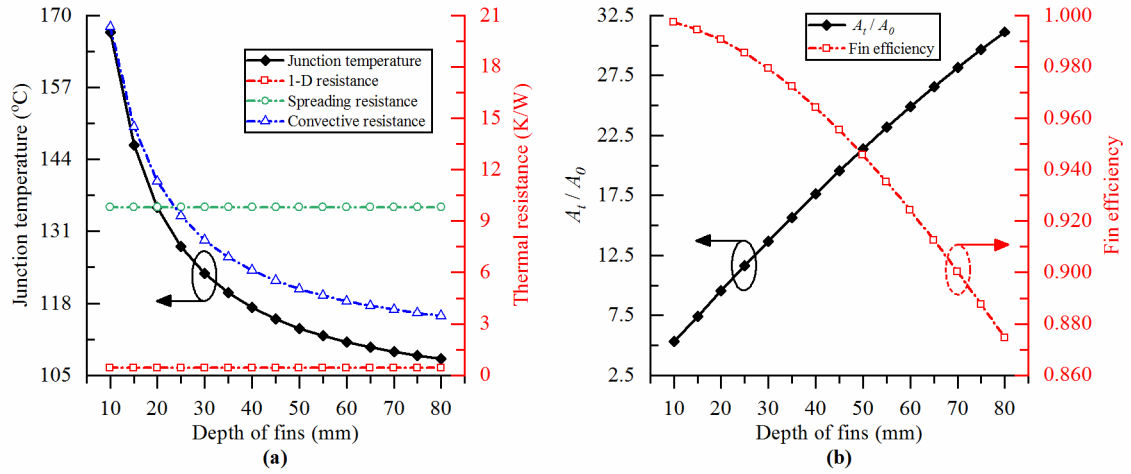

FIGURE 9. Dependence of (a) junction temperature (left y-axis) and thermal resistance (right y-axis); (b) ratio factor (left y-axis) and fin efficiency (right y-axis) on depth of fins.

is only 0.61 °C. The convective resistance decreases slightly by about 0.29 K/W, and the spreading and the 1-D thermal resistances remain virtually unchanged. It is not because the heatsink material does not mean much to promote convection. According to (1), the single fin efficiency is 0.96 for the iron heatsink and 0.99 for the copper. The cooling capacities of the two heatsinks are both sufficient for the current heat power, using a copper heatsink may not be significantly better than the iron one. Just because of this, although the thermal conductivity is much lower than that of copper, aluminum alloy remains the most common material for lower cost and weight.

Besides the material, the structure of heatsinks also plays an important role in its performance. Figure 8(a) shows the dependence of junction temperature and thermal resistance on the spacing of fins. When the spacing increases from 1 mm to 6 mm, the junction temperature rises from 112.78 °C to 155.61 °C, and the convective thermal resistance increases from 4.85 K/W to 17.08 K/W. Figure 8(b) shows fin efficiency remains unchanged since the perimeter and cross-sectional area of the single fin stay unchanged. However, the ratio of the total equivalent area to the original area ($\alpha = A_t/A_0$) drops from 22.23 to 6.31. It is because the number of fins reduces with the increase of spacings, which leads to a decrease in the available area for convection. It shows that the closely spaced fins are preferred because of the larger equivalent area. However, it is noteworthy that the analysis above is based on the assumption that the convective heat transfer coefficient stays constant, with the proviso that the spacing can not be too close to limit the airflow between the fins, thereby reducing the coefficient. The assumption is reasonable to the range of spacings used in this paper [30]. As shown in Fig. 9(a), there is an obvious negative relationship between junction temperature and depth of fins. The longer fins provide a larger area for heat exchange and then lower the convective thermal resistance. When the depth

increases from 10 mm to 80 mm, the junction temperature decreases from 166.99 °C to 107.93 °C. However, the descent rate of junction temperature decreases with the increase of depth. It is because the fin efficiency happens to drop from 0.99 to 0.87 when the depth changes from 10 mm to 80 mm [shown in Fig. 9(b)], which slows down the growth rate of the total equivalent area. When the depth of the fins has been already great, continuing to lengthen the depth will lead to inefficiency and waste. It can be concluded that the heatsink helps to reduce the convective thermal resistance and promote convective heat dissipation, thereby achieving better thermal management. Improving the fin efficiency and optimizing the structure to provide larger equivalent areas can both improve the performance of heatsinks. However, if the heat power is particularly high, especially for the integrated LED arrays, or the module size is strictly limited, it is more appropriate to use coolant or apply the forced convection.

V. CONCLUSION

In this paper, an N-layer model of high-power LED systems is proposed. The model can be used for the analysis and optimization of thermal management of LEDs. Due to the characteristic of the ''N-layer'', the model is flexibly applied to the LED system of different packaging structures. The corresponding analytical solutions to temperature field, junction temperature, and thermal resistance are given, which are generalized to *Nth* to adapt to the model. For verification, the results from analytical calculations with the layered model and FEM simulations with the complete model are compared. The analytical method is proved to be both valid and simple through the comparison. By calculating the junction temperature and thermal resistance of an LED module, the significance of the layer-by-layer analysis is shown. And the impacts of the PCB composition and the heatsink on heat dissipation are discussed. The results reveal strong dependences of spreading thermal resistance on PCB compositions, and convective thermal resistance on heatsink structure, respectively. The work could be helpful to the design and estimation works for high-power LED systems. It is noteworthy that the N-layer model is an ideal model to a certain extent. It is not suited to the LED system of irregular packaging structures. However, it is especially suitable to analyze the ''thin layer'' problem where the target area is much smaller than the entire model.

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