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Assessment of Low-Loss Configurations for Efficiency Improvement in Hybrid Modular Multilevel Converters

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ABSTRACT Hybrid modular multilevel converters (HMMC) address the DC-fault blocking limitations of the half-bridge submodules (HB-SMs) of the standard MMC by combining HB-SMs with full-bridge submodules (FB-SMs). In order to improve the overall conversion efficiency, this article proposes two low-loss configurations for the HMMC. The main improvement in the proposed HMMCs is achieved by the combination of low-loss unipolar and low-loss bipolar SMs in the same arm of the HMMC. It is shown that the simplest structure (LLH1) can reduce the SM losses (switching and conduction losses in an SM) by 30% compared to the HMMC at the cost of limited fault blocking capabilities. The fully controlled structure (LLH2) reduces SM losses by 10% compared to the HMMC, and 30% compared to the FBSM-based MMC. These results represent an increase of 20% over the typical HBSM-based MMC for a converter (LLH2) that can provide fault-blocking capabilities. Assessment of efficiency in both HMMCs is provided over a range of operating conditions both in inverter and rectifier mode from an 800-MVA HVDC system model.

INDEX TERMS High-voltage direct current (HVDC), hybrid power electronics converters, losses, modular multilevel converter, submodules/cells.

I. INTRODUCTION

High-voltage direct-current (HVDC) systems deliver flexible, highly controllable transmission network platforms, well-suited to the challenges of a future power system with high percentage of distributed and renewable energy sources in its energy generation mix [1]. The modular multilevel converter (MMC) enables HVAC-HVDC interconnection and currently represents the most competitive converter topology among all voltage-sourced converters (VSCs) for use in HVDC systems [2], [3]. Its modular and scalable characteristics allow the MMC to meet different voltage level requirements with superior harmonic performance, inherent fault redundancy, reduced voltage ratings of semiconductors, and high efficiency [4], [5]. As a result of these well-recognised advantages, it has become the de-facto topology in HVDC transmission systems. More than 30 projects have been put into operation or under construction utilising MMCs globally [6]. Some notable examples include the Zhangbei DC Grid Project, Nanao Multi-terminal VSC HVDC, BorWin3, etc.

Although the MMC offers many benefits, handling the DC-side faults is a key challenge related to converter protection. The DC faults usually result from faulty cables, pollution, or lightning stroke, and protection against such faults is one of the main limitations of current VSC-HVDC solutions [7]. DC-side faults collectively refer to two types of faults on the DC-side of HVDC systems, pole-to-ground faults and pole-to-pole faults. In practice, pole-to-ground DC faults are more common [8]. However, the impact of pole-to-pole DC faults tends to be more severe. According to this reason, pole-to-pole faults are typically considered in

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worst-case design [9]. Since DC-fault currents have large amplitudes and very high ramp rates, electrical equipment is likely to sustain serious damage. Unipolar SMs, which can only generate one voltage polarity in the output terminals, are not able to clear the DC-side fault current due to the freewheeling effect of diodes [10]. If such a fault occurs, the capacitor in unipolar SMs is discharged rapidly and the diodes may be damaged by over-current [11]. Therefore, introducing DC-side fault blocking capabilities is necessary for expanding the use of MMC-type converter topologies. Meanwhile, as a result of the fast-rising fault currents, fault recognition and clearance must be completed within a short period, typically just a few milliseconds [12]. These requirements create major challenges for DC fault clearing technologies across most MMC-HVDC systems.

One of the commonly used solutions for DC protection is that of a DC circuit breaker (DCCB) as external protection [12]. Many circuit breaker topologies have been developed, including mechanical DCCBs, semiconductor-based DCCBs, solid-state DCCBs, as well as hybrid DCCBs [13]. However, utilising DCCBs requires a whole new set of additional equipment leading to a technically challenging, lossy and expensive solution [9]. Unlike unipolar SMs, bipolar SMs can provide DC-fault blocking capabilities without a DCCB; using bipolar-based MMC could be an alternative approach. Under the blocking state of the converter, all insulated-gate bipolar transistors (IGBTs) in the bipolar SMs are turned off and the converter arm generates a negative polarity voltage that can block fault currents in the DC-side. However, compared to the unipolar SMs configuration, bipolar SMs require more complicated topologies, resulting in both higher cost and higher losses compared to MMCs with unipolar SMs [14]. In addition, another way of providing DC fault blocking capability is through the use of line communicated converter (LCC)-VSC hybrid converter [15], [16]. However, the LCC-VSC is a novel topology rather than a traditional MMC.

In order to balance the needs for lower MMC losses while maintaining fault ride-through capabilities, the relationship between the MMC DC and AC voltages has been studied. The reverse voltage generated by series bipolar SMs in an MMC needs to be greater than the AC voltage (line-to-line) in order to clear fault currents on the DC-side. This means that MMCs with bipolar SMs only require half the total voltage of its arms to block the fault [17]. Consequently, hybrid MMC (HMMC) configurations were proposed to provide such functionality as bipolar-SM-based MMC with reduced cost and losses. The typical configuration of the HMMC uses bipolar full-bridge SMs (FB-SMs) and unipolar half-bridge SMs (HB-SMs) [18], which also correspond to two of the most commonly used SMs in practical applications. An alternative to the HMMC for bipole HVDC systems was developed, formed by two symmetrical MMCs, which consists of one arm based on diagonal-bridge SMs (DB-SMs) and a second arm with HB-SMs in each pole of the bipole [19].

In VSC-HVDC projects, the losses of converters in the high voltage and high power transmission account for a great proportion of the total losses of converter stations [20], thus the evaluation of losses is very essential in MMC. The high losses in MMC lead to both the lower overall converter efficiency and the increased life cycle cost of the whole system. Besides, the size as well as the cooling requirements in an SM design are affected by the power losses. Therefore, the reduction of losses is a key priority in the design of the MMC. Compared to FB-SM-based MMC, the HMMC demonstrates lower losses and the DC-side fault clearing capacity as it uses fewer semiconductor switching devices [17]. However, in terms of losses, HB-SMs and FB-SMs do not represent the most effective options in HMMC, since there exist both unipolar and bipolar SMs which have lower losses than HB-SM and FB-SM, separately [21], [22]. Consequently, there are other SM configurations which can provide similar functionalities to the HMMC at potentially lower losses.

An overview of DC-fault clearing approaches for MMCs in HVDC systems and the development of HMMCs are provided in this paper. This work aims to identify optimal configurations in terms of SM topology and a combination of SMs at a hardware level, from a loss perspective, for an HMMC that provides similar functionalities to the HB-FB HMMC at lower loss [17]. Based on prior reviews of the literature, three low-loss SM topologies have been utilised in the novel HMMC to replace the conventional HB-SMs and FB-SMs. Building on the modelling of an 800-MVA HVDC transmission system, two low-loss hybrid configurations for the MMC are proposed in this work as alternatives to HMMC. This work offers an assessment and evaluation of efficiency in MMCs and HMMCs for HVDC systems to support the theoretical analysis. In addition, detailed comparisons and analysis of losses for SMs in HMMCs over a range of operating points are provided.

II. DC FAULTS AND THE HYBRID MMC

A. DC FAULT CLEARING

To prevent severe damage caused by DC-side faults, it is essential for an MMC to have a quick response to ride-through the fault currents, especially in overhead lines [23]. When a non-permanent DC fault occurs, MMCs are required to clear the DC-side fault so as power transmission can be resumed as quickly as possible. Three main approaches that deal with DC-side faults in the MMC are considered practical: *i)* using a DCCB to isolate the fault, *ii)* utilising bipolar SMs that provide DC fault blocking capability, or *iii)* using an LCC-VSC hybrid converter.

In recent years, many topologies of DCCB have been proposed in the literature. Among them, the hybrid DCCB, which has fast current interruption capabilities, has drawn the greatest attention from a commercial perspective [12], [24]. Unlike a common circuit breaker, the hybrid DCCB contains a main DC breaker, an additional low-loss branch as well as an energy dissipation branch [11]. It is illustrated

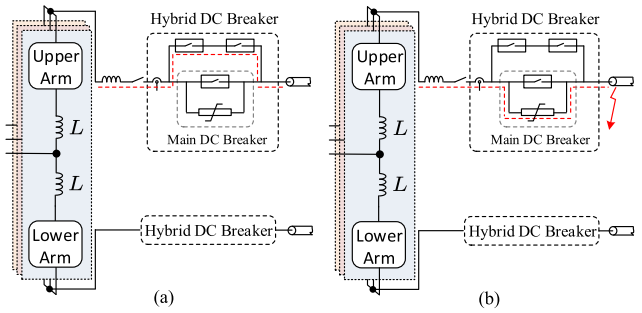

FIGURE 1. Fault clearing process of DCCB in MMC: (a) before fault, and (b) during fault after blocking.

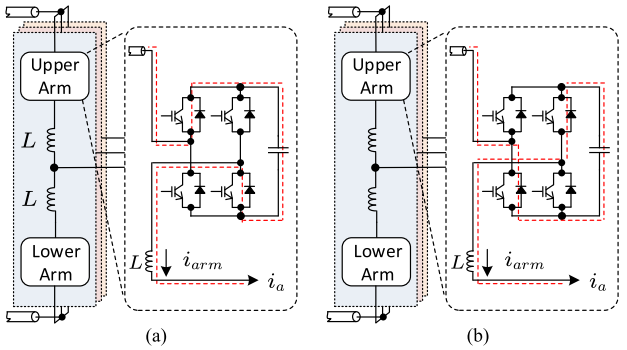

FIGURE 2. Fault clearing process of FB-SM-based MMC: (a) before fault, and (b) during fault after blocking.

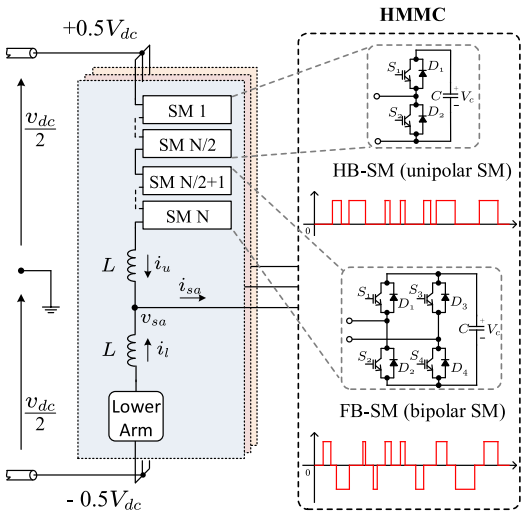

FIGURE 3. Configuration of HMMC.

in Fig. 1, the current in hybrid DCCB flows through the additional branch during normal operating condition, keeping zero current passing through the main DC breaker. During the DC-side fault, the bypass is open and the current has to flow through the main DC breaker. Thus, with the assistance of the energy dissipation branch, current could be interrupted using the main DC breaker [25]. The DCCB has the ability to interrupt the short-circuit currents within a short period and the energy stored in the inductors can be dissipated [26]. Meanwhile, the DCCB is lossy and expensive for utilisation, which is a critical hurdle for their mainstream adoption in HVDC systems.

In terms of employing bipolar SMs to handle DC-side faults, the FB-SM is the most common topology [27]. Different from some non-controllable bipolar SMs, the FB-SM can output negative voltages regardless of the arm current direction. The fault clearing process of FB-SM-based MMC is illustrated in Fig. 2. In its blocking state, the IGBTs of the FB-SM are turned off, thus the diodes provide paths for the arm current; the reverse voltage is generated by the SM capacitors to block the DC-side fault. The benefit of the FB-SM is that it has DC-fault blocking capabilities without disconnecting the converter, which allows for faster system recovery. However, compared with HB-SMs, twice as many semiconductors are required leading to higher cost and losses.

B. HYBRID MMC

An HMMC uses both HB-SMs and FB-SMs in each of the converter arms (Fig. 3) while each phase-leg comprises two arms (one upper and one lower arm). One arm of the HMMC includes one inductor and N SMs as HB-SM and FB-SM combinations, typically half of them are FB-SMs while the other half are HB-SMs. Thus, in comparison with the FB-SM-based MMC, an HMMC provides capability to block a DC fault with fewer components and reduced losses. This paper only considers the situation that no negative output voltage is generated under normal states in HMMC. Assuming that the number of FB-SMs in each arm is M, capacitor voltages are equal to V_c for all SMs, and the modulation index of the HMMC is 1. Since the arm voltages lie between 0 and NV_c, the DC voltage for the HMMC is given by

$$V_{dc} = NV_c \tag{1}$$

The maximum value of AC voltage for the HMMC is

$$V_{ac}^{max} = \frac{1}{2}V_{dc} = \frac{1}{2}NV_c \tag{2}$$

If taking into account the negative output of FB-SMs in HMMC under normal states, the modulation index of HMMC can be beyond 1. By increasing the value of modulation index, and for a given DC voltage, a higher AC voltage can be generated. Similarly, when the DC-side voltage is reduced, the AC voltage can be maintained constant [28]. As a result, the flexibility can be extended in HMMC. A complete design study about modulation index for the HMMC was presented in [29], including analysis of the influence of the modulation index selection on the number of SMs as well as the overall efficiency of the HMMC.

The capacitance and voltage ripple of capacitors in SM are the key factors affecting the operation, cost, as well as size of an MMC. Due to the differences between HB-SMs and FB-SMs, as well as the increased modulation index, the capacitor voltage ripple and balancing in an HMMC is more complicated [30], [31] than a non-hybrid MMC. To address this issue, the different behaviours of FB-SM and HB-SM

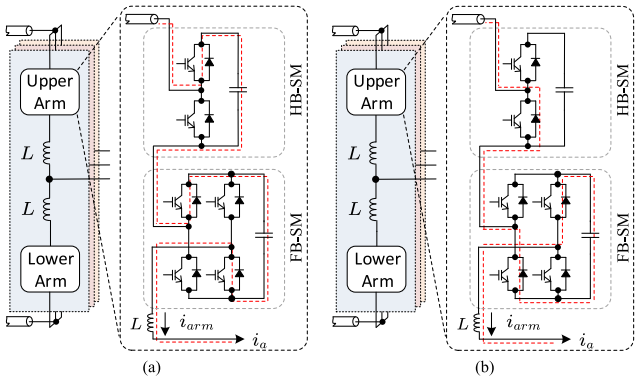

FIGURE 4. Fault clearing process of HMMC: (a) before fault, and (b) during fault after blocking.

should be considered at the design stage. A method for selecting the SM capacitor voltages was proposed in [32], which also defines three kinds of SM capacitor voltage ripple and provides analysis of charging and discharging periods in capacitors in HMMC. To balance the voltages and reduce the voltage ripple in capacitors in an HMMC, a second-order circulating current injection method was also developed [33]. By modifying the injected circulating current via various phase angle and amplitude, both reduced capacitor voltage ripple and balanced capacitor voltage can be realized with lower current stress of semiconductor devices.

The differences between HB-SMs and FB-SMs in an HMMC also lead to uneven loss distribution and mismatched pulses in the voltages in output terminal. Reference [18] proposed an improved phase-shifted carrier modulation scheme to mitigate the uneven distribution and eliminate the mismatches, by decreasing the switching frequency in FB-SMs and setting an appropriate phase-shift angle between HB-SM and FB-SM in triangular carriers.

C. FAULT CLEARING IN HMMCs

The DC-fault clearance process of the HMMC when the converter is in normal state and during fault after blocking is illustrated in Fig. 4. In normal state, the FB-SM is not required to generate negative voltages. Therefore, the circuit of the HMMC can be seen as topologically similar to the conventional MMC based on HB-SM. However, when a DC-side fault occurs, the negative outputs of FB-SMs in the HMMC begin to take effect. During the DC-fault, the HB-SMs are bypassed while the capacitors in FB-SMs are charged, which forms an AC feeding path to block the DC-fault currents.

Considering the DC fault ride-through capability of the HMMC, the number of the two sorts of SMs in an HMMC should meet certain requirements. According to (2), during the DC fault, the maximum line-to-line AC voltage in the HMMC is

$$u_{max} = \frac{\sqrt{3}}{2} N V_c \tag{3}$$

Since there are M FB-SMs presented in one arm, the reverse voltage that generated by the SMs during faults on the DC-side is

$$u_{arm} = M V_c \tag{4}$$

To block the DC-side fault successfully, the reverse voltages formed by the two arms has to be larger than the amplitude of AC line-to-line voltage during the fault.

$$2u_{arm} = 2M V_c \geq \frac{\sqrt{3}}{2} N V_c = u_{max} \tag{5}$$

Therefore, considering fault blocking in the HMMC, the number of FB-SMs in each arm should meet the following criteria:

$$M \geq \frac{\sqrt{3}}{4} N \tag{6}$$

The modulation index and charging and discharging time in the HMMC also define the number of unipolar and bipolar SMs that can be used in the topology [17], [32]. According to (6), in each arm of the HMMC, two possible solutions for the number of HB-SMs and FB-SMs are:

- $1/2N$ HB-SMs, $1/2N$ FB-SMs
- $1/3N$ HB-SMs, $2/3N$ FB-SMs

To illustrate the DC-side fault clearance after blocking of the HMMC, a detailed dynamic model was presented in [34]. This model provides analysis of minimizing the time of fault clearance and over-voltages of capacitors, which contributes to the design of DC fault clearance strategies. A fault ride-through strategy was developed and verified in [35] to deal with both sorts of DC-fault in the HMMC. The strategy realizes the DC-side fault clearance and continuous operation for pole-to-ground fault in HMMC. Another option is the continuous operation as a Static Synchronous Compensator (STATCOM) in the case of a pole-to-pole DC-side fault. In order to avoid energy dissipation and achieve faster power recovery, the DC-side fault currents can be interrupted from the source side by using the negative output of FB-SMs [36]. This approach can also be applied to radial and meshed DC grids, as well as HVDC systems in symmetrical bipolar and monopole configurations.

III. LOSSES OF SMs

A. SMs FOR MMCs

The main component of the MMC is its SMs, which contribute to the modularity of the topology. The MMC arm is composed of series connected SMs and operates as a controllable voltage source. The arm voltage is defined by the number of SMs inserted in the arm at any time. The internal structure of the SM provides many of the features of an MMC, such as its fault blocking capability, reliability and redundancy, and internal voltage balance demands. In addition, the topology of an SM defines many operational variables, such as its switching frequency, power losses, capacitor voltage, etc. As a result, there are over 50 topologies of SM proposed for MMCs in the last 15 years. Considering the requirements of HVDC transmission, the total number of SMs under consideration can be further reduced to 27 [37], which includes both unipolar and bipolar configurations.

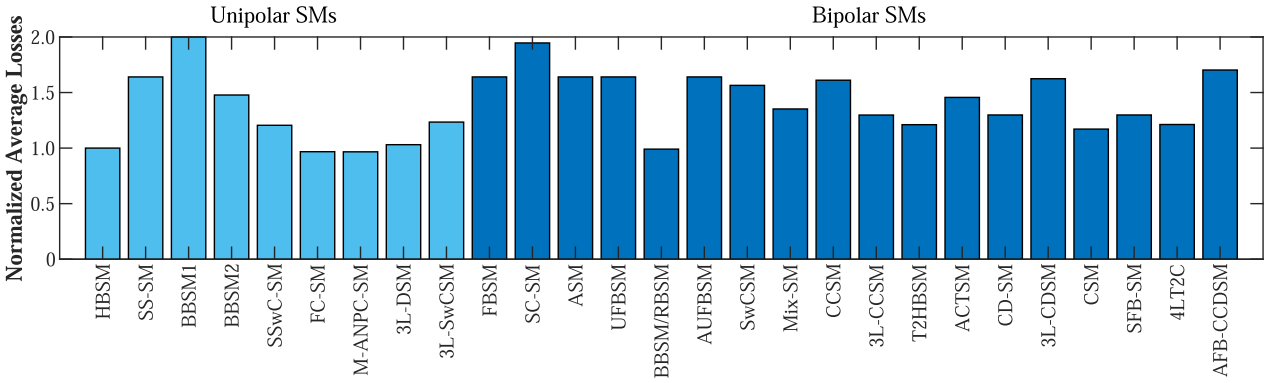

FIGURE 5. Average losses of SMs in an MMC. All values presented in the figure are normalized to the value of the HB-SM losses [37].

In terms of the ability of generating negative output voltages, SMs can be classified into unipolar SMs or bipolar SMs. The unipolar SMs can only generate positive voltage levels, however, bipolar SMs can generate either positive or negative output voltages. Thus, bipolar SMs that normally have more semiconductor devices can inject opposite voltages to block the DC-fault current. While for unipolar SMs, a separate device (e.g. DCCB) is demanded to provide the capability of the dc-fault blocking [10]. Other SM categories consider the output voltage levels, dc-fault ride-through capability, negative output voltage controllability, etc.

In these SMs, HB-SM and FB-SM are the most conventional SMs with simple topologies and have been widely utilised in practice. The switched capacitor SMs contain two capacitors that can be either connected in series or parallel, leading to the same voltages of capacitors in single SM [38]–[40]. Consequently, only half of voltage sensors are required and voltage ripple in capacitors are reduced. Some neutral point clamped (NPC) and T-type SMs have been excluded from the analysis since they could not assure the same charging and discharging time in different capacitors. In order to address this issue, the extension of T-type SMs have been proposed with more complicated topologies and voltage balancing capability [41], [42]. In addition, some unidirectional SMs cannot meet the requirements in HVDC applications as they only operate under specific current direction. A comprehensive introduction and analysis of the SMs that are suitable for HVDC applications can be found in [37].

B. LOSS CALCULATION AND COMPARISON

In the detailed SM loss calculation model, a common device has been used across all different SMs to maintain consistency of results. A heat sink is utilised in the thermal model to offer a common isotherm environment to IGBTs and diodes in SMs, and the switching energy losses of semiconductor devices are added based on the thermal description provided in the corresponding datasheet [43]. In order to generate the switching signals to the different SMs, individual sorting algorithms for each SM have been developed in the model with the measurement of all capacitor voltages, the direction of arm currents, and external switching signal used by the internal voltage balancing algorithm. The total losses of SMs consist of both the conduction losses and switching losses, which are calculated separately by the blocks in the model and added together. Detailed explanation of the losses calculation process of MMC SMs refers to [22].

In order to compare the SM power losses directly, 27 SMs were classified into 9 unipolar SMs and 18 bipolar SMs. The average losses are illustrated in Fig. 5, in which unipolar and bipolar SMs are lumped together. The results of SM losses are from MMCs that use only one SM configuration (i.e., not hybrid MMCs). To make a more direct comparison and eliminate other effects, the SM losses have been normalized to the HB-SM losses. The losses normalization also takes into account the number of output voltage levels, since the number of SMs used in each MMC arm are not the same for different topologies. It can be seen that due to more complicated structures that provide additional functionalities, the losses of bipolar SMs are generally higher than the losses of unipolar SMs.

Concerning the unipolar SMs, structures such as the bidirectional blocking SM1 (BBSM1) may incur up to double the losses of the HB-SM because of the bidirectional switch which consists of four diodes and an IGBT. Another example is that of the series switch SM (SS-SM) which may incur up to 1.7 times the losses of the HB-SM due to additional switches added at the midpoint of HB-SM. On the other hand, the lowest loss is shown in modified active neutral-point clamped unipolar SM (M-ANPC-SM, Fig. 6), which is 0.1% lower than the flying capacitor SM (FC-SM) and 3.3% lower than the HB-SM. The low loss of M-ANPC-SM is the result of the shared currents in two parallel current paths during bypass state. Thus, the M-ANPC-SM is a great candidate for a unipolar SM in the design of low-loss HMMCs.

For bipolar SMs, the single-clamped SM (SC-SM) presents the highest losses, generating about 1.9 times the average losses of a HB-SM. The lowest loss is observed in the bidirectional blocking SM (BBSM)/reverse blocking SM (RBSM)

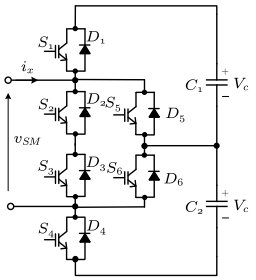

FIGURE 6. The topology of M-ANPC-SM.

TABLE 1. M-ANPC-SM switching states table.

States	S_1	S_2	S_3	S_4	S_5	S_6	V_{out}	I_x>0	I_x<0
State 1	0	1	1	0	1	1	0	-	-
State 2	0	0	0	1	1	0	V_C	C_2 charging	C_2 discharging
State 3	1	0	0	0	0	1	V_C	C_1 charging	C_1 discharging
State 4	1	0	0	1	0	0	$2V_C$	C_1C_2 charging	C_1C_2 discharging

at about 60% of the losses of the FB-SM. However, the fault blocking capability is provided by an auxiliary capacitor that charges through the fault current, rather than the main SM capacitor. Certain bipolar SMs with low losses like the self-blocking composite multilevel SM (CSM) or the T-type half-bridge-based SM (T^2HBSM) have fewer negative voltage level than their positive level. Although they have DC-fault blocking capability, they cannot block the DC-side fault for the whole MMC in hybrid configurations, thus they are excluded in the subsequent analysis. The active clamped T-type SM (ACTSM), which has two both positive and negative output levels, becomes the second candidate for bipolar SM in low-loss HMMC.

IV. LOW-LOSS HYBRID MMC CONFIGURATIONS

Different low-loss SM topologies are available in the current literature. By utilizing lower loss SM configurations in an HMMC, there are opportunities for optimization of hybrid configurations. Based on the previous analysis, this section introduces two low-loss hybrid MMC configurations.

A. STRUCTURE OF LOW-LOSS HMMC 1 (LLH1)

As discussed in Section III, the unipolar SM that has the lowest loss is the M-ANPC-SM, which is a modification of the NPC-SM, addressing the voltage balancing issues of that SM. This is achieved by replacing two diodes with switches, and also modifying the terminals in the NPC-SM [41]. Referring to the switching states in Table 1, the two capacitors of the M-ANPC-SM can be charged and discharged separately to provide the same charging and discharging time. At zero output level, the four middle switches are on, with the current shared between the two possible paths.

In terms of bipolar SMs, the BBSM/RBSM (Fig. 7) that replaces the lower switch in the HB-SM by two anti-paralleled RB-IGBTs, has the lowest losses. A bypass circuit including an auxiliary capacitor and one diode is

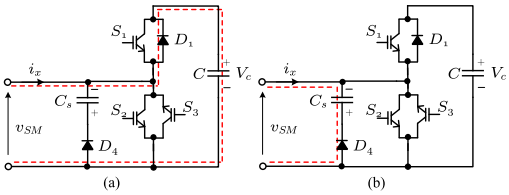

FIGURE 7. The topology of BBSM: (a) normal state, and (b) blocking state.

TABLE 2. BBSM/RBSM switching states table.

States	S_1	S_2	S_3	V_{out}	I_x>0	I_x<0
State 1	0	1	1	0	-	-
State 2	1	0	1	V_C	C charging	C discharging
State 3	0	0	0	V_C	C charging	-
State 4	0	0	0	$-V_{cs}$	-	C_S charging

TABLE 3. ACTSM switching states table.

States	S_1	S_2	S_3	S_4	S_5	S_6	V_{out}	I_x>0	I_x<0
State 1	0	1	1	1	1	0	0	-	-
State 2	1	0	0	1	1	0	V_C	C_1 charging	C_1 discharging
State 3	0	1	1	0	0	1	V_C	C_2 charging	C_2 discharging
State 4	1	0	0	0	0	1	$2V_C$	C_1C_2 charging	C_1C_2 discharging
State 5	0	0	0	0	0	0	$2V_C$	C_1C_2 charging	-
State 6	0	0	0	0	0	0	$-2V_C$	-	C_1C_2 charging

connected in parallel with the two RB-IGBTs [44]. In normal operation, S_3 is always on while S_1 and S_2 operate in complementary states to generate different output voltage levels, which is shown in Table 2. When the DC-side fault occurs, as shown in Fig. 7b, the bypass circuit provides the DC-fault blocking capability to the BBSM/RBSM.

B. STRUCTURE OF LOW-LOSS HMMC 2 (LLH2)

The BBSM/RBSM in LLH1 has the lowest losses in bipolar SMs, however, it is not an optimal choice due to its topology. In BBSM/RBSM, the auxiliary capacitor in the bypass snubber circuit, which generates reverse voltage, is smaller compared with normal SM capacitor and may discharged slowly because of the parasitic resistance. While adding another capacitor in the SM leads to higher cost and larger occupation. Therefore, although the LLH1 has the lowest losses, the topology of BBSM/RBSM is less practical in a hybrid configuration due to its limited DC fault blocking capability.

The ACTSM (Fig. 8) is an extension of T-type SM with lower losses, in which S_2 and S_3 operate as a bidirectional switch [45]. The dotted red line in Fig. 8a illustrates the path of current flow when the SM is under state 4 in Table 3 and the current is positive. During a DC-side fault, the two capacitors are charged in series leading to $-2V_c$ blocking output in ACTSM. Consequently, when the DC-side fault occurs, the negative voltage generated by the ACTSM can block the fault for the whole HMMC including the unipolar SMs.

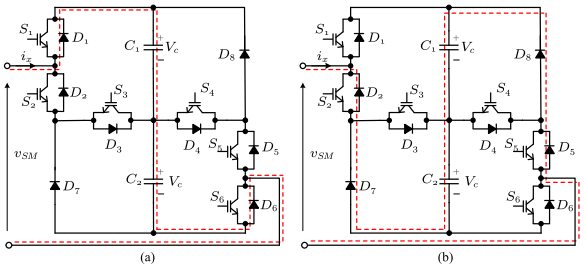

FIGURE 8. The topology of ACTSM: (a) normal state, and (b) blocking state.

C. COMPLETE HMMC HVDC SYSTEM

The configuration of two types of the proposed low-loss HMMC in this study is shown in Fig. 9. Similar to the HMMC, half of the SMs are unipolar and the other half are bipolar SMs in each arm of the two proposed HMMCs. In order to achieve the lowest loss HMMC, LLH1 combines the M-ANPC-SM as unipolar SM with the BBSM/RBSM as bipolar SM. For achieving the same number of output levels, since the M-ANPC-SM is a three-level SM, the number of M-ANPC-SMs in LLH1 should be half of HB-SMs used in an equivalent HMMC. During a DC-side fault in MMC, the M-ANPC-SMs are bypassed while the BBSMs/RBSMs are blocked, which leads to similar fault response as the HMMC.

Due to the limited DC fault blocking capability in BBSM/RBSM, LLH2 MMC with a mixture of ACTSM and M-ANPC-SM is also proposed. The ACTSM is a 3-level bipolar SM, thus the number of ACTSM is half of the BBSM/RBSM in LLH1. Similar to LLH1, the M-ANPC-SMs are bypassed while the ACTSMs are blocked during the DC-side fault. Therefore, fault ride-through capability is provided by both LLH1 and LLH2 configurations, proposed in this work.

In this paper, an 800 MVA, ±200kV, 400-SM per arm MMC-HVDC system is utilised for loss calculation. The nominal voltage in each SM is selected equal to 1 kV, which allows for the selection of the FZ1500R33HL3 Infineon IGBT module [43] (i.e. a device used in current HVDC systems) as the common device across all SM topologies. For this module, the steady-state current rating is 1.5 kA and the voltage rating is 3.3 kV. In order to mitigate the second-harmonic components of the arm currents, the circulating current suppression controller (CCSC) is utilised in the system.

Since the system configuration is universal, Fig. 10 provides not only output (voltage and current) but also internal (arm currents and SM capacitors) waveforms of the HVDC system under inverter operation at unity power factor. The large amplitude of the 401-level multilevel output voltage results in low distortion, sinusoidal (Fig. 10b) output currents. Controllers for balancing of the SM capacitor voltages and regulation of the circulating currents eliminate the impact of higher order harmonics in the currents of MMC arm (Fig. 10c) as well as average voltages of SM capacitors (Fig. 10d).

An MMC switching model considering all 400 SMs would require extraordinary high computational capacity and long simulation times. On the other hand, simulating a single SM in the MMC would not provide appropriate representation for the voltage balancing requirements of the HMMC or meet other simulation criteria. Consequently, a hybrid model for the MMC arm, based on switching SM and average model has been used [21]. One of the arms of the MMC (in this model, phase *A* and the upper arm are selected) is shown in Fig. 11,

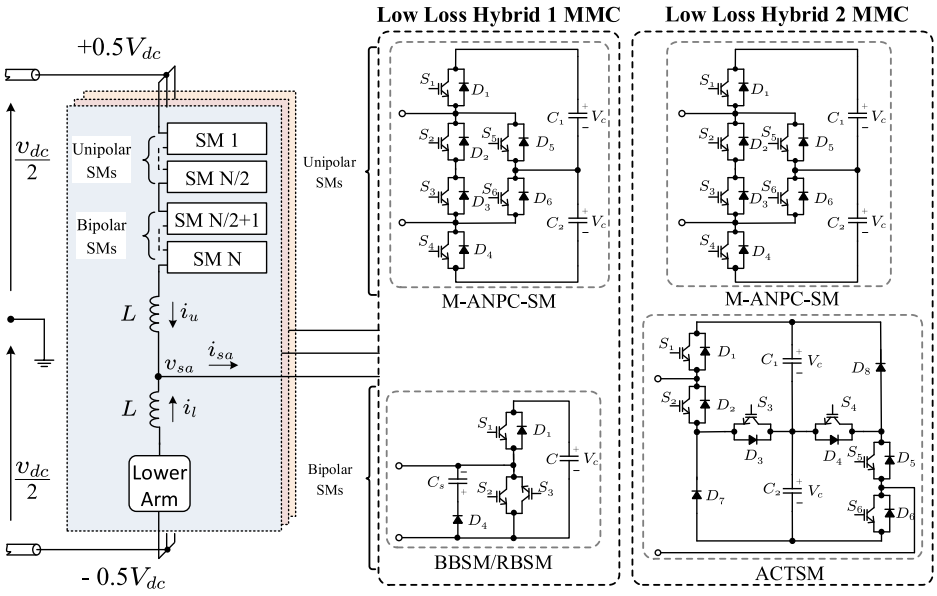

FIGURE 9. Configuration of the two proposed low-loss HMMC.

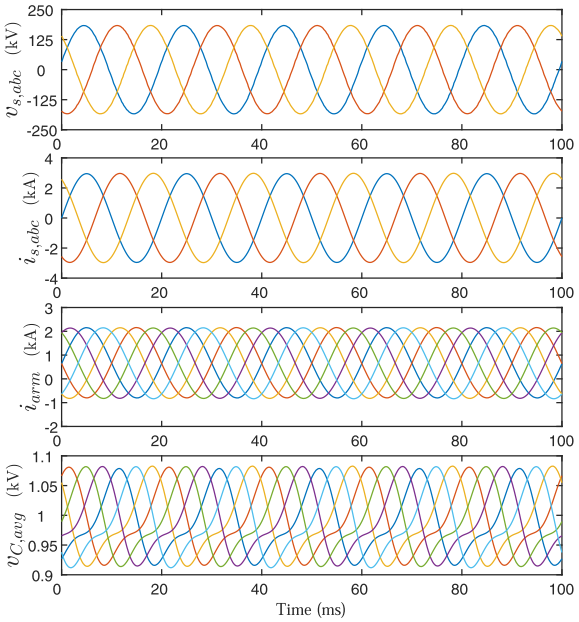

FIGURE 10. Waveforms of currents and voltages in generic unipolar / bipolar hybrid MMCs in the HVDC system: (a) converter voltages ($v_{s,abc}$), (b) output / load currents ($i_{s,abc}$), (c) currents (i_{arm}) in the converter arms (6 waveforms), and (d) average voltages ($v_{C,avg}$) of the SM capacitors (6 waveforms).

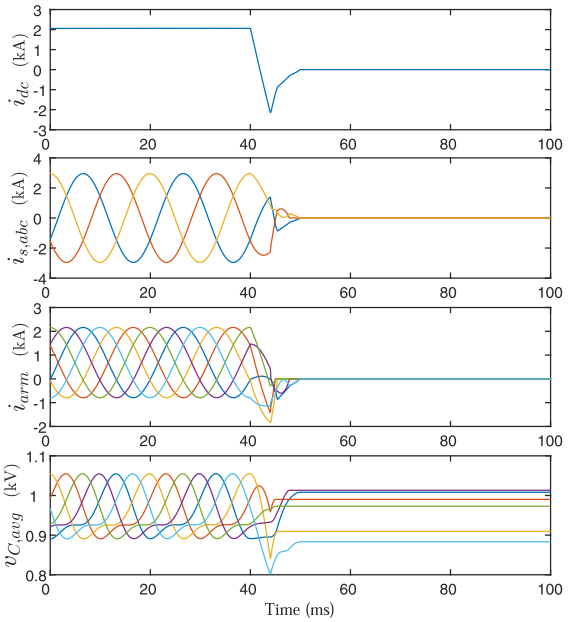

FIGURE 12. Waveforms of currents and voltages in the typical HMMC when DC-fault occurs: (a) DC current (i_{dc}), (b) output / load currents ($i_{s,abc}$), (c) currents (i_{arm}) in the converter arms, and (d) average voltages ($v_{C,avg}$) of the SM capacitors.

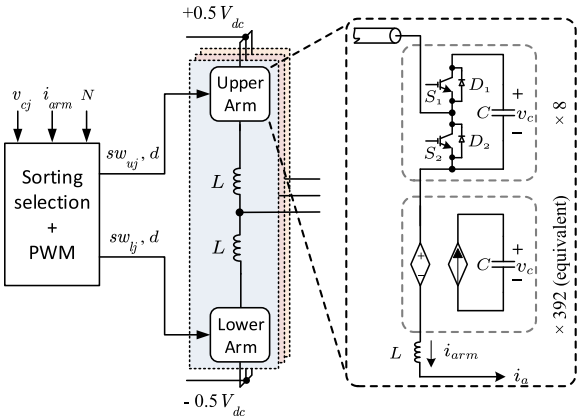

FIGURE 11. Hybrid MMC arm modelling based on switching and average models.

The hybrid model realizes 8 SMs in a detailed switching representation and the remaining SMs (392) are represented in the arm average model. The rest of the converter is also modelled using an average representation [46]. Experimental verification of losses and thermal performance for a single SM were provided in [47], verifying that the switching average model can provide an accurate representation of power losses as the detailed switching model. This method simplifies the whole model, and also retains the detailed information required for SM loss analysis under various operating conditions.

The DC-fault blocking capability and response of the HMMC with 50% unipolar SMs and 50% bipolar SMs in the HVDC system is shown in Fig. 12. While the system operates in steady-state, a pole-to-pole DC-fault is applied in the HMMC at 40 ms with very small fault impedance (0.1 Ω), used to represent a worst case of DC-fault. After the occurrence of the DC-side fault, the HMMC remains working and the blocking time after detection of the fault is 4 ms. It can be seen that during this period, the current in the DC-side (Fig. 12a) collapse and the currents in the converter arms (Fig. 12c) increase sharply. After the blocking time, the over-currents are detected and the HMMC can be blocked by bipolar SMs. The capacitors in SMs start charging (Fig. 12d) thus reverse voltages are generated to block the DC-fault. Eventually, the DC current, output currents, and arm currents fall into zero within 10 ms after converter blocking.

V. RESULTS AND COMPARISON

The following section provides results for the different HMMCs, as well as a comparison with non-hybrid MMCs using HB-SMs and FB-SMs across multiple operating conditions.

A. AVERAGE LOSSES AT UNITY POWER FACTOR

Fig. 13 shows the average losses of the two non-hybrid MMCs and the three HMMCs at unity power factor. Operation of all five MMCs are considered under both rectifier and inverter modes. In order to provide a direct comparison between the losses of the different MMCs, the losses are normalized to the HB-SM-based MMC losses in the two operation modes, separately.

The extremes of the losses are seen in the non-hybrid MMCs, with the lowest losses measured in the HB-SM MMC and the highest losses in the FB-SM MMC. This is anticipated

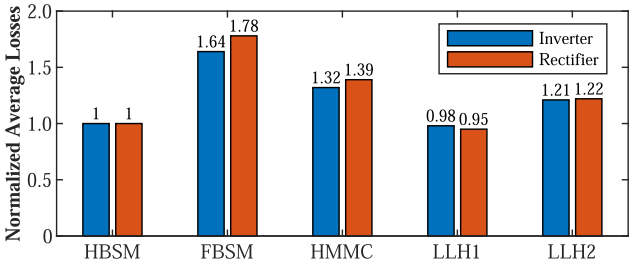

FIGURE 13. Normalized average losses of the five MMCs considered in this analysis.

as it aligns with the comparison of SM losses in Section III and previous literature in the topic. These two values also define the benchmarks for the HMMCs. The combination of HB-SMs and FB-SMs in the HMMC offers the ability to block DC side faults, while the losses remain lower (≈20% lower in inverter mode and ≈22% lower in rectifier mode) than the losses of the FB-SM MMC.

Compared to HMMC, both low-loss HMMCs offer a reduction in the losses. The lowest loss occurs in LLH1; ≈5% lower than the HB-SM MMC and ≈30% lower than the HMMC, while 60% lower compared to the FB-SM MMC. This is directly attributed to the lower losses of the M-ANPC-SM that is used instead of the HB-SM. The fully controllable bipolar ACTSM used in LLH2, replacing the BBSM, will result in higher losses, as shown in Section III. The losses are approximately 1.2 times the losses of the HB-SM MMC, but more importantly ≈10% lower than the losses of the HMMC. The result shows that, while realizing the same function, both of the two low-loss HMMCs have lower losses than the FB-SM-based MMC and HMMC.

B. EFFECT OF POWER FACTOR ANGLE

Simply using the normalized average value for the losses does not provide an accurate reflection of the converter losses as neither the internal SM voltage balancing requirements, nor the influence of the SM voltage balancing algorithm for the converter arm are reflected. Therefore, using a single value cannot demonstrate the further effects on the consecutive period losses and expected minimum and maximum losses. In order to incorporate these aspects in the analysis, this section provides continuous simulation and statistical analysis under steady-state operating conditions. This section takes into account the median loss, the loss within the interquartile range over a predetermined period, and the minimum and maximum losses of a single time period in the time interval. The red marks correspond to the average value of the losses in the MMC over the same time interval.

Figs. 14 to 16 show the losses of all HMMCs across seven different power factor set-points and both operation modes. Since HVDC converters are mainly operated at unity power factor (or close to unity) and the converter is unlikely to operate at low power factors ($pf < 0.7$) for a long time, this work only considers the power factors within the typical working range for analysis. Again, the SM losses have been

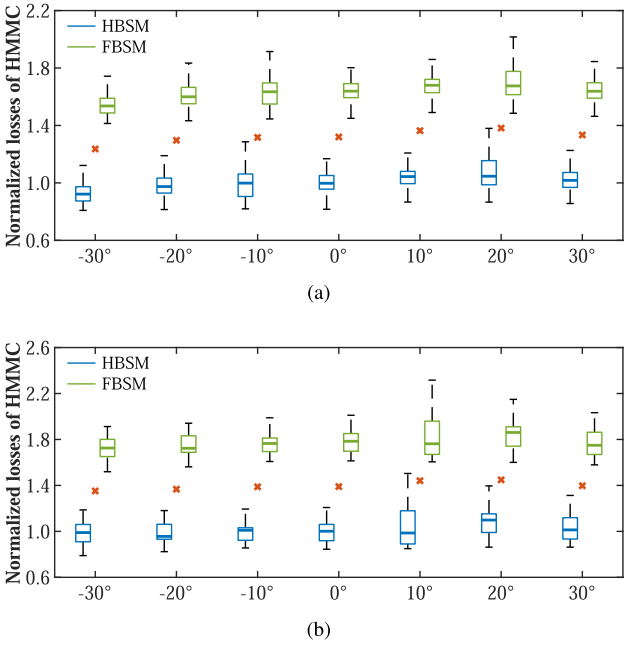

FIGURE 14. HMMC losses in: (a) inverter mode, and (b) rectifier mode.

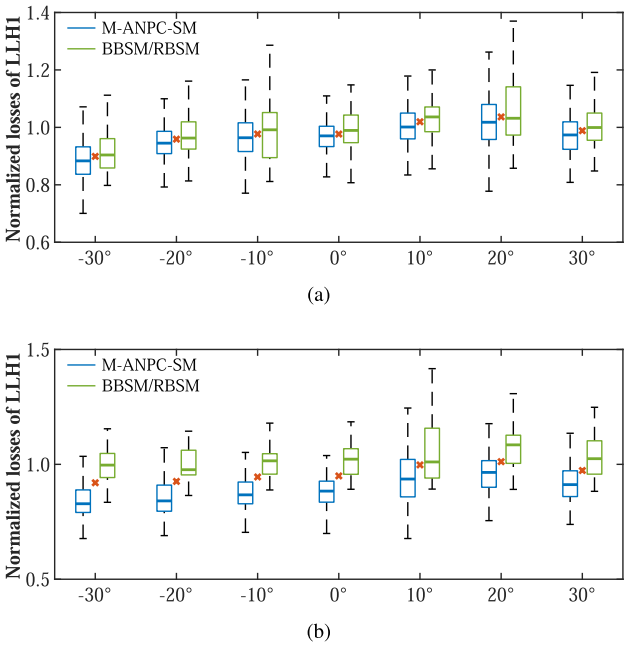

FIGURE 15. LLH1 MMC losses in: (a) inverter mode, and (b) rectifier mode.

normalized to the average value of the HB-SM losses per level in the two operation modes at unity power factor, separately. The average losses of MMCs have been normalized to the average loss of the HB-SM MMC at unity power factor.

The average losses of the HMMC are 1.25 - 1.45 times the losses of HB-SM MMC at the operated power factors (Fig. 14). The variation of average losses in the HMMC at different power factor angles is about 10%. For the two SMs, the median of FB-SM losses are 1.5 - 1.8 times higher than the

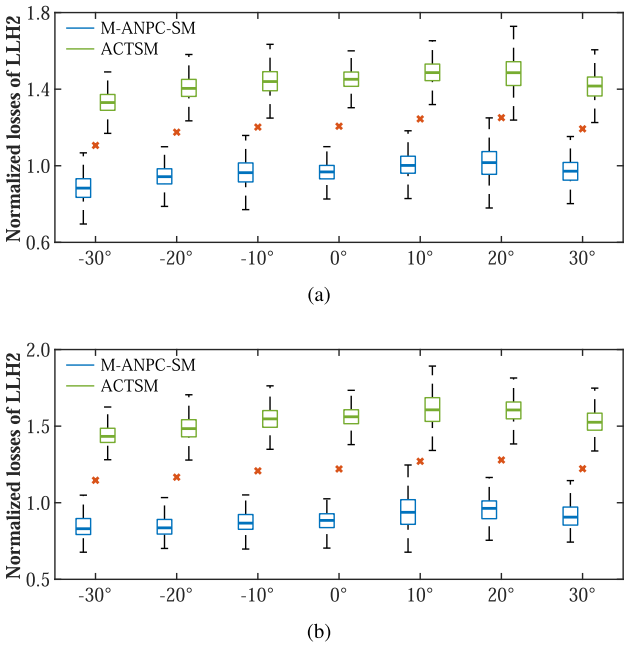

FIGURE 16. LLH2 MMC losses in: (a) inverter mode, and (b) rectifier mode.

average losses of HB-SM. At most power factors, the losses of at any single fundamental period may vary up to 30% above or below the median loss value. Since the devices that conduct the arm current are different in the two operation modes, there are some differences between Fig. 14 (a) and (b). In inverter mode, the highest variation of SM losses occurs at 20°, while under the rectifier operating mode, the variation above the median loss value is up to 60% at 10° for both HB-SM and FB-SM.

In LLH1, both SMs demonstrate the lowest losses under the classification of unipolar and bipolar SMs, separately. From the results, the losses of the M-ANPC-SM per level are lower than the BBSM/RBSM. Compared with HMMC, the variation of SM losses is smaller and the distribution of losses among the SMs is tighter. The largest variation of SM losses is about 40% at 10° and 20°. The average losses in LLH1 are about 0.9 - 1.0 times the total losses of HB-SM-based MMC at different angles, and the variation of average losses is about 10%. In both operating modes, the average loss is the lowest at −30° while the highest at 20°.

In LLH2, the ACTSM has higher losses than the BBSM/ RBSM. Correspondingly, the losses of ACTSM are higher than the M-ANPC-SM per level. From Fig. 16, the average losses of LLH2 are 1.1 - 1.3 times the HB-SM MMC. Same as LLH1, the average loss is the highest at 20° while the lowest at −30°. The median value of ACTSM losses are 1.3 - 1.5 times the HB-SM in inverter mode, and 1.4 - 1.6 times the HB-SM in rectifier mode. The maximum losses variation of the ACTSM in one period is about 40%.

C. COMPARISON TO HMMC

Fig.17 shows the relative improvement in the converter losses offered by the hybrid configurations of LLH1 and LLH2

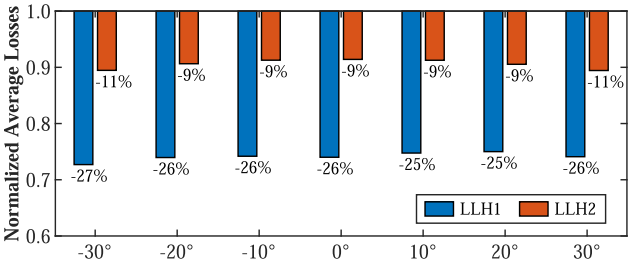

FIGURE 17. Average reduction in losses of LLH1 and LLH2 normalized to HMMC under inverter mode at different power factors.

compared to the HMMC in inverter mode. The percentages illustrate the different loss reduction of LLH1 and LLH2 over HMMC at seven power factor set-points. In terms of LLH1, the power losses are reduced by more than 25% compared to the HMMC. The highest reduction is 27% that occurs at −30°, while the lowest one is 25% at 10° and 20°. Compared to the HMMC, the LLH2 shows 9% reduction in the calculated losses from -20° to 20°, and 11% at ±30°. In the comparison of the two low-loss HMMCs, the losses of LLH2 are about 16% lower than those in the LLH1 when the MMC operates at typical power factors. A similar trend is observed in rectifier operation mode. The LLH1 shows a reduction of 30% compared to the HMMC, while the LLH2 losses are reduced by 13%, confirming that the low-loss configurations can provide improvement without substantial change to the operation or fault-blocking capabilities of the HMMC.

VI. CONCLUSION

In this paper, two different low-loss Hybrid Modular Multilevel Converter (HMMC) configurations have been proposed to improve the overall conversion efficiency of HMMCs. The low-loss HMMCs (LLH) offer similar functionalities to the conventional HMMC, but use lower loss unipolar and bipolar SMs in the converter arms. Specifically, instead of HB-SM and FB-SM in the HMMC, LLH1 comprises M-ANPC-SMs and BBSM/ RBSMs, while LLH2 comprises M-ANPC-SMs and ACTSMs. A detailed loss analysis of the HMMC and the two proposed low-loss HMMCs under different operating conditions is also provided in this paper. According to the loss comparison, improvements in the converter efficiency is achieved by both proposed HMMCs with reduction in the losses ranging from 25% to 32% in LLH1 and from 9% to 15% in LLH2 across all operating modes. It can be concluded that the two hybrid configurations are higher efficiency options for the HMMC in the aspect of losses. Furthermore, within a single period, the variations between minimum and maximum losses demonstrate the influence of power factor to the losses of HMMCs.

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