IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received November 11, 2021, accepted November 21, 2021, date of publication November 25, 2021,
date of current version December 3, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3130736

Fault Interruption Scheme for HVDC System Using SiC-MESFET and VCB Based Hybrid Circuit Breaker

WAHEED A. KHAN[1], ALI RAZA[2], M. REHAN USMAN[1], (Member, IEEE), SHAHZAIB HAMID[1], SAIF-UR-REHMAN[1], M. ARSLAN USMAN[3], (Member, IEEE), AND CHRISTOS POLITIS[3], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Superior University, Lahore 54660, Pakistan
[2]Department of Electrical Engineering, Khwaja Fareed University of Engineering and Information Technology, Rahim Yar Khan 64200, Pakistan
[3]Faculty of Science, Engineering and Computing, Kingston University London, Kingston upon Thames KT1 2EE, U.K.

Corresponding author: M. Rehan Usman (rehanusman@gmail.com)

ABSTRACT As high voltage DC power system is gaining popularity, power electronic switching devices are becoming increasingly advanced to overcome problems of timely fault isolation. In this context, hybrid DC circuit breakers (DCHCBs), especially, together with wideband gap-based semiconductor devices, play a crucial role to tackle the current and voltage at high power and frequency. In this paper, a hybrid DC circuit breaker is designed leading to development of a fault interruption scheme for HVDC power system, as in HVDC system, fault interruption is considered more critical compared to the conventional high voltage AC (HVAC) power system. The proposed design of hybrid circuit breaker (HCB) involves combination of mechanical and electronic switches for efficient fault interruption. The mechanical part is covered by using vacuum circuit breaker (VCB) and the electronic switching part involves use of SiC-MESFET as these are more powerful and fast switching elements. For the fault interruption schemes to be valid, artificial current zero is created using current commutation. The system model is designed using Simulink and comparisons are carried out between the proposed hybrid scheme and the recent fault interruption schemes in terms of power loss and fault clearing time. The results of the proposed design are measured in terms of system current, commutation current and voltage across the commutation capacitor.

INDEX TERMS Hybrid DC circuit breaker (DCHCB), vacuum circuit breaker (VCB), MOSFET and MESFET as switch.

I. INTRODUCTION

Fault interruption is an essential part of any power system, but in high voltage DC (HVDC) power system, it is considered as a crucial function because of artificial current zero (ACZ) state. The main difference between AC and DC current is due to frequency. In conventional high voltage AC (HVAC) power system, the current zero state is achieved automatically due to its alternating nature, but in DC there is no current zero crossing point due to which it is very important to force current to zero, called as ACZ, so that fault interruption processes can be carried out smoothly [1]. The working process of DC circuit breaker becomes complicated due to the absence of frequency in the HVDC power system. Therefore, on very high voltages, DC circuit breakers cannot work quickly and efficiently. This process becomes even more complex and critical with the introduction of multi terminal direct current (MTDC) power system [1], [2]. To deal with the issue, several circuit breaker-designs have been proposed, using simple mechanical circuit breakers (MCBs) and combination of mechanical and electronic switches called as hybrid circuit breakers (HCB). For HVDC applications, limited work has been performed on DC circuit breaker designs, where each has certain advantages and disadvantages, but no contribution has tried to give an overall picture [3], [4]. In this work, the MOSFET / MESFET based hybrid DC circuit breaker design is proposed to develop fault interruption scheme for HVDC power system.

A hybrid DC circuit breaker can be a combination of MCBs connected in series or combination of MCB and solid-state devices. The latter is the focus of this research. The design of a

The associate editor coordinating the review of this manuscript and approving it for publication was Hazlie Mokhlis.

simple DC-MCB is much like an AC circuit breaker, the only difference is absence of resonance response. The tripping speed of a MCB is much slower as compared to an HCB and it does not perform optimally in voltage source convertor (VSC) based network, as explained in [1]. Furthermore, HCB have quick interruption response but with a tradeoff of heat losses [5].

In an advance HVDC system, the quick fault interruption process should be controllable, easy to maintain and should have low cost with lower losses which is only possible by using DC-HCB approach. The working principle and the proposed design are explained latter in this paper after the related works section.

The remaining paper is segmented as follows; section 2 gives the state-of-the-art recent related works, section 3 provides the design and working principle of the proposed hybrid DC circuit breaker, section 4 provides the simulation-based results followed by conclusion in section 5.

II. RELATED WORKS

Early works on HVDC circuit breaker design were based on MCBs, that mainly include vacuum circuit breaker (VCB) and SF_6 gas interrupting unit (GIU) etc. But these breakers alone were not considered fast enough to provide optimal fault interruption, increasing the risk factor of creating economical losses, especially, because of short circuit faults [6]. Later, to reduce the fault interruption timing, researchers started working on hybrid approaches for HVDC circuit breaker design that included combination of mechanical breakers and solid-state devices. Furthermore, MCBs are good in current-carrying function and solid-state circuit breakers (SSCB) are well in high-speed arc less interrupting function. So, HCB, having combination of MCB and SSCB, have advantages of both [7]. To-date several works have been published presenting fault interruption system using hybrid HVDC circuit breakers. Recent, state-of-the-art related work to such systems is as follows.

In [5], the authors have proposed a DC circuit breaker which consists of semiconductor devices connected in series with a snubber circuit. The proposed circuit realizes high blocking voltage and reduces the surge voltage accompanying the current clearing by using a freewheeling diode. In [8], four-terminal radial HVDC network model is presented, where DC fault interruption current as well as fault clearing time are achieved by using a DC-MCB together with forced current zero formation scheme. In [9], two kinds of interruption testing methods, i.e., power frequency current peak method and charged reactor method, are presented for improving DC current interruption performance using saturable reactor implementation that reduces the value of C and L.

During fault occurrence, high stresses is created on the DC circuit breaker, for investigating such problem four basic circuits are discussed in [10]. Two basic working configurations of hybrid DC circuit breaker are discussed in [11]. First configuration uses a current impulse generated by the high voltage commutation branch itself, which provides an artificial current zero crossing in the mechanical switch and second working configuration uses an additional low voltage commutation switch which is connected in series to the mechanical switch. The authors in [12] have presented a cost effective and efficient DC fault protection strategy for a multi terminal (MT) DC system by developing a solid-state device-based hybrid DC circuit breaker. Similarly, three types of IGBT models are adopted in [13] for the purpose of DC breaker design. Another approach is adapted by the authors of [14] using hybrid current limiting circuit (HCLC) which consists of a current limiting inductor (CLI) and an energy dissipation circuit used in parallel with the CLI. HCLC effectively works in term of fault isolation at low voltages cannot operate on high-voltage system.

To improve the efficiency of fault interruption schemes, researchers are working on hybrid approaches for DC circuit breaker designs. The authors in [15] have proposed a hybrid model with SF6 interrupter and Vacuum interrupter connected in series to improve dynamic electric recovery strength (DDRS), which is an important factor for arc extinguishing in fault interruption process of HVDC system. Switching arc is important parameter for designing of an HVDC circuit breaker. The study of arc behavior in arc-based current limiting AC circuit breakers helps to develop effective method for interruption of DC fault currents [16]. During the separation of CB contacts the shorter arc time and larger electrode separation is required to improve the dielectric strength [17]. In [18], the authors have worked on DC line fault identification based on pulse injection from hybrid HVDC breaker designed using solid-state devices. In [19], modelling, experimental validation, and application of voltage source converter (VSC) assisted resonant current (VARC) based HVDC circuit breakers is presented. Similarly, multiple circuit topologies of HVDC breakers are proposed in [20]. For a bi-directional conduction and circuit blocking the state grid corporation of China (SGCC) designed a hybrid circuit breaker using IGBTs and full-bridge circuit as a load commutation switch presented in [21]. In [22], multiple full bridge cells are used in series with main breaker to achieve bi-directional conduction and blocking. A unique liquid metal switch with two stage commutation circuit used in [23] as an alternative of line commutation switch (LCS) for hybrid HVDC circuit breaker. In [24], the authors presented a current commutated hybrid DC circuit breaker which includes mechanical switches for the normal current path to reduce the transmission losses. Similarly, the authors in [25] preformed research on the current commutation measures of a hybrid DC breaker. They proposed a current commutation drive circuit (CCDC) used in series with a mechanical vacuum switch to reduce the fault interruption time.

Multiple review articles like [26] have been published to date giving different concepts and challenges related to HVDC breakers using different technologies presented by different contenders. The power loss in hybrid HVDC breaker was studied in [27] and Multiple challenges in HVDC breaker

development were discussed in [28]. To the best of authors knowledge all the works investigated so far, emphasis on efficient fault interruption in terms of fast and timely isolation of the faulty system in a safe manner. Similar trend is followed for works performed in hybrid approaches comprising of semiconductor devices-based HCBs. The fault interruption optimization in HVDC is still on going, especially, for faults like short circuiting where timely interruption is of utmost importance [6]. Similarly, in this context, this work provides an efficient and fast fault interruption process for HVDC system using a hybrid SiC-MESFET and VCB based circuit breaker compared with hybrid approach using MOSFET and with MCB. One important thing to remember here is that SiC-MESFETs can operate at high temperatures as they have high thermal conductivity, making them more suitable for the HVDC applications, however, testing of their thermal conductivity is not part of this work as it is already a well explored area [30]. Major contributions of this work are summarized as follows:

- Design of fast and efficient fault interruption process for HVDC system using SiC-MESFET and VCB based hybrid DC circuit breaker.
- Validation of the proposed design using Simulink based MATLAB simulations at high voltages and currents for HVDC system.

III. SYSTEM MODEL

This section presents the system model of the proposed HVDC fault interruption scheme containing description of both mechanical and solid-state part of the breaker. In the proposed design, VCB is used as a mechanical circuit breaker and MOSFET / MESFET is used as solid-state device for hybrid switching mechanism. This work also provides performance analysis between MOSFET and MESFET, that which one is better for the proposed HCB. To start, the description of fault interruption handling using VCB is provided first, followed by the description of MESFET part to develop better understanding of latter proposed hybrid DC breaker.

A. DC HIGH-VOLTAGE INTERRUPTION USING VCB

The block diagram of fault interruption process using VCB is shown in Fig. 1. As shown in the figure, there are three branches in this scheme for fault interruption, i.e., vacuum circuit breaker (VCB), metal oxide varistors (MOVs) and commutation branch that further consists of pre-charged capacitor C connected in series with inductor L as shown in Fig. 1(b). When fault occurs, considering that impulse of fault current reaches a certain safe value, the contacts of VCB open, creating an arc between the contacts. This process is followed by closing of the commutation branch switch S allowing the pre-charged commutation capacitor along with the inductor to generate high frequency oscillations which are then overlapped on the VCB current. This produces an artificial zero crossing which forces the arc to quench, that was generated due to VCB contacts. VCB has higher arc extinguishing ability due to perfect insulation. The VCB

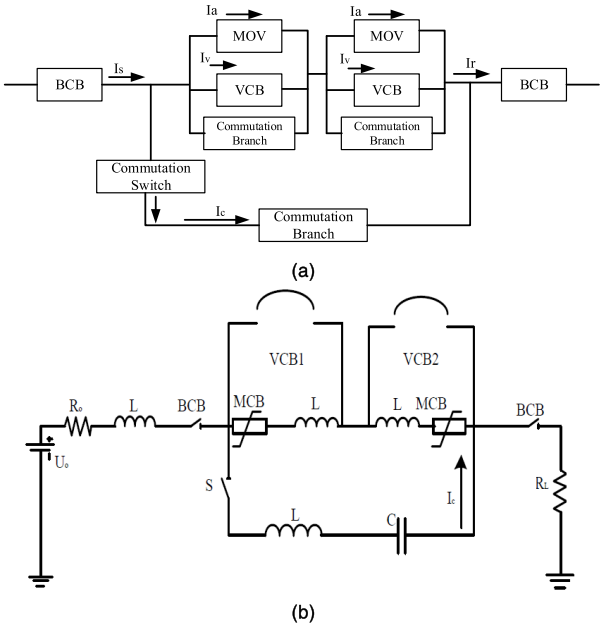


FIGURE 1. Fault interruption mechanism using vacuum circuit breaker (VCB). (a) Block diagram, (b) Schematic diagram.

operating mechanism is based on electromagnetic repulsion mechanism (ERM) and permanent magnet (PM) system as shown in Fig. 2. In case of fault occurrence, the ERM part provides quick response and PM reduces the mechanical impact produced by the ERM. The process is further elaborated in the work published in [29]. For easy and efficient operation, in this work two small gap VCBs are used with low voltage over a single long gap VCB with high voltage as in case of fault interruption, time of VCB can be minimized due to smaller moving parts with smaller axial dimension. Furthermore, the transient recovery voltage (TRV) will be decreased with the use of two small VCBs. TRV is the voltage that appears across the contact gap when the interruption occurs. It is a function of the reactive elements on the line and load side of the VCB [30]. Normally a VCB working is based on following main factors:

- Dielectric strength between contacts when opening.
- High frequency current Quenching capability at zero crossing.

1) DIELECTRIC STRENGTH

The dependency of contact distance and dielectric strength is given by [30]:

$$U = A\left(t - t_{open}\right) + B \tag{1}$$

where, t_{open} is the moment of contact separation, A is the rate of rise of dielectric strength and B is the breaker TRV just before current zero. In the case of restriking effect produced by restrike voltage, the strength of dielectric is measured as:

$$U = TRV_{Limit} - \left(A\left(t - t_{open}\right) + B\right) \tag{2}$$

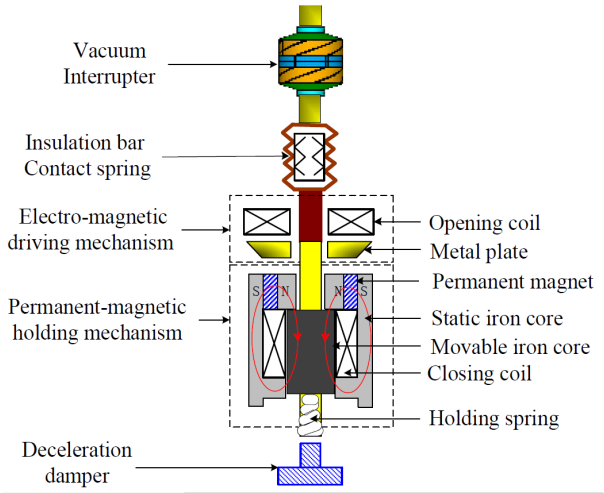


FIGURE 2. Vacuum circuit breaker (VCB) structure diagram [29].

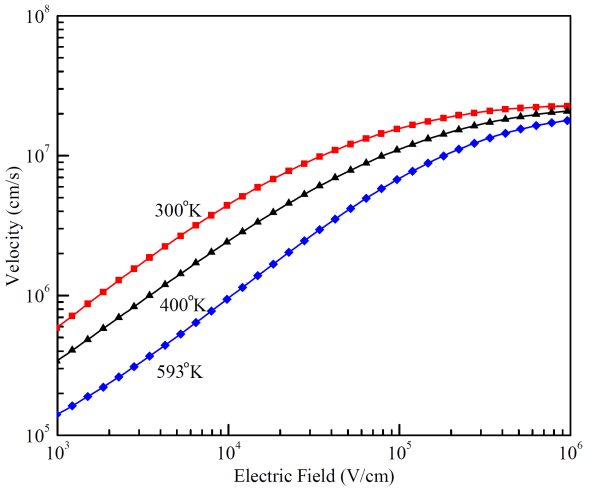


FIGURE 3. Behavior of electron drift velocity v as a function of variation in electric field E and temperature T [34].

where, TRV_{Limit} is the strength of dielectric that the breaker can handle and is calculated as:

$$TRV_{Limit} = k\_af.k\_pp.E\_mag.\sqrt{(2/3)} \tag{3}$$

where, k_{af} is the amplitude factor, k_{pp} is the first pole of clear factor and E_{mag} is the breaker rated voltage. When the breaker contacts open mechanically, the dielectric strength between the contacts increases with time and when the TRV increases the dielectric strength, reignition occurs hence leading to high frequency currents after which quenching takes place [30].

2) QUENCHING CAPABILITY

Vacuum circuit breakers have the capability to quench high frequency currents, therefore current may be quenched at artificial zero crossing for arc extinction. The rate of change of current at the artificial zero crossing determines the arc extinction. The VCB quenching capability is calculated using [30]:

$$\frac{d_i}{d_t} = C\left(t - t_{open}\right) + D \tag{4}$$

where, t_{open} gives the moment of contact separation.

The TRV can be controlled in each submodule, given in Fig. 1, by resistance and capacitance part. In case of fault, the surge arrestor limits the fault current value and absorbs energy during interruption process. After forcing the current to zero there is a chance of presences of some residual current. To prevent the residual current, two backup circuit breakers (BCB) are used. BCBs are used on each side of the VCB as shown in Fig. 1. The main benefit of using BCBs on each side is: as the commutation capacitor is charged by BCB so if the generating voltage system is on the right side and fault occurs on the left side, then capacitor can be charged from the BCB on the right side. Furthermore, BCB can isolate the whole DC system.

After the detailed description of and working of VCB fault mechanism, next subsection provides the description of metal

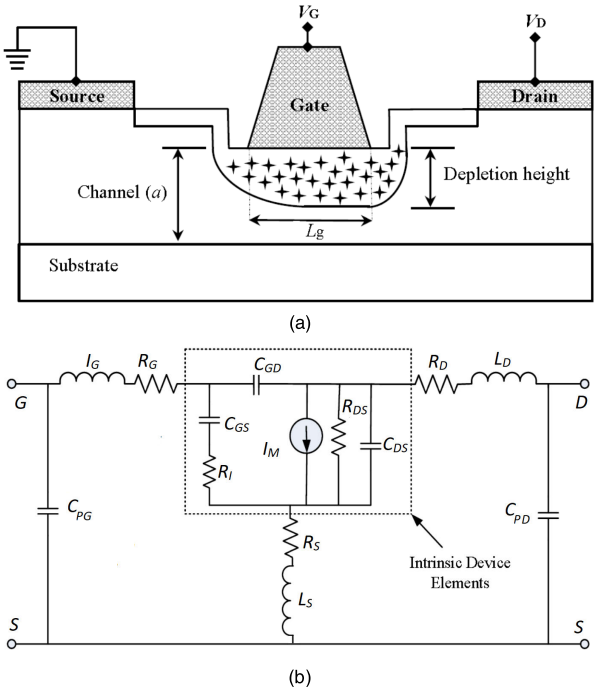


FIGURE 4. MESFET (a) Cross-sectional view (b) AC equivalent circuit model.

semiconductor field effect transistor (MESFET) as they are used in combination with the VCB for the proposed hybrid DC breaker design.

B. METAL SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MESFET)

Silicon Carbide (SiC) and Gallium Nitrate (GaN) based semiconductors are 3rd generation wideband gap (WBG) devices mainly MESFETs. These devices have high electron mobility, high thermal conductivity, radiation hardness and are immune to hot carriers degradation, which makes them

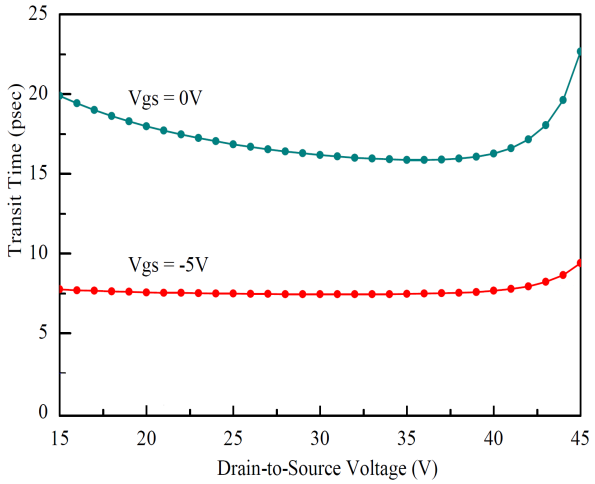


FIGURE 5. Transit time delay (τ) of $L_g = 0.5\ \mu$m SiC-MESFET [35].

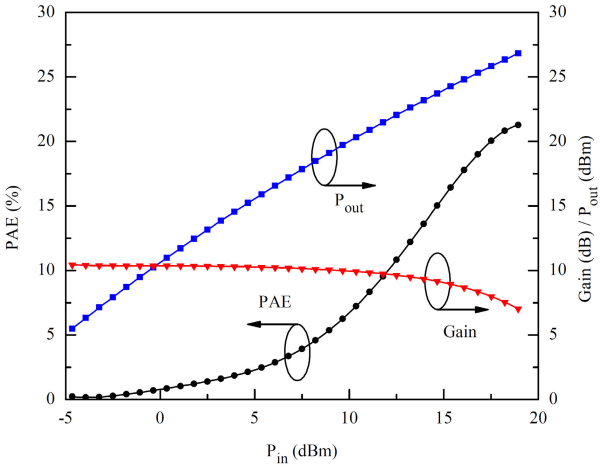


FIGURE 6. SiC-MESFET input/output power characteristics [36].

superior to other semiconductor devices [31]. Furthermore, they have better performance at high temperatures and high biasing leading to high switching speeds, as the electrical parameters of these devices, such as field velocity v and mobility μ are temperature dependent. The average properties of different semiconductor devices in comparison to GaN and SiC based devices is given in Table 1 [32]. The behavior of electron drift velocity v as a function of variation in electric field E and Temperature T for MESFETS is provided in Fig. 3 and is given by [33], [34]:

$$v(E) = E \times \mu(E) \tag{5}$$

$$\mu(E) = \frac{\mu_o(N,T)}{\left(1 + \left(\frac{\mu_o E}{v_s}\right)^{\alpha}\right)^{\frac{1}{\alpha}}} \tag{6}$$

where, $\mu_o(N, T)$ is the low field mobility which is function of carrier concentration N and temperature T and v_s is the saturation velocity.

Cross-sectional view of MESFET device is shown in Fig. 4(a). Gate controls the flow of current by handling the Schottky barrier height. A MESFET operates by applying drain to source voltage (V_{ds}) and gate to source voltage (V_{gs}), and the current is biased by both V_{ds} and V_{gs}. Fig. 4(b) shows the AC equivalent model of the MESFET device, where C_{pd} and C_{pg} denotes the pad capacitors of drain and gate, respectively, R_S, R_G and R_D represent source, gate, and drain resistances respectively, L_S, L_G and L_D are the source, gate and drain inductances respectively. The high frequency characteristics of the device depends on the gate length L_g (Fig. 4(a)) which ensures fast switching and due to this reason MESFET as a circuit breaker can provide optimal results. Transit Delay τ is the main characteristic on which switching frequency of the device is dependent. Transit delay τ is the device charging and discharging time of the gate depletion and depends on gate length L_g, and gain of the device G_m.

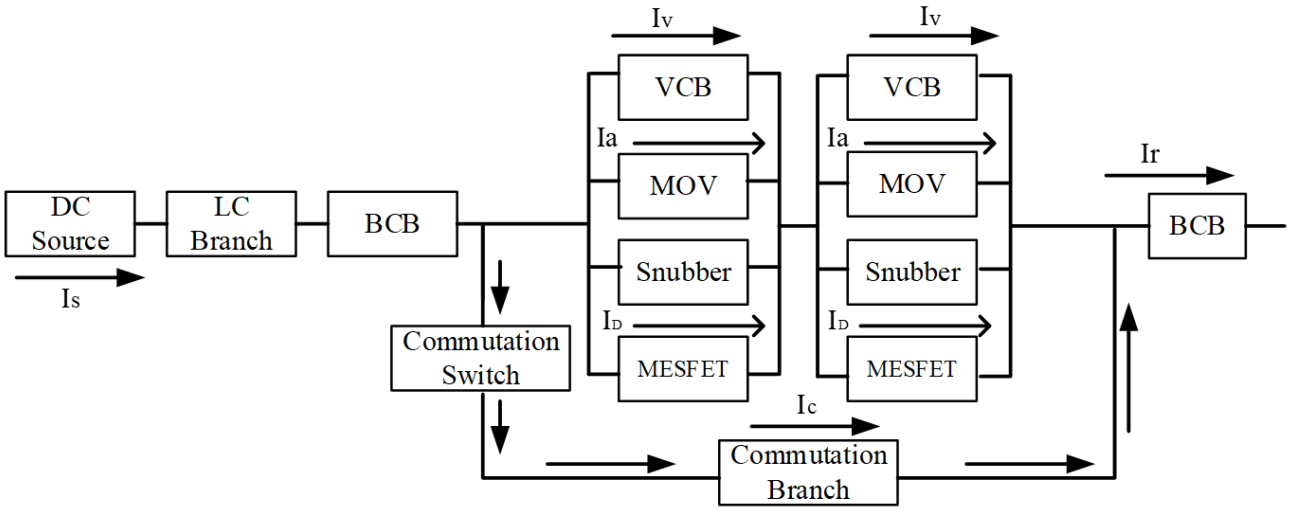


FIGURE 7. The block diagram of hybrid DC interruption with MESFETs.

TABLE 1. Average properties of semiconductor materials [30].

Material	E_g (eV)	ε_r	μ (cm^2/V)	E (MV/cm)	κ ($W/cm.K$)	v_s (cm/s)	T_{max} (^oC)
Si	1.12	11.7	1400	0.3	1.5	$1X10^7$	300
GaAs	1.4	12.8	8500	0.4	0.5	$1X10^7$	300
GaN	3.39	9.0	900	3.3	1.3	$2.5X10^7$	600
SiC-4H	3.26	9.66	1000	3.0	4.9	$2.5X10^7$	700

It is always desirable to have low τ (approximately 1 *psec*) and is expressed as:

$$\tau = \frac{L_g}{V_{gs}} = \frac{(C_{gs} + C_{gd})}{2G_m} \tag{7}$$

where, G_m is the transconductance and C_{gs} and C_{gd} are the gate to source and gate to drain capacitances of the device respectively shown in Fig. 4 and the τ performance is shown in Fig. 5 [35]. Furthermore, another reason for choosing 4H-SiC MESFET, for the proposed hybrid scheme, is because these devices can perform better in harsher environments due to their power performance [36]. For MESFET operation, power added efficiency (PAE), power density (PD) and power gain are important parameters for the measurement of device performance. These characteristics are shown in Fig. 6 [37], where PAE is observed as 21.1% for maximum input power with gate length of $L_g = 0.5$ μm at 2 GHz. To understand additional working and advantages of MESFETs the references provided in this subsection can be investigated further.

As aforementioned that SiC based MESFETs can give optimal performance with respect to switching frequency, so the proposed hybrid approach makes use of 4H-SIC based MESFET together with the VCB explained in next sub-section.

C. PROPOSED HVDC HYBRID CIRCUIT BREAKER (HCB) SCHEME

The proposed DC HCB can contain multiple n series of modules each having four main parallel parts, i.e., A VCB working at low voltage, MOV as varistor, commutation branch and semiconductor part using MESFET. Increasing n results in size reduction of mechanical breaker part as well as ease in commutation process. The proposed breaker in this work has two modules connected in series as shown in the block diagram given in Fig. 7, where the VCBs are working as mechanical switches and are controlled by the MESFETs. As aforementioned in subsection A of this section, VCB works on the principle of ERM given in Fig. 8. It is shown that in case of fault occurrence, the MESFET is triggered first generating a pulse current i_1 in the coil, inducing a pulse magnetic field around it. This magnetic field further induces eddy current in the metal plate. This process creates a repulsive force F_r between the metal plate and the coil, resulting in rapid movement of the metal plate. The topology given in Fig. 8(a) first works in RLC discharging mode and when capacitor's zero crossing voltage is achieved, the diode D stops the reverse charging of the capacitor. At this point, the circuit starts working in RL discharging mode. The equivalent circuit of ERM is provided in Fig. 8(b) where the metal plate is shown as an equivalent to inductance and a resistance connected in series. The pulse current generated by the MESFET is given as:

$$i_1(t) = \begin{cases} \dfrac{U_c}{\omega L_{\text{eq}}} e^{-\alpha t} \sin(\omega t) & 0 < t < t_1 \\ \dfrac{U_c}{\omega L_{\text{eq}}} e^{-\alpha t(2t-t_1)} \sin(\pi - \beta) & t \le t_1 \end{cases} \tag{8}$$

TABLE 2. Simulation parameters.

Parameters	Values
Source Voltage	80 kV, 200kV, 360kV
Short circuit resistance	0.79Ω
Input Inductance	23mH and 75mH
Output Resistance	24.2Ω
Charging Resistance	3000Ω
Snubber Circuit Resistance	$R_1 = R_2 = 100\Omega$
Snubber Circuit Capacitance	$C_1 = C_2 = 12$nF
Surge Arrestor (MOV)	80kV
Voltage across Commutation Capacitance	80kV
Commutation Frequency	4kHz
Maximum Current	4.8kA, 15kA, 6kA
Commutation Capacitance	3.64μF
Commutation Inductance	64.4μH
System Current in normal mode	1kA
Counter Current After Fault	10kA injected at 3ms
SiC-MESFET Parameters	
Gate Length L_g	0.5μm
Width W	400μm
Buffer Layer doping density N_b	6×10^{15}cm^{-3}
Input Resistance R_I	5.59Ω
Source resistance R_S	0.5Ω
Gate resistance R_G	5Ω
Drain resistance R_D	1.5Ω
Source inductance L_S	2pH
Gate inductance L_G	35pH
Drain inductance L_D	35pH
gate to source capacitance C_{gs}	230fF
gate to drain capacitance C_{gd}	30fF
Transconductance G_m	9.83ms
Doping Density N	1.5×10^{17}cm^{-3}
Transient Delay τ	22.66ps
Cutoff Frequency f_T	3.51GHz

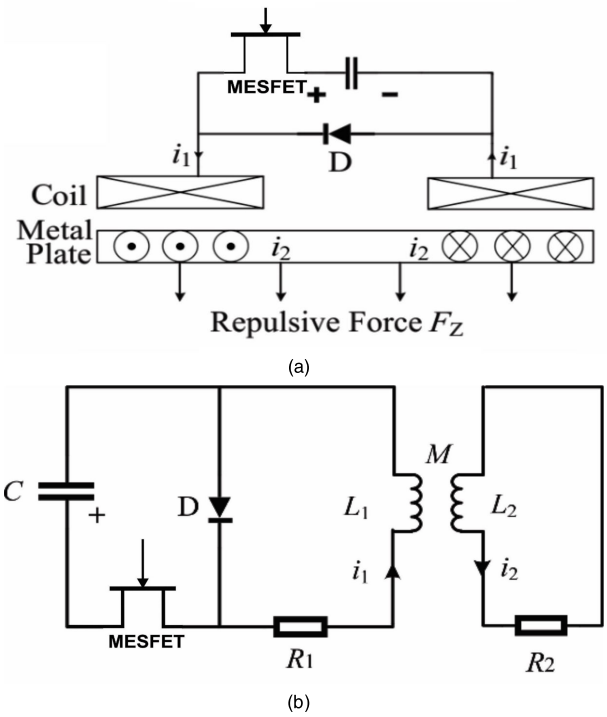


FIGURE 8. MESFET-VCB (a) ERM working principle (b) ERM equivalent circuit.

where, L_{eq} is the metal plate's equivalent inductance, U_c is the pre-charged capacitor voltage, M is the metal plate and coil's mutual inductance, and L_1 & L_2 are the self-inductances generated across the coil and the metal plate respectively. Furthermore, α, β, ω, t_1, and L_{eq} in (8) are given by:

$$\alpha = \frac{R}{2L} \tag{9}$$

$$\beta = arctan\left(\frac{\omega}{\alpha}\right) \tag{10}$$

$$\omega = \sqrt{\frac{1}{L_{eq}C} - \left(\frac{R}{2L}\right)^2} \tag{11}$$

$$t_1 = \frac{\pi - \beta}{\omega} \tag{12}$$

$$L_{eq} = L_1 - \frac{M^2}{L_2} \tag{13}$$

The electromagnetic repulsive force F_r is given by [38]:

$$F_r = i_1 i_2 \frac{dM}{ds} = \frac{1}{2} i_1 2 \frac{dL_{eq}}{ds} \tag{14}$$

where, s gives metal plate's displacement. ERM can be additionally determined by:

$$m\frac{d^2s}{d^2t} = F_r - F_d - F_h \tag{15}$$

where, F_h is the holding force produced by the holding spring and the PM, F_d gives the resistance during the ERM motion process, and m presents the movable part's mass. The ERM process is followed by the opening of VCB which is further followed by the closing of commutation switch to start the commutation process for achieving artificial current zero. As mentioned earlier in the subsection A (for VCB) of this section, here also MOV limits the fault current value and absorbs energy during interruption process and BCB prevent the residual current. This whole interruption process is provided in Fig. 9 and is summarized as follows according to time T:

T0: The system is stable and is working in normal condition with commutation capacitor fully charged.

T1: Fault takes place and fault current appears in the system current. As the fault occurs, the MESFET is triggered it generates a pulse current to initiate the ERM process explained earlier in this section. ERM further initiates the contacts opening mechanism of VCB for quick response and arc starts to appear across the contacts.

T2: As the fault current reaches a certain limit, the commutation switch will check the TRV, if its value increases the dielectric strength, high frequency current (commutation current) is injected to start the commutation process.

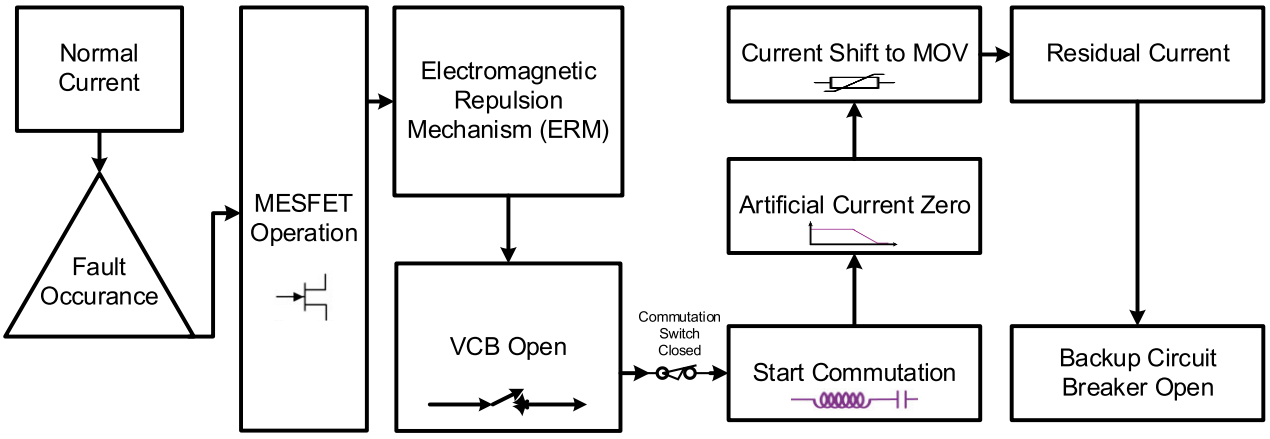


FIGURE 9. The block diagram of hybrid DC interruption with MESFETs.

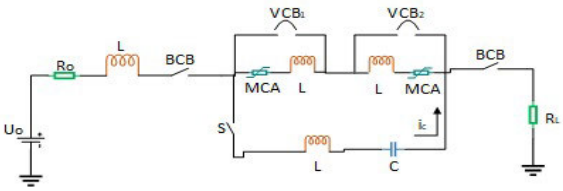


FIGURE 10. Simulink model for DC MCB using VCB.

T2 - T3: After the commutation switch closes, current starts shifting from VCB to commutation branch. At the same time commutation capacitor starts discharging.

T3: After the current is completely transferred to commutation branch, the first commutation process is completed. As the VCB opens and TRV appears, the arc quenching process starts, and snubber circuit comes into action. There are two responsibility of snubber circuit.

- First, the high capacitance in the snubber branch equally shares the TRV in the entire circuit.
- Secondly, the resistance in the RC circuit limits the oscillating frequency of TRV hence limiting the rising recovery voltage.

T3 - T4: When the arc is quenched, due to forcefully created current zero, high energy is generated. This energy is absorbed by the inductor connected in series with the MOV. Furthermore, after the voltage of pre-charged commutation capacitor declines toward zero, second commutation starts where the current starts to transfer from the commutation branch to MOV branch.

T4: Second commutation is completed when the total current is shifted to MOV branch.

T5: The total current flowing through the system is sum of the varistor branch current, commutation current, and charging capacitor, which needs to be fully quenched. Some residual current always remains, even after the MOV absorbs most of the energy. Due to this reason, BCB is used to remove the residual current. The significance of using BCB for removing the residual current is also shown in the simulation section.

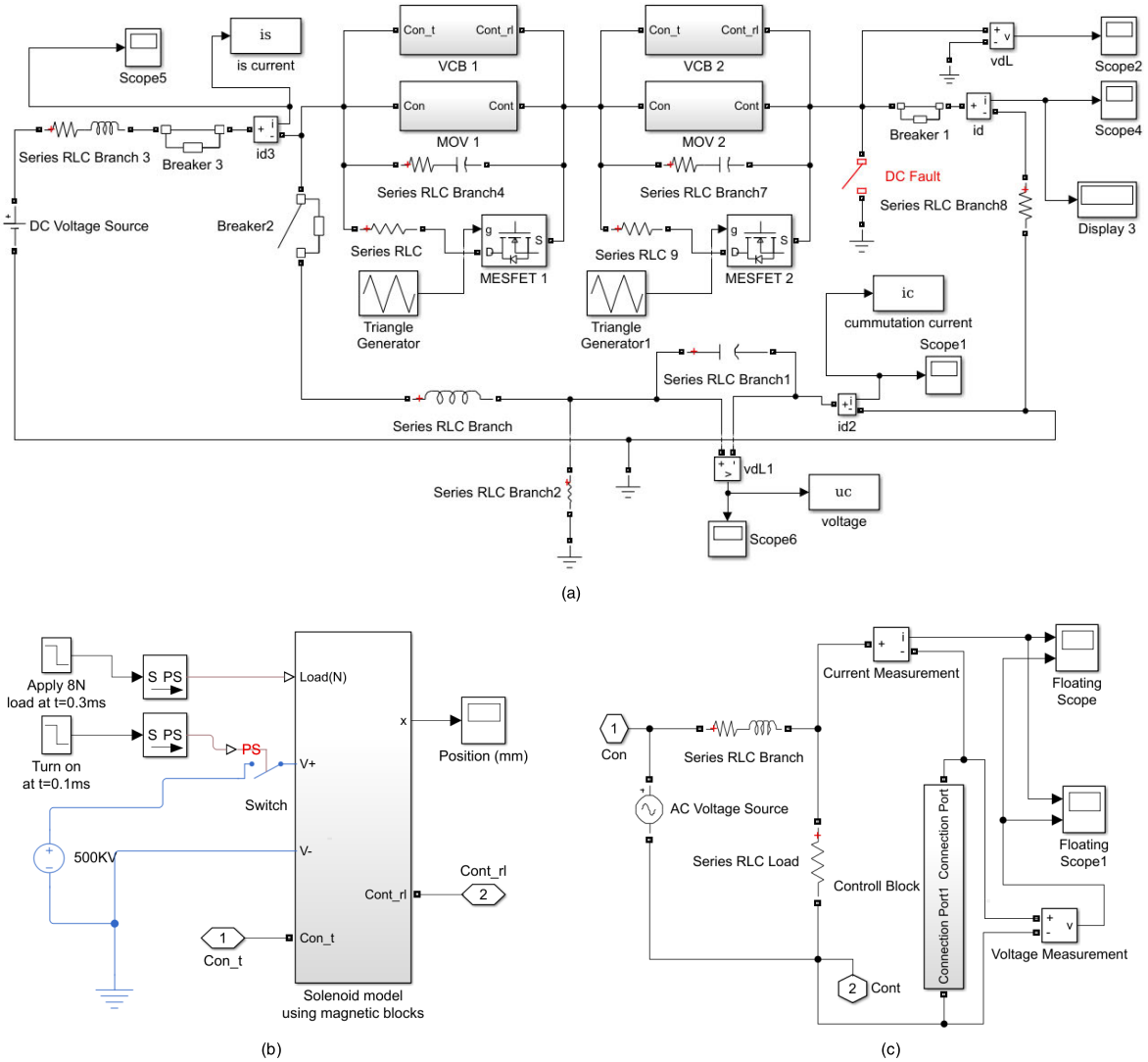


FIGURE 11. (a) Simulink model for HVDC HCB using MOSFET / MESFET. (b) VCB subsystem block (c) MOV subsystem block.

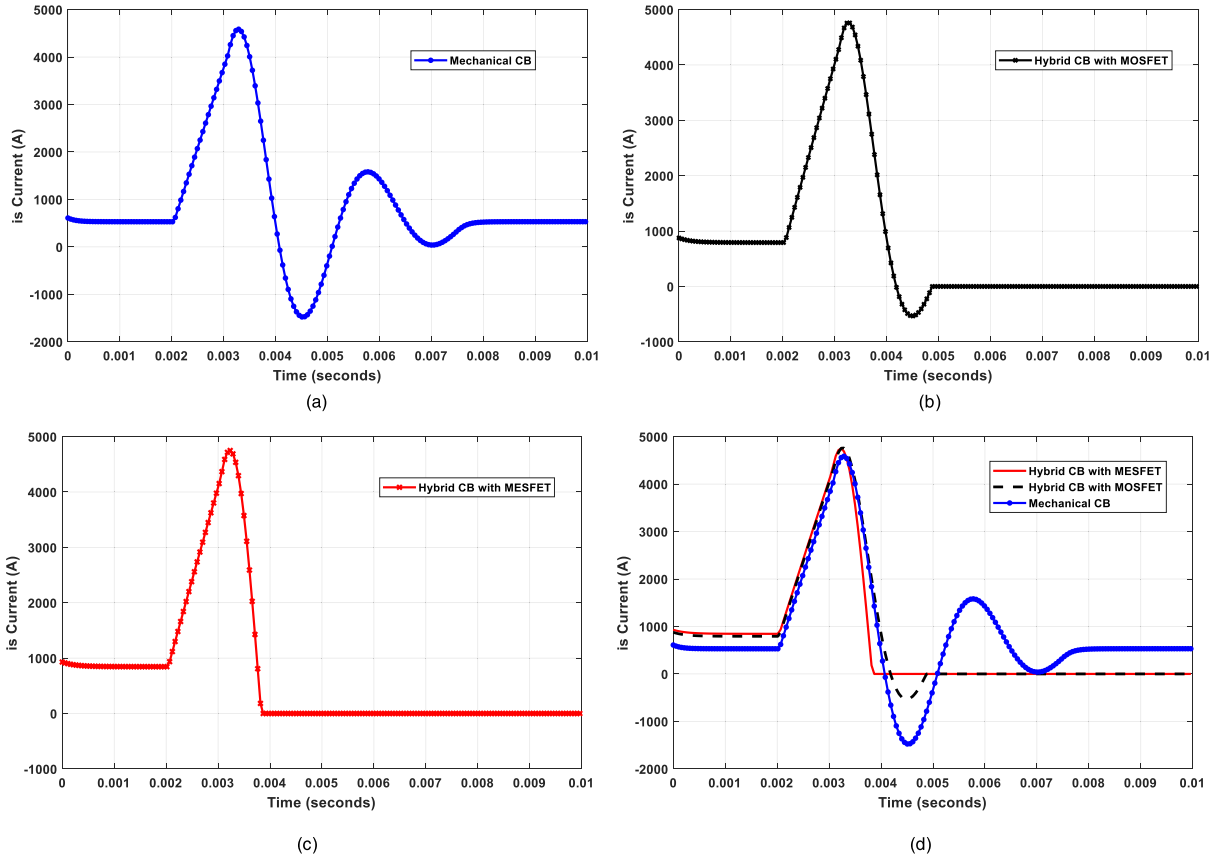


FIGURE 12. System Current i_S results: (a) MCB using VCB, (b) HCB with MOSFET and VCB, (c) HCB with MESFET and VCB, (d) Comparison between the results in (a), (b), and (c).

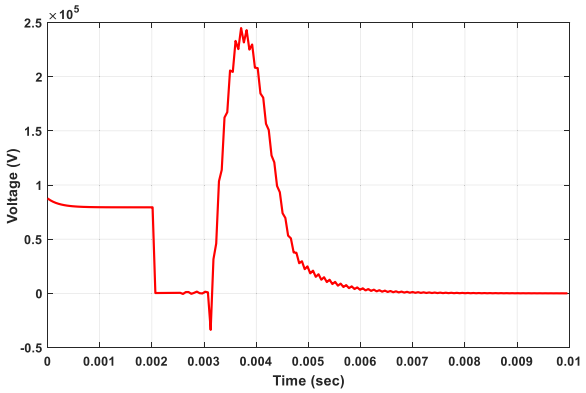


FIGURE 13. VCB TRV curve of the system.

TABLE 3. Summary of the DC breaker.

	HCB with MESFET	HCB with MOSFET	MCB with VCB
Power Loss	Low	Low	High
Total clearing time	3.8ms	4.8ms	6.8ms
Peak current	12KA	14KA	22KA
Capacitor size	Medium	Medium	Large

After detailed explanation of the proposed hybrid fault interruption scheme, next, the simulation model and results for validation of the proposed work are provided.

IV. SIMULATION MODEL, RESULTS AND DISCUSSION

This section presents the MATLAB Simulink based simulation model of the proposed HVDC fault interruption scheme. The simulations are provided in three parts, i.e., HVDC MCB using VCB, HVDC HCB using MOSFET with VCB and HVDC HCB using MESFET with VCB. The Simulink models for HVDC MCB using VCB (Fig. 1) and for HVDC HCB using MESFET (Fig. 7) are given in Figs. 10 and 11. The simulation parameters are given in Table 2 and the results are provided in Figs 12 – 14. The system is designed using two VCB modules connected in series. It is assumed that source voltage is on the left side of the system while fault occurrence is on the left side as shown in Fig. 11.

The results provided in Fig. 12 show that 1KA current is flowing in normal condition where the fault occurs at 2ms in all three cases, i.e., (a) MCB with VCB, (b) HCB with MOSFET and VCB (c) HCB with MESFET and VCB. It is shown that as the fault occurs at 2ms the current starts to rise and as it reaches a limit of 4.3KA the VCB contacts initiate the opening process and the commutation switch S closes. The results show that the quenching of arc is completed at 6.8ms for the case in Fig. 12(a), 4.8ms for the case in

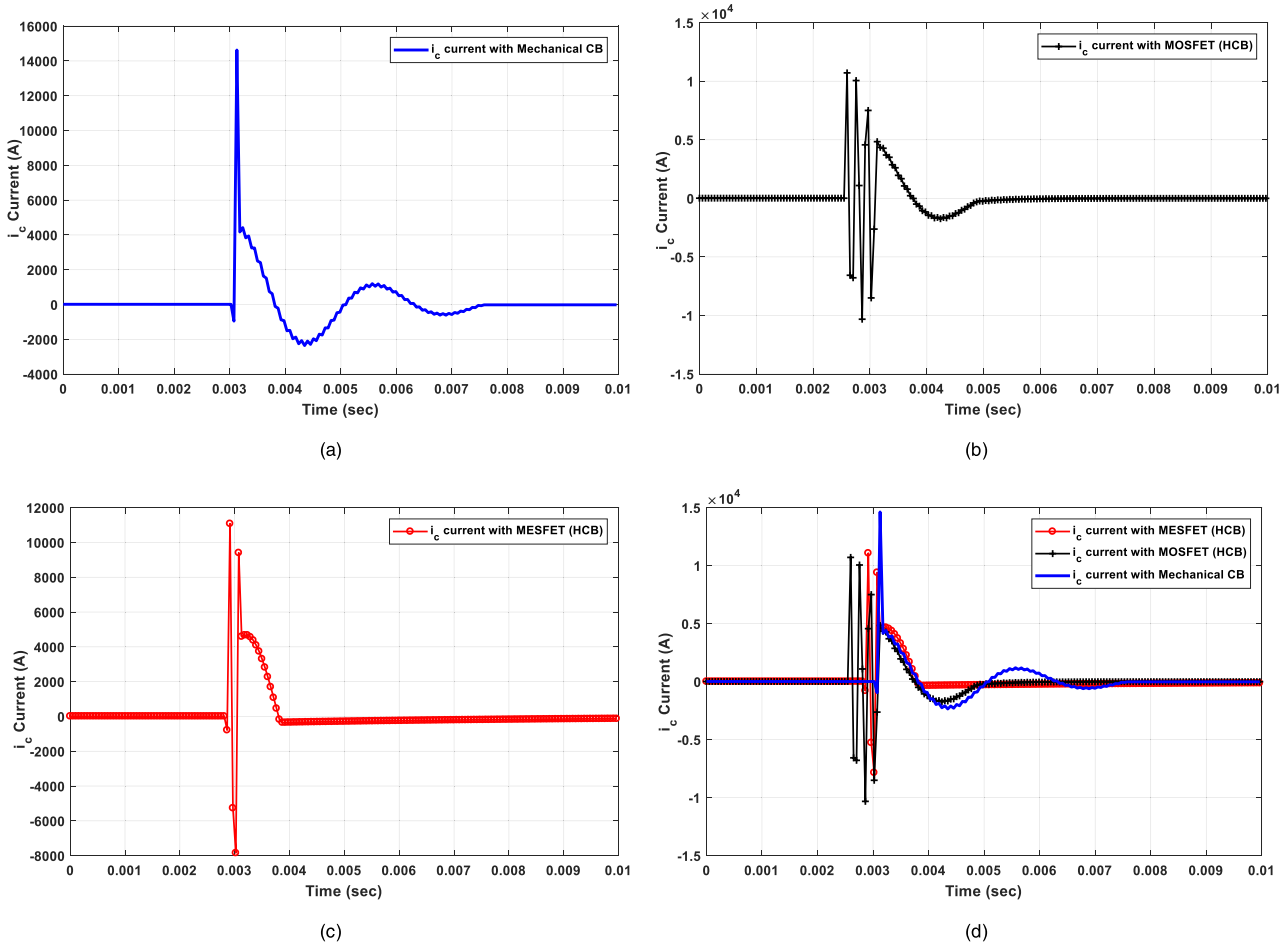


FIGURE 14. Commutation current i_c results: (a) MCB using VCB, (b) HCB with MOSFET and VCB, (c) HCB with MESFET and VCB, (d) Comparison between the results in (a), (b), and (c).

TABLE 4. Comparison (simulation).

	Y. Wu, et al. [23]	Proposed HCB with MESFET	A. Suzuki, et al. [39]	Proposed HCB with MESFET
	200kV & 15kA		360kV & 6kA	
Fault Clearance Time	8ms	3.7ms	7.8ms	2.7ms

Fig 12(b) and 3.8ms for case in Fig 12(c) at the zero crossing, but in (a) it can be seen that, even with arc quenched, there is some residual current remaining. This is because for the case in Fig. 12(a) BCB is not considered and the result is derived to show the effect of BCB absence in the circuit. For results in Figs 12(b) and 12(c), it can be seen that there is no residual current after the arc is quenched and the system current becomes zero due the presence of BCB. The result provided in Fig. 12(d) shows the comparison between the results of Figs 12(a, b, c).

When the contacts of VCB open, the transient recovery voltage TRV appears across the contact gap shown in the result in Fig 13. As mentioned earlier in previous section of this paper, that appearing of TRV leads to high currents and at the same time commutation switch is closed which results in high oscillating currents being injected into the system [30]. The impact of using MOSFET and MESFET with VCB on this commutation current is shown in Figs 14(b) and 14(c) respectively, compared with results of using only VCB in Fig 14(a). Figure 14(d) shows comparison of all three. It can be seen that the commutation current for MESFET based HCB in Fig. 14(c) after, high frequency oscillations, reaches zero earlier at 3.8ms than the other two. Due to this reason the system current in Fig 12. (c) settles to zero earlier than the other two cases. Which shows that MESFET based HCBs have better performance compared to MOSFETS based HCBs and simple VCB based MCBs.

The results in Fig 15 are given for the voltage across the commutation capacitor. The results show the behavior of the commutation capacitor when the commutation switch S closes. As soon as the commutation switch closes, the commutation capacitor starts to discharge creating commutation. The oscillation in the result of MCB using VCB in Fig 15(a) show the charging and discharging of the commutation capacitor due to the absence of BCB, whereas there is no oscillation in the results of HCB using MOSFET and MESFET in Figs. 15(b) and 15(c) respectively once the discharging

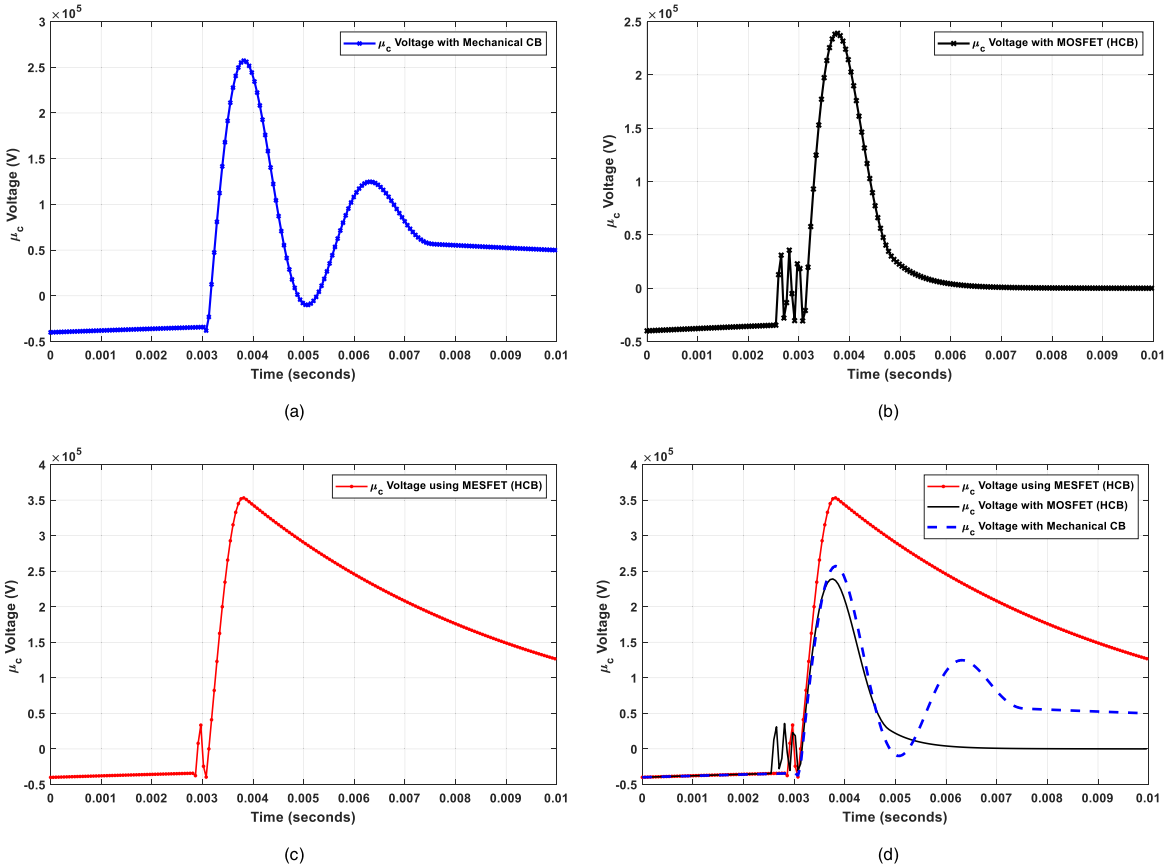


FIGURE 15. Results of voltage across the commutation capacitor u_C: (a) MCB using VCB, (b) HCB with MOSFET and VCB, (c) HCB with MESFET and VCB, (d) Comparison between the results in (a), (b), and (c).

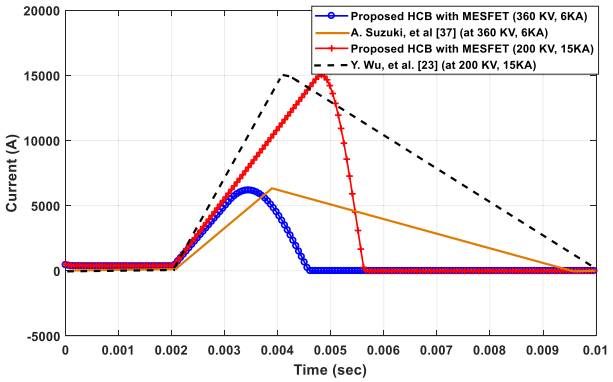


FIGURE 16. Simulation comparison of fault current breaking time of the proposed design with works provided in [23] and [39].

starts because of the presence of BCB. The results show that charging of the commutation capacitor, in case of MESFET based HCB, is more abrupt as compared to the other two cases.

The findings of cases under consideration, based on the simulation results, are summarized in Table 3. Considering that each research on HVDC system has its unique requirements, so the purpose of this work is not to contest anyone's contribution. However, for the sake of providing significance of the proposed HCB design using SiC-MESFETs in terms of fault current breaking time, a few comparisons, using simulated data, are provided with the existing research in Fig 16 and Table 4. The results are provided are for two configurations, i.e., 200KV with peak current of 15KA and 360KV with peak current of 6KA. The results show that the given design in this work performs better in both configurations. The summary of the simulation comparison is provided in Table 4.

V. CONCLUSION

The work performed in this paper provides a new fault interruption scheme using SiC-MESFET and VCB based hybrid circuit breaker for HVDC system. This work provides the benefits of using multiple series modules each having four main parallel parts, i.e., A VCB working at low voltage, MOV as varistor, commutation branch and semiconductor part using MESFET, i.e., easy commutation with cost reduction due to reduced size of VCB. The main contribution of the proposed work is to reduce the fault clearance time, which is visible from results that the proposed scheme performs better than compared to MCB using VCB, and HCB using MOSFET & VCB, as well as the previously proposed works. The proposed design is much better than the MCB in terms of time interruption, less commutation current, higher frequency

in commutation process, and minimum magnitude of residual current due to BCB presence. Furthermore, it is signified that MESFET shows better performance than MOSFET, when used as CB, because of its fast-switching mechanism. The material chosen in fabrication of MESFETs plays a vital role. MESFETs with wide band gap materials (SiC/GaN) are very promising for microelectronics and power electronics industry, especially when it comes to breaker design, as they can perform better in harsher environments like high temperatures. To continue the work further hardware testing of the proposed design will be performed for further validation.

REFERENCES

[1] Z. Q. Shi, Y. K. Zhang, S. L. Jia, X. C. Song, L. J. Wang, and M. Chen, "Design and numerical investigation of A HVDC vacuum switch based on artificial current zero," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 22, no. 1, pp. 135–141, Feb. 2015.

[2] H. A. Darwish, M. A. Izzularab, and N. I. Elkalashy, "Real-time testing of HVDC circuit breakers Part 1: Bench test development," in *Proc. Int. Conf. Electr., Electron. Comput. Eng.*, Sep. 2004, pp. 765–769.

[3] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[4] C. Du and C. Wang, "Review of DC circuit breaker technology for HVDC application," in *Proc. 22nd Int. Conf. Electr. Mach. Syst. (ICEMS)*, Harbin, China, Aug. 2019, pp. 1–6.

[5] K. Sano and M. Takasaki, "A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2690–2699, Jul. 2014.

[6] G. A. Ludin, M. A. Amin, H. Matayoshi, S. S. Rangarajan, A. M. Hemeida, H. Takahashi, and T. Senjyu, "Solid-state DC circuit breakers and their comparison in modular multilevel converter based-HVDC transmission system," *Electronics*, vol. 10, no. 10, p. 1204, May 2021.

[7] A. Shukla and G. D. Demetriades, "A survey on hybrid circuit-breaker topologies," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 627–641, Apr. 2015.

[8] K. Tahata, S. El Oukaili, K. Kamei, D. Yoshida, Y. Kono, R. Yamamoto, and H. Ito, "HVDC circuit breakers for HVDC grid applications," in *Proc. 11th IET Int. Conf. AC DC Power Transmiss. (ACDC)*, Birmingham, U.K., Feb. 2015, pp. 1–9.

[9] S. Tokoyoda, M. Sato, K. Kamei, D. Yoshida, M. Miyashita, K. Kikuchi, and H. Ito, "High frequency interruption characteristics of VCB and its application to high voltage DC circuit breaker," in *Proc. 3rd Int. Conf. Electr. Power Equip.-Switching Technol. (ICEPE-ST)*, Busan, South Korea, Oct. 2015, pp. 117–121.

[10] A. Mokhberdoran, A. Carvalho, H. Leite, and N. Silva, "A review on HVDC circuit breakers," in *Proc. Renew. Power Gener. Conf.*, Naples, Italy, Sep. 2014, pp. 1–6.

[11] Y. Li, X. Shi, F. Wang, L. M. Tolbert, and J. Liu, "DC fault protection of multi-terminal VSC-HVDC system with hybrid DC circuit breaker," in *Proc. IEEE Energy Convers. Congr. Expo.*, Milwaukee, WI, USA, Sep. 2016, pp. 1–8.

[12] K. Nikolaos, S. Vasileios, I. Mohammad, S. Patrick, S. Saadman, and K. Petros, *DC Circuit Breaker and their Use in HVDC Grids*. London, U.K.: Imperial College London, Accessed: Jul. 16, 2021. [Online]. Available: http://www2.ee.ic.ac.U.K./nikolaos.kostoulas10/yr2proj/HVDC%20Circuit%20Breakers%20Report.pdf

[13] N. Lin and V. Dinavahi, "Detailed device-level electrothermal modeling of the proactive hybrid HVDC breaker for real-time hardware-in-the-loop simulation of DC grids," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1118–1134, Feb. 2018.

[14] J. Liu, N. Tai, C. Fan, and S. Chen, "A hybrid current-limiting circuit for DC line fault in multiterminal VSC-HVDC system," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5595–5607, Jul. 2017.

[15] X. Cheng, P. Yang, G. Ge, K. Su, and M. Liao, "The novel hybrid HVDC circuit breakers with series-connected vacuum and the SF6 interrupters," in *Proc. 28th Int. Symp. Discharges Electr. Insul. Vac. (ISDEIV)*, Greifswald, Germany, Sep. 2018, pp. 247–250.

[16] T. Qin, E. Dong, G. Liu, and J. Zou, "Recovery of dielectric strength after DC interruption in vacuum," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 23, no. 1, pp. 29–34, Feb. 2016.

[17] D. Dáring, D. Ergin, K. Wárflinger, J. Dorn, F. Schettler, and E. Spahic, "System integration aspects of DC circuit breakers," *IET Power Electron.*, vol. 9, no. 2, pp. 219–227, Feb. 2016.

[18] G. Song, T. Wang, and K. S. T. Hussain, "DC line fault identification based on pulse injection from hybrid HVDC breaker," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 271–280, Feb. 2019.

[19] S. Liu, M. Popov, S. S. Mirhosseini, S. Nee, T. Modeer, L. Angquist, N. Belda, K. Koreman, and M. A. M. M. van der Meijden, "Modeling, experimental validation, and application of VARC HVDC circuit breakers," *IEEE Trans. Power Del.*, vol. 35, no. 3, pp. 1515–1526, Jun. 2020.

[20] D. Jovcic, G. Tang, and H. Pang, "Adopting circuit breakers for high-voltage DC networks: Appropriating the vast advantages of DC transmission grids," *IEEE Power Energy Mag.*, vol. 17, no. 3, pp. 82–93, May 2019.

[21] T. Augustin, S. Norrga, and H.-P. Nee, "Modelling of HVDC breakers for HVDC grid simulations," in *Proc. 13th IET Int. Conf. AC DC Power Transmiss. (ACDC)*, Manchester, U.K., Feb. 2017, pp. 1–6.

[22] W. Zhou, X. Wei, S. Zhang, G. Tang, Z. He, J. Zheng, Y. Dan, and C. Gao, "Development and test of a 200 kV full-bridge based hybrid HVDC breaker," in *Proc. Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, Sep. 2015, pp. 1–7.

[23] Y. Wu, Y. Wu, M. Rong, and F. Yang, "Development of a novel HVDC circuit breaker combining liquid metal load commutation switch and two-stage commutation circuit," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6055–6064, Aug. 2019.

[24] R. Hasegawa, K. Kanaya, Y. Koyama, T. Matsumoto, and T. Ishiguro, "Principle experiment of current commutated hybrid DCCB for HVDC transmission systems," in *Proc. Int. Power Electron. Conf.*, Nigata, Japan, May 2018, pp. 2011–2015.

[25] W. Wen, Y. Huang, Y. Sun, J. Wu, M. Al-Dweikat, and W. Liu, "Research on current commutation measures for hybrid DC circuit breakers," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1456–1463, Aug. 2016.

[26] M. Barnes, D. Sergio Vilchis-Rodriguez, X. Pei, R. Shuttleworth, O. Cwikowski, and A. C. Smith, "HVDC circuit breakers—A review," *IEEE Access*, vol. 8, pp. 211829–211848, 2020.

[27] M. Hesami, A. Bakhshi, S. Mousavi, K. Rouzbehi, and J. M. Escaño, "HVDC breaker power loss reduction by bridge-type hybrid breakers," *Energies*, vol. 14, no. 6, p. 1526, Mar. 2021.

[28] A. Raza, A. Mustafa, U. Alqasemi, K. Rouzbehi, R. Muzzammel, S. Guobing, and G. Abbas, "HVdc circuit breakers: Prospects and challenges," *Appl. Sci.*, vol. 11, no. 11, p. 5047, May 2021.

[29] A. Raza, W. A. Khan, M. Ellahi, and B. Masood, "Design of interruption process for HVDC system using vacuum circuit breaker based on virtual current zero," in *Proc. 43rd Annu. Conf. Ind. Electron. Soc.*, Beijing, China, Oct. 2017, pp. 4755–4762.

[30] J. Helmer and M. Lindmayer, "Mathematical modeling of the high frequency behavior of vacuum interrupters and comparison with measured transients in power systems," in *Proc. 17th Int. Symp. Discharges Electr. Insul. Vac.*, Berkeley, CA, USA, 1996, pp. 323–331.

[31] L. Lukasiak and A. Jakubowski, "History of semiconductors," *J. Telecommun. Inf. Technol.*, vol. 4, pp. 3–9, Jan. 2010.

[32] R. Gilmore and L. Besser, *Practical RF Circuit Design for Modern Wireless Systems: Active circuits and systems*, vol. 2. Norwood, MA, USA: Artech House, 2003.

[33] R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.

[34] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC [MESFETs]," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1442–1447, Jul. 2001.

[35] S. Rehman, M. M. Ahmed, U. Rafique, and M. N. Khan, "A nonlinear model to assess DC/AC performance reliability of submicron SiC MESFETs," *J. Comput. Electron.*, vol. 17, no. 3, pp. 1199–1209, Sep. 2018.

[36] S. Katakami, S. Ono, and M. Arai, "RF characteristics of a fully ion-implanted MESFET with highly doped thin channel layer on a bulk semi-insulating 4H-SiC substrate," *Mater. Sci. Forum*, vols. 600–603, pp. 1107–1110, Sep. 2008.

[37] M. Tsukima, T. Takeuchi, K. Koyama, and H. Yoshiyasu, "Development of a high-speed electromagnetic repulsion mechanism for high-voltage vacuum circuit breakers," *Electr. Eng. Jpn.*, vol. 163, no. 1, pp. 34–40, Apr. 2008.

[38] X. Han, W. Sima, M. Yang, L. Li, T. Yuan, and Y. Si, "Transient characteristics under ground and short-circuit faults in a ±500kV MMC-based HVDC system with hybrid DC circuit breakers," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1378–1387, Jun. 2018.

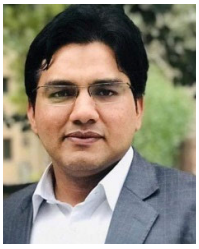
[39] A. Suzuki and H. Akagi, "HVDC circuit breakers combining mechanical switches and a multilevel PWM converter: Verification by downscaled models," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4259–4269, May 2019.

WAHEED A. KHAN received the B.Sc. degree in electrical engineering from the University of Engineering and Technology, Lahore, Pakistan, in 2010, and the M.Sc. degree in electrical engineering from The University of Lahore, Lahore, in 2014. He is currently pursuing the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, Superior University, Lahore. He is also working as a Lecturer with the Department of Electrical Engineering, Superior University. His research interests include smart HVDC systems, smart energy management systems, and power electronics.

ALI RAZA was born in Multan, Pakistan. He received the B.S. and M.S. degrees in electrical engineering, in 2012 and 2017, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the Khwaja Fareed University of Engineering and Information Technology (KFUEIT), Rahim Yar Khan, Pakistan. He has served as an Electrical Engineer for Masood Spinning Mills, Kabirwala, Pakistan. During his job, he has supervised many mega projects of solar system up to 7MWatts. His research interests include smart grid, demand side response, HVDC systems, and power electronics. His main research interest includes HVDC systems.

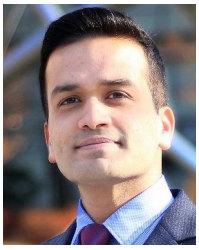
M. REHAN USMAN (Member, IEEE) was born in 1986. He received the B.S. degree in electrical engineering from the COMSATS Institute of Information Technology, Lahore, Pakistan, in 2008, the M.S. degree in electrical engineering with specialization in telecommunications from BTH, Sweden, in 2010, the M.S. degree in project management and operational development from KTH, Sweden, in 2013, and the Ph.D. degree in IT convergence engineering from the Kumoh National Institute of Technology (KIT), South Korea, in 2018. He is currently an Assistant Professor with the Department of Electrical Engineering, Superior University, Lahore. His research interests include coexistence among networks, cognitive radio, MIMO, NOMA, small cells in next-generation wireless networks (5G and Beyond), image classification and detection, and video quality assessment.

SHAHZAIB HAMID received the B.S. degree in electrical engineering from the University of Central Punjab, Lahore, Pakistan, in 2015, and the M.S. degree in computer engineering with a specialization in artificial intelligence from the University of Engineering and Technology, Lahore, in 2017. He is currently pursuing the Ph.D. degree in electrical engineering with COMSATS University, Lahore. He is working as a Lecturer in the Department of Electrical Engineering, Superior University, Lahore, Pakistan. The main area of specialization in Ph.D. degree is computer vision and machine learning. His main research interests include artificial intelligence, machine learning, computer vision, the IoT, robotics, and practical microcontroller applications.



SAIF-UR-REHMAN received the B.Sc. degree (Math (A+B), Phy) from BZU and the B.S. and M.S. degrees in electronic engineering from Mohammad Ali Jinnah University, Islamabad, and the Ph.D. degree in electrical engineering from the Capital University of Science and Technology (CUST), in 2019.

He is currently working as an Assistant Professor with Superior University, Lahore, where he is involved in research and teaching activities with the Department of Electrical Engineering and has more than ten years of teaching experience. He has more than ten journals articles in reputed journals and has also presented number of research papers at international conferences in Pakistan, Thailand, and Saudi Arabia. His research interests include microelectronics, modeling and simulation of high-frequency and high-power FETs, and antenna design. He is a Registered Engineer with the Pakistan Engineering Council (PEC), Islamabad.



M. ARSLAN USMAN (Member, IEEE) was born in 1988. He received the B.S. degree in electrical engineering from the COMSATS Institute of Information Technology, Lahore, Pakistan, in 2010, the M.S. degree in electrical engineering with Specialization in signal processing from Blekinge Tekniska Hogskola (BTH), Karlskrona, Sweden, in 2013, and the Ph.D. degree in IT convergence engineering from the Kumoh National Institute of Technology (KIT), South Korea, in 2018. After completion of his Ph.D., he continued working as a Postdoctoral Fellow with the WENS Laboratory, Department of IT Convergence Engineering, Kumoh National Institute of Technology, in August 2018. He is currently working as a Postdoctoral Research Fellow with the Wireless Multimedia and Networking (WMN) Research Group, Department of Networks and Digital Media, Kingston University London, U.K. His research interests include video quality assessment, image classification and detection, and next generation wireless networks (MIMO, NOMA, and small cells in next generation networks).

CHRISTOS POLITIS (Senior Member, IEEE) is currently a Professor (Chair) of wireless communications at the School of Computer Science and Mathematics (CSM), Kingston University. There, he is the Co-Director of the Digital Information Research Centre (DIRC) with a staff of about 25 academics, 20 postdoctoral researchers, and over 60 Ph.D. students, making it one of the largest in the field in the U.K. Upon joining Kingston University, in 2007, he co-founded and led a Research Group on Wireless Multimedia and Networking (WMN). He teaches modules on wireless systems and networks. Prior to this post, he worked at Ofcom, the U.K. Regulator and Competition Authority, as a Senior Research Manager. While at the University of Surrey, he held a postdoctoral position working on virtual distributed testbeds at the Centre for Communication Systems Research (now the 5G Innovation Centre). This was preceded by placements with Intracom-Telecom SA and Maroussi 2004 SA in Athens, Greece. He has managed to raise funding from the EU and U.K. research and technology frameworks under the ICT and Security programmes. He holds two patents and has published over 170 papers in international journals and conferences and chapters in ten books. He has advised several governmental and commercial organizations on their research programmes/agendas and portfolios. He is a U.K. Chartered Engineer and a member of the Technical Chamber of Greece.