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A Scalable Discrete-Time Integrated CMOS Readout Array for Nanopore Based DNA Sequencing

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ABSTRACT This paper introduces a high-speed mixed-signal readout array in 130-nm CMOS for the amplification and digitization of picoampere-range signals. Its design is inspired by the needs of emerging DNA sequencing technologies based on biological nanopore sensors. To overcome switching and substrate noise this system adopts an in-pixel analog-to-digital converter (ADC) architecture and a novel readout technique while consuming 10x less power than similar designs described in the literature. The in-pixel ADC architecture is inherently scalable and immune to electrical interference which can be extended to 100s of channels. With a 5 pF input capacitance, the amplifiers achieve a maximum bandwidth of 100 kHz and demonstrate a noise floor as low as 4 fA/$\sqrt{\text{Hz}}$ and a gain in the range of GΩ at 10 kHz. Circuit noise behaviour and theoretical maximum performance estimates using behavioural models are also discussed.

INDEX TERMS DNA, nanopore, continuous-time, ammeter, low noise, amplifier, ROIC, discrete-time, transimpedance, TIA, SAR, ADC, pico-ampere, nano-ampere.

I. INTRODUCTION

This paper presents a new CMOS "readout" chip capable of amplifying and digitizing very weak electrical current signals. The size of these signals is commensurate with those processed by a new generation of DNA sequencing machines. This application emphasizes not only sensitivity to small signal levels, but also bandwidth and the need to simultaneously operate over many parallel channels. To properly deal with these competing constraints as they stand now, and as they are expected to evolve, requires specially formulated readout chips, a problem addressed by the design described in this paper.

In more depth, our chip's purpose is to simultaneously carry out amplification, filtering, and digitization for individual signals as low as 10 picoampere (pA). As a necessity, this design aimed to achieve suitable per-channel signal processing quality. This goal targets the ability to process at sufficient sensitivities (∼1 pArms) and speeds (at least 4 kHz) per channel. Our system met and exceeded these application-realistic specifications.

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Of equal importance, however, was to forward a design that could practically achieve these per-channel performance targets across an array of simultaneously active pixels. For truly scalable designs, such a system should maintain its signal qualities while demonstrating a rich variety of functions, programmability, and excellent power efficiency. Over the reminder of the paper we provide the details of such a design including its specifications (§ III), the system architecture (§ IV), circuit design (§ V), experimental measurement results (§ VI), and comparison to other state-of-the-art contributions (§ VII).

First however we outline the exciting application that has motivated and constrained this design: nanopore-based DNA sequencing.

II. NANOPORE-BASED DNA SEQUENCING

An illustration of the essential technical features of a nanopore-based DNA sequences are shown in Fig. 1. The concept is straightforward: as a DNA strand goes through a small hole (the nanopore) a weak current indicative of the DNA's molecular structure (i.e., the sequence of bases A, C, G, T) is excited [1]. This is essentially the resistive pulse sensing (RPS) concept as exploited by classic instruments

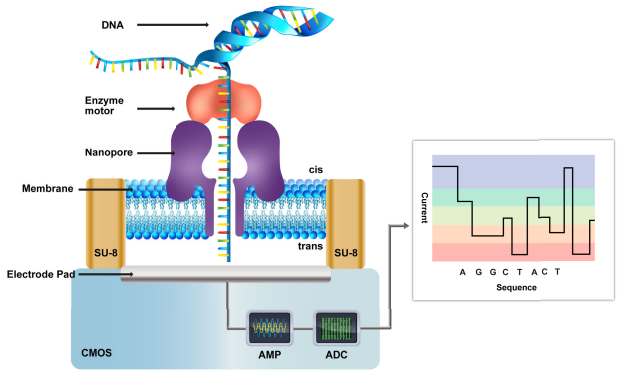


FIGURE 1. A cross-section illustration of a hypothetical nanopore-based DNA sequencing system with close interface to a CMOS readout circuit [32].

such as the Coulter particle counter [2]. An ensuing analysis (''basecalling'') of this current enables one to compute the sequence of the DNA strand that instigated it.

The thought of extending this concept to DNA sequencing is at least three decades old [3], but it was not until 2014 that mass-made nanopore-based DNA sequencing machines became generally available to laboratory practitioners [4]. This time span underscores the substantial difficulty of adapting the idea to practical DNA sequencing contexts. Although by some measures the fidelity of the nanopore-based approach is presently $\sim 10\times$ worse than incumbent DNA sequencing machines [5] it demonstrates profound advantages in many other aspects, even in this early phase of it technological development.

Among their benefits, nanopore-based sequencers can measure DNA samples directly (rather than relying on chemically modified proxies); they also conduct their measurements in a streaming, real-time, fashion (rather than batch mode); they have been shown to measure contiguous DNA up to about $10^3\times$ longer than most other sequencing methods; they sense about $10^5\times$ faster than incumbent technology; and, given their ability to pack many sensors in a small volume, they achieve a throughput per m^3 that is over $10\times$ better than established techniques. As a result, even palm-sized nanopore-based DNA sequencers have been marketed and have inspired excitement for the wide-spread deployment of DNA sequencing in low-cost and mobile contexts across a broad array of applications [6].

Numerous innovations were required to make nanopore-based sequencing practical. Naturally, the engineering of the nanopore sensor itself was critical. Presently, only bio-engineered ''biological nanopores'' (i.e., protein structures) have demonstrated commercial viability for DNA sequencing. Alternative fabrication methods (e.g., ''solid-state nanopores''), although very promising [7] have not yet managed to meet the needs of DNA sequencing applications at scale. Currently, for commercial production, in excess of 10^4 biological pores can be arrayed at densities over 10 nanopores/mm^2.

Of nearly equal importance to the nanopores themselves, have been the readout circuits that prepare these sensors' weak current outputs for ensuing digital analysis (i.e., basecalling). Readout chips must not only be able to digitize these small currents with sufficient accuracy and speed, but it is essential that they do so in an arrayed fashion. Many of the outstanding benefits of nanopore-based sequencers would be useless without the opportunity to register multiple measurements simultaneously.

This context served as the core inspiration for the CMOS readout chip we describe below. We sought to present a design that satisfied the core electrical signal processing requirements of nanopore-based DNA sequencing while also addressing the scales at which practical utilization of such a chip now calls for. Beyond satisfying the state-of-the-art as it is, we also sought to forward a design that could serve the technology as it evolves. For example, although the rates at which biological nanopore sequencers could measure DNA increased rapidly between 2014 and 2016 (from 30 Hz to 450 Hz) no further advances in per-channel speed have since been announced.

To our knowledge, a readout system as described here has not been presented in the open literature. However, a number of contributions to the area have been presented and serve as inspiration for our design. Previous works tend to focus on the realization of the analog facets of nanopore readout systems: the analog front-end (AFE). In this vein, work on suitable amplifiers has been especially active [8]–[21]. However it is almost certainly the case that as nanopore-based technology evolves, *systems* that consist of an array of channels and systems to provide a means to digitize all those channels will become critical. On this front, there have been relatively few reports.

Designs that contain readout arrays of four and twenty channels intended for use with solid-state nanopores are presented in [22] and [23], respectively. However, these contributions do not invoke any on-chip analog-to-digital converter (ADC) by which these signals may be digitized locally. To our knowledge, they also do not possess a facility to multiplex their channel signals through a limited set of chip output ports. Some interesting current readout arrays for electrochemical sensors have been presented in [24]–[30] but the bandwidth of amplifiers range from tens up to a thousand Hz. Biological nanopore experiments need tens of kHz bandwidth. A notable current readout array with 10 kHz bandwidth is presented in [31]. However, this contribution cannot be used with large input capacitance seen in nanopore sensors due to its amplifier topology. Also the system is not fully integrated as it uses off chip ADCs. We believe these are critical needs for practical systems expected to support large numbers of channels. Such features are important for nanopore-based systems intending to achieve high throughput with high sensitivity and low cost as they allow the measurements of many channels to be emitted as a serialized output stream.

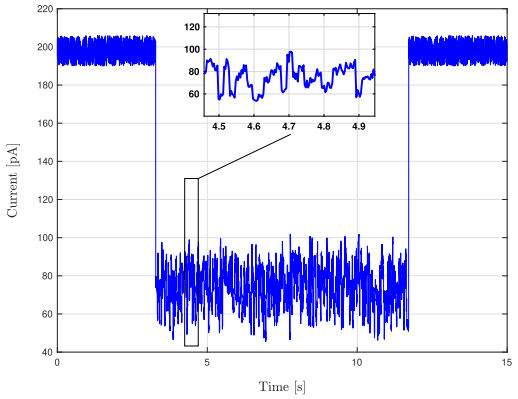


FIGURE 2. An illustration of the current through a single biological nanopore. Before and after DNA translocation a quiescent baseline current, I_{base} flows through the pore. This current drops (3-12 seconds in the illustration) when a DNA translocates through the pore. The inset provides a close-up of this translocation current.

III. SYSTEM SPECIFICATIONS

As noted above, the focus of this paper is on readout systems intended for signal conditioning of biological nanopore sensor arrays. At present, the biological nanopore sensing modality is arguably the most practical existing means of realizing high-throughput multi-channel nanopore-based DNA sequencing in the miniature. In this context, the signal specification for our system is discussed in § III-A. § III-B presents the amplifier requirements.

A. SIGNAL SPECIFICATION

A sense of the signal emerging from a biological nanopore in response to its interaction with a DNA strand is shown in Fig. 2. As with classic RPS, in the absence of DNA translocation through a nanopore, a quiescent "baseline" current, I_{base}, flows through the sensor. In realistic DNA-sequencing applications based on biological nanopores $I_{\text{base}}\approx$200 pA.

Once, a DNA strand enters the pore, thus obtruding its opening, there is a sudden drop in I_{base}, by about 150 pA. Thereafter, as shown in § II, there are fluctuations in this low current, between about 50 and 100 pA. These fluctuations are a reflection of the DNA's finer structure. Once a DNA strand has completely traversed the sensor, the current returns to typical I_{base} levels.

While the pore is obtruded by DNA, the induced low current fluctuations (see inset of Fig. 2) may be modelled as an aperiodic non-overlapping random pulse train [4]. Focusing only on the AC component of such a current signal, we can express its double-sided power spectrum with

$$S_{ii}(f) = \frac{2(\delta_i^2)}{f_t} \cdot \frac{1}{1 + (2\pi f/f_t)^2} \tag{1}$$

where δ_i^2 it the mean-square of the DNA signal fluctuations and f_t is the average translocation rate. In modern nanopore-based sequencers $\delta_i \approx 10$ pArms and $f_t \approx 450$ Hz [4].

In such a signal, 95% of the AC power lies below $2f_t$. This suggests that to barely accommodate existing nanopore-based sequencers a readout system should exhibit a bandwidth of B=1 kHz while adequately amplifying the small input with minimal noise injection. We turn to a deeper consideration of these points next.

B. AMPLIFIER GAIN AND NOISE REQUIREMENTS

As indicated above, between its maximum unperturbed I_{base} and its minimum obtruded current, the sensor's output signal swings across a range of about 150 pA. Mapping this swing to a V_{FS} = 1-V ADC full-scale input range, a practical levels for portable technologies, requires the readout to realize a resistive gain of $R_{\text{G}} \approx 6$ GΩ (196 dBΩ).

For the readout system's SNR requirements we need to account not only for the signal, but also the data processors that may follow it. As noted above, complex detection schemes are needed to convert measured nanopore data to base sequence equivalents of the corresponding DNA. The readout system must not further complicate this process by injecting too much noise of its own. For this purpose, maintaining an SNR of 20 dB should be sufficient [33].

For the minimal requirements noted above – B=1-kHz, SNR=100, δ_i=10 pArms, f_t=450 Hz – an average input-referred amplifier spot noise of

$$\sqrt{\overline{i_n^2}} = \sqrt{\frac{\delta_i^2}{\text{SNR} \cdot B}} \approx 50\ \text{fA}/\sqrt{\text{Hz}} \tag{2}$$

is needed.

A more aggressive objective is to target faster nanopore systems capable of accommodating higher f_t and thus faster sequencing rates. Indeed, today's biological nanopores are subject to intricate means of slowing down their reading ability in order to accommodate the bandwidth limits of existing readout circuitry. For example, a 20× boost in the readout system's measurement bandwidth B would require the design to achieve an average noise of about 10 fA/$\sqrt{\text{Hz}}$ instead. Our work targets such potential future performance standards.

IV. SYSTEM ARCHITECTURE

As mentioned earlier, the information signal from a biological nanopore is only about 10 pArms. This calls for an ultra-sensitive, high gain, amplifier. But intending to enable high throughput measurements by arraying a single chip with many such amplifiers, all simultaneously active, invites substantial engineering challenges. Expecting the chip to also digitize these signals imposes further complications. Even with different supplies for digital & analog components and deep n-well to provide substrate isolation, digital components are a major source of noise. Consequently, a careful choice of system components and architecture is needed to preserve the sensitivity of the analog components.

Fig. 3 shows an overview of our overall system architecture. At the highest level our design consist of three main blocks: our custom CMOS chip (digital pixel readout integrated circuit – DPROIC), a control and interface block (CI), and a networking block (NW). The CI supports all vital functions of DPROIC (reset, bias, clocking, programming, serial

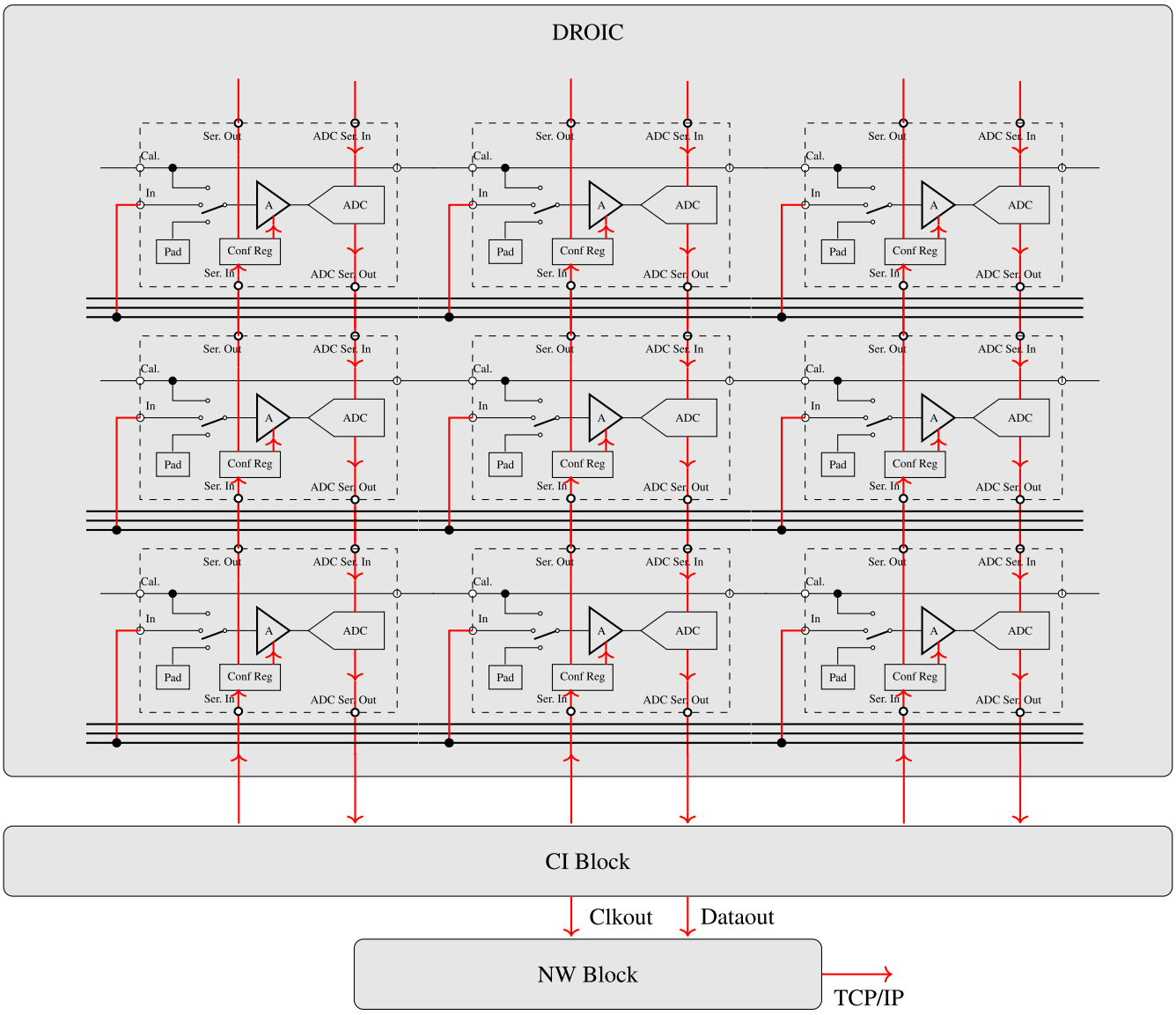


FIGURE 3. Simplified overview of system for nanopore readout (Only three rows and three columns have been shown to keep the image simple).

communications, etc.). The NW is responsible for forwarding the digitized measurement results from the CI to a remote processing system (e.g., the basecaller).The CI and NW are implemented on programmable hardware, CPLD and FPGA, respectively.

In this paper, we discuss in detail only the DPROIC block, who's internals are further elaborated in Fig. 3. As shown, the design consist of 30 channels/pixels. A major design choice for DPROIC was to implement in-pixel digitization capability. This decision affords the most flexibility for scaling. Per-pixel digitization enables more sophisticated data movement over very large arrays and it minimizes the distance over which analog data needs to be transported. Rough initial estimates indicated that even with this added complexity an extremely large array could be constructed within die sizes currently used for DNA sequencing (exceeding 100 mm^2).

V. READOUT CIRCUIT IMPLEMENTATION

This section presents an analysis of our readout system channels, its AFE component is discussed in § V-A & § V-B and its ADC in § V-C4.

A. DISCRETE-TIME AFE: AMPLIFICATION SEQUENCE

Using a capacitive-feedback TIA as the first stage provides low noise amplification (e.g. by obviating a noisy feedback resistance or active equivalent as present in continuous-time designs [16], [32]), but consequently requires a reset mechanism to avoid saturation of the amplifier. The gain of the integrator stage is dependent on its integration time period T_{INT} and on the value of the feedback capacitor C_F used. Longer integration periods and smaller feedback capacitor values give higher gain which can be expressed as

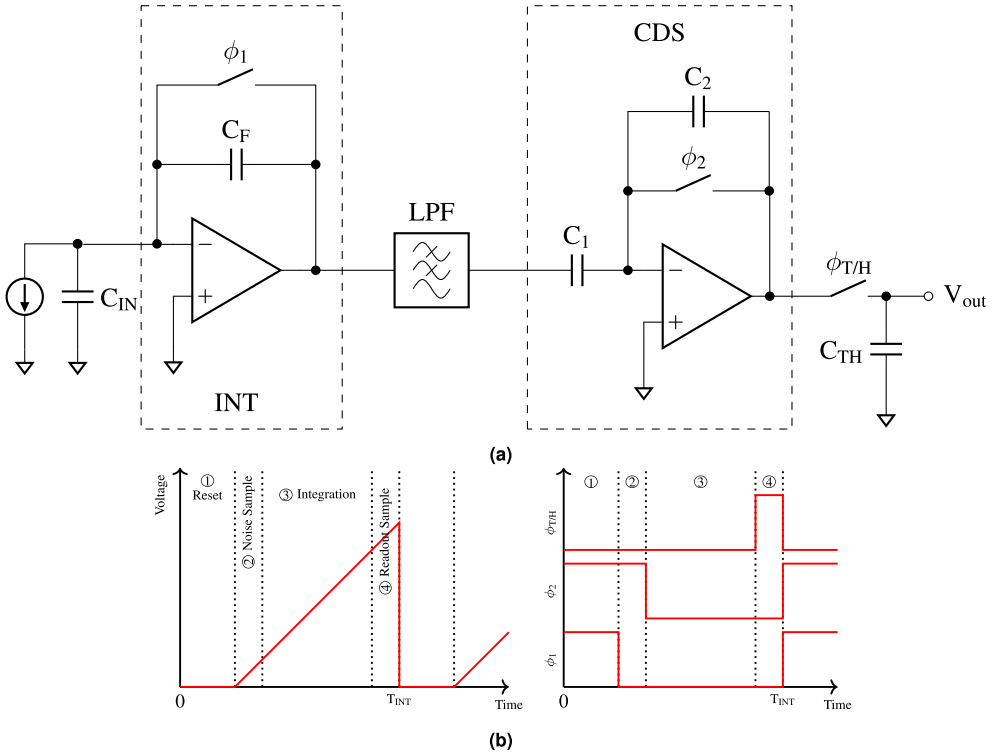


FIGURE 4. (a) DT capacitive feedback TIA. (b) Illustration of the amplifier output (left) and phase timing (right) for the amplifier.

the transimpedance

$$R_{\text{TIA}} = \frac{K \cdot T_{\text{INT}}}{C_{\text{F}}} \tag{3}$$

where K represents the fraction of the integration period over which the DT-TIA is actually engaged in integrating the input.

The AFE's output and control signals are shown in Fig. 4b where four main phases are identified:

1) Reset: The switch control signals ϕ_1 and ϕ_2 go high. As a result, the charge in the DT-TIA and CDS stages from the preceding sampling epoch is flushed by ϕ_1 and ϕ_2, respectively.
2) Noise Sample: ϕ_1 goes low and ϕ_2 remains high. In this brief phase, the DT-TIA commences signal integration while the CDS continues in reset. Effectively, a sample of the apparatus noise is captured on C_1.
3) Integration: ϕ_2 joins ϕ_1 in the low state. Both the DT-TIA integrator and CDS are activated. The CDS acts as a second stage amplifier. The noise sample captured in phase ② is removed.
4) Readout Sample: The control $\phi_{\text{T/H}}$ goes high. The sample is captured on $C_{\text{T/H}}$. This concludes the amplification process for this epoch.

B. DISCRETE-TIME AFE: NOISE ANALYSIS

To convey underlying system features, a first-order noise analysis of the DT-AFE is presented in § V-B1.

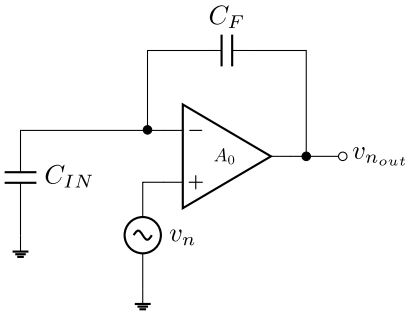


FIGURE 5. Integrator opamp noise equivalent circuit.

1) NOISE SIMULATION WITH FIRST-ORDER MODEL

The noise transfer function of the amplifier can be calculated in three steps: 1.) noise of the DT-TIA's integrator opamp amplified due to parasitic input capacitance, 2.) noise filtering due to the filter, 3.) noise shaping due to CDS and sampler. The signal transfer function can be calculated in two steps: integration stage, differentiation (CDS) stage.

Since the TIA has a synchronous reset (i.e. the sampling period, T_{S}, is equal to integration period, T_{INT}), the equivalent noise model of the integrator is captured by the schematic in Fig. 5. The equivalent input-referred current noise of CMOS opamp is 0.1×10^{-15} A/$\sqrt{\text{Hz}}$ and hence can be ignored. The input-referred voltage noise of the opamp, v_n, is amplified and filtered by the opamp. The noise transfer function (NTF) of

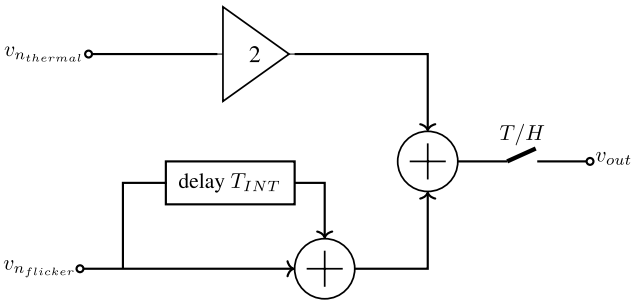


FIGURE 6. CDS equivalent circuit.

the integrator is given by

$$H_{\mathrm{i}}(f) = \frac{C_{\mathrm{T}}}{C_{\mathrm{F}} + C_{\mathrm{T}}/A_0} \cdot \frac{1}{1 + f/f_{\mathrm{c}}} \tag{4}$$

where

$$C_{\mathrm{T}} = C_{\mathrm{F}} + C_{\mathrm{IN}} \tag{5}$$

in which C_{F} is the integrator feedback capacitor, C_{IN} is the nanopore parasitic capacitor, A_0 is the DC gain of the opamp and f_c is the 3-dB cut-off frequency of the opamp. This noise is filtered using our LPF ($f_{\mathrm{c}} \gg f_{\mathrm{LPF}}$), so the NTF can be updated to

$$H_{\mathrm{LPF}}(f) = \frac{C_{\mathrm{T}}}{C_{\mathrm{F}} + C_{\mathrm{T}}/A_0} \cdot \frac{1}{1 + f/f_{\mathrm{LPF}}}. \tag{6}$$

The noise power spectral density (PSD) at the output of a LPF is thus given by

$$S_{\mathrm{LPF}}(f) = |H_{\mathrm{LPF}}|^2 \cdot S_{\mathrm{n}}(f) \tag{7}$$

where the opamp's input referred noise PSD may be modelled using [34]

$$S_{\mathrm{n}}(f) = S_{\mathrm{V_0}} \left(1 + \frac{f_{\mathrm{flc}}}{f}\right). \tag{8}$$

This model captures the opamp's underlying thermal noise component, $S_{\mathrm{V_0}}$, and flicker corner frequency f_{flc}. For our design estimates, we employ typically reported values for these terms: $S_{\mathrm{V_0}}$ around 2.5×10^{-17} V^2/Hz (i.e. $v_n \approx 5$ nV/$\sqrt{\mathrm{Hz}}$) [20], [32] and f_{flc} around 10 kHz.

The equivalent noise model of the CDS is captured by the schematic in Fig. 6. The PSD at the output of CDS is given by

$$S_{\mathrm{CDS}}(f) = |2A_{\mathrm{CDS}} \cdot \sin(2\pi f T_{\mathrm{INT}})|^2 \cdot S_{\mathrm{LPF,Flicker}} + |2A_{\mathrm{CDS}}|^2 \cdot S_{\mathrm{LPF,Thermal}} \tag{9}$$

where $A_{\mathrm{CDS}} = C_1/C_2$ is the gain of CDS. Eq. (9) has two parts. The first term corresponds to the high pass filtering experienced by the flicker noise component out of the LPF. As thermal noise is uncorrelated noise, it is not cancelled by the CDS. The second term in (9) represents the amplified thermal noise.

Finally, the noise PSD at the output of the T/H is given by

$$S_{\mathrm{OUT}}(f) = |H_{\mathrm{T/H}}|^2 \cdot S_{\mathrm{CDS}} = |sinc(\pi f T_{\mathrm{INT}})|^2 \cdot S_{\mathrm{CDS}}. \tag{10}$$

The signal transfer function (STF) of the amplifier, from the integrator to T/H, is given by

$$H_{\mathrm{SIG}}(f) = R_{\mathrm{TIA}} \cdot A_{\mathrm{CDS}} \cdot |sinc(\pi f T_{\mathrm{INT}})|\,. \tag{11}$$

Fig. 7a shows the input referred noise density of the DT-AFE for various sampling frequencies, f_{S}, with C_{IN} set to 5 pF. The flat profile at low frequencies is indicative of the degree to which the system suppresses flicker noise. At 1-kHz sampling frequencies the system can achieve a sub 0.1 fA/$\sqrt{\mathrm{Hz}}$ spot noise that rises in proportion with sampling frequency, due to diminishing transimpedance gain. At f_S = 100-kHz (signal bandwidth of 50 kHz) this parameter reaches 6 fA/$\sqrt{\mathrm{Hz}}$. Integrating the input-referred noise density across operating bandwidth we approximate the system SNR as a function of signal bandwidth in Fig. 7b. This estimate demonstrates the potential of DT-AFEs for future nanopore sequencers. For DT-AFEs based on 5-nV$\sqrt{\mathrm{Hz}}$ amplifiers, a 20-dB SNR is possible for 25 kHz signals, about 25-times greater than the minimal contemporary needs noted above.

C. READOUT CHANNEL: IMPLEMENTATION

This subsection briefly outlines the circuit components used for the implementation of the readout channel.

1) INTEGRATOR

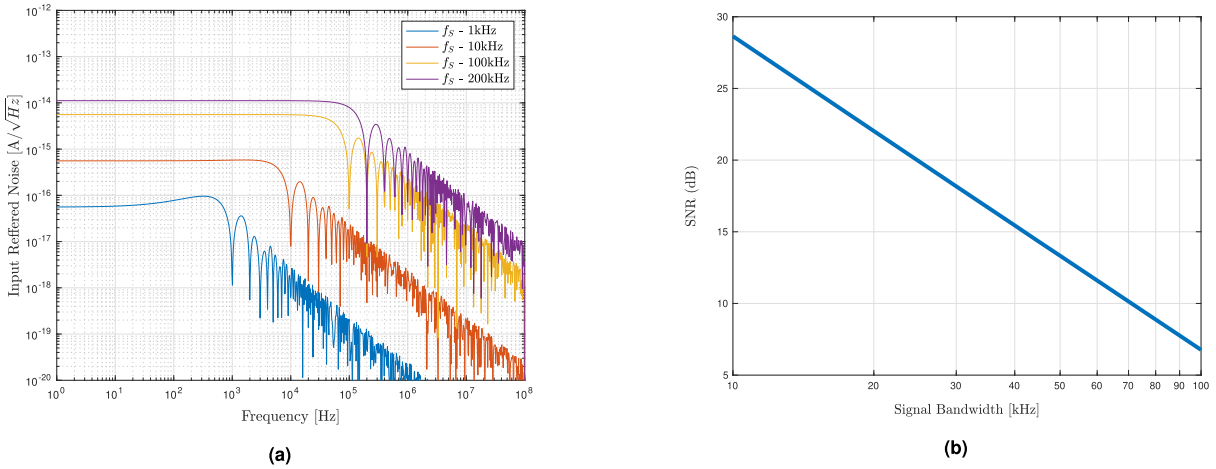
The amplifier uses an active integrator. The folded cascode opamp used in the integrator. It consumes of 105 μA current from a 1.2 V power supply. The opamp has been optimized for low noise. An input PMOS differential pair and large devices are used to reduce flicker noise. The opamp has a simulated thermal noise of 7.7 nV/$\sqrt{\mathrm{Hz}}$ while the corner frequency is approximately 5 kHz. The open-loop DC gain of the opamp is 65 dB while the unity gain bandwidth is 100 MHz. The value of feedback capacitor C_i can be varied from 25 fF to 150 fF.

2) FILTER

The amplifier uses a Gm-C filter. To implement an RC filter in range of tens of kHz requires a large resistor and hence a large area. The resistor can be also implemented using a transconductor or active resistor. Though mosfet-C filter have better linearity, Gm-C filter have faster settling time. The time constant of a Gm-C filter is given by

$$\tau_{\mathrm{LPF}} = \frac{C_{\mathrm{LPF}}}{g_{\mathrm{m}}} \tag{12}$$

where C_{LPF} is the capacitor used in the filter and g_{m} is the transconductance of the transistor. The filter's time constant can be varied by either changing the capacitor or the g_{m} of the transistor. In this implementation, the time constant is varied by changing the g_{m} using the bias current while 1 pF capacitance was used. The W/L of PMOS device was chosen



(a) (b)

FIGURE 7. (a) Input referred noise density of DT-TIA at various sampling frequencies (f_S). (b) SNR with respect to signal bandwidth for DT TIA model.

TABLE 1. Simulated input referred noise of the amplifier for various bandwidth with a 5 pF input capacitance and a 20 fF integrator feedback capacitance.

Bandwidth (kHz)	Input Ref. Noise Flr. (fA/$\sqrt{\text{Hz}}$)	Integrated Noise (pArms)
10	4.68	0.336
12.9	5.87	0.478
18.2	7.94	0.765
30.7	12.53	1.56
100	36.25	8.12

to be 1μm/2μm. The PMOS source follower transistor was biased in sub-threshold region and has a g_m that can be varied from 100 nS to 5 uS. The g_m of the voltage follower remains constant from 0.05 to 1 V input voltage. The Gm-C filter settle faster compared to comparable RC filter due to large V_{GS} during reset.

3) CORRELATED DOUBLE SAMPLING

An active CDS was employed in the amplifier. By using active CDS, the signal can be further amplified for data conversion. The CDS uses the same opamp used in the integrator. The value of C_1 used is 350 fF while C_2 can be varied from 50 fF to 150 fF. The effect of kT/C noise of C_2 is negligible.

The performance of the amplifier with respect to bandwidth is shown in Table. 1. The simulation was performed with a 5 pF input capacitance and 20 fF feedback capacitor. It is evident from the results that noise floor is dependent on sampling period and integration period.

4) ADC

SAR ADCs are usually used for medium resolution and data rates in the range of few mega samples per second (MSps) while operating at low power [35]. For 10-bit resolution, single slope or double slope ADC would require a very fast clock (0.5-1 GHz). Due to high gain amplifier, implementing such high speed digital circuits can introduce noise in analog circuits.

TABLE 2. Gain and bandwidth options for components in each channel.

Component	Effect	Settings
Integrator	Feedback Capacitor	20fF, 50fF, 100fF
Gm-C Filter	Current/Gm	3 Current Settings
CDS	Gain	2x, 4x, 8x

The SAR ADC included in this design consists of a capacitive digital-to-analog converter (DAC), a comparator and digital circuits to perform a binary search algorithm. The digital output of the ADC can be in serial or parallel form.

In this design, a 10-bit synchronous SAR ADC was implemented. This implementation uses a split capacitor DAC [35] for smaller area and a class AB latched comparator to reduce kickback noise.

Table 2 shows the options available for gain and bandwidth adjustment in each channel. Fig. 8 shows the layout of the DNA nanopore array. The 3 × 2 mm chip is fabricated in 0.13-μm CMOS technology. The area of each channel is 320 × 220 μm^2.

D. READOUT MODES

Nanopore readout system need ultra-sensitive amplifiers but this makes integration of readout circuitry challenging. An AC noise from digital switching of ADCs couples into the high impedance input node of sensitive amplifiers from substrate and power supply through a capacitive link. The noise can minimized using deep n-well & p+ guard ring and using separate power supply for digital and analog circuits. The noise sampling phase occurs after the amplifier is reset while the sampling phase occurs at the end amplification period. To minimize the impact of this AC noise due to digital circuit, the readout needs to be performed outside

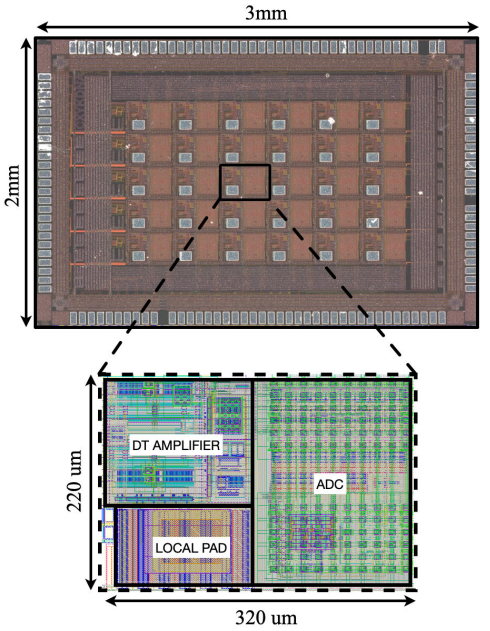


FIGURE 8. Chip micrograph and detailed floorplan of a channel.

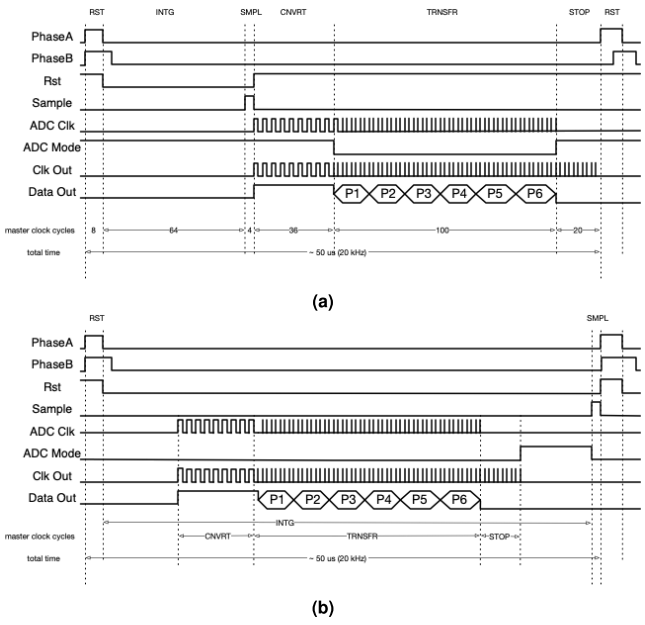


FIGURE 9. (a) Timing diagram for serial ADC operation scheme (b) Timing diagram for parallel ADC operation scheme.

the these two phases otherwise it corrupts the measured signal.

To overcome this problem this section shows two ADC operation modes, serial and parallel. The timing diagram of serial and parallel mode is shown in Fig. 9a and 9b respectively. In the serial operation mode, the ADC conversion and data transfer is done right after the output is sampled. The amplifier is not operated while the ADC is performing conversion. This leaves some dead-time when the amplifier is non-operational. In parallel mode, the ADC conversion

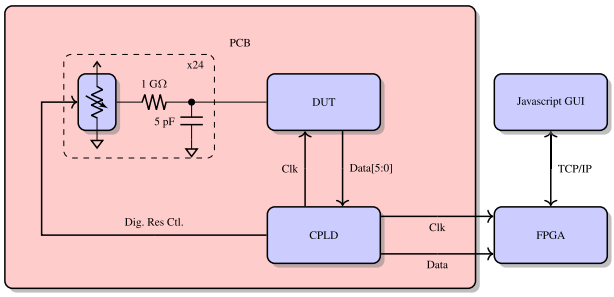


FIGURE 10. Block diagram of the implemented TIA test setup.

and data transfer are performed between the two CDS samples. It is clear from Fig. 9 that parallel mode improves the integration time and hence the overall performance of the amplifier.

VI. MEASUREMENT RESULTS

A. MEASUREMENT SETUP

The block diagram for test setup has been shown in Fig. 10. The sensor is modeled on PCB using a 1-GΩ resistor and 5-pF capacitor. Due to ultra-sensitive amplifiers careful testbench considerations were needed. Digital resistors are low noise compared to on-desk voltage sources. They also provide the opportunity to generate analog waveforms for multiple channels simultaneously. Hence digital resistors, which act as a voltage divider, were used along with 1-GΩ resistors to generate test signals in the range of pico-amperes.

Another important design choice was to use a complex programmable logic device (CPLD) instead of a field programmable gate array (FPGA). Intel CPLDs do not need any external oscillator. This is very useful as it provides isolation from large noisy signal of the oscillator. The entire analog frontend and CPLD are placed inside a shielded box. Another FPGA board which is isolated from the analog frontend is used to receive the data transmitted from the CPLD. The CPLD serializes the data from all ADCs and forwards it to the Xlinix Zynq 702 FPGA evaluation board. The CPLD is also responsible for loading the configuration registers on the test chip.

The Xlinix FPGA receives the serialized data along with its clock and stores deserialized data it a buffer. This data is transferred via TCP/IP socket to a Javascript graphical user interface (GUI) application. The data is plotted and saved by the GUI in real-time. To guarantee real-time operation the FPGA uses DMA to transfer data from buffer to TCP/IP socket.

B. AFE MEASUREMENT RESULTS

1) TRANSIENT RESULTS

Fig. 11 shows the transient output of the integrator, filter and CDS for a DC input current of 10 pA. The integration time for this measurement was set to 61 μs. The reset period of the integrator and filter is 6 μs while for the CDS it is 15 μs.

TABLE 3. Gain and input referred noise for various gain and filter settings.

Gain Setting (binary)	Filter Setting (binary)	Input Current (pA)	Output Voltage (mV)	Gain (GΩ)	Inp. Ref. Noise (pArms)	Sampling (kSps)	Filt. Band. (kHz)
110	111	40	240	6	1.49	13.95	90
	101	40	240	6	2.15	13.95	500
	100	40	240	6	1.4	13.95	90
	000	40	240	6	1.33	13.95	15
100	111	40	520	13	1.73	13.95	90
	101	40	520	13	1.94	13.95	500
	100	40	520	13	1.71	13.95	90
	000	40	520	13	1.5	13.95	15
010	111	40	340	8.5	1.29	13.95	90
	101	40	340	8.5	1.7	13.95	500
	100	40	340	8.5	1.27	13.95	90
	000	40	340	8.5	1	13.95	15

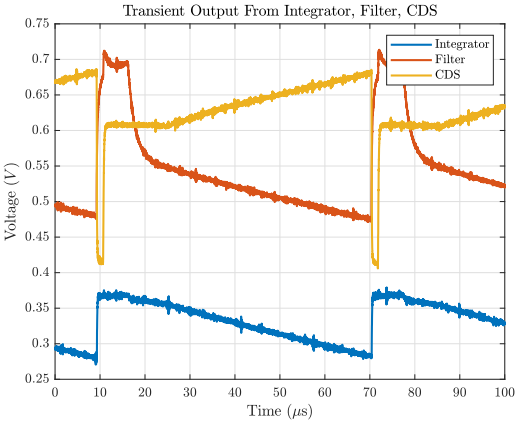


FIGURE 11. Transient output of integrator, filter and CDS for 10 pA DC current.

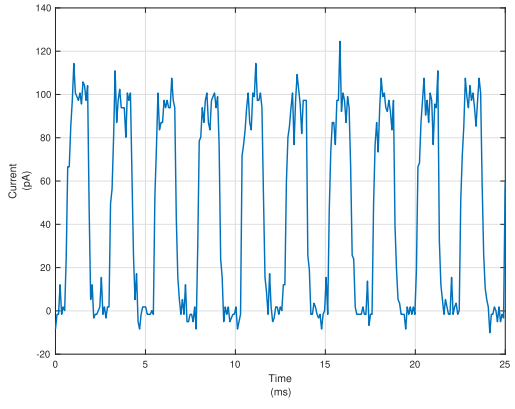


FIGURE 12. Digitized output for 400 Hz input square wave with a 100 pA pk-pk amplitude digitized at 16 KS/s.

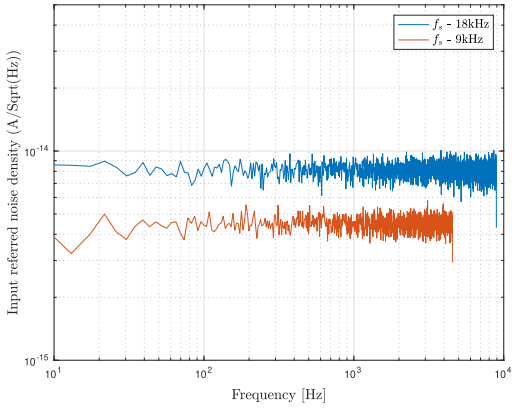


FIGURE 13. Open-input noise spectrum of the system at 9 kHz and 18 kHz sampling frequency.

TABLE 4. Performance summary for the nanopore detector array.

System	
Technology	0.13 μm
Supply Voltage	1.2 V
Chip Dimensions	3 mm×2 mm
No. of Channels	30
Power Dissipation	10.25 mW
Interference	0.1%
Channel	
Bandwidth	0-100 kHz
Area	320 μm×220 μm
Input-Ref. Noise	1 pArms
Input Capacitance	5 pF
Amp. Power Dissipation	0.22 mW

C. COMPLETE CHAIN RESULTS

1) TRANSIENT RESULTS

The transient output for 400 Hz 100 pA pk-pk input square wave is shown in Fig. 12. The input capacitance of amplifier was 5 pF and sampling frequency was 16 KS/s.

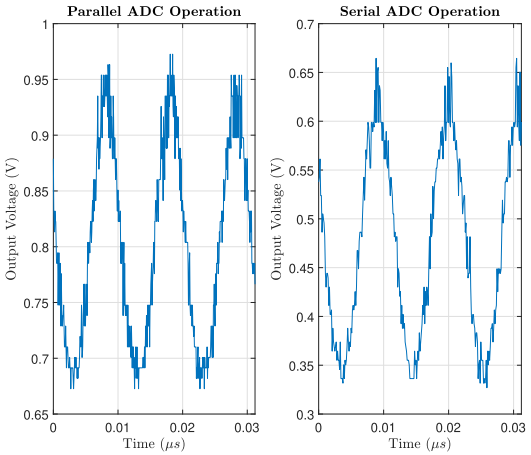
2) GAIN AND NOISE

Fig. 13 shows the open-input noise spectrum at various sampling frequency. The noise measurement for various gain settings of the integrator is shown in Table 3. The optimal gain setting is '010' as this maximizes the gain without

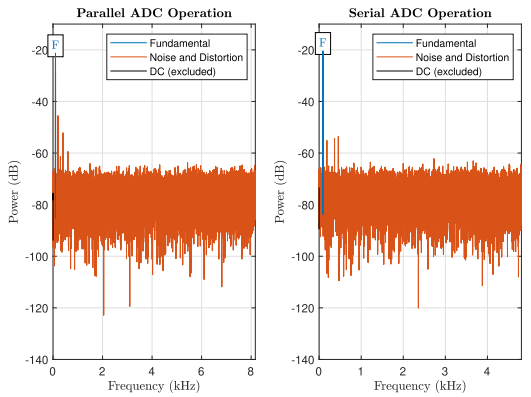
TABLE 5. Performance comparison with state-of-art nanopore arrays and amplifiers.

	This Work	[22],'12	[23],'16	[20],'14	[13],'12[1]	[16],'09	[8],'16
Technology	0.13 m	0.18 μm	0.18 μm	0.35 μm	0.5 μm	0.35 μm	.18 μm
Supply Voltage	1.2 V	1.5 V	1.5 V	3.3 V	3.3 V	3.3 V	1.8 V
No. of Channels	30	4	25	1	2	1	1
Power/Channel	340 μW	4.5 mW	5.1 mW	40 mW	1.5 mW	-	5.22 mW
Bandwidth	0-14 kHz	0-1MHz	0-1MHz	0-10 kHz	0-10 kHz	0-1 MHz	0-10 kHz
Channel Area	0.07 mm^2	0.25 mm^2	0.16 mm^2	-	0.13 mm^2	0.35 mm^2	0.0912 mm^2
Input-Ref. Noise	$\sim$1 pArms	$\sim$155 pArms	$\sim$129.4 pArms	1.2 pArms	2.44 pArms	-	1.25 pArms
Noise Floor	4.5 fA/$\sqrt{\text{Hz}}$ @ 10 kHz	$\sim$31 fA/$\sqrt{\text{Hz}}$	$\sim$31 fA/$\sqrt{\text{Hz}}$	6 fA/$\sqrt{\text{Hz}}$	5 fA/$\sqrt{\text{Hz}}$	6 fA/$\sqrt{\text{Hz}}$	11.6 fA/$\sqrt{\text{Hz}}$
Input Capacitance	5 pF	3 pF	10 pF	3 pF	47 pF	0 pF	0 pF
Integrated ADC	Yes	No	No	Yes	No	No	No

[1] The chip does not include an on-chip CDS.



(a)



(b)

FIGURE 14. (a) Transient output of sine wave (100 pA) digitized with two ADC operation mode. (b) Spectrum of sine wave (100 pA) digitized with two ADC operation mode.

clipping the signal, even though setting '100' provides the maximum gain. The bandwidth of the measurement was set to 13.95 kHz. The least observed noise at this bandwidth is 1 pArms.

3) READOUT MODE

As highlighted in § V-D, the amplifier is sensitive to ADC digital noise. This section provides a digitized results comparison for each mode.

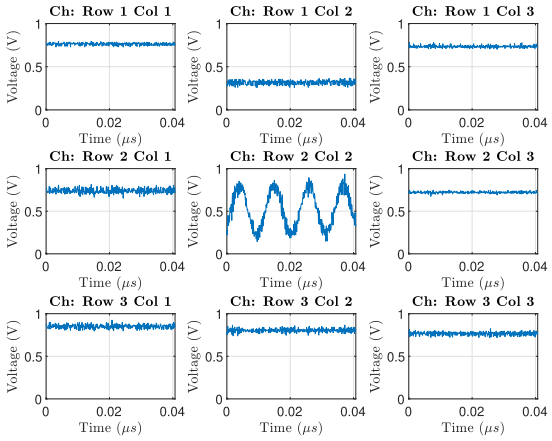


FIGURE 15. Transient output multiple channels operating in parallel with one channel stimulated.

It can be seen in Fig. 14 that amplifiers operate normally even with the ADC operating during the integration phase. But ADC operation causes a heavy DC offset in the output signal. During the serial ADC operation, the offset current was 10 pA while for parallel operation the offset current was 300 pA. This is probably due to unwanted current injection from the substrate during ADC operation but with proper input current offset cancellation circuitry it can be corrected easily.

By operating the ADC in parallel, the dead time is removed and it improves the performance of the system. But this comes with added distortion. The SNDR of serial readout mode for bandwidth of 4 kHz is 21.35 dB while for parallel readout it is 19.58 dB for 100 pA signal sampled using 16 kSps.

4) CHANNEL INTERFERENCE

The transient output of nine channels measured simultaneously is shown in Fig. 15. It was noted that two channel in the same row exhibit a spur which is about 1000 times smaller than the signal in the active channel. This due to the capacitive coupling from wire routing of the input signal. If the local-pads are used there will much lower electrical coupling. The SNDR at 4 kHz bandwidth for 150 pA input signal is 24.12 dB.

A summary of the systems main physical and performance characteristics is given in Table 4.

VII. CONCLUSION

This paper presented a signal conditioning array for nanpore-based DNA sequencing. The array consists of 30 channels, each channel contains a DT amplifier and in-pixel SAR ADC. The DT amplifiers have a gain of GΩ and are capable of sensing a pico-ampere current. This chip is a complete system with integrated electrode and readout circuits which sets the stage for high throughput DNA sequencing experiments. The chip has been validated against emulated nanopore signals and was found functional. The chip is intended for use with biological nanopore and has on-chip electrodes to implement highly integrated sensors. The performance comparison with other nanopore arrays have been presented in Table 5. The system is the first complete array ROIC with multiple channels and integrated ADCs found in literature for nanopore based DNA sequencing. Using novel readout techniques, triple-well isolation, filtering and low crosstalk PCB components the system was able to overcome problems caused by integrating digital circuits. Furthermore, the power consumption of the amplifier is 10x lower compared to state-of-art DT amplifier with comparable noise and bandwidth presented in [20] and [13]. The channels also has the smallest area consumption compared to other state of the art nanopore amplifiers which is imperative for large arrays. The chip also contains various gain & filter settings as well as calibration circuits to deal with process variations. The system has 1000x smaller cross-talk in neighbouring channels compared to actual signal amplitudes. This low electrical cross-talk and in-pixel ADC architecture, facilities the ability to scale to hundreds of channel.

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