IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 1, 2021, accepted November 15, 2021, date of publication November 17, 2021,
date of current version December 3, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3128948

Asynchronous Digital Low-Dropout Regulator With Dual Adjustment Mode in Ultra-Low Voltage Input

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ABSTRACT This paper presents the asynchronous digital low-dropout regulator (AD-LDO) with dual adjustment mode in ultra-low voltage input. The architecture of the proposed AD-LDO consists of the asynchronous control loop and the power PMOS array. The proposed AD-LDO is controlled by switched bidirectional asynchronous control loop which can eliminate the clock power consumption of synchronous LDO. The dual adjustment mode can not only provide wider loading current, but also can reduce output voltage ripple. Moreover, the proposed AD-LDO only uses one bidirectional asynchronous control loop for two adjustment modes, so it can save area and reduce power consumption. Under the 350mV input voltage and 300mV output voltage, the proposed AD-LDO can provide 2.4mA output current with 99.8% current efficiency and only consume 5μA quiescent current. Therefore, the proposed LDO is suitable for applications of wearable electronic devices with an ultra-low supply voltage.

INDEX TERMS Asynchronous digital low-dropout regulator, asynchronous control loop, ultra-low voltage, dual adjustment mode, wearable electronic devices.

I. INTRODUCTION

In recent years, integrated circuit (IC) design of wearable electronic products has developed in the direction of ultra-low voltage, ultra-low power consumption and high integration. The most important issues of wearable electronic products are small area and low power consumption. In power management system, there are two kinds of power circuits to provide the required power supply voltage: the switching converters, and the low-dropout regulators (LDOs). The advantage of LDO is that it does not require additional inductors like switching converters. Therefore, it is suitable for integration in a chip. Another important issue is power consumption. The power consumption of a circuit can be given as follows:

$$\text{Power consumption} = C_{LD} \times V_{DD}^2 \times f + I_{off} \times V_{DD} \quad (1)$$

where C_{LD} is the equivalent load capacitance, V_{DD} is the supply voltage, f is the operating frequency, and I_{off} is the standby current. According to the formula (1), the most effective method to reduce power consumption is to decrease the supply voltage V_{DD} for extending use time of wearable electronic produces. As illustrated in Fig. 1, the system-on-a-chip (SoC) of a wearable electronic product includes various analog, digital, mixed-signal, and RF circuits. In references [1]–[11], many circuits with a supply voltage of 0.3V have been proposed. Therefore, the design of power management IC will focus on ultra-low voltage design to achieve ultra-low power consumption.

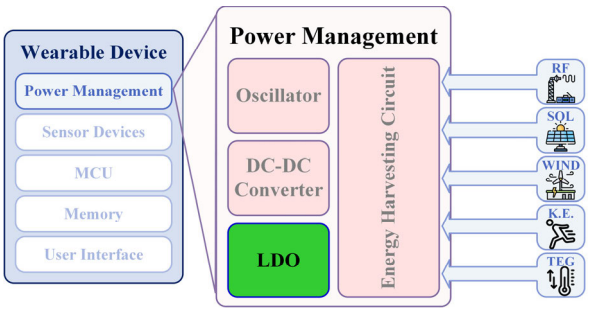

FIGURE 1. Clock frequencies of modern consumer electronic applications.

The associate editor coordinating the review of this manuscript and approving it for publication was Meng Huang.

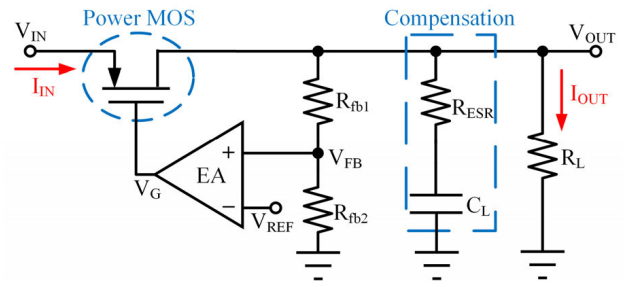

FIGURE 2. Architecture of conventional LDO.

The LDO is more suitable for ultra-low power circuits than the switch converter because it has the advantages of small chip area, low circuit complexity, and low output voltage ripple. As shown in Figure 2, the traditional analog LDO consists of the error amplifier (EA), the power MOS, two feedback resistors (R_{fb1} and R_{fb2}), a load capacitor (C_L), and an equivalent series resistance (R_{ESR}) in parallel with a load resistor (R_L). The operation performs the following steps in order. First, the EA compares the voltage error between feedback voltage (V_{FB}) and reference voltage (V_{REF}) to generate an analog voltage signal (V_G) to control the power MOS. Second, a corresponding output current is generated to regulate the output voltage by adjusting the V_G voltage of the power MOS. Since there is no influence of the switch, the output voltage of the LDO is more stable than the switching converter. However, due to limitation of the threshold voltage (V_{TH}) and voltage headroom, the traditional analog LDO is difficult to design in ultra-low voltage systems. Conversely, the digital LDO is easily to design in ultra-low voltage system.

Figure 3 shows the branch diagram of digital LDOs architecture. The circuit architecture is divided into three parts: synchronous, asynchronous and hybrid. Most architectures of digital LDOs are synchronous system [11], [20]–[25], [27]–[32]. The advantage of the synchronous digital LDO is that the design is simple, and the clock is responsible for the operation of the circuit. However, the synchronous digital LDO is controlled by the clock, and it will encounter several problems. The first is the clock skew problem, which will cause the internal control state value of the digital LDO to be wrong, and the output voltage of the digital LDO cannot be locked. The second is the operating frequency setting problem. As shown in Fig. 4 [16], the clock (F_{clk}) frequency is related to the tracking time and the current efficiency. Due to the high frequency, the tracking time is short. However, it will cause a large power consumption of quiescent current in the locked state. On the contrary, the low frequency cause the long tracking time, but the quiescent current power consumption is lower. Both NMOS and PMOS power MOSs are used to reduce the effect of transient response on output voltage in [16]. In [17], [18], asynchronous multi-loop is used to improve the problem of slow thermal code tracking, speed up the tracking speed and voltage regulation accuracy. However, it takes a lot of quiescent current. In [26], the asynchronous method is use to fast lock, and then switch to an analog LDO for voltage stabilization. However, the analog LDO cannot be used at ultra-low voltage. Reference [33] uses asynchronous-flash for fast tracking, and then use bidirectional synchronous shift register for voltage regulation. In [16]–[18], [26] and [33], asynchronous digital LDO uses handshaking protocol to communicate with neighboring circuits instead of clock signals. It has the advantages of high tracking speed and no clock skew problem. Since there is no clock, the quiescent current power consumption in the locked state is extremely low. Therefore, this paper proposed an asynchronous digital low-dropout regulator with dual adjustment mode in ultra-low voltage input in a standard 90 nm CMOS process technology.

(1) Only one switched bidirectional asynchronous control loop. The proposed AD-LDO only uses the same SBACL for two adjustment modes, so it can save area and reduce power dissipation.
(2) Ultra-low voltage applications. This indicates that the architecture can be applied to 0.35V and low-power applications.

The remainder of this paper is organized as follows: Section II describes the circuit structure and operating principle of the proposed AD-LDO. Section III presents the simulation results. Finally, the conclusion is drawn in Section IV.

II. CIRCUIT STRUCTURE AND OPERATING PRINCIPLE OF THE PROPOSED AD-LDO

Figure 5 shows the circuit architecture of the proposed asynchronous digital LDO which consists of the asynchronous digital control loop and the power PMOS array. In Ref [16], the whole circuit consists of a phase-locked loop (PLL), a switching regulator and an asynchronous digital LDO. The coarse adjustment circuit is designed with asynchronous digital LDO, and the fine adjustment circuit is realized with a switching regulator. However, the proposed AD-LDO only utilizes an asynchronous digital LDO to complete the coarse and fine adjustment of the lock. Thus, this can save a lot of chip area and power consumption.

The voltage difference between the reference voltage V_{REF} and the output voltage V_{OUT} is converted into the set of digital codes through dual adjustment mode in the asynchronous digital control loop. The set of digital codes controls the subsequent power PMOS array to charge the output voltage V_{OUT}. Therefore, the output voltage is regulated. In addition, the transfer function in [25] mentions a digital LDO as a first-order feedback system. Therefore, the proposed AD-LDO has enough phase margin to keep the circuit in a stable state. The relative operating principles and circuit architecture of the asynchronous digital control loop and the power PMOS array are as follows.

A. THE DESIGN CONCEPT OF DUAL ADJUSTMENT MODE

Figure 6 illustrates the operation principle of the coarse adjustment mode, the fine adjustment mode and the dual

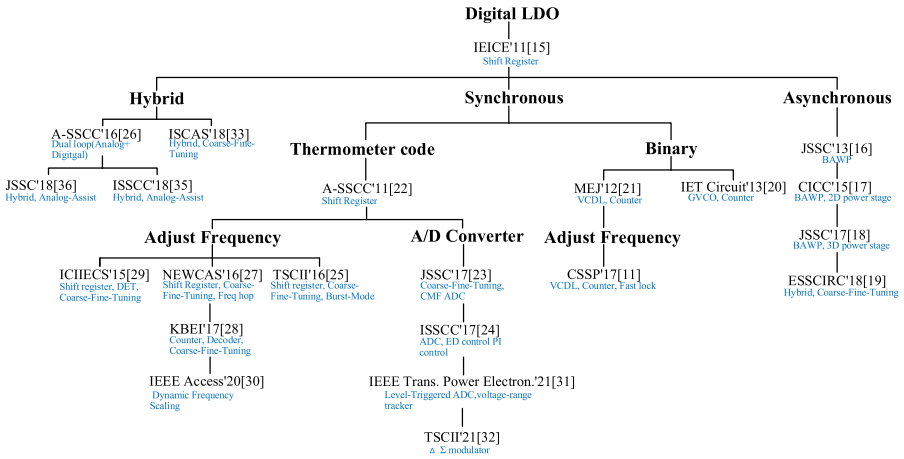

FIGURE 3. The systematic integration of digital LDO.

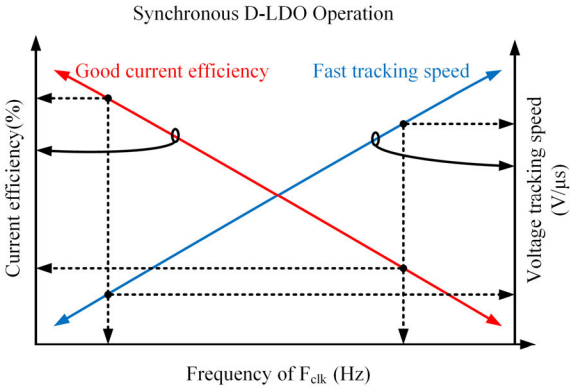

FIGURE 4. The performance analysis of synchronous LDO.

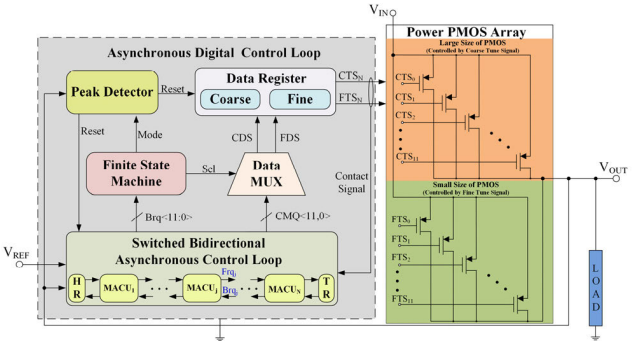

FIGURE 5. The architecture of proposed asynchronous LDO.

adjustment mode. The traditional digital LDO only uses the coarse adjustment mode or the fine adjustment mode to track the reference voltage. If the coarse adjustment mode is selected, it has the advantage of fast locking, but the output voltage has a large voltage ripple after locking. On the contrary, if the fine adjustment mode is selected, the tracking time will be longer, but the output voltage will be more stable after the lock. Based on the above, the proposed AD-LDO adopts dual adjustment mode to achieve fast locking and low output voltage ripple characteristics.

B. THE ASYNCHRONOUS DIGITAL CONTROL LOOP

The asynchronous digital control loop consists of a switched bidirectional asynchronous control loop (SBACL), a finite state machine (FSM), a data MUX, a peak detector, and a data register. The peak detector circuit structure is shown in Fig. 7. The circuit consists of two inverters with different logic threshold voltages and digital logic gates. When the mode signal is high, the peak detector is operating in the coarse adjustment mode. This circuit will not activate the detection function. On the contrary, when the mode signal is low, it is the fine adjustment mode. If the feedback voltage (VFB) exceeds the set voltage range of two inverters, the XNOR will output a high level. At the same time, the mode signal is low and a pulse signal (Reset) is generated after the subsequent logic gate operation. The Reset signal is provided to the system to restart the coarse adjustment mode.

In the initial state, the asynchronous digital control loop operates in the coarse adjustment mode. After the SBACL compares the reference voltage V_{REF} and the feedback voltage V_{OUT}, it generates a set of coarse adjustment digital codes CTS_N to control the subsequent large size PMOS array to achieve fast locking operations. When the fast locking operation is completed, coarse adjustment digital codes CTS_N will be recorded in the coarse data register. Then enter the fine adjustment mode, the SBACL sends a control signal Brq <11:0> to the FSM to generate two control output signals Sel and Mode. The fine adjustment digital code of SBACL is sent to data register through the output FDS of the data MUX under the selection signal Sel. Another signal Mode is sent to the peak detector to detect whether the V_{OUT} voltage change exceeds the fine adjustment range. In the fine adjustment mode, the reference voltage V_{REF} and the feedback voltage V_{OUT} are compared through the SBACL to generate a set of the fine adjustment digital codes FTS_N. This set of digital codes control the subsequent small size PMOS array to achieve fine-tuning operation. When the fine-tuning operation is completed, fine adjustment digital codes FTS_N

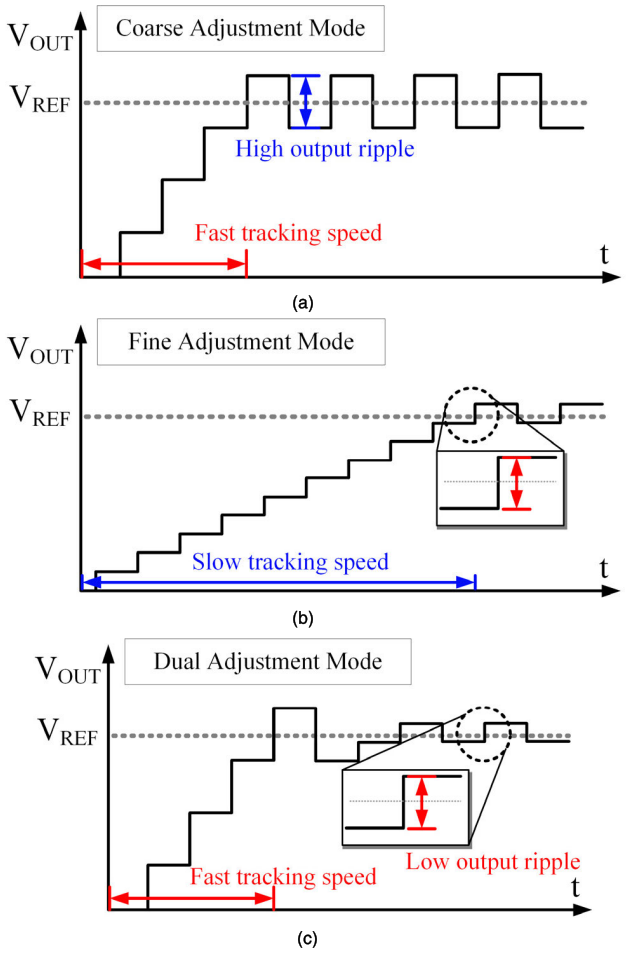

FIGURE 6. The operation principle of (a) the coarse adjustment mode (b) the fine adjustment mode and (c) the proposed dual adjustment mode.

will be recorded in the fine data register. The lock time T_{LOCK} of the proposed AD-LDO is given as follows:

$$\begin{aligned} T_C &= I_C \times R_{LOAD} \times \sum_{n=0}^{j-N} T_n; \\ T_F &= I_F \times R_{LOAD} \times \sum_{n=0}^{i-N} T_n \qquad (2) \\ T_{LOCK} &= T_C + T_F \\ &= I_C \times R_{LOAD} \times \frac{1+j-N}{2} \times (j-N) \times T_n \\ &\quad + I_F \times R_{LOAD} \times \frac{1+i-N}{2} \times (i-N) \times T_n \qquad (3) \end{aligned}$$

$$\begin{aligned} \text{if } I_C &= mI_F \\ \text{then } T_{LOCK} &= \frac{1+m}{m} \times I_C \times R_{LOAD} \times \left[\frac{1+j-N}{2} \right. \\ &\quad \left. \times (j-N) + \frac{1+i-N}{2} \times (i-N) \right] \times T_n \qquad (4) \end{aligned}$$

where R_{LOAD} is an equivalent resistance of loading, N is the total number of modified asynchronous control units

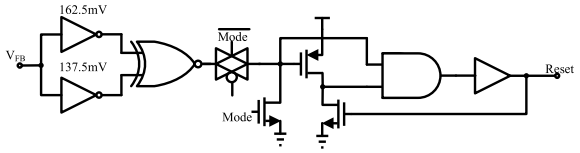

FIGURE 7. Circuit structure of the peak detector.

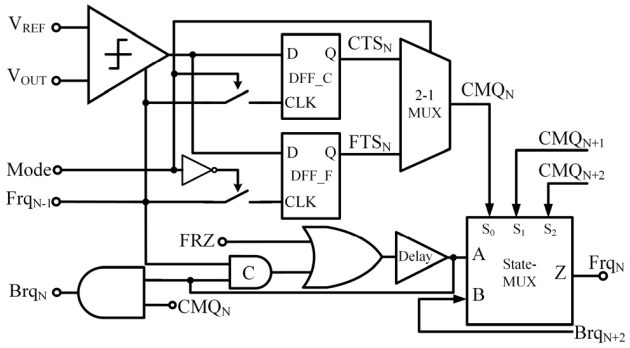

FIGURE 8. Circuit structure of the proposed modified asynchronous control unit.

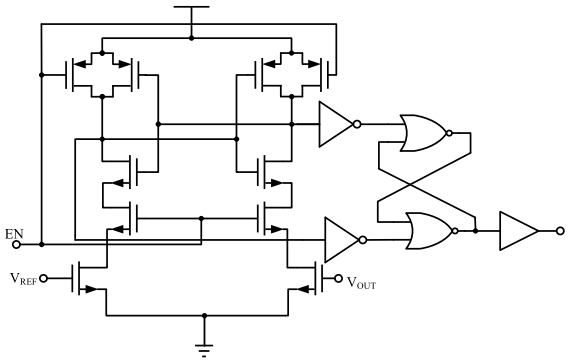

FIGURE 9. Circuit structure of the clocked-comparator.

(MACU). I_C and I_F are the currents of large size PMOS and small size PMOS, respectively. T_C is the time of the coarse adjustment operation to the (j-N)th stage, T_F is the time of the fine adjustment operation to the (i-N)th stage, and T_n is the operating time of each MACU in SBACL. The total lock time T_{LOCK} can be expressed in formula (3). If I_C is m multiplied by I_F, the relational expression of T_{LOCK} is as shown in formula (4). Therefore, the ratio of the coarse current to the fine current can be set to reduce the lock time keep the voltage ripple low.

C. SWITCHED BIDIRECTIONAL ASYNCHRONOUS CONTROL LOOP (SBACL)

As shown in Fig. 5, the SBACL consists of the heading reflector (HR), MACUs and the terminal reflector (TR). The HR and the TR [16] are used as the boundary of the SBACL. The MACU circuit structure is illustrated in Fig. 8. When the Mode signal is high, the SBACL is in the coarse adjustment mode. The comparator of the MACU is shown in Fig. 9. It is a clocked-comparator structure. The comparator of the MACU is triggered by the previous-stage forward signal to

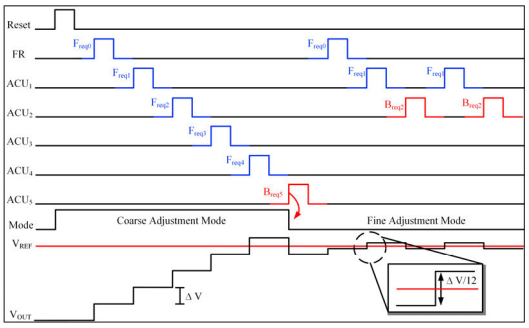

FIGURE 10. Timing diagram of AD-LDO.

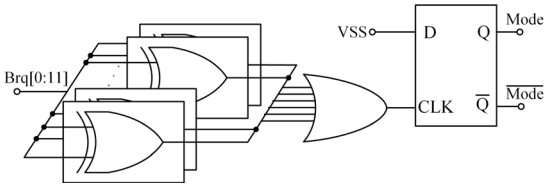

FIGURE 11. Circuit structure of finite state machine.

compare the voltage difference between V_{REF} and V_{OUT}, and the resulting output signal is sent to the output CTS_N of the DFF_C. Then send the CTS_N signal to CMQ_N by selecting 2-1 MUX to control the subsequent large size PMOS for fast locking. Moreover, the 2-1 MUX output signal CMQ_N and output signals $CMQ_N + 1$ and $CMQ_N + 2$ of the next two stages are sent to the State-MUX as selection signals. As shown in Table 1, the MACU passes the forward signal to the next stage MACU or backward signal to the previous stage MACU by selecting the signal combination. As described above, each stage of MACU will do the same operation until the SBACL completes the coarse adjustment operation. After the coarse adjustment operation is completed, the DFF_Cs of MACUs saves the coarse adjustment digital codes and then enters fine adjustment mode. When the Mode signal is low, the SBACL is in fine adjustment mode. The same MACU is used for the fine adjustment operation without extra area cost. The comparator of the MACU compares the voltage difference between V_{REF} and V_{OUT}, and the resulting output signal is sent to the output FTS_N of the DFF_F. Then send the FTS_N signal to CMQ_N by selecting 2-1 MUX to control the subsequent small size PMOS for low output voltage ripple operation. Finally, after the fine adjustment operation is completed, the DFF_Fs of MACUs saves the fine adjustment digital codes. Therefore, the dual adjustment mode proposed in this paper only uses one set of SBACL without increasing extra area cost.

D. OPERATION PRINCIPLE OF THE AD-LDO

The timing diagram of the proposed SBACL is shown in Fig. 10. The FSM is mainly used to decide whether to use coarse adjustment mode or fine adjustment mode. Figure 11 illustrates the circuit structure of the FSM. Initially, the whole system is reset to coarse adjustment mode. The comparator of the first MACU compares the voltage difference between

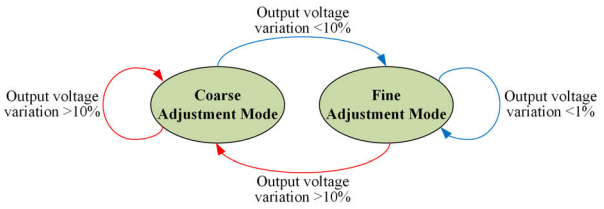

FIGURE 12. Circuit structure of finite state machine.

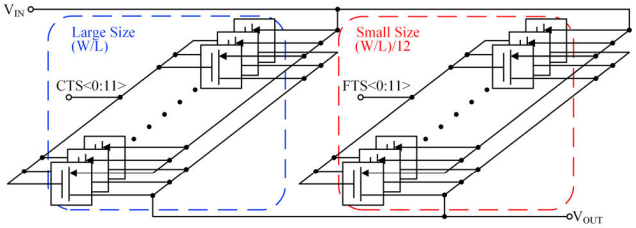

FIGURE 13. Circuit structure of power PMOS array.

TABLE 1. Truth table of MUX.

S_0	S_1	S_2	V_{OUT}
1	X	X	0
0	0	0	A
0	0	1	B
0	1	0	A
0	1	1	A

V_{REF} and V_{OUT}. If the V_{OUT} is lower than the V_{REF}, the $MACU_1$ generates signal 0 and stores it in the coarse data register DFF_C, and turns on the subsequent large-size PMOS to charge the V_{OUT}. In the meanwhile, forward signal (F_{req0}) is sent to coarse data registers $MACU_2$. The remaining tracking operations from F_{req1} to F_{reqN} can repeat F_{req0}. When the backward signal B_{req5} appears, the output Mode signal of the FSM changes from high to low. Then the SBCAL enters the fine adjustment mode. The SBACL restarts tracking from the first MACU, generates a digital control signal and stores it in the fine data register DFF_C, and turns on/off the subsequent small-size PMOS to charge/discharge V_{OUT}. When the entire tracking operation finally stabilizes to a set of F_{req1} and B_{req2}, and then the entire AD-LDO tracking is completed.

When the system enters the fine adjustment mode, the output voltage is monitored by a peak detector. As illustrated in Fig. 12, once the output voltage variation exceeds the 10% the peak detector will generate a reset signal to reset the entire system. The formula of output voltage variation is given as follow:

$$\text{Output voltage variation} = \frac{|V_{OUT} - V_{REF}|}{V_{REF}} \times 100\% \quad (5)$$

E. POWER PMOS ARRAY

As illustrated in Fig. 13, the power PMOS array includes large-size PMOS and small-size PMOS, which are used for large current and small current respectively. Moreover,

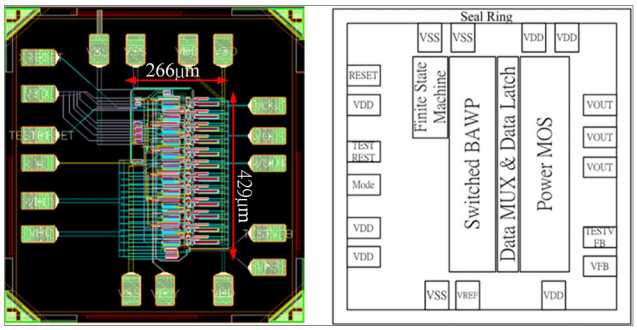

FIGURE 14. The chip layout of the proposed AD-LDO.

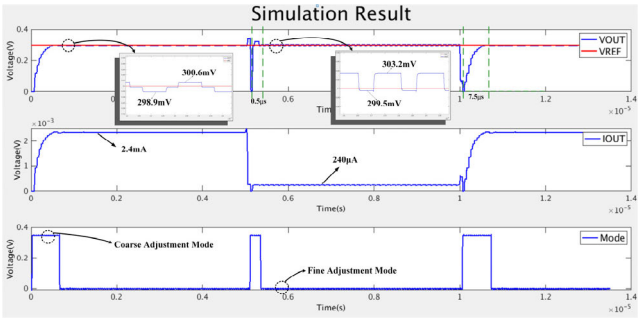

FIGURE 15. Circuit structure of power PMOS array.

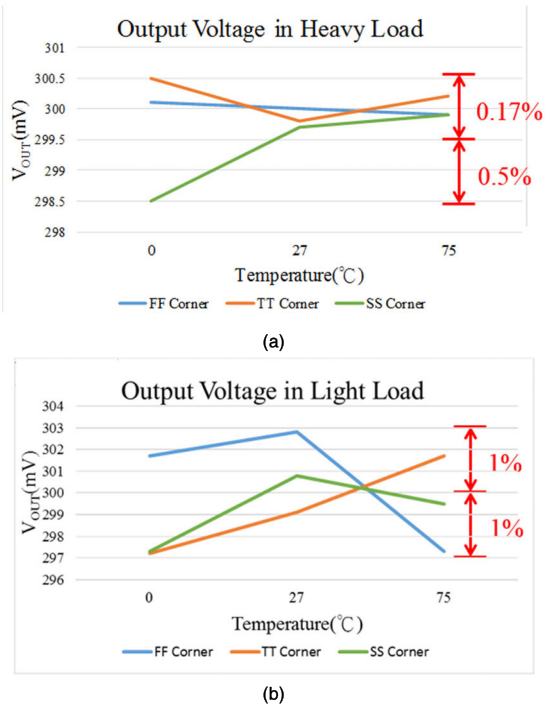

FIGURE 16. Circuit structure of power PMOS array.

large-size PMOSs are used for coarse adjustment, and small-size PMOSs are used for fine adjustment, both of which are 12 bits. As shown in Fig. 5, because the digital code for coarse and fine adjustment is generated with the same SBACL, power consumption and area can be saved. The power PMOS array is controlled by the thermal code which is stored in the data register. The size of power PMOS is directly related to the output load current and output regulated voltage. So the output current can be defined as

$$I_H = N \times I_C; \quad I_F \geq \frac{I_C}{N} \tag{6}$$

$$I_F \times R_{LOAD} \leq 0.01 \times V_{REF} \tag{7}$$

where I_H is the heavy load current, N is the number of PMOS bits, R_{LOAD} is the load resistance, I_C and I_F are the currents of the large size and small size PMOS, respectively. As in formula (6), N in the proposed AD-LDO is equal to 12, so the heavy load current I_H is 12 times that of the coarse adjustment current I_C. And the fine adjustment current I_F is one-twelfth of the coarse adjustment current. The large size of the PMOS can immediately provide a large current I_C to achieve fast tracking. The small size of the PMOS can supply small current I_F to reduce the output voltage ripple. As shown in formula 7, it is the limit to maintain the system operation in the fine adjustment mode.

III. SIMULATION RESULTS

The proposed AD-LDO was designed in TSMC standard 90 nm CMOS process technology. The chip layout of the proposed AD-LDO is shown in Fig. 14 and the active area is 0.114mm^2. The input voltage is 0.35 V, the output voltage is adjusted to 0.3 V, and the load current range is 0.2mA $\sim$ 2.4mA.

Figure 15 is the simulation waveforms from heavy load (2.4mA) to light load (0.24mA) and from light load (0.24mA) to heavy (2.4mA) load. Regardless of the conversion, the entire system will be reset first. Start tracking from the coarse adjustment mode until the output voltage change is less than 10%, and then enter the fine adjustment mode. As shown in Fig.15, the longest tracking time is 7.5μs from light load to heavy load. Finally, the output voltage V_{OUT} is regulated. Figure 16 shows the simulation results of output voltage changes under heavy load and light load in different corners of the environment. As shown in the simulation waveform, the maximum voltage variation is $\pm$1% at light load. The comparisons of the prior digital LDOs are shown in Table 2. This paper proposes the new asynchronous digital LDO with dual adjustment mode under 0.35V input voltage. It can provide a stable output voltage of 0.3 V and a heavy load current of 2.4 mA. The quiescent current is only 5μA and the current efficiency is 99.8%. Quiescent current includes leakage current and other wasted current of the whole circuit. Other indexes such as line regulation, load regulation and current efficiency are listed in Table 2 respectively. In digital LDO, we often use line regulation to express PSRR. The line regulation of the proposed AD-LDO is 4.5mV/V. The load regulation of the proposed AD-LDO is 0.3 mV/mA low than most papers. Moreover, the proposed AD-LDO has a very low ratio of voltage change divided by current change. The proposed dual adjustment mode technology has the characteristics of low output voltage ripple and fast tracking. Although the dual adjustment mode tracking architecture is used, only

TABLE 2. Comparison of prior digital LDOs.

	This work	CSSP'17[11]	CICC'15[17]	JSSC'17[23]	TCASII'16[25]	NEWCAS'16[27]	Access'20 [30]		PE'21 [31]	TCASII'21 [32]
Technology	90nm	90nm	65nm	65nm	65nm	130nm	28nm		65nm	110nm
Type of LDO	Async. Digital	Digital	Async. Digital	Async. Digital	Digital	Digital	Digital		Digital	Digital
Input Voltage(V)	0.35	0.35	0.6-1	0.6-1	0.9-1.8	0.6	0.5-1		0.6-1.2	0.6-1.2
Output Voltage(V)	0.3	0.3	0.55-0.95	0.55-0.95	0.8-1.5	0.4	0.45-0.95		0.55-1.15	0.5-1.1
Imax(mA)	2.4	2.4	500	500	100	25	0.5-2	2-10	25	40
Line Regulation(mV/V)	4.5	4.286	N/A	40	3	2.5	9.5		5	N/A
Load Regulation(mV/mA)	0.3	1.4	0.15-0.2	0.25	0.06	2.4	2.2		0.2	0.25
Quiescent Current(μA)	5	15.22(Tracking) 3.987(Regulating)	350	300	750	5.1@1MHz 49.8@100MHz	1		7.8-21.35	94
Output Capacitor(μF)	Not Required	Not Required	0.002	0.0015	0.001	N/A	100		0.84	2
Current Efficiency(%)	99.8	99.8	99.8	99.8	99.92	99.9	99.97		99.91	99.77
Active Area(mm*mm)	0.114	0.1982	0.291	0.158	0.01	N/A	0.016		0.041	0.07
ΔV_{OUT}(mV) / ΔI_{LOAD}(mA)	0.33	21.3	0.5	0.67	0.56	2	32	6.5	3.92	3.3

one SBACL circuit is used. Consequently, the area cost is saved. Therefore, the proposed AD-LDO is suitable for SoC applications of wearable electronic devices with an ultra-low supply voltage.

IV. CONCLUSION

This paper proposes a new design for an asynchronous digital controlled LDO with dual adjustment mode technique in ultra-low voltage. The coarse adjustment mode is fast tracking, and the fine adjustment mode is to reduce output voltage jitter. Base on simulation results of 90nm CMOS process technology, it can provide a stable output voltage of 0.3 V and a load current of 0.24 mA to 2.4 mA. For a supply voltage of 0.35 V, the quiescent current is only 5 μA, and the current efficiency is 99.8%. Therefore, the proposed AD-LDO is suitable for wearable electronic devices with an ultra-low supply voltage.

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