IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 20, 2021, accepted November 4, 2021, date of publication November 16, 2021,
date of current version November 24, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3128421

Voltage Balancing Strategy for V-Clamp Multilevel Converter Under High Modulation Index and High Power Factor Condition

YAO XUE, (Student Member, IEEE), CHENCHEN WANG, (Senior Member, IEEE), JIAWEI GUO, TRILLION Q. ZHENG, (Senior Member, IEEE), AND XIAOFENG YANG, (Senior Member, IEEE)
School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China

Corresponding author: Chenchen Wang (chchwang@bjtu.edu.cn)

This work was supported by the Key Program of National Natural Science Foundation of China under Grant 51737001.

ABSTRACT Featured with the simple structure, V-clamp multilevel converter (VMC) shows good prospect in the high-voltage and high-power applications. But VMC is endangered by the deviation of dc-link capacitors voltage, especially under the high modulation index (MI) and high power factor (PF) condition. Thus, a voltage balancing strategy for three-phase seven-level VMC is proposed in this paper. This strategy re-designs the carriers and reference to achieve capacitors voltage balancing with reduced switching actions. Besides, an active compensation control for capacitors voltage is presented to improve the dynamic performance. Compared with the conventional virtual space vector modulation, the proposed strategy significantly reduces the switching loss while provides a better output voltage under the high MI and high PF condition. The simulation model and experimental prototype of VMC with 7.2kW/220V are constructed to verify the validity of the proposed strategy.

INDEX TERMS V-clamp multilevel converter, carrier-based modulation, capacitor voltage balancing, reduce switching loss.

I. INTRODUCTION

Due to the small electromagnetic interference and lower switching stress, multilevel converters have been widely used in high-power applications [1], [2]. Conventional topologies for multilevel converters include neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). Among them, NPC and FC higher than three levels suffer from the mass clamping devices, hence they are hard to be applied to higher voltage (over 6kV) applications. Although the CHB offers a solution in this case, it is limited by the requirement of multiple isolated dc sources [3]–[5].

The V-clamp Multilevel Converter (VMC) is a suitable topology for the high-voltage applications [6]. Compared with the conventional topologies, VMC shows advantages as follows:

1) The clamping devices in VMC is reduced than that in NPC and FC counterparts.

2) VMC needs single dc source and contains no flying capacitors, which leads to simple structure and small volume.

3) The series-connected switches in VMC only sustain one level voltage during commutation process. Hence, the series-connected switches can be controlled as simple as one switch and the dynamic voltage unbalancing issue is avoided.

VMC attracts much attention in recent years [7]–[9]. The topology extension form of VMC is deduced in [7]. And a direct torque control for VMC is studied in [8]. In [9], a back-to-back VMC system is applied in 6.6kV motor drive application, which achieves transformer-less operation and good harmonic characteristics.

In spite of its merits, VMC with passive front-end has the same issue of dc-link capacitors voltage unbalancing as NPC. Since VMC higher than three levels contains multi intermediate nodes, the dc-link capacitors voltage are prone to deviate from the rated valve. Which results in the deterioration of the output performance and failure of system [10]. It has been revealed that the traditional algorithms based on nearest-three space vector modulation (SVM) failed to

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

maintain capacitors voltage balancing under the high modulation index (MI) and high power factor (PF) condition [11], [12]. However, converters are generally operated at high MI to improve the utilization of dc-link voltage. Moreover, the high PF operating capability is required in many applications, such as mining, traction and power transmission [13]. Therefore, the study on voltage balancing strategy for VMC under high MI and high PF condition is necessary.

Various investigations have been done to solve the above-mentioned issue [14]–[20]. Additional circuit is applied to keep capacitors voltage equal in [14], [15]. But this method results in extra investment and complex structure. In [16], a voltage balancing control based on divided SVM is proposed for five-level converter. The five-level vector space is divided into six two-level vector spaces, and redundant vectors are selected based on the capacitors voltage. However, transition levels are generally injected to avoid multilevel voltage jumping in each switching cycle, which results in extra switching actions [17]. The virtual SVM (VSVM) only uses the self-balancing virtual vectors, thus the natural capacitors voltage balancing within one switching cycle is achieved under ideal and steady states [18]. In the practical system, however, VSVM still need a closed-loop control to eliminate the effects of non-ideal factors (parameter differences, dead-zone effects, etc.) [19]. Besides, VSVM requires complex computation and unneglectable increase of switching loss in the converters with higher levels. In [20], the algorithm of VSVM is simplified, but the drawback of high switching loss still remains.

This paper proposed a voltage balancing strategy for the VMC under high MI and high FP condition. In the proposed strategy, carrier waves are re-designed firstly, in this way the dc-link capacitors voltage balancing for full operating range is achieved naturally. Furthermore, by injecting a proper zero-sequence component to reference waves, one phase is clamped to the highest or lowest level in certain sectors, then the switching loss is significantly reduced. Besides, considering the error caused by non-ideal factors, this paper also provides an active compensation control to improve the dynamic performance of the proposed strategy. Finally, the simulation and experimental results verify the validity of the proposed strategy.

II. CAPACITORS VOLTAGE BALANCING CRITERION OF VMC

A. CONFIGURATION OF 3P7L-VMC

As illustrated in Fig. 1, three-phase seven-level (3P7L) VMC shares six common dc-link capacitors. The negative dc bus is taken as the reference zero level, and the rated voltage of each capacitor E is taken as the one level voltage. Each phase leg consists of six clamping branches and one power arm, then the output terminal can be clamped to the seven levels (0, E, $2E$, $3E$, $4E$, $5E$ and $6E$) of dc-link. The dc bus current $\boldsymbol{I_{dc}} = [i_{dcP}, i_{dcN}]^{\mathrm{T}}$, capacitors current $\boldsymbol{I_C} = [i_{C1}, i_{C2}, i_{C3}, i_{C4}, i_{C5}, i_{C6}]^{\mathrm{T}}$, capacitors voltage $\boldsymbol{V_C} = [v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}, v_{C6}]^{\mathrm{T}}$,

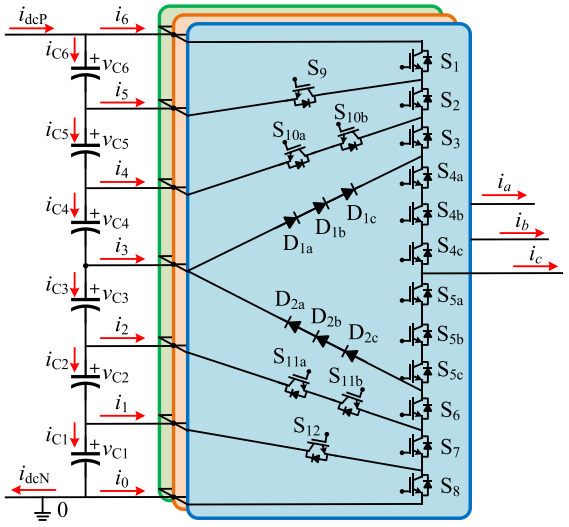

FIGURE 1. Configuration of three-phase seven-level VMC.

TABLE 1. Switching states of seven-level VMC.

States	$S_1/\overline{S_9}$	$S_2/\overline{S_{10}}$	$S_3/\overline{S_5}$	$S_6/\overline{S_4}$	$S_7/\overline{S_{11}}$	$S_8/\overline{S_{12}}$
$6E$	1	1	1	0	0	0
$5E$	0	1	1	0	0	0
$4E$	0	0	1	0	0	0
$3E$	0	0	0	0	0	0
$2E$	0	0	0	1	0	0
E	0	0	0	1	1	0
0	0	0	0	1	1	1

intermediate current $\boldsymbol{I_I} = [i_1, i_2, i_3, i_4, i_5]^{\mathrm{T}}$ and output current $\boldsymbol{I_O} = [i_a, i_b, i_c]^{\mathrm{T}}$ are also indicated in Fig. 1.

The switching states of 3P7L-VMC is shown in Table 1, where "0" and "1" represent the off-state and on-state respectively. Since the series-connected switches in VMC are controlled simultaneously, the switching states of S_{4a}, S_{4b} and S_{4c} are represented by S_4 here. So does the S_5, S_{10} and S_{11}. It can be seen that, there is no redundant current path contained capacitors in VMC, which means the current flows through the certain dc-link node when the output level is determined. This feature also exists in NPC. It indicates that the capacitors voltage unbalancing mechanism of VMC and NPC are the same.

B. CPACITORS VOLTAGE BALANCING CERTERION

The criterion for the capacitors voltage balancing in VMC is discussed in this section. For simplified analysis, the following assumptions are set: 1) the capacitance of each capacitor is C. 2) the initial voltage of each capacitor is E.

Generally, the voltage variation of capacitor Δv_C is affected by its current i_C. In order to ensure the voltage balancing, the integration value of i_C should be zero:

$$\Delta v_C = \frac{1}{C}\int i_C d\theta = 0 \tag{1}$$

where θ is the phase angle.

Consequently, the integration values of all capacitors currents $\boldsymbol{I_C}$ in the 3P7L-VMC need to be zero:

$$\int \boldsymbol{I}_{\mathrm{C}} d\theta = \boldsymbol{0} \tag{2}$$

According to kirchhoff's current law, i_{dcP}, i_{dcN}, i_0 and i_6 will not cause the unbalancing of capacitors voltage. Therefore, regardless of these current components, the relationship of $\boldsymbol{I_C}$ and $\boldsymbol{I_I}$ can be obtained as (3).

$$\boldsymbol{I}_{\mathrm{C}} = \boldsymbol{A}\boldsymbol{I}_{\mathrm{I}} \tag{3}$$

where

$$\boldsymbol{A} = \frac{1}{6}\begin{bmatrix} -5 & -4 & -3 & -2 & -1 \\ 1 & -4 & -3 & -2 & -1 \\ 1 & 2 & -3 & -2 & -1 \\ 1 & 2 & 3 & -2 & -1 \\ 1 & 2 & 3 & 4 & -1 \\ 1 & 2 & 3 & 4 & 5 \end{bmatrix}$$

Further deduction shows that the rank of matrix $\boldsymbol{A}$ equals to the unknown number, which is 5. Therefore, (3) has the unique solution. By substituting (2) to (3):

$$\int \boldsymbol{I}_{\mathrm{I}} d\theta = 0 \tag{4}$$

It can be seen that, the capacitors voltage balancing is guaranteed when (4) is satisfied. Since the average value of $\boldsymbol{I_I}$ in each switching cycle can be calculated directly by the duty ratio and output currents, equation (4) is taken as the criterion for capacitors voltage balancing in this paper.

III. PROPOSED VOLTAGE BALANCING STRAGEGY

A. MODIFIED CARRIER-BASED MODULATION

This paper presented a modified CBM (MCBM) for 7L-VMC. Fig. 2 shows its carriers in one carrier period T_{c}. The MCBM contains six carriers, which are v_{t1}, v_{t2}, v_{t3}, v_{t4}, v_{t5} and v_{t6}. Where, v_{t1} and v_{t6} are the cascaded triangular waves, they are represented as line segments in the interval [0, T_{c}/2]. On the other hand, v_{t2}, v_{t3}, v_{t4} and v_{t5} are represented as fold-line segments in the interval [0, T_{c}/2]. They have the same start-point (0, 1) and end-point (T_{c}/2, −1), while their mid-points are (T_{c}/10, 0), (T_{c}/5, 0), (3T_{c}/10, 0) and (2T_{c}/5, 0) respectively. Besides, carrier waves in interval [0, T_{c}/2] are symmetrical to the carrier waves in interval [T_{c}/2, T_{c}].

As shown in Fig. 2, the output level is decided by the comparison results between the carriers and reference voltage v_{ref}. When $-1 \le v_{\mathrm{ref}} < v_{\mathrm{t1}}$, the output level is 0. When $v_{tn} \le v_{\mathrm{ref}} < v_{\mathrm{t}(n+1)}$, the output level is nE, where $n = 1, 2, 3, 4, 5$. When $v_{\mathrm{t6}} \le v_{\mathrm{ref}} < 1$, the output level is $6E$.

In the digital control, the generation of v_{t1} and v_{t6} is the same as the conventional three-level PD-PWM. Besides, the general generation flow chart of v_{t2} to v_{t5} is illustrated in Fig. 3, where N_{clk} is the basic clock counter. N_{clk} increases 1 in each clock cycle (T_{clk}). N_{PRD} is the count value of half T_{c}, and $N_{\mathrm{PRD}} = T_{\mathrm{c}}/2T_{\mathrm{clk}}$. N_{tn} is the count value of v_{tn}, and $N_{tn} = N_{\mathrm{PRD}}(v_{tn} + 1)$. According to the judgement result of carrier location, the step value of N_{tn} per T_{clk} is selected and the value of v_{tn} can be obtained.

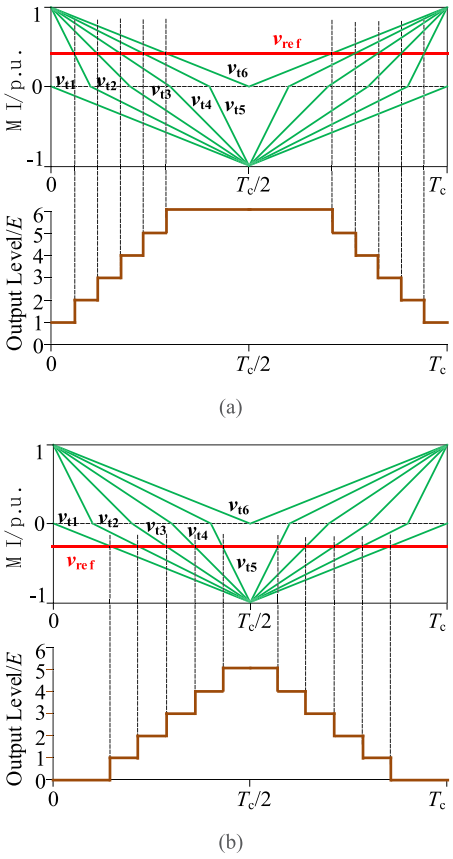

FIGURE 2. Modified carrier-based modulation for 7L-VMC. (a) $0 < v_{\mathrm{ref}} < 1$. (b) $-1 < v_{\mathrm{ref}} < 0$.

Based on the MCBM, the duty ratios of all intermediate levels in each carrier cycle are the same, which benefits the equal energy distribution among the dc-link capacitors. Another advantage of MCBM is the simplicity for digital implementation as (5).

$$\begin{cases} d_0 = \begin{cases} -v_{\mathrm{ref}}, & v_{\mathrm{ref}} \le 0 \\ 0, & v_{\mathrm{ref}} > 0 \end{cases} \\ d_{\mathrm{I}} = d_1 = d_2 = d_3 = d_4 = d_5 = \dfrac{1 - |v_{\mathrm{ref}}|}{5} \\ d_6 = \begin{cases} 0, & v_{\mathrm{ref}} \le 0 \\ v_{\mathrm{ref}}, & v_{\mathrm{ref}} > 0 \end{cases} \end{cases} \tag{5}$$

where, d_j represents the duty ratio of jE level, $j = 0, 1, 2, 3, 4, 5, 6$. Since the value of d_1, d_2, d_3, d_4 and d_5 are equal, they are represented as d_{I} here.

B. DISCONTINUOUS REFERENCE WAVES

As seen in Fig. 2, when the conventional sine references are applied, the MCBM needs 10 switching actions per phase in one T_{c}. In this case, MCBM only reduces 2 switching actions than VSVM in 3P7L-VMC. The number of switching actions is still high, which leads to the high system switching loss and limitation for practical applications.

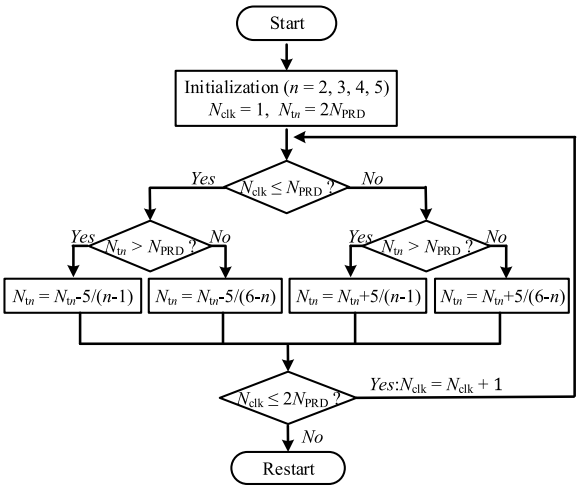

FIGURE 3. Generation flow chart of v_{t2} to v_{t5}.

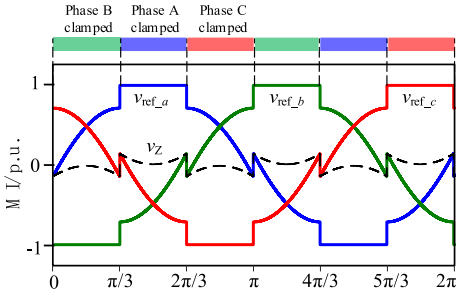

FIGURE 4. Discontinuous reference waves for 3P7L-VMC.

The MCBM releases the control freedom of zero-sequence voltage, which is different from VSVM. Therefore, this paper adopts the discontinuous references to reduce the switching loss.

As shown in Fig. 4. The final three-phase references v_{ref_a}, v_{ref_b} and v_{ref_c} are obtained by injecting the zero-sequence component v_Z to the original sine references v_{ref_a0}, v_{ref_b0} and v_{ref_c0}. In this way, one reference is clamped to -1 or 1 during each $\pi/3$, and the number of switching actions in clamped phase keeps 0.

Equations (6)-(8) give the expressions of v_{ref_a}, v_{ref_b} and v_{ref_c}

$$\begin{cases} v_{ref\_a} = v_{ref\_a0} + v_Z \\ v_{ref\_b} = v_{ref\_b0} + v_Z \\ v_{ref\_c} = v_{ref\_c0} + v_Z \end{cases} \tag{6}$$

$$\begin{cases} v_{ref\_a0} = M \sin\theta \\ v_{ref\_b0} = M \sin(\theta - 2\pi/3) \\ v_{ref\_c0} = M \sin(\theta + 2\pi/3) \end{cases} \tag{7}$$

where M is the modulation index.

v_Z is calculated as

$$v_Z = \begin{cases} 1 - v_{max}, & |v_{max}| \ge |v_{min}| \\ -1 - v_{min}, & |v_{max}| < |v_{min}| \end{cases} \tag{8}$$

where $v_{max} = \max(v_{ref\_a0}, v_{ref\_b0}, v_{ref\_c0})$, $v_{min} = \min(v_{ref\_a0}, v_{ref\_b0}, v_{ref\_c0})$.

C. VOLTAGE BALANCING MECHANISM

With the above-mentioned MCBM and discontinuous reference waves, the capacitors voltage balancing can be achieved naturally in the ideal and steady system. The balancing mechanism is analyzed in the following text.

Firstly, set the three-phase output current as

$$\begin{cases} i_a = I_m \sin(\theta - \varphi) \\ i_b = I_m \sin(\theta - \varphi - 2\pi/3) \\ i_c = I_m \sin(\theta - \varphi + 2\pi/3) \end{cases} \tag{9}$$

where I_m is the amplitude of output currents, φ is the power factor angle.

Assuming the output current is unchanged during one T_c. According to the area equivalence principle and (5), the equivalent value of each intermediate current i_I is the same, which can be expressed as:

$$i_I = d_{I\_a} i_a + d_{I\_b} i_b + d_{I\_c} i_c \tag{10}$$

where d_{I_x} represents the duty ratio of intermediate level of phase x, $x = a, b, c$.

In combination with (5)-(10), the integration value of i_I in each phase within one fundamental period T_f can be obtained. Taking phase a as example:

$$\begin{aligned} &\int_0^{2\pi} i_{I\_a} d\theta \\ &= \int_0^{2\pi} d_{I\_a} i_a d\theta \\ &= \frac{I_m}{5} \int_0^{2\pi} [\sin(\theta - \varphi) - |M \sin\theta + v_Z(\theta)| \sin(\theta - \varphi)] d\theta \\ &= \frac{I_m}{5} \int_0^{\pi} \begin{bmatrix} |M \sin\theta + v_Z(\theta)| \sin(\theta - \varphi) \\ - |v_Z(\theta + \pi) - M \sin\theta| \sin(\theta - \varphi) \end{bmatrix} d\theta \end{aligned} \tag{11}$$

From (8), it is obvious that v_Z meets the relationship of

$$v_Z(\theta) = -v_Z(\theta + \pi) \tag{12}$$

Hence, the solution of (11) is obtained as

$$\int_0^{2\pi} i_{I\_a} d\theta = 0 \tag{13}$$

Similarly, the same solutions can be obtained in other phases. The total average i_I is zero within one fundamental period. From (4), it can be known that the criterion of capacitors voltage balancing is satisfied with the proposed strategy, and it is irrelevant to the MI and PF. When the balanced load are connected, based on the symmetry, the 3P7L-VMC system can achieve capacitors voltage balancing within one-third fundamental period for full operation range.

It is noteworthy that, as long as v_Z meets the limitation of (12), the result of (13) can be obtained and the natural capacitors voltage balancing of system is achieved.

Hence the applied reference waves are not directly associated with the MCBM. Other reference waves that meet the limitation of (12) are also available for system to achieve different control objections. In this paper, the v_Z shown in (8) is selected to reduce the switching loss under the high PF condition.

IV. ACTIVE COMPENSATION CONTROL

In the practical system, the natural voltage balancing may be deteriorated by the non-ideal factors, such as the capacitance differences between dc-link capacitors, insertion of dead-zone, and the switching delay and voltage drop [21]. Therefore, an active compensation control (ACC) for capacitors voltage balancing is provided here to improve the system dynamic characteristics.

Noted that, since the zero-sequence voltage has been determined in (8), the ACC needs to regular capacitors voltage without changing the phase output voltage.

Fig. 5 shows an example of the ACC. When $v_{C4} < v_{C5}$, i_{C4} should be increased and i_{C5} should be decreased to eliminate the voltage difference. If the output current i_o is positive, the duty ratio adjustment of each output level is shown in (14), where, $d = K(v_{C5} - v_{C4})$, K is the adjust coefficient.

$$\begin{cases} \Delta d_0 = \Delta d_1 = \Delta d_2 = \Delta d_6 = 0 \\ \Delta d_3 = \Delta d_5 = d_\Delta \\ \Delta d_4 = -2d_\Delta \end{cases} \tag{14}$$

Consequently, the adjustment of each capacitors current can be obtained from (3) and (14).

$$\begin{cases} \Delta i_{C1} = \Delta i_{C2} = \Delta i_{C3} = \Delta i_{C6} = 0 \\ \Delta i_{C4} = d_\Delta i_o \\ \Delta i_{C5} = -d_\Delta i_o \end{cases} \tag{15}$$

It can be seen that, the voltage difference between C_4 and C_5 is reduced with the ACC, while other capacitors voltage are not affected. Moreover, the removed area is equal to the added area in Fig. 5. Hence, the equivalent output voltage keeps unchanged with ACC.

Considering the voltage deviations of all capacitors, the general duty ratio adjustments can be obtained directly by (16). Meanwhile, the reference variation Δv_{ref} keeps zero, as shown in (17).

$$\begin{cases} \Delta d_0 = 0 \\ \Delta d_1 = dir(i_o)K(-v_{C2} + v_{C3}) \\ \Delta d_2 = dir(i_o)K(2v_{C2} - 3v_{C3} + v_{C4}) \\ \Delta d_3 = dir(i_o)K(-v_{C2} + 3v_{C3} - 3v_{C4} + v_{C5}), \quad v_{ref}>0 \\ \Delta d_4 = dir(i_o)K(-v_{C3} + 3v_{C4} - 3v_{C5} + v_{C6}) \\ \Delta d_5 = dir(i_o)K(-v_{C4} + 3v_{C5} - 2v_{C6}) \\ \Delta d_6 = dir(i_o)K(-v_{C5} + v_{C6}) \end{cases}$$

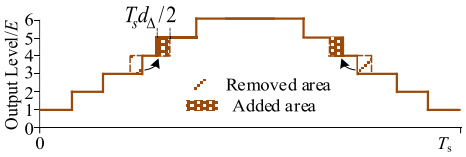

FIGURE 5. Example of active compensation control.

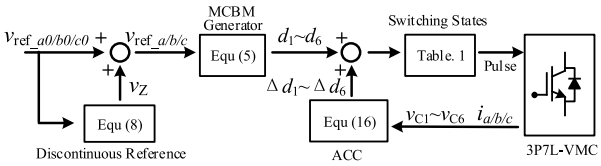

FIGURE 6. Control diagram of the proposed strategy.

$$\begin{cases} \Delta d_0 = dir(i_o)K(-v_{C1} + v_{C2}) \\ \Delta d_1 = dir(i_o)K(2v_{C1} - 3v_{C2} + v_{C3}) \\ \Delta d_2 = dir(i_o)K(-v_{C1} + 3v_{C2} - 3v_{C3} + v_{C4}) \\ \Delta d_3 = dir(i_o)K(-v_{C2} + 3v_{C3} - 3v_{C4} + v_{C5}), \quad v_{ref}\leq 0 \\ \Delta d_4 = dir(i_o)K(-v_{C3} + 3v_{C4} - 3v_{C5} + v_{C6}) \\ \Delta d_5 = dir(i_o)K(-v_{C4} + v_{C5}) \\ \Delta d_6 = 0 \end{cases} \tag{16}$$

where, $dir(i_o)$ represents the direction of i_o, $dir(i_o) = 1$ when $i_o > 0$; $dir(i_o) = 0$ when $i_o = 0$; and $dir(i_o) = -1$ when $i_o < 0$.

$$\Delta v_{ref} = \frac{1}{3}\sum_{i=0}^{6} i\Delta d_i = 0 \tag{17}$$

Noted that, the ACC ignores the voltage difference between C_1 and C_2 when $v_{ref} > 0$. In this way, the 0 level is excluded in this stage, which avoids the extra switching action. Similarly, the voltage difference between C_5 and C_6 is also ignored when $v_{ref} \leq 0$, and the $6E$ level is excluded. Besides, the duty ratio adjustment of each output level must be less than its original value. For the three-phase VMC system, the duty ratio adjustments of each phase can be calculated respectively.

Finally, the control diagram of the proposed strategy is illustrated in Fig. 6. The switching pulses can be easily obtained by three equations and switching states table.

V. CHARACTERISTICS ANALYSIS

This section analyses the characteristics of the proposed strategy, including the capacitors voltage ripple, switching loss and total harmonic distortion (THD) of line-to-line voltage. The analysis results are compared with VSVM [18].

A. CAPACITORS VOLTAGE RIPPLE

VSVM realizes the capacitors voltage balancing within one T_c, which means its average value of voltage ripple in T_c is zero. Generally, the capacitors voltage ripple in VSVM is

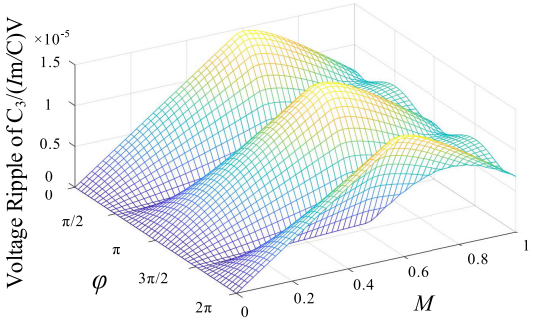

FIGURE 7. Voltage ripple of C_3 with proposed strategy.

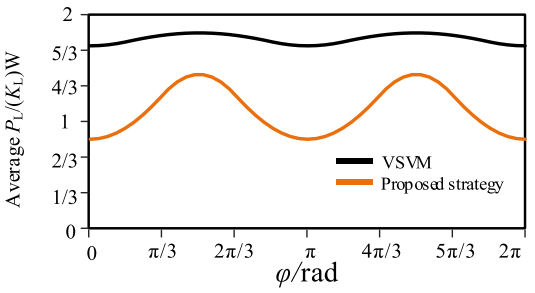

FIGURE 8. Average switching loss of VSVM and proposed strategy.

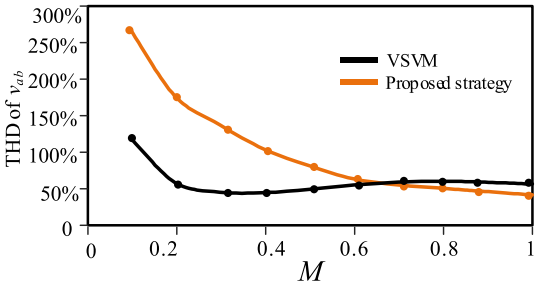

FIGURE 9. Average switching loss of VSVM and proposed strategy.

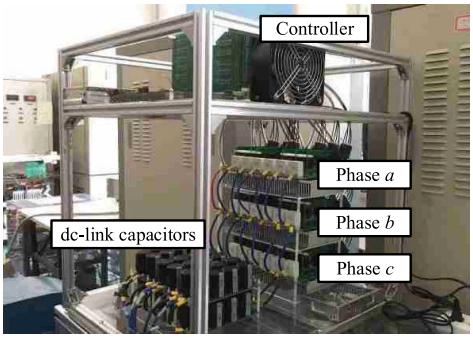

FIGURE 10. Experimental platform of 3P7L-VMC.

smaller. For the proposed strategy, the voltage balancing is achieved within one-third T_f. The voltage ripple is effected by the C, I_m, MI and PF. Its amplitude of voltage ripple is calculated here.

According to (3) and (5), the capacitors current meets (18). Hence the voltage ripple amplitudes of C_1-C_6 meet the relationship of 5:3:1:1:3:5. Subsequently, by combining (1), (5)-(10), (18), the voltage ripple amplitude of C_3 is obtained as shown in Fig. 7.

$$i_I = -\frac{2i_{C1}}{5} = -\frac{2i_{C2}}{3} = -2i_{C3} = 2i_{C4} = \frac{2i_{C5}}{3} = \frac{2i_{C6}}{5} \tag{18}$$

It can be seen that in Fig. 7, the capacitors voltage ripple increases along with the PF when MI is low; however, the trend is opposite when MI is high. With the MI increasing from 0 to 1, the voltage ripple firstly increases and then decreases. Overall, the proposed strategy has a good performance of voltage ripple under the high MI and high PF condition.

B. SWITCHING LOSS

The switching loss of single switch P_L in one T_f is expressed as (19) [22].

$$P_L = \frac{1}{2\pi}\frac{E(t_{on}+t_{off})}{2T_f}\int_0^{2\pi} i_s(\theta)d\theta = K_L\int_0^{2\pi} i_s(\theta)d\theta \tag{19}$$

where, t_{on} and t_{off} are the switching turn-on time and turn-off time respectively. And i_s represents the switching current. $i_s = |i_o|$ when the switch acts. Otherwise, $i_s = 0$.

It should be noted that, in the different intervals of one T_f, the phase switching actions n_s per carrier cycle are different. Take phase a as example. For the VSVM, $n_s = 12$ in the intervals $[0, \pi/6)$, $[5\pi/6, 7\pi/6)$ and $[11\pi/6, 2\pi]$; $n_s = 10$ in the intervals $[\pi/6, 5\pi/6)$ and $[7\pi/6, 11\pi/6)$. For the proposed strategy, $n_s = 10$ in the intervals $[0, \pi/3)$, $[2\pi/3, 4\pi/3)$ and $[5\pi/3, 2\pi]$; $n_s = 0$ in the intervals $[\pi/3, 2\pi/3)$ and $[4\pi/3, 5\pi/6)$. Taking account of the difference of n_s, the average switching loss of VSVM and the proposed strategy can be obtained as Fig. 8.

In Fig. 8, the proposed strategy has less switching loss compared with the VSVM with full range. The reduction is obvious especially under the high PF condition. When the PF is 1, a 51.2% reduction of switching loss is achieved.

C. THD OF LINE-TO-LINE VOLTAGE

The THD of line-to-line voltage v_{ab} in VSVM and the proposed strategy under different MI is illustrated in Fig. 9. The comparison is based on the ideal simulation environment.

Fig. 9 shows that the proposed strategy has higher THD of v_{ab} at low MI. However, when MI is higher than 0.65, the output voltage THD in the proposed strategy is smaller than the VSVM.

It can be concluded from the above-mentioned analysis, with a certain increase of capacitors voltage ripple, the pro-

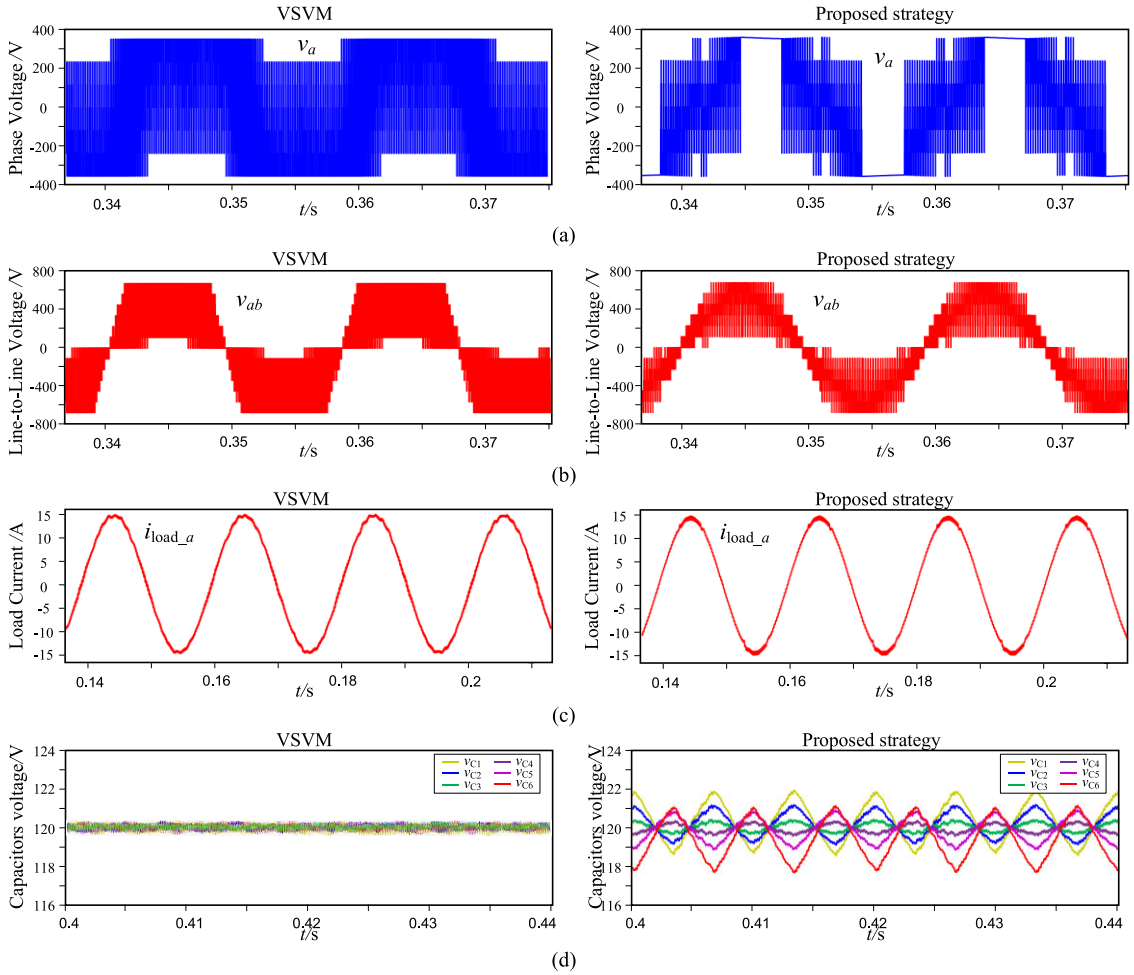

FIGURE 11. Simulation results of conventional VSVM and the proposed strategy. (a) Phase a voltage v_a. (b) Line-to-line voltage v_{ab}. (c) Load a current i_{load_a}. (d) Capacitors voltage v_{C1}-v_{C6}.

posed strategy achieves significantly reduction of switching loss and lower THD of line-to-line voltage than VSVM under the high MI and high PF condition.

VI. SIMULATION AND EXPERIMENT

In order to verify the feasibility of the proposed voltage balancing strategy, the simulation model and experimental platforms of 3P7L-VMC are constructed in this paper. Fig. 10 shows the experimental platform. The main parameters are listed in the Table 2.

TABLE 2. Parameters for simulation and experimental platform.

Parameters	Symbol	Value
Rated system capacity	S	7.2kVA
Rated dc-link voltage	V_{dc}	720V
dc-link capacitance	C	3.76mF
Carrier frequency	f_c	5kHz
Amplitude of output current	I_m	14.5A
Filter inductance	L_f	2mH
Filter capacitance	C_f	10μF

A. SIMULATION RESULTS

Fig. 11 shows the simulation results of VSVM and the proposed strategy under the high MI and high PF condition (MI = 0.87 and PF = 1). It is known from Fig. 11(a) that, the phase a voltage v_a of VSVM contains six levels (for two-third of T_f) or seven levels (for one-third of T_f) per switching cycle. However, v_a of the proposed strategy contains six levels (for two-third of T_f) or be clamped without switching actions (for one-third of T_f). In this way, the switching loss are significantly reduced in the proposed strategy. The line-to-line voltage v_{ab} is shown in Fig. 11(b). Noted that, the THD of v_{ab} in the proposed strategy (46.4%) is less than that in the VSVM (58.5%). Consequently, a good performance of load a current i_{load_a} is achieved in the proposed strategy, as shown in Fig. 11(c). From Fig. 11(d), the VSVM achieves voltage balancing within one carrier cycle, its capacitors voltage ripple are negative related to the carrier frequency. In this simulation case, its capacitors voltage ripple is about 0.12V. It also can be seen in Fig. 11(d), capacitors voltage balancing of the proposed strategy is attained within

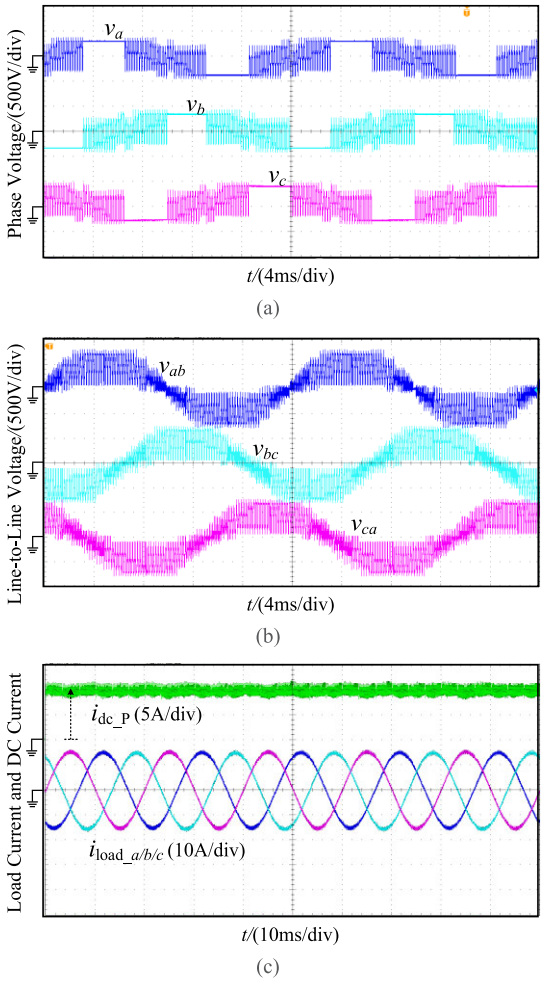

FIGURE 12. Experimental results of the proposed strategy. (a) Phase voltage. (b) Line-to-line voltage. (c) Load current and dc-link current.

TABLE 3. Performance comparison for VSVM.

Performance	High MI High PF	High MI Low PF	Low MI High PF	Low MI Low PF
C_3 voltage ripple/V	0.12	0.14	0.11	0.12
THD of v_{ab}	59.2%	58.6%	48.2%	48.3%
Switching loss/W	20.3	19.7	20.1	19.9

one-third T_f. The ripple of v_{C1} and v_{C6}, v_{C2} and v_{C5}, v_{C3} and v_{C4} are opposite. Their amplitudes are 1.5V, 0.9V and 0.3V, respectively.

Except the simulation results of high MI and high PF (MI = 0.87 and PF = 1) condition shown in Fig. 11, other three operation conditions are also discussed, including the high MI and low PF (MI = 0.87 and PF = 0.1), low MI and high PF (MI = 0.5 and PF = 1), and low MI and low PF (MI = 0.5 and PF = 0.1) conditions. The performance comparison for VSVM and the proposed strategy is summarized in Table 3 and Table 4. From these results, some observations can be obtained as following.

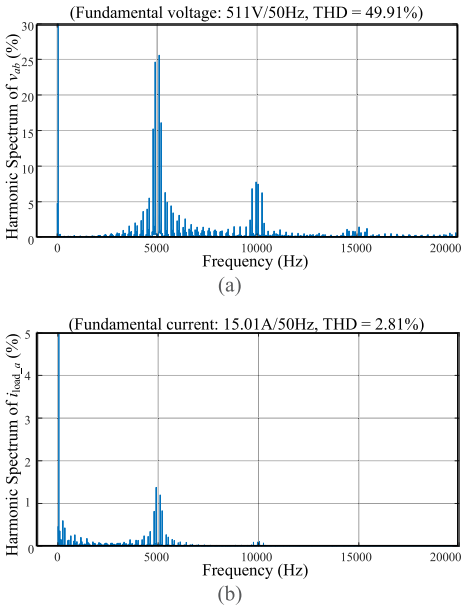

FIGURE 13. Harmonic spectrums of the proposed strategy. (a) Line-to-line voltage. (b) Load current.

TABLE 4. Performance comparison for proposed strategy.

Performance	High MI High PF	High MI Low PF	Low MI High PF	Low MI Low PF
C_3 voltage ripple/V	0.3	0.32	0.48	0.19
THD of v_{ab}	46.4%	46.5%	82.6%	80.9%
Switching loss/W	10.2	15.6	10.2	15.8

1) Both VSVM and the proposed strategy can achieve the dc-link capacitors voltage balancing under full operation conditions.
2) Lower voltage ripple is the main advantage of VSVM. Its amplitude of voltage ripple have little difference under different operation conditions.
3) For the proposed strategy, its output voltage THD decreases when MI increases. Under the high MI region, the output voltage THD of proposed strategy is lower than VSVM.
4) The proposed strategy has less switching loss than VSVM under full operation conditions. This loss reduction ratio reaches about 50% under the unity PF condition.

Consequently, for the proposed strategy, the benefits of reduction of switching loss and lower output THD are obvious under the high MI and high PF condition.

B. EXPERIMENTAL RESULTS

The steady experimental results of the proposed strategy under high MI and high PF condition are shown in Figs. 12-15.

Fig. 12 shows the overall output waveforms of 3P7L-VMC, it verifies the validity of proposed strategy. In Fig. 12(a), v_a is

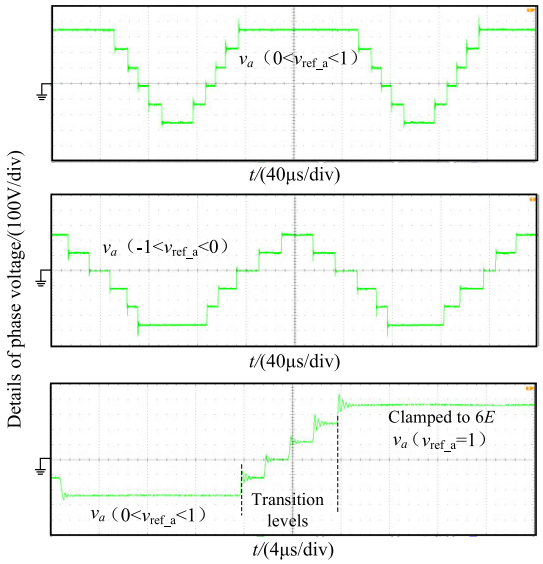

FIGURE 14. Details of phase voltage v_a.

clamped to 360V or −360V for one-third T_f, other two phases voltage are the same but phase-shifted ±120°. As shown in Fig. 12(b), v_{ab} is synthesized by thirteen levels, each level voltage is 120V. The line-to-line voltage is sine wave with high frequency harmonics. The load current and dc current are illustrated in Fig. 12(c). As seen, good performance of load current is achieved in this system. The average value of i_{dcP} is about 10A. And carrier frequency fluctuation can be observed in the i_{dcP}.

Fig. 13 shows the harmonic spectrums of line-to-line voltage and load current. The THD of v_{ab} is 49.91%. As seen, its most harmonics are around the carrier frequency f_c and twice f_c. Hence the resonant frequency of LC filter is set as $f_c/5$ to achieve a good attenuation effect. The three-phase load current are shown in Fig. 13(b), and its THD is about 2.81%.

Fig. 14 shows the details of v_a. When $0 < v_{ref\_a} < 1$, v_a contains E-$6E$ levels; and when When $-1 < v_{ref\_a} < 0$, v_a contains 0-$5E$ levels. Noted that, before v_a is clamped to $6E$ ($v_{ref\_a} = 1$) in the next T_c, the transition levels of $2E$-$5E$ are injected to avoid multilevel jumping. Each transition level remains $2\mu s$ for the complete action of switches. Similarly, the transition levels are also required before v_a is out of clamping states of $6E$. Since the transition levels are only injected twice in one fundamental cycle, the switching loss and THD will not be affected obviously.

Fig. 15 shows the capacitors voltage. The waveforms of condition without initial voltage offset is illustrated in Fig. 15(a). The balancing of all dc-link capacitors voltage is achieved within one-third T_f. Where C_1 and C_6 have the larger voltage ripples than other capacitors, their amplitude is about 1.7V (1.46% of rated voltage). The system can operate well at steady condition. In Fig. 15(b), set the initial value of v_{C1}-v_{C6} as $0.9E$, $0.85E$, $1.3E$, $1.2E$, $0.85E$ and $0.9E$, respectively. After the ACC is trigged, the voltage balancing

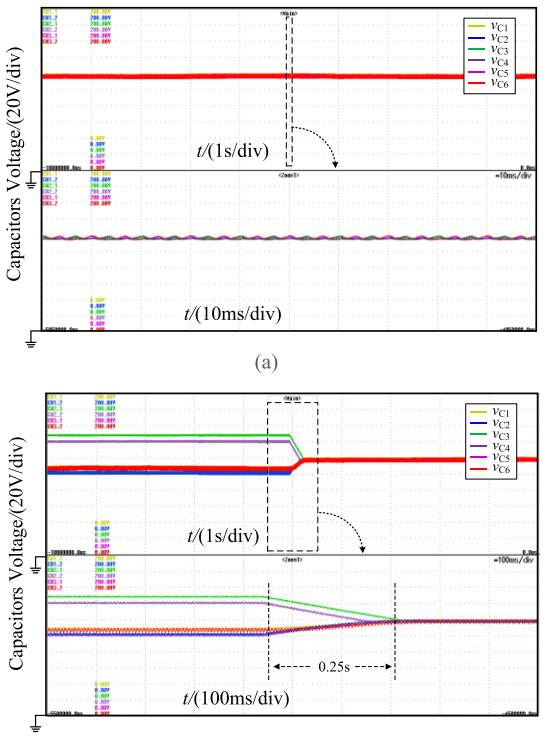

FIGURE 15. Experimental results of capacitors voltage. (a) Without initial voltage offset. (b) With initial voltage offset.

TABLE 5. Power analysis of experimental results (MI = 0.87, PF = 1).

Balancing strategy	Power loss/W	Efficiency
VSVM	261	96.39%
The proposed	248	96.58%

is achieved again in 250ms. This verifies the effectiveness of the ACC.

To verify the analysis of switching loss for the VSVM and the proposed strategy, the experimental results of power loss and efficiency are obtained by the power analyser (HIOKI 3390), as summarized in Table. 5. It can be seen that, the system efficiencies of VSVM and the presented strategy are 96.39% and 96.58% respectively. The power loss of VSVM is 261W, which is 13W higher than the presented strategy. This power loss difference is basically coincided with the aforementioned analysis.

The dynamic experimental results, including the start-up and the input voltage variation experiments, are shown in Fig. 16 and Fig. 17 respectively. As seen in Fig. 16(a), during the start-up phase, the modulation index increases from 0 to 0.87 in 200ms. The waveforms of v_a and v_{ab} change according to M. Correspondingly, the amplitude of i_{load_a} increases to its rated value gradually. The waveforms of capacitors voltage are shown in Fig. 16(b), before the system starts up, the parameter differences lead to certain offset of capacitors voltage. This voltage offset is eliminated quickly when the system starts up and the ACC is trigged.

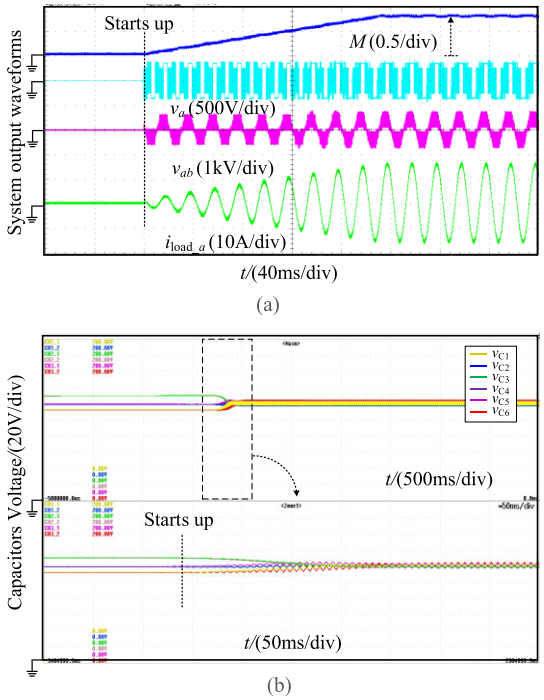

FIGURE 16. Experimental results of start-up. (a) System output waveforms. (b) Capacitors voltage.

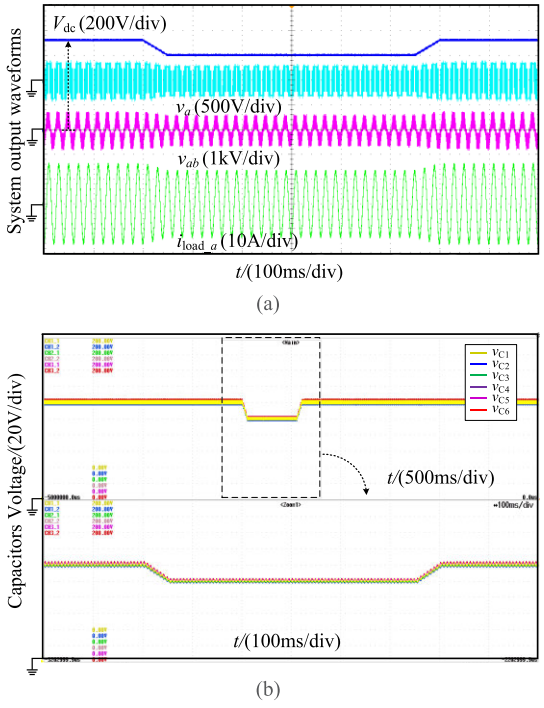

FIGURE 17. Experimental results of input voltage variation. (a) System output waveforms. (b) Capacitors voltage.

In Fig. 17, the modulation index keeps 0.87, while the input voltage V_{dc} drops from 720V to 600V firstly and then recovers after 0.5s. It can be seen that, the system output voltage and current change smoothly during the V_{dc} variation process. And the dc-link capacitors voltage keeps balanced under both the steady and dynamic conditions.

VII. CONCLUSION

A voltage balancing strategy for V-clamped multilevel converter is proposed in this paper. The carrier waveforms are modified firstly to achieve the natural voltage balancing. The discontinuous reference waves are also adopted to clamp one phase in each carrier cycle, which reduces the switching loss. Furthermore, an active compensation control for voltage balancing is presented. By adjusting the duty ratio of output levels, the capacitors voltage is compensated without changing the output voltage.

Simulation and experimental results show following features of the proposed strategy: 1) carrier-based modulation leads to the simple calculation. 2) Capacitors voltage balancing with full operation range is obtained. 3) Compared with the virtual space vector modulation, the proposed strategy achieves reduction of switching loss and lower THD of output voltage under the high modulation ratio and high power factor condition. Its disadvantage is the larger capacitors voltage ripple. 4) The active compensation control enhances the system dynamic performance.

Consequently, the proposed strategy provides an effective solution for V-clamp multilevel converter under the high modulation ratio and high power factor condition.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] C. Wang, Z. Li, and H. Xin, "Neutral-point voltage balancing strategy for three-level converter based on disassembly of zero level," *J. Power Electron.*, vol. 19, no. 1, pp. 79–98, Jan. 2019.

[3] J. Jamaludin, N. A. Rahim, and H. W. Ping, "Multilevel voltage source inverter with optimised usage of bidirectional switches," *IET Power Electron.*, vol. 8, no. 3, pp. 378–390, Mar. 2015.

[4] B. Jin and X. Yuan, "Topology, efficiency analysis, and control of a four-level -type converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1044–1059, Jun. 2019.

[5] A. Khodaparast, J. Adabi, and M. Rezanejad, "A step-up switched-capacitor multilevel inverter based on 5-level T-type modules," *IET Power Electron.*, vol. 12, no. 3, pp. 483–491, Mar. 2019.

[6] Y. Xue, X. Yang, L. Yuan, and T. Q. Zheng, "Operation and control of a seven-level V-clamp multilevel converter," *Energies*, vol. 12, no. 24, p. 4761, Dec. 2019.

[7] A. Chen, C. Zhang, H. Ma, and Y. Deng, "A novel multilevel inverter topology with no clamping diodes and flying capacitors," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Ramanathapuram, India, Nov. 2008, pp. 3184–3187.

[8] O. C. Sekhar and K. C. Sekhar, "A novel five-level inverter topology for DTC induction motor drive," in *Proc. IEEE Int. Conf. Adv. Commun. Control Comput. Technol. (ICACCCT)*, Ramanathapuram, India, Aug. 2012, pp. 392–396.

[9] M. Mazuela, I. Baraia, A. Sanchez-Ruiz, I. Echeverria, I. Torre, and I. Atutxa, "DC-link voltage balancing strategy based on SVM and reactive power exchange for a 5l-MPC back-to-back converter for medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7864–7875, Dec. 2016.

[10] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[11] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5579–5591, Oct. 2014.

[12] P. H. Raj, A. I. Maswood, G. H. P. Ooi, and Z. Lim, "Voltage balancing technique in a space vector modulated 5-level multiple-pole multilevel diode clamped inverter," *IET Power Electron.*, vol. 8, no. 7, pp. 1263–1272, Jul. 2015.
[13] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
[14] X. Zeng, H. Wang, X. Zhang, D. Gong, and X. Yang, "Transformer-less five-level high-voltage full-scale converter with a self-balance auxiliary circuit for 10 MW wind turbines," *IET Power Electron.*, vol. 10, no. 14, pp. 1841–1851, Nov. 2017.
[15] L. Wang, H. Wang, M. Su, Y. Sun, J. Yang, M. Dong, X. Li, W. Gui, and J. Feng, "A three-level T-type indirect matrix converter based on the third-harmonic injection technique," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 841–853, Jun. 2017.
[16] H. A. Hotait, A. M. Massoud, S. J. Finney, and B. W. Williams, "Capacitor voltage balancing using redundant states of space vector modulation for five-level diode clamped inverters," *IET Power Electron.*, vol. 3, no. 2, pp. 292–313, Mar. 2010.
[17] W. Sheng and Q. Ge, "A novel seven-level ANPC converter topology and its commutating strategies," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7496–7509, Sep. 2018.
[18] S. Busquets-Monge, J. Bordonau, and J. Rocabert, "A virtual-vector pulsewidth modulation for theFour-level diode-clamped DC–AC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1964–1972, Jul. 2008.
[19] Q. Yuan, A. Li, J. Qian, and K. Xia, "DC-link capacitor voltage control for the NPC three-level inverter with a newly MPC-based virtual vector modulation," *IET Power Electron.*, vol. 13, no. 5, pp. 1093–1102, Apr. 2020.
[20] M. S. Busquets, R. Maheshwari, and N. S. Munk, "Overmodulation of n-level three-leg DC-AC diode-clamped converters with comprehensive capacitor voltage balance," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1872–1883, May 2013.
[21] R. J. Kerkman, D. Leggate, D. W. Schlegel, and C. Winterhalter, "Effects of parasitics on the control of voltage source inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 140–150, Jan. 2003.
[22] N.-V. Nguyen, B.-X. Nguyen, and H.-H. Lee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3958–3966, Sep. 2011.

YAO XUE (Student Member, IEEE) was born in Yuncheng, Shanxi, China, in 1991. He received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2014, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include multilevel converters and VSC-HVDC.

CHENCHEN WANG (Senior Member, IEEE) was born in Anhui, China, in 1981. He received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2003 and 2008, respectively. He is currently working as a Professor with the School of Electrical Engineering, Beijing Jiaotong University, Beijing. His current research interests include electric drive and multilevel converters.

JIAWEI GUO was born in Wuqiao, Hebei, China, in 1998. He received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2020, where he is currently pursuing the M.S. degree in electrical engineering. His current research interests include multilevel converters and railway electrification systems.

TRILLION Q. ZHENG (Senior Member, IEEE) was born in Jiangshan, Zhejiang, China, in 1964. He received the B.S. degree in electrical engineering from Southwest Jiaotong University, Sichuan, China, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 1992 and 2002, respectively.

He is currently a University Distinguished Professor with Beijing Jiaotong University. He is also the Director of the Center for Electric Traction, founded by Ministry of Education, China. His current research interests include the power supplies and AC drives of railway traction systems, high performance and low loss power electronics systems, PV-based converters and control, active power filters, and power quality correction.

Dr. Zheng was a recipient of the Youth Award of Railway Science and Technology of Zhan Tianyou, in 2005, and Zhongda Scholar for power electronics and motor drive area, by Delta Environmental and Educational Foundation, in 2007.

XIAOFENG YANG (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2003 and 2011, respectively.

From 2003 to 2005, he was a Power Supplier Engineer with the Seventh Research Institute, China Ministry of Information Industry, Guangzhou, Guangdong. From 2012 to 2014, he was a Postdoctoral Fellow with North Carolina State University, Raleigh, NC, USA. He is currently an Associate Professor with Beijing Jiaotong University. His current research interests include high-power energy converter, electrical energy router, and transit power supply.