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A Non-Pulsating Input Current Step-Up DC/DC Converter With Common Ground Structure for Photovoltaic Applications

SHAHRUKH KHAN, (Student Member, IEEE), MOHAMMAD ZAID, (Member, IEEE), MOHAMMAD MUKTAFI ALI KHAN, AND ADIL SARWAR, (Senior Member, IEEE)
Department of Electrical Engineering, Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University, Aligarh 202002, India
Corresponding author: Mohammad Zaid (mohammad.zaid@zhcet.ac.in)

ABSTRACT Many of the High Gain Step-Up DC/DC converters proposed in the literature do not share common ground and have a pulsating or discontinuous input current, making the converter unsuitable for solar photovoltaic applications. In this article, a non-pulsating input current (NPIC) with a high-gain DC/DC step-up converter is proposed and analyzed in detail. The converter shares a common ground structure and a voltage conversion ratio more than twice that of the Traditional quadratic boost converter (TQBC). The converter has two switches that operate in phase, which makes it easy to control. Also, the voltage stress across all semiconductor devices is lower than the output voltage, which enhances the efficiency of the converter. The loss analysis is carried out with the PLECS software, integrating the real models of switches and diodes from the technical datasheet. To confirm and validate the functionality of the proposed converter, a 200 W hardware prototype is being developed in the laboratory. It was observed that the maximum efficiency was 94.5% with an input voltage of 16V. The converter achieves high gain at low duty cycles and has been shown to perform well in open loop conditions.

INDEX TERMS Boost converter, non-pulsating input current (NPIC), quadratic gain, voltage stress.

I. INTRODUCTION

The voltage produced at the output of many distributed generation (DG) sources such as solar photovoltaic (PV) systems, batteries, and fuel cells is low and needs to be increased to higher levels for practical applications. The high-gain DC/DC converter plays an important role in DC Microgrid and EV. These converters can generate controllable high DC voltage at the output. There are numerous applications for these converters. These converters are used in EV, solar PV, robotics, and aerospace applications [1]. High-gain converters are advantageous over traditional boost converters (TBC) and their variants [1] because they are operated at much lower duty ratios to achieve the same voltage gain. This leads to better efficiency. These converters are broadly classified into isolated and non-isolated structures [2]-[8]. The requirement of electrical isolation between input and load to prevent flow of direct flow of current is fulfilled by isolated converters. The high frequency transformer is used to achieve isolation, but increases cost [3]-[7] and size. High step-up converters [8]-[13] with switched capacitor (SC) voltage multiplier perform better than in semiconductors voltage stress and power density. The capacitor in the SC circuit is charged by the input source when the switch is ON, and the stored energy is discharged when the switch is OFF, so the voltage conversion ratio is significantly improved. The converter proposed in the literature [14]-[15] do not operate in wide range of duty cycles. Such converters fall in the category of quazi-z-source or z-source converters where the inductor is replaced by an impedance network. In [16], a transformerless active switched inductance (ASL) with a simple structure with a low voltage load on the active switch is presented. To further increase the voltage gain and reduce the voltage load of hybrid switching reactors, converters are presented in [17]. An active LC network is used to overcome the disadvantage of the ASL network, as shown in [18]. These converters use two switches similar to the converter proposed in this article, but the converter in [18] lacks a common ground structure.

The common ground between input and output can be used to increase system performance, eg, photovoltaic systems

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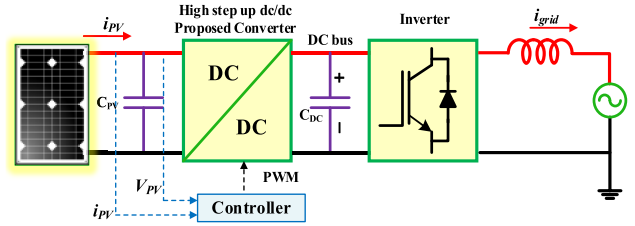

FIGURE 1. Application of a step-up DC/DC converter in grid-tied photovoltaic system.

connected to the grid without a transformer [2]. The general diagram of the photovoltaic system connected to the grid showing the application of the proposed converter is shown in Figure 1. The proposed converter has a common connection between the input source and the output loads. A voltage doubler is a very common method of multiplying the voltage conversion ratio [19]. In [19] a new impedance network is presented and the converter has the function of expanding the impedance network in n stages, but this deteriorates the efficiency of the converter.

A continuous input current of the step-up converter makes it suitable for renewable energy applications. This non-pulsating input current (NPIC) and the continuous current are included in the proposed converter. In the publication [20] a modified SEPIC converter with high gain with continuous input current is described. In [21] a buck-boost converter with a continuous input and output port with a higher conversion rate is proposed. In [22] another buck-boost topology, but it has a discontinuous input current that limits some applications. A switched inductor voltage multiplier with a capacitor is used in a traditional quadratic boost converter (TQBC) (Figure 2) in [23] to achieve twice of quadratic gain but the converter utilizes three inductors, unlike the proposed converter. The voltage stress of the converter reported in [23] is the same as the output voltage which is a major demerit of the converter.

Interleaving of the boost converter reduces the input ripple, but the switches operate with a phase shift of 180 degrees if a two-phase interleaved boost converter is proposed. A clamped structure is proposed in [24] which is used with an interleaved converter to enhance the voltage conversion ratio but the common connection between output and input is lost. In [25] a quadratic gain converter is proposed that has a conversion ratio of exactly half that of the proposed converter. However, the above converters only take into account the voltage stress on the switch in the off state. No voltage stress on semiconductor components should be neglected. The output diodes in the converters discussed above have a voltage stress equal to the output voltage, so a high-rated power diode should be used at the output. The proposed converter is advantageous over these converters with low voltage stress on the output power diode.

The above discussion considers the voltage conversion ratio and voltage stress of semiconductor devices without considering the nonpulsating nature of the input current. A pulsating input current can shorten the life of the electrodes in energy storage applications [26]. An LC filter can be used to reduce the ripple in the input current, but the circuit becomes bulky and degrades the efficiency of the converter and the dynamic response of the converter [26]. Interleaving seems promising to reduce the input ripples, but the control of the switches is very complex, and extra circuitry will be required which makes the circuit bulky, unlike the proposed converter.

Knowledge of the need for a higher voltage gain, a low voltage stress on semiconductor components, a non-pulsating nature of the input current, and a common ground structure. This article proposes a high-gain DC / DC converter with the attractive properties mentioned above. The proposed topology has a simple structure and is easy to implement and can also be used for industrial use.

The remainder of the literature is as follows. Section II presents the operating principle of the proposed NPIC converter. Steady-state analysis of the NPIC converter in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) in detail. Section III presents the parameter guidelines of the NPIC converter and section IV covers the non-ideal analysis of the NPIC converter. Comparative analysis among the recent similar converters is done in Section V. To determine the efficacy of the converter hardware, results are presented in Section VI. Finally, the literature is concluded in Section VII.

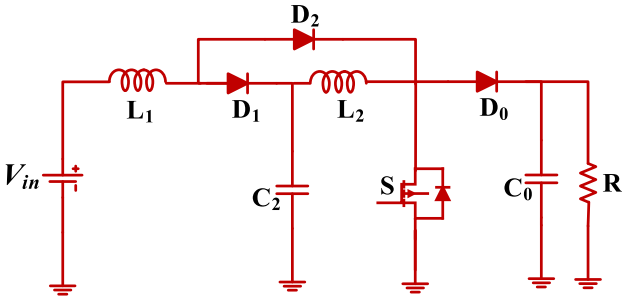

FIGURE 2. Traditional quadratic boost converter (TQBC).

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER (NPIC)

A. CIRCUIT DESCRIPTION

The proposed topology (NPIC) consists of two power switches ($S_1$and S_2), five diodes (D_1, D_2, D_3, D_4, and D_5), two inductors (L_1 and L_2), five capacitors (C_0, C_1, C_2, C_3, and C_4) as shown in Figure 3. The load R is taken as purely resistive. The inductor L_1 is always attached to the input source V_{in}, which contributes to the NPIC nature of the proposed converter. This is useful in reducing the current stress on the input dc source. The operation of the NPIC converter is explained in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

In the following analysis, some logical assumptions are considered: a) All the semiconductor power devices and passive elements are Ideal and non-dissipative. b) Capacitance of all the capacitors is high enough to hold the voltage constant.

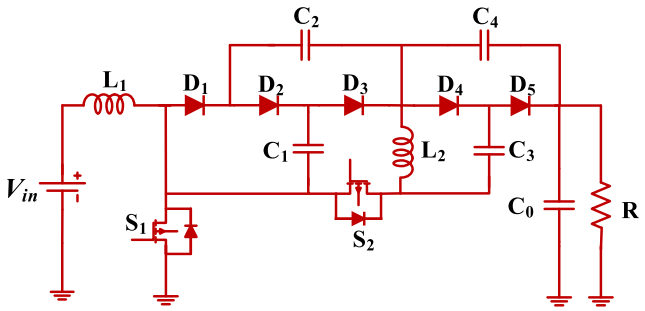

FIGURE 3. Proposed Step-Up NPIC Converter.

c) All the inductors, capacitors and resistors are linear, time-invariant, and independent of frequency.

B. CIRCUIT ANALYSIS IN CCM MODE

The converter operation in CCM mode can be divided into two modes: a) Mode 1 and b) Mode 2. Some characteristic waveform in this mode of operation is depicted in Figure 4.

MODE 1 (t_0 to t_1): Both the switches are turned ON. In this mode, the equivalent circuit is depicted in Figure 5(a). Diodes D_2 and D_4 are forward biased. Diodes D_1, D_2, and D_5 are reverse biased. Inductor L_1 is charged through input dc source and L_2 is charged through capacitor voltage C_3. The voltage and current relations can be obtained as

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C3} \\ V_{C3} = V_{C1} + V_{C2} \\ V_0 = V_{C3} + V_{C4} \end{cases} \tag{1}$$

$$\begin{cases} i_{in} = i_{L1} \\ i_{C1,on} = i_{D2} = i_{S1} - i_{S2} - i_{L1} \\ i_{C2,on} = i_{C1,on} \\ i_{C3,on} = i_{D4} = i_{S2} - i_{L2} \\ i_{C4,on} = i_{S1} - i_{L1} \\ i_{C0,on} = i_o + i_{S1} - i_{L1} \end{cases} \tag{2}$$

where i_{L1} and i_{L2} are ripple-free inductor currents, i_{in} is input current, i_{S1} and i_{S2} is on state current through the switches S_1 and S_2.

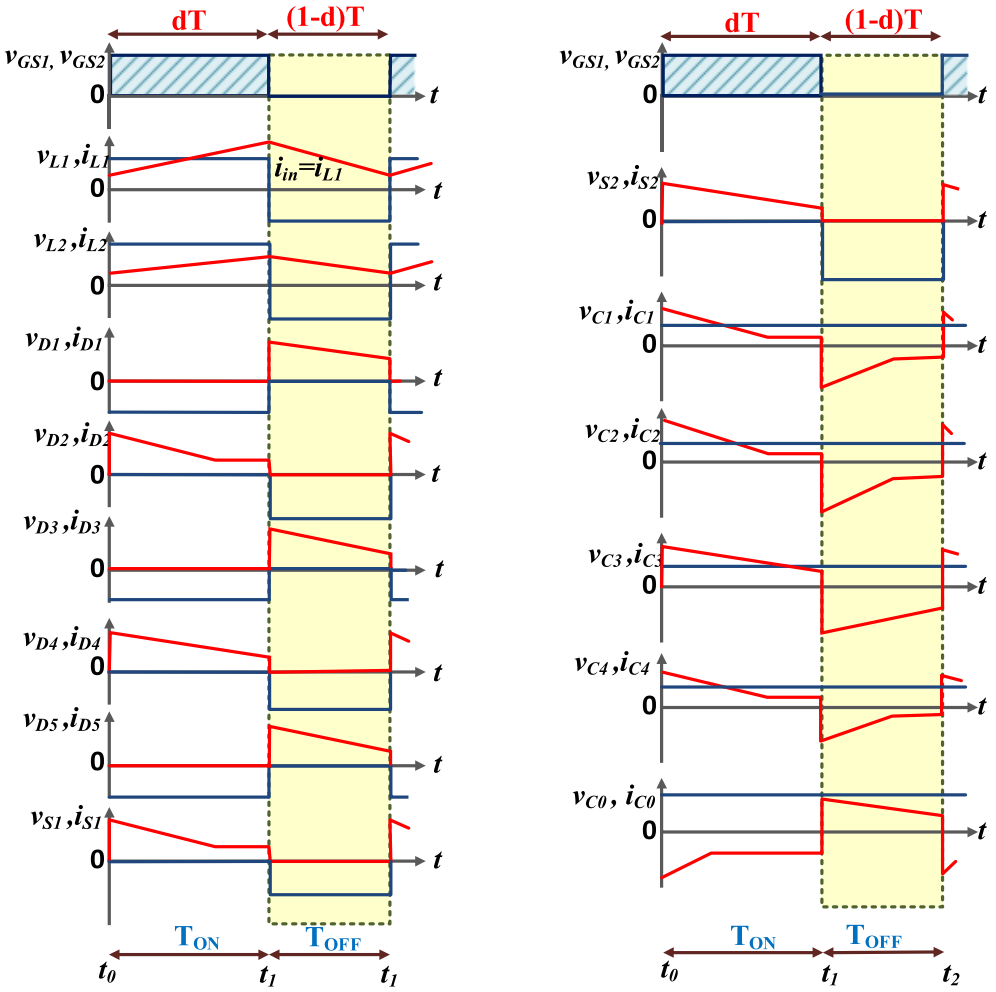

FIGURE 4. Key waveforms in CCM Mode: Current Waveforms (Red Line) and Voltage Waveforms (Blue line).

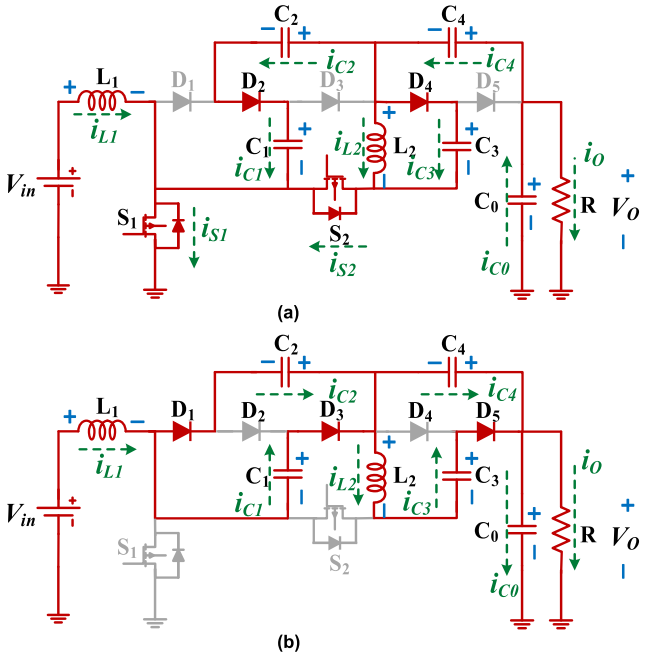

FIGURE 5. (a). Mode 1 of proposed NPIC converter. (b). Mode 2 of proposed NPIC converter.

MODE 2 (t_1 to t_2): Both switches are turned OFF at the beginning of this Mode 2. Diodes D_1, D_2, and D_5 are forward biased. Diodes D_2 and D_4 are reverse biased. Inductor L_1 is discharged and L_2 is discharged to supply energy load R. In this mode, the equivalent circuit diagram is depicted in Figure 5(b). The voltage and current relations can be obtained as

$$\begin{cases} V_{L1} = V_{in} + V_{C2} + V_{C4} - V_O \\ V_{L2} = V_{C3} - V_{C4} \\ V_{C1} = V_{C2} \end{cases} \tag{3}$$

$$\begin{cases} i_{in} = i_{L1} \\ i_{C1,off} = i_{D3} = i_{L1} - i_{D1} \\ i_{C2,off} = i_{D1} \\ i_{C3,off} = i_{D5} = i_{L2} \\ i_{C4,off} = i_{L1} - i_{L2} \\ i_{C0,off} = i_{L1} - i_o \end{cases} \tag{4}$$

C. VOLTAGE GAIN CALCULATION

Applying voltage second balance on inductor L_2 during one switching period T.

$$\begin{cases} \int_O^T V_{L2}.dt = 0 \\ d\,(V_{C3}) + (1-d)\,(V_{C3} - V_{C4}) = 0 \\ V_{C3} = (1-d)\,V_{C4} \end{cases} \tag{5}$$

The following relation between capacitor voltages can be obtained by equations (1), (3) and (5)

$$V_{C1} = V_{C2} = \frac{V_{C3}}{2} = \frac{(1-d)\,V_{C4}}{2} = \frac{V_O(1-d)}{2(2-d)} \tag{6}$$

Applying voltage second balance on inductor L_1 during one switching period T.

$$\begin{cases} \int_O^T V_{L1}.dt = 0 \\ d\,(V_{in}) + (1-d)\,(V_{in} + V_{C2} + V_{C4} - V_O) = 0 \\ (V_{in}) + (1-d)\left(V_{in} + \dfrac{V_O\,(1-d)}{2\,(2-d)} + \dfrac{V_O}{(2-d)} - V_O\right) = 0 \\ V_O = \dfrac{2(2-d)}{(1-d)^2} V_{in} \end{cases} \tag{7}$$

The voltage conversion ratio of the NPIC converter can be expressed using equation (7) where d is the duty cycle.

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{2(2-d)}{(1-d)^2} \tag{8}$$

D. VOLTAGE STRESS CALCULATION

According to the above analysis, the voltages stress of capacitors can be expressed using equation (6).

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{V_O(1-d)}{2(2-d)} = \dfrac{V_{in}}{(1-d)} \\ V_{C3} = \dfrac{V_O(1-d)}{(2-d)} = \dfrac{2V_{in}}{(1-d)} \\ V_{C4} = \dfrac{V_O}{(2-d)} = \dfrac{2V_{in}}{(1-d)^2} \end{cases} \tag{9}$$

The voltage stress on the power switches S_1 and S_2 in the proposed converter is V_{S1}, and V_{S2} can be calculated as

$$\begin{cases} V_{S1} = V_O - V_{C1} - V_{C4} = \dfrac{(1-d)\,V_O}{2\,(2-d)} = \dfrac{V_{in}}{(1-d)} \\ V_{S2} = V_{C1} + V_{C4} - V_{C3} = \dfrac{(1+d)\,V_O}{2\,(2-d)} = \dfrac{(1+d)V_{in}}{(1-d)^2} \end{cases} \tag{10}$$

The voltage stress on the power diodes D_1 to D_5 in the proposed converter is V_{D1}, and V_{D5} can be calculated as

$$\begin{cases} V_{D1} = V_{D2} = V_{D3} = V_{C1} = \dfrac{(1-d)\,V_O}{2\,(2-d)} = \dfrac{V_{in}}{(1-d)} \\ V_{D4} = V_{D5} = V_{C4} = \dfrac{V_O}{(2-d)} = \dfrac{(1+d)V_{in}}{(1-d)^2} \end{cases} \tag{11}$$

E. CALCULATION OF CURRENT STRESS

Since the circuit is loss free. On applying energy conservation i.e. $I_O V_O = I_{in} V_{in}$, where I_O is average output current equal to V_O/R

The average input current I_{in} or average inductor current L_1 is given by the below equation

$$I_{in} = I_{L1} = i_{L1} = \frac{V_O}{V_{in}} I_O = \frac{2(2-d)}{(1-d)^2} I_O \tag{12}$$

The ampere second balance on capacitor C_0 gives the following relation

$$\begin{cases} \int_0^T i_{C0}(t)\,.dt = 0 \\ \int_O^{dT} (i_{L1} - i_{S1} - i_O)\,dt - \int_{dT}^T (i_{L1} - i_O)\,.dt = 0 \\ di_{S1} = i_{L1} - i_O = \dfrac{3-d^2}{(1-d)^2} i_O \end{cases} \quad (13)$$

The average current through switch $S_1(I_{S1})$ is given using the result obtained in equation (13)

$$I_{S1} = di_{S1} = \frac{3-d^2}{(1-d)^2} I_O \quad (14)$$

Ampere second balance on capacitor C_4 gives the following relation

$$\begin{cases} \int_0^T i_{C4}(t)\,.dt = 0 \\ \int_O^{dT} (i_{L1} - i_{S1})\,dt - \int_{dT}^T (i_{L1} - i_{L2}).dt = 0 \\ di_{S1} + (1-d)\,i_{L2} = i_{L1} = \dfrac{2\,(2-d)}{(1-d)^2} I_O \\ (1-d)\,i_{L2} = I_O \end{cases} \quad (15)$$

The average current through the inductor L_2 is obtained by equation (15)

$$I_{L2} = i_{L2} = \frac{I_O}{(1-d)} \quad (16)$$

Ampere second balance on capacitor C_3 gives the following relation

$$\begin{cases} \int_0^T i_{C3}(t)\,.dt = 0 \\ \int_O^{dT} (i_{S2} - i_{L2})\,dt - \int_{dT}^T i_{L2}.dt = 0 \\ di_{S2} = i_{L2} = \dfrac{I_O}{(1-d)} \end{cases} \quad (17)$$

The average current through switch $S_2(I_{S2})$ is given using the result obtained in Equation (17)

$$I_{S2} = di_{S2} = \frac{I_O}{(1-d)} \quad (18)$$

In Mode 1,

$$\begin{cases} i_{D2} = i_{S1} - i_{S2} - i_{L1} = \dfrac{(2-d)I_O}{d(1-d)} \\ i_{D4} = i_{S2} - i_{L2} = \dfrac{I_O}{d} \end{cases} \quad (19)$$

In Mode 2,

$$\begin{cases} i_{D1} = \dfrac{(2-d)I_O}{(1-d)^2} \\ i_{D3} = i_{L1} - i_{D1} = \dfrac{(2-d)I_O}{(1-d)^2} \\ i_{D5} = \dfrac{I_O}{(1-d)} \end{cases} \quad (20)$$

The average values of currents (I_{Dx}) through all the diodes D_1 to D_5 can be expressed as

$$\begin{cases} I_{D1} = I_{D2} = I_{D3} = \dfrac{(2-d)I_O}{(1-d)} \\ I_{D4} = I_{D5} = I_O \end{cases} \quad (21)$$

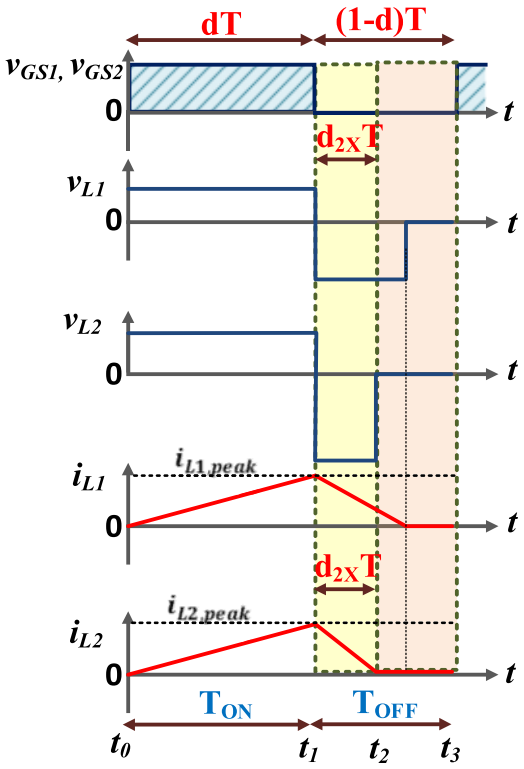

FIGURE 6. Key waveforms in DCM mode.

F. VOLTAGE GAIN ANALYSIS IN DCM MODE

The characteristic waveform is shown in Figure 6. The analysis is done in three modes.

MODE 1 (t_0 to t_1): The switch is turned ON at t=0. This mode is the same as Mode 1 in CCM. Both the inductor current start increasing from zero and reaches to peak value at instant t=dT. The peak value of currents through inductors L_1 and L_2 expressed as

$$\begin{cases} i_{L1,peak} = \dfrac{V_{in}}{L_1} dT \\ i_{L2,peak} = \dfrac{V_{C3}}{L_2} dT \end{cases} \quad (22)$$

MODE 2 (t_1 to t_2): The switch is turned OFF at the end of the dT interval similar to Mode 2 of CCM. Currents start to decrease with a constant slope, and the current of L_2 reaches zero at the end of the $d_{2x}T$ interval. The current of the L_1inductor continues to fall further as depicted in the figure. The inductor L_2 peak current in terms of $d_{2x}T$ can be expressed as

$$i_{L2,peak} = \frac{V_{C4} - V_{C3}}{L_2} d_{2x} T \quad (23)$$

MODE 3 (t_2 to t_3): Both the switches are still OFF. The current in the inductor L_2 is zero. Therefore, the voltage across the inductor L_2 is zero. By using equations (22) and (23) the parameter d_{2x} can be expressed as

$$d_{2x} = \frac{V_{C3}}{V_{C4} - V_{C3}} d = \frac{V_{C3}}{V_O - 2V_{C3}} d \tag{24}$$

During the OFF state of both switches. The average current through the capacitor C_3, I_{C3} can be expressed as

$$I_{C3} = \frac{1}{2} d_{2x} . i_{L2,peak} - I_O \tag{25}$$

When substituting (22) into (25), I_{C3} can be derived as

$$I_{C3} = \frac{1}{2} d_{2x} \frac{V_{C3}}{L_2} dT - \frac{V_O}{R} \tag{26}$$

Since the average capacitor current is zero, therefore using (26)

$$d_{2x} = \frac{2V_O \beta_{L2}}{V_{C3} d} = \frac{V_O (1-d) \beta_L}{V_{in} d} \tag{27}$$

where $\beta_L = \frac{2L_2}{RT}$

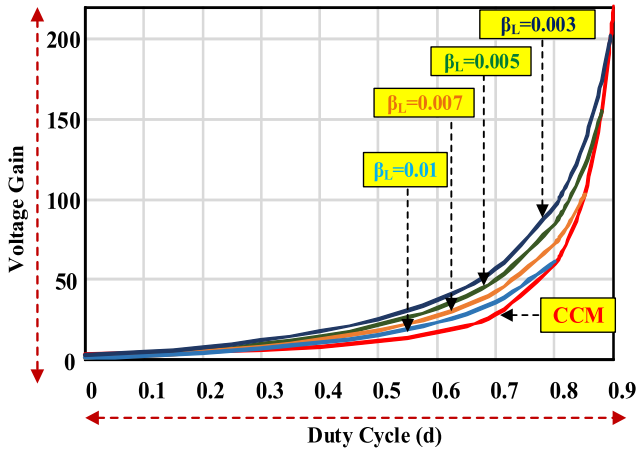

FIGURE 7. Voltage gain of the NPIC converter versus duty cycle.

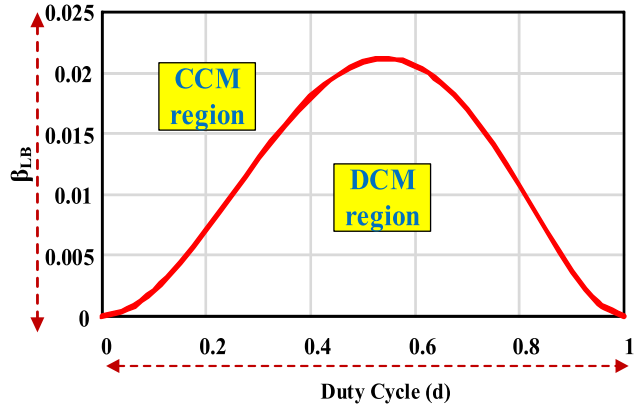

FIGURE 8. Boundary Normalized Inductor time (β_{LB}) constant versus duty cycle.

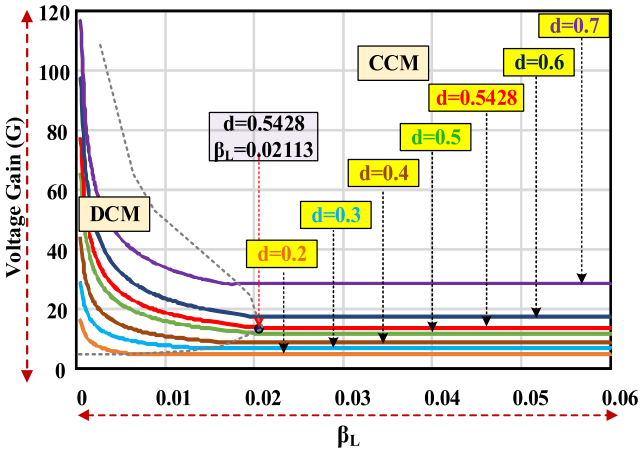

FIGURE 9. External characteristic of the NPIC converter.

When substituting the value of d_{2x} from (27) into equation (24)

$$\left(\frac{V_O}{V_{in}}\right)^2 - \frac{1}{(1-d)} \frac{V_O}{V_{in}} - \frac{d^2}{2(1-d)^2 \beta_L} = 0 \tag{28}$$

On solving the quadratic equation (28) the voltage gain in DCM mode can be expressed as

$$G_{DCM} = \frac{V_O}{V_{in}} = \frac{1}{(1-d)} \left(1 + \sqrt{1 + \frac{2d^2}{\beta_L}}\right) \tag{29}$$

The curve of voltage gain in this mode is presented in Figure 7.

G. BOUNDARY CONTINUOUS MODE OPERATION

In this mode of operation, the voltage gain of CCM is equal to the voltage gain in DCM mode.

$$G_{CCM} = G_{DCM}$$

The boundary normalized inductor time constant can be derived using (8) and (29)

$$\beta_{LB} = \frac{d^2 (1-d)^2}{2(2-d)} \tag{30}$$

Figure 7 shows the boundary normalized inductor time constant versus duty ratio (d). The boundary between the CCM and DCM is depicted in Figure 8.

H. EXTERNAL CHARACTERISTIC OF NPIC CONVERTER

On combining the equation (29) with (30) the external characteristic of the NPIC converter can be depicted in Figure 8. It is to be noted from Figure 8 and Figure 9 the maximum value of β_{LB} is 0.02113 at d=0.5428.

I. INPUT CURRENT RIPPLE

The difference between the maximum ($i_{L1,max}$) and minimum ($i_{L1,min}$) of the inductor, current L_1 is the input current ripple

of the NPIC converter. Δi_{in} is the input current ripple. The following equations can be obtained.

$$i_{L1,max} - i_{L1,min} = \frac{V_{in}d}{L_1 f_S} \tag{31}$$

The input current ripple can be expressed as

$$\begin{aligned}\Delta i_{in} &= i_{L1,max} - i_{L1,min} \\ &= \frac{V_{in}d}{L_1 f_S} = \frac{V_O d(1-d)^2}{2L_1 f_S(2-d)}\end{aligned} \tag{32}$$

The relationship between the duty cycle of the NPIC converter and traditional boost converter (TBC) can be expressed as (33) under the same conditions of inductor current, output, and input voltage.

$$d = d_T - \sqrt{(d_T-1)(d_T-3)} \tag{33}$$

The reduction in the input current ripple of the proposed NPIC converter in comparison to TBC can be expressed as (34)

$$\begin{aligned}\Delta i_T - \Delta i_{in} &= \frac{V_{in}d_C}{L_1 f_S} - \frac{V_{in}d}{L_1 f_S} \\ &= \frac{V_{in}d_C}{L_1 f_S} - \frac{V_{in}\left[d_T - \sqrt{(d_T-1)\,(d_T-3)}\right]}{L_1 f_S} \\ &= \frac{V_{in}\sqrt{(d_T-1)(d_T-3)}}{L_1 f_S}\end{aligned} \tag{34}$$

where Δi_T is the input ripple of the TBC and d_T is the duty of the TBC.

III. PARAMTER DESIGN GUIDELINES

A. INDUCTOR SELECTION

The ON state of the current ripple in an inductor can be expressed as

$$\Delta i_{L1} = \frac{V_{in}}{L_1}dT \tag{35}$$

$$\Delta i_{L2} = \frac{2V_{in}}{L_2(1-d)}dT \tag{36}$$

Hence the inductance value of L_1 and L_2 is calculated using equations (37) and (38)

$$L_1 = \frac{V_{in}}{\Delta i_{L1}}dT = \frac{V_{in}}{r_{L1}\%I_{L1}}dT \tag{37}$$

$$L_2 = \frac{2V_{in}}{\Delta i_{L2}(1-d)}dT = \frac{2V_{in}}{r_{L2}\%I_{L2}(1-d)}dT \tag{38}$$

where $r_{L1}\%$ and $r_{L2}\%$ is percentage ripple allowed in the inductor currents L_1 and L_2.

To operate the inductors in CCM mode, the following equation in (40) and (41) must be valid.

$$\begin{cases} I_{L1} - \dfrac{\Delta i_{L1}}{2} > 0 \\ I_{L2} - \dfrac{\Delta i_{L2}}{2} > 0 \end{cases} \tag{39}$$

$$\begin{cases} L_1 > \dfrac{d(1-d)^4 R}{4(2-d)^2 f_S} \\ L_2 > \dfrac{d^2(1-d)^2 R}{2(2-d) f_S} \end{cases} \tag{40}$$

TABLE 1. Voltage and current stress of Semiconductors.

Parameter	Voltage Stress	Current Stress
S_1	$\frac{(1-d)V_O}{2(2-d)}$	$\frac{3-d^2}{(1-d)^2}I_O$
S_2	$\frac{(1+d)V_O}{2(2-d)}$	$\frac{I_O}{(1-d)}$
D_1	$\frac{(1-d)V_O}{2(2-d)}$	$\frac{(2-d)I_O}{(1-d)}$
D_2	$\frac{(1-d)V_O}{2(2-d)}$	$\frac{(2-d)I_O}{(1-d)}$
D_3	$\frac{(1-d)V_O}{2(2-d)}$	$\frac{(2-d)I_O}{(1-d)}$
D_4	$\frac{V_O}{(2-d)}$	I_O
D_5	$\frac{V_O}{(2-d)}$	I_O

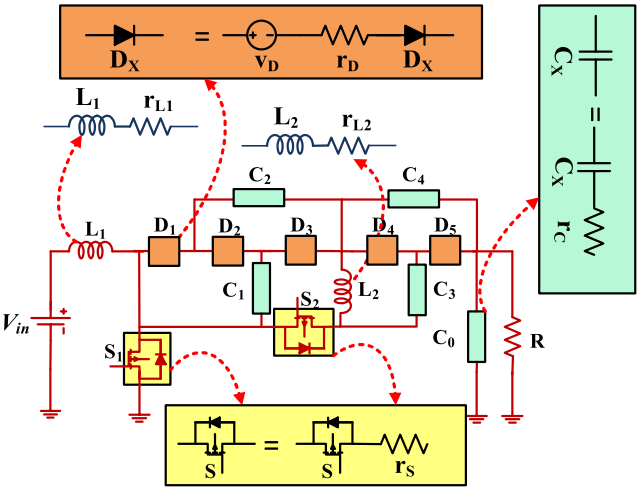

FIGURE 10. Non-Ideal Model of the NPIC Converter.

B. CAPACITOR SELECTION

The capacitor selection can be made by equation (41)

$$\begin{cases} C_1 \geq \dfrac{(2-d)\,I_O}{(1-d)\,\Delta v_{C1} f_S} = \dfrac{(2-d)\,I_O}{(1-d)\,r_{C1}\%V_{C1} f_S} \\ C_2 \geq \dfrac{(2-d)\,I_O}{(1-d)\,\Delta v_{C2} f_S} = \dfrac{(2-d)\,I_O}{(1-d)\,r_{C2}\%V_{C2} f_S} \\ C_3 \geq \dfrac{I_O}{\Delta v_{C3} f_S} = \dfrac{I_O}{r_{C3}\%V_{C2} f_S} \\ C_4 \geq \dfrac{(3-d)\,I_O}{(1-d)\,\Delta v_{C2} f_S} = \dfrac{(3-d)\,I_O}{(1-d)\,r_{C3}\%V_{C3} f_S} \\ C_0 \geq \dfrac{\left(3-d^2\right)I_O}{(1-d)\,\Delta v_{C2} f_S} = \dfrac{(3-d)\,I_O}{(1-d)\,r_{C3}\%V_{C3} f_S} \end{cases} \tag{41}$$

where $r_{C1}\%$, $r_{C2}\%$, $r_{C3}\%$, $r_{C4}\%$ and $r_{C0}\%$ is percentage ripple allowed in capacitor voltages.

C. SEMICONDUCTOR SELECTION

The parameter selection of power switch and diodes are based on their current and voltage stresses respectively, as tabulated in Table 1 as calculated in section II.

IV. NON IDEAL ANALYSIS OF NPIC CONVERTER

The actual real-world model of the NPIC will have some non-idealities. The non-ideal model of the NPIC converter is presented in Figure 10. The inductors (L_1 and L_2) equivalent series resistance (ESR) r_{L1} and r_{L2} is considered. MOSFETS S_1 and S_2 have on resistance equal to r_{S1} and r_{S2}. The diodes D_1 to D_5 forward voltage drop is V_F and on-resistance equal to r_D. The ESR of capacitors C_0 to C_4 is r_C.

A. POWER LOSS IN INDUCTORS

The ohmic losses in the inductor depend on the current through the inductors L_1 and L_2. P_{L1} and P_{L2} are the ohmic losses in the inductor L_1 and L_2 and $I_{L1_{rms}}$ and $I_{L2_{rms}}$ are root mean square value of inductor currents.

$$P_{L,total} = \sum_{k=1}^{k=2} \left(I_{Lk_{rms}}\right)^2 r_{Lk} = I_{L1_{rms}}^2 r_{L1} + I_{L2_{rms}}^2 r_{L2} \quad (42)$$

$$\begin{cases} I_{L1_{rms}} = \dfrac{2(2-d)}{(1-d)^2} I_O \\ I_{L2_{rms}} = \dfrac{1}{(1-d)} I_O \end{cases}$$

$$P_{L,total} = \left(\frac{2\,(2-d)}{(1-d)^2} I_O\right)^2 r_{L1} + \left(\frac{1}{(1-d)} I_O\right)^2 r_{L2} \quad (43)$$

If it is assumed $r_{L1} = r_{L2} = r_L$

$$\begin{aligned} P_{L,total} &= \frac{4\,(2-d)^2}{(1-d)^4}\frac{r_L}{R}P_0 + \frac{1}{(1-d)^2}\frac{r_L}{R}P_0 \\ &= \left(\frac{5d^2 - 18d + 17}{(1-d)^4}\right)\frac{r_L}{R}P_0 \end{aligned} \quad (44)$$

B. POWER LOSS IN SWITCHES

The two types of losses that occur in the MOSFET are ohmic loss and switching loss. Ohmic loss occurs due to the ON resistance of the MOSFET.

$I_{S1_{rms}}, I_{S2_{rms}}$ is the root mean square value of current passing through switch S_1 and S_2. The total ohmic losses, $P_{S,total}^{ohmic}$ occurring in both the switches is the summation of individual ohmic losses that occur in both switches.

$$P_{S,total}^{ohmic} = \sum_{k=1}^{k=2} \left(I_{Sk_{rms}}\right)^2 r_{Sk} = I_{S1_{rms}}^2 r_{S1} + I_{S2_{rms}}^2 r_{S2} \quad (45)$$

$$\begin{cases} I_{S1_{rms}} = \left(\dfrac{3-d^2}{\sqrt{d}\,(1-d)^2}\right) I_0 \\ I_{S2_{rms}} = \dfrac{1}{\sqrt{d}(1-d)} I_O \end{cases}$$

$$P_{S,total}^{ohmic} = \left(\frac{\left(3-d^2\right)^2}{d(1-d)^4}\right) I_0^2 r_{S1} + \left(\frac{1}{d(1-d)^2}\right) I_0^2 r_{S2} \quad (46)$$

If it is assumed $r_{L1} = r_{L2} = r_L$

$$P_{S,total}^{ohmic} = \left(\frac{d^4 - 5d^2 - 2d + 10}{d(1-d)^4}\right)\frac{r_S}{R}P_0 \quad (47)$$

Total switching loss in the MOSFET is denoted by

$$\begin{aligned} P_{S,total}^{SW} &= \sum_{k=1}^{k=2} \frac{1}{2}\left(\frac{V_{Sk} I_{Sk}}{T}\right)(t_r + t_s) \\ &= \frac{1}{2}\left(\frac{V_{S1} I_{S1} + V_{S2} I_{S2}}{T}\right)(t_r + t_s) \end{aligned} \quad (48)$$

$$P_{S,total}^{SW} = \frac{(4 + d - d^2)\,(t_r + t_s) f_S}{4d(1-d)(2-d)} P_0 \quad (49)$$

where,t_r and t_S are rise and fall time of switches respectively and f_S is switching frequency.

Total loss in the switches is the summation of ohmic loss and switching loss.

$$\begin{aligned} P_{S,total} &= P_{S,total}^{ohmic} + P_{S,total}^{SW} \\ &= \left(\frac{d^4 - 5d^2 - 2d + 10}{d(1-d)^4}\right)\frac{r_S}{R}P_0 \\ &\quad + \left(\frac{(4 + d - d^2)\,(t_r + t_s) f_S}{4d(1-d)(2-d)}\right) P_0 \end{aligned} \quad (50)$$

C. POWER LOSS IN DIODES

Switching loss is neglected in power diodes. Losses occurring due to the on-resistance of the diode and the forward voltage drop are only considered in the calculation. On the basis of the calculation in Section II, the average and RMS values of current through diodes can be calculated as

$$\begin{cases} I_{D1,avg} = I_{D2,avg} = I_{D3,avg} = \dfrac{(2-d) I_O}{(1-d)} \\ I_{D4,avg} = I_{D5,avg} = I_O \\ I_{D1_{rms}} = I_{D2_{rms}} = I_{D3_{rms}} = \dfrac{(2-d)\,I_O}{\sqrt{d}\,(1-d)} \\ I_{D4_{rms}} = I_{D5_{rms}} = \dfrac{I_O}{\sqrt{d}} \end{cases} \quad (51)$$

The power loss associated with the forward voltage drop V_F in power diodes can be calculated as

$$\begin{aligned} P_{VF,total} &= \sum_{k=1}^{k=5} I_{Dk,avg}.V_F \\ &= I_{D1,avg}.V_F + I_{D2,avg}.V_F + I_{D3,avg}.V_F \\ &\quad + I_{D4,avg}.V_F + I_{D5,avg}.V_F \\ P_{VF,total} &= \frac{(8-5d)\,I_O V_F}{(1-d)} = \frac{(8-5d)\,V_F}{(1-d)\,V_O} P_O \end{aligned} \quad (52)$$

The ohmic loss occurring in power diodes due to internal resistance r_D can be calculated as

$$\begin{aligned} P_{rD,total} &= \sum_{k=1}^{k=5} I_{Dk_{rms}}^2.r_D \\ &= I_{D1_{rms}}^2.r_D + I_{D2_{rms}}^2.r_D + I_{D3_{rms}}^2.r_D \\ &\quad + I_{D4_{rms}}^2.r_D + I_{D5_{rms}}^2.r_D \\ P_{rD,total}^{ohmic} &= \frac{(5d^2 - 10d + 14)}{d\,(1-d)^2}\frac{r_D}{R}P_O \end{aligned} \quad (53)$$

The total power loss in the diodes is the sum of the loss due to forward voltage drop and ohmic loss.

$$\begin{aligned} P_{D,total} &= P_{rD,total}^{ohmic} + P_{VF,total} \\ &= \frac{(5d^2 - 10d + 14)}{d\,(1-d)^2}\frac{r_D}{R}P_O + \frac{(8-5d)\,V_F}{(1-d)\,V_O}P_O \end{aligned} \quad (54)$$

D. POWER LOSS IN CAPACITORS

The RMS value of the current through the capacitors can be expressed as

$$\begin{cases} I_{C1_{rms}} = \dfrac{(2-d)I_O}{(1-d)\sqrt{d(1-d)}} \\ I_{C2_{rms}} = \dfrac{(2-d)I_O}{(1-d)\sqrt{d(1-d)}} \\ I_{C3_{rms}} = \dfrac{I_O}{\sqrt{d(1-d)}} \\ I_{C4_{rms}} = \dfrac{(3-d)I_O}{(1-d)\sqrt{d(1-d)}} \\ I_{C0_{rms}} = \dfrac{(3-d)I_O}{(1-d)\sqrt{d(1-d)}} \end{cases} \tag{55}$$

The total losses in the capacitors due to ESR of the capacitor r_C can be expressed as

$$\begin{aligned} P_{rC,total} &= \sum_{k=0}^{k=4} I_{Dk_{rms}}^2 . r_C \\ &= I_{C0_{rms}}^2 . r_C + I_{C1_{rms}}^2 . r_C + I_{C2_{rms}}^2 . r_C \\ &\quad + I_{C3_{rms}}^2 . r_C + I_{C4_{rms}}^2 . r_C \\ P_{C,total} &= \frac{(5d^2 - 24d + 29) I_O^2 r_C}{d(1-d)^3} \\ &= \frac{(5d^2 - 24d + 29)}{d(1-d)^3} \frac{r_C}{R} P_O \end{aligned} \tag{56}$$

Thus, the efficiency (η) of the proposed NPIC converter can be calculated as

$$\eta = \frac{P_O}{P_O + P_{L,total} + P_{S,total} + P_{D,total} + P_{C,total}}$$

$$\eta = \frac{1}{1 + A_1 \frac{r_L}{R} + A_2 \frac{r_S}{R} + A_3 \frac{r_D}{R} + A_4 \frac{r_C}{R} + A_5 \frac{V_F}{V_O} + A_6} \tag{57}$$

where,

$$\begin{cases} A_1 = \dfrac{5d^2 - 18d + 17}{(1-d)^4}, A_2 = \dfrac{d^4 - 5d^2 - 2d + 10}{d(1-d)^4} \\ A_3 = \dfrac{5d^2 - 10d + 14}{d\,(1-d)^2}, A_4 = \dfrac{\left(5d^2 - 24d + 29\right)}{d\,(1-d)^3} \\ A_5 = \dfrac{(8-5d)}{(1-d)}, A_6 = \dfrac{(4 + d - d^2)\,(t_r + t_s) f_S}{4d(1-d)(2-d)} \end{cases}$$

Therefore non-ideal gain in CCM mode can be expressed as

$$G_{CCM_{non-ideal}} = \frac{V_0}{V_{in}} \eta$$

$$G_{CCM_{non-ideal}} = \frac{2(2-d)}{(1-d)^2} \left(\frac{1}{1 + A_1 \frac{r_L}{R} + A_2 \frac{r_S}{R} + A_3 \frac{r_D}{R} + A_4 \frac{r_C}{R} + A_5 \frac{V_F}{V_O} + A_6} \right) \tag{58}$$

The curve of ideal voltage gain and non-ideal voltage gain with $r_{S1} = r_{S2} = 0.07\Omega, r_{L1} = r_{L2} = 0.2\Omega, r_C = 0.1\Omega, r_D = 0.04\Omega, V_F = 0.4V$ with duty ratio is shown in Figure 11. The deviation is due to the presence of parasitic elements.

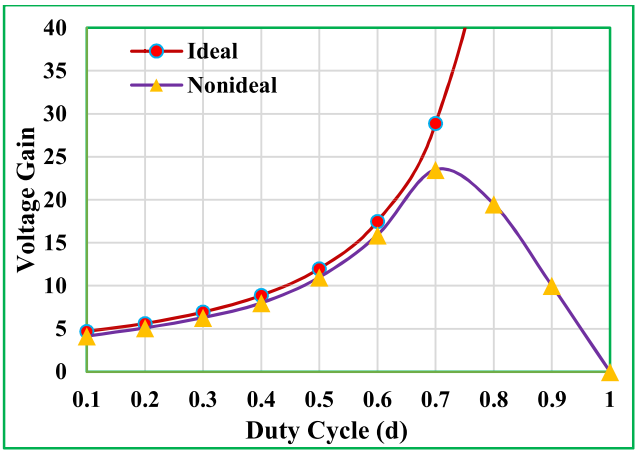

FIGURE 11. Ideal and Non-Ideal Voltage Gain versus duty ratio.

V. COMPARISION AMONG SIMILAR DC/DC NON ISOLATED CONVERTER

In this section the comparative analysis of the NPIC converter with other previous topologies is carried out. The comparison is made based on the number of active and passive elements, the voltage gain and the voltage across the switch when the switch is off, the type of input current, and the availability of a common ground between the source and the load., as shown in Table 2. The comparison of the boosting capability of the proposed converter is shown in Figure 12 (a). It should be noted that the NPIC converter has the highest voltage in all duty cycles. According to Table 2, the converter indicated in [C] has the maximum number of components equal to 16, while the NPIC converter has a total of 14 components, which is the same as the converter indicated in [A]. The NPIC converter utilizes two switches equal to converters reported in [F] and [H] while all the converters reported in Table 2 utilizes a single switch. The NPIC converter, TQBC, [B], [F], [H], and [I] utilizes two inductors, whereas the converter reported in [C], [D], [E], and [G] uses three inductors and the converter in [A] utilizes four inductors. The converter reported in [3] has the maximum number of diodes, while the NPIC converter uses five diodes which is less than the converter in [A]. The NPIC converter has the maximum number of capacitors. Since voltage gain is not a sufficient metric to evaluate the performance of the converter, several devices have been involved in the comparison of the converter. The voltage gains per inductor, voltage gain per switch, voltage gain per diode and voltage gain per capacitor count is presented in Figure 12(b) to Figure 12(e) respectively.

It can be observed that the proposed converter has the highest voltage gain per inductor as depicted in Figure 12(b). The voltage gain per switch count is depicted in Figure 12(c) since the converter reported in [G] consists of a single switch, so it has the highest voltage gain per switch. The voltage gain per switch of the NPIC converter is highest except converter

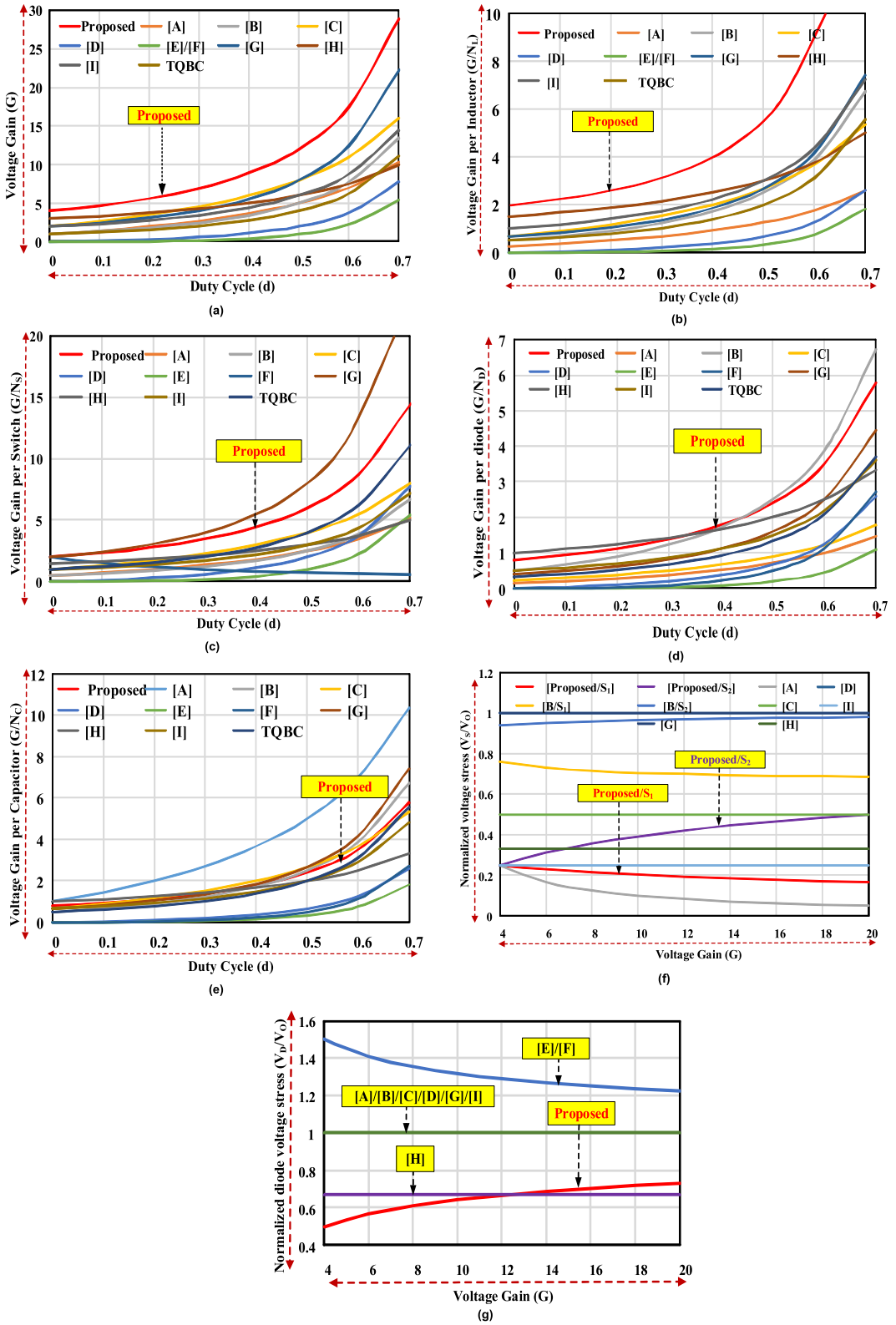

FIGURE 12. (a). Comparison curve of voltage gain versus duty cycle. (b). Comparison curve of voltage gain per inductor count versus duty cycle. (c). Comparison curve of voltage gain per switch count versus duty cycle. (d). Comparison curve of voltage gain per diode count versus duty cycle. (e). Comparison curve of voltage gain per capacitor count versus duty cycle. (f). Comparison curve of Normalized voltage stress versus Voltage gain. (g): Comparison curve of output voltage stress versus voltage gain.

presented in [G] but the overall gain of the converter [G] is less than the proposed converter. The proposed converter consists of five diodes, the voltage gain per diode count is depicted in Figure 12(d), the converter presented in [B] is

TABLE 2. Comparison among similar DC/DC converters.

Topology	Reactive Components		Semiconductor Components		Voltage Gain (V_O/V_{in})	Voltage stress (V_S/V_O)	Output diode stress (V_D/V_O)	Input current Type	Common Ground Between load and Source
	N_L	N_C	N_S	N_D					
Proposed	2	5	2	5	$\frac{2(2-d)}{(1-d)^2}$	$S_1: \frac{1}{G(1-d)}$ $S_2: \frac{(1+d)}{G(1-d)^2}$	$\frac{1}{2-d}$	*Non-Pulsating Continuous*	✓
TQBC	2	2	1	3	$\frac{1}{(1-d)^2}$	1	1	*Non-Pulsating Continuous*	✓
[A]	4	1	2	7	$\frac{1+3d}{1-d}$	$\frac{1}{G}$	1	*Pulsating Continuous*	×
[B]	2	2	2	2	$\frac{1+d-d^2}{(1-d)^2}$	$S_1: \frac{2(1+G)}{G+\sqrt{5G+4G^2}}$ $S_2: \frac{2(1+G)^2}{3G+2G^2+\sqrt{5G+4G^2}}$	1	*Pulsating Continuous*	×
[C]	3	3	1	9	$\frac{2(1+2d)}{1-d}$	$\frac{1}{2}$	1	*Pulsating continuous*	×
[D]	3	3	1	3	$\frac{d}{(1-d)^2}$	1	1	*Non-Pulsating Continuous*	✓
[E]	3	3	1	5	$\frac{d^2}{(1-d)^2}$	$1+\frac{1}{\sqrt{G}}$	$\frac{1}{d}$	*Non-Pulsating Continuous*	✓
[F]	2	2	2	2	$\frac{d^2}{(1-d)^2}$	$S_1: \frac{1}{G}+\frac{1}{\sqrt{G}}$ $S_2: 1+\frac{1}{\sqrt{G}}$	$\frac{1}{d}$	*Pulsating Discontinuous*	✓
[G]	3	3	1	5	$\frac{2}{(1-d)^2}$	1	1	*Non-Pulsating Continuous*	✓
[H]	2	3	2	3	$\frac{3}{1-d}$	$\frac{1}{3}$	$\frac{2}{3}$	*Pulsating Continuous*	×
[I]	2	3	1	4	$\frac{(2-d)}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	1	*Pulsating Continuous*	✓

N_S: Switch Count; N_L: Inductor Count; N_D: Diode Count; N_C: Inductor Count, ✓: Yes, ×: No
[A]: L. S. Yang et. al.[17] [B]: Y. Tang et al. [18] [C]: T. Shanthi et. al.[19] [D]: P. K. Maroti et al. [20][E]: N. Zhang et al. [21] [F]: S. Miao et al. [22] [G]:Rezaie et. al[23] [H]: Y. Zeng et. al [24] [I]: G. G. Kumar et. al [25]

advantageous of all converters in this term due to the low count of diodes, but the NPIC converter the has also highest share of the diode in achieving gain except [B]. The voltage gain per capacitor count is depicted in Figure 12(e). It is observed that the NPIC converter has a lower voltage gain per capacitor count than [A], [B] and [G].

The voltage stress of the switch is an important criterion for evaluating DC / DC topologies. A diagram of the normalized voltage stress of the switch is shown in Figure 12 (f). The topology specified in [F] has the highest voltage stress of both switches, but is not shown in this figure. The NPIC converter has a lower voltage load than TQBC, [B]. The switch S_1 of the NPIC converter has the lowest stress of all the listed converters except [A]. The voltage stress on the output diode is equal to the output voltage on the converters [A], [B], [C], [D], [G], and [I], as shown in Figure 12 (g). This disadvantage is overcome in the proposed NPIC converter, in which the voltage load on the output diode is less than the output voltage. The converter specified in [E] / [F] has a voltage stress that is greater than the output voltage. Low voltage stress on semiconductor components leads to lower costs and higher efficiency.

The NPIC converter has an inductor at the input side which makes the converter input current continuous and non-pulsating unlike converters in [A], [B], [C], [F], [G] and [I] which has pulsating input current which makes them applicable for photovoltaic applications. The converter in [F] has a discontinuous input current which restricts its operation.

Application for MPPT applications. A common ground connection between the load and the source makes the converter suitable for various applications. There is more safety, fewer protection problems and reduced electromagnetic interference (EMI). Moreover, there is no extra dv/dt between the input and output grounds. NPIC converter, TQBC and

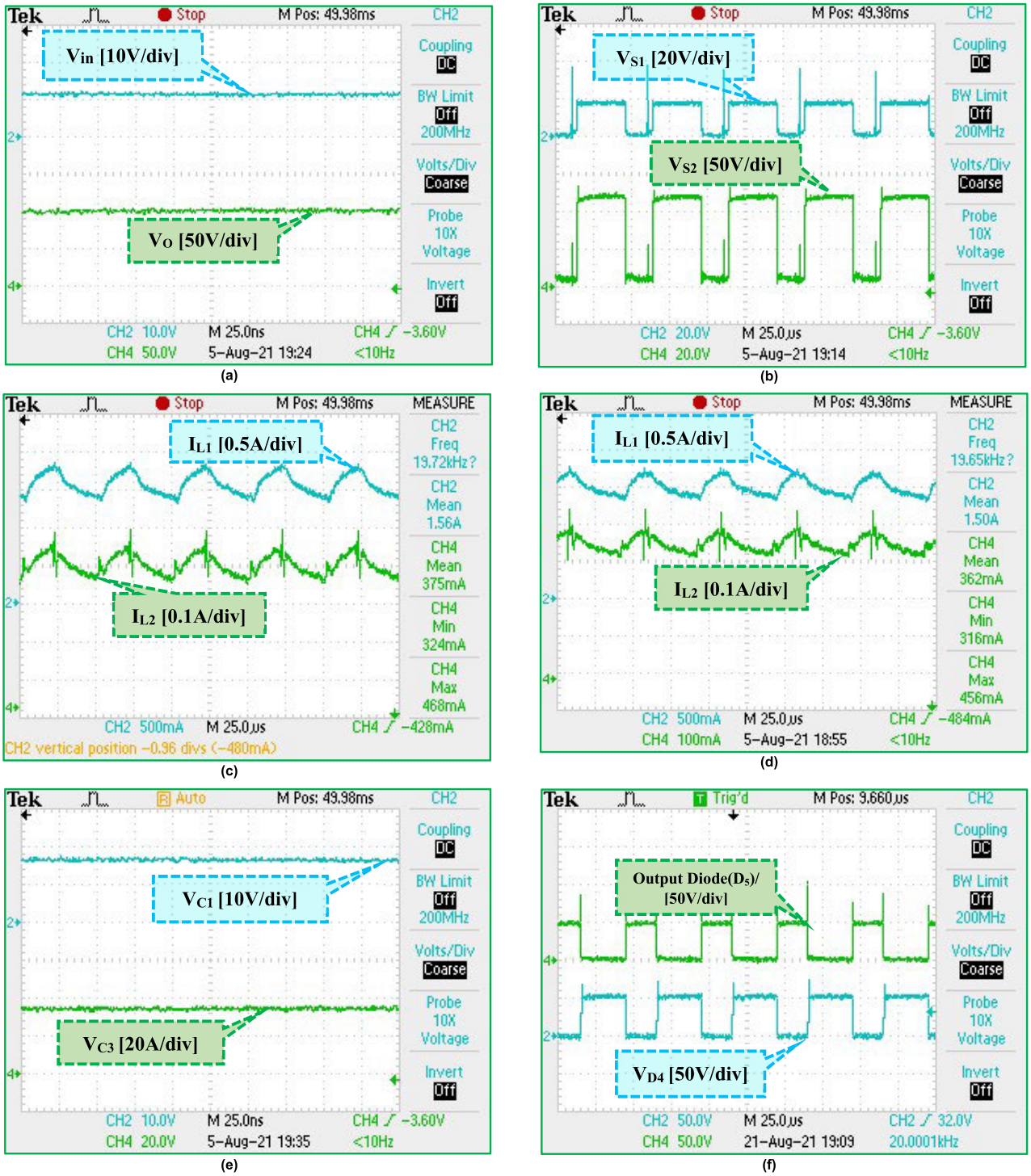

FIGURE 13. (a). Bottom to Top: Output Voltage, Input Voltage at d=0.4 and *fs* = 20 KHz. (b). Bottom to Top: MOSFET (S_2) Voltage, MOSFET (S_1) Voltage at d=0.4 and *fs*=20 KHz. (c). Bottom to Top: Inductor current L_2 and Inductor current L_1 at d=0.4 and *fs* =20 KHz. (d). Bottom to Top: Inductor current L_2 and Inductor current L_1 at d=0.3 and *fs* =20 KHz. (e). Bottom to Top: Capacitor voltage (C_1) and Capacitor (C_3) Voltage waveforms. (f). Bottom to Top: Diode voltage (D_4) and Output Diode voltage (D_5) at d=0.3. (g). Bottom to Top: Diode voltage (D_1) and Output Diode voltage (D_2) at d=0.3. (h). Change in output voltage by a dynamic change in input voltage. (i). Effect of Dynamic change in the duty cycle on the output voltage.

converters reported in [D], [E], [F], and [G] and [I] have a common ground between source and load which is advantageous for all the other converters listed in Table 2. Therefore, it can be concluded that the NPIC converter has many advantages over the other listed converters.

VI. HARDWARE RESULTS OF THE NPIC CONVERTER

To validate the performance of the NPIC converter, a 200W hardware model is built with the specifications defined in Table 3. The input voltage waveforms and output voltage are shown in Figure 13(a). In the same figure, the input voltage

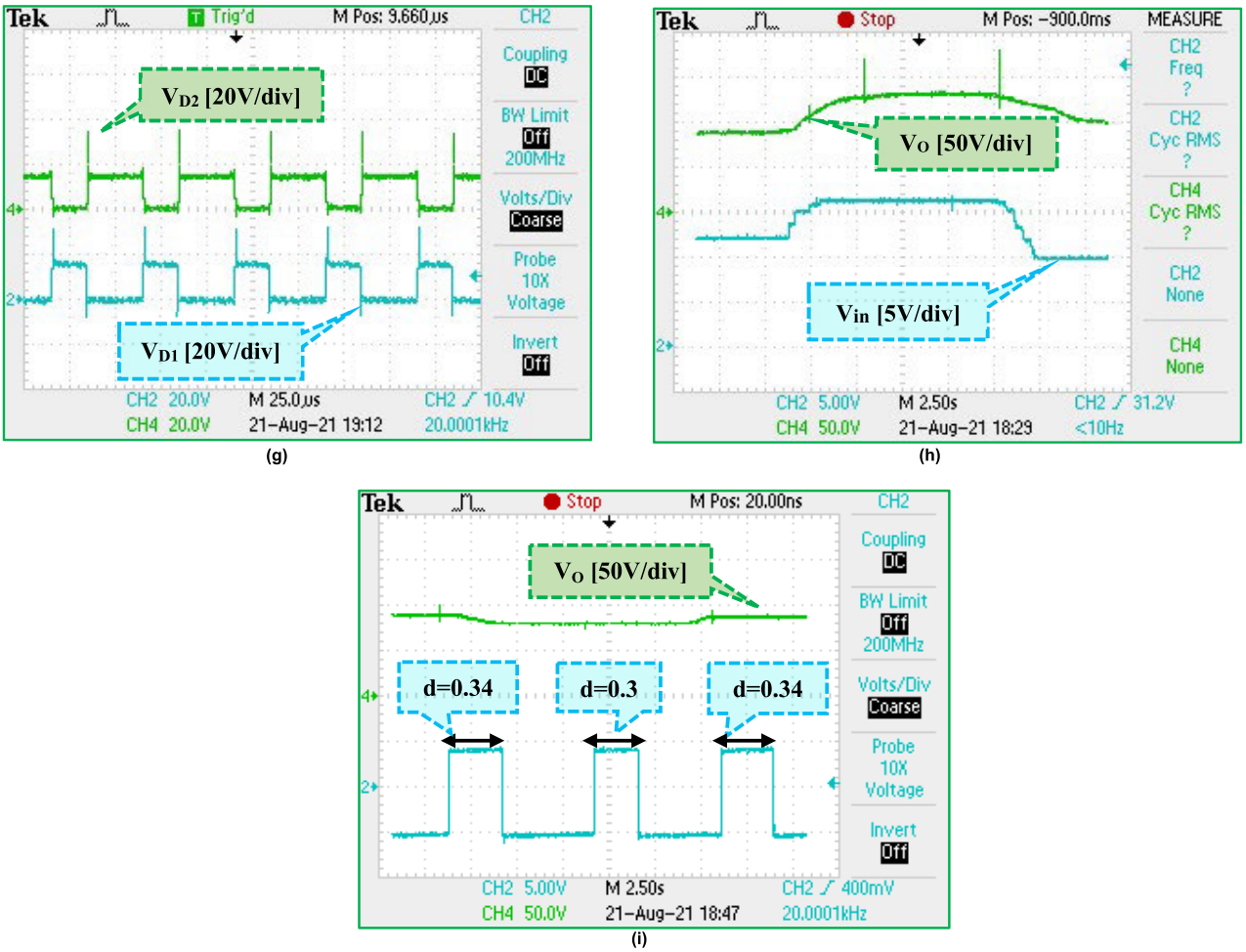

FIGURE 13. *(Continued.)* **(a). Bottom to Top: Output Voltage, Input Voltage at d=0.4 and *fs* = 20 KHz. (b). Bottom to Top: MOSFET (S_2) Voltage, MOSFET (S_1) Voltage at d=0.4 and *fs*=20 KHz. (c). Bottom to Top: Inductor current L_2 and Inductor current L_1 at d=0.4 and *fs* =20 KHz. (d). Bottom to Top: Inductor current L_2 and Inductor current L_1 at d=0.3 and *fs* =20 KHz. (e). Bottom to Top: Capacitor voltage (C_1) and Capacitor (C_3) Voltage waveforms. (f). Bottom to Top: Diode voltage (D_4) and Output Diode voltage (D_5) at d=0.3. (g). Bottom to Top: Diode voltage (D_1) and Output Diode voltage (D_2) at d=0.3. (h). Change in output voltage by a dynamic change in input voltage. (i). Effect of Dynamic change in the duty cycle on the output voltage.**

is observed to be 12V and 102V at a duty ratio of 40%. The blocking voltage waveforms of both MOSFETS S_1 and S_2 are shown in Figure 13(b). The blocking voltages V_{S1} and V_{S2} of the switch S_1 are 20V and the switch S_2 is 46 V, which is 19.6% and 45% of the output voltage (V_O). The open-loop operation of the NPIC Converter is done in CCM mode. The inductor currents (I_{L1} and I_{L2}) waveform associated with CCM Mode is shown in Figure 13(c, d) at a duty percentage of 40% and 30% at a constant resistive load of 450 ohms. As the duty ratio is decreased from 40% to 30%, the mean value of the currents of inductors L_1 and L_2 will decrease. From the same Figure 13(c) it can be seen that the mean value of the inductor currents L_1 and L_2 is 1.56A and 0.375A at a duty cycle of 40%. The ripple values of the inductor current are nearly equal to 25% in $L_1$and L_2. When the duty cycle is reduced to 30% the mean values of the inductor currents L_1 and L_2 are 1.5A and 0.362A, respectively.

The input current of the converter is equal to i_{L1}, hence the converter naturally has a continuous input current. In most of the switched capacitor topologies, a high ripple in input current is observed due to the large current drawn by the capacitors for charging. The voltages of the capacitors are depicted in Figure 13(e). The capacitor voltages C_1 and C_3 are found to be 17V and 34V, respectively. When both the switches are ON, the output diode D_5 is OFF and diode D_4 is ON. The standing voltages of diodes D_5 and D_4 are equal to 48V at a duty of 30% which is almost 57% of $V_o$as depicted in Figure 13(f). When the diode D_1 is ON, diode D_2 is OFF as shown in Figure 13(g) the blocking voltages of both the diodes are equal to 17 V which is equal to 20% of the V_o. Low voltage stress across the semiconductors (switches and diodes) allows the use of low voltage rating devices with low on-resistance, to improve the efficiency. The converter performance in dynamic conditions from Figure 13(h-i). In Figure 13(h) as the input voltage increases from 12V to 16V, the output voltage increases from 90V to 120V at a fixed duty of 0.34. In the next Figure 13(i) as the duty cycle is decreased from 0.34 to 0.3 with a fixed

TABLE 3. Hardware Specifications of the converter.

Elements	Specification
Maximum Power	200W
Input Voltage	12V/16V
Output Voltage	100 V
Switching Frequency(f_s)	20kHz
Duty Ratio	30% to 40%
Load Resistance	R=400-600 Ω
Inductors	L_1=L_2=500μH
Capacitors	C_2=100μF/63V, C_1=C_3= C_4= C_5=47μF/200V & C_O=68μF/350V
Power MOSFET	SPW52N50C3
Diodes	SF8L60USM
Gate Drivers IC	TLP250H

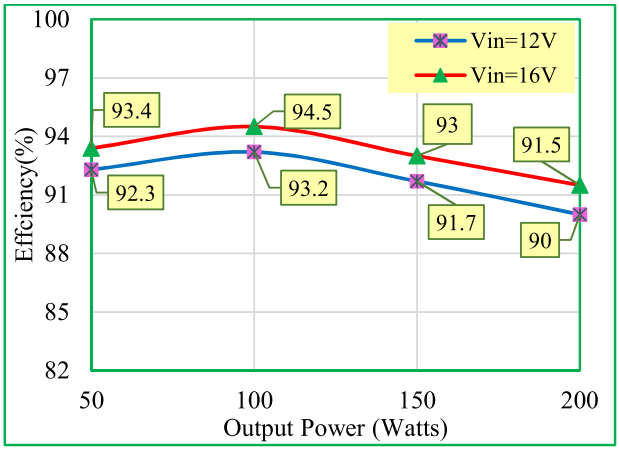

FIGURE 14. Efficiency of the NPIC Converter for different output power.

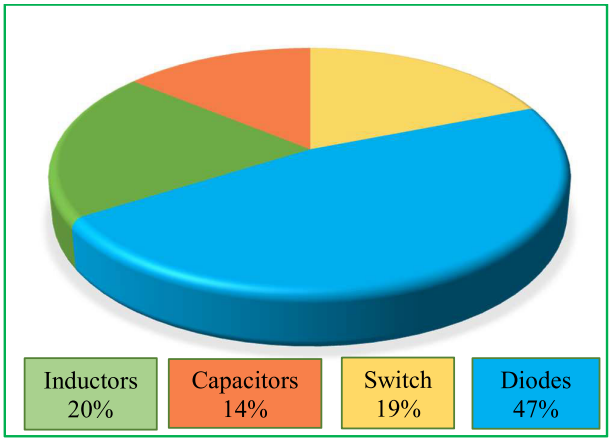

FIGURE 15. Losses in different components in the proposed converter.

input voltage of 12V, the output voltage is decreased from 90V to 82V.

The efficiency versus output power of the converter is presented in Figure 14, as the output power is increased the efficiency decreases as the current in the converter increases which results in more power loss in the converter. As the input voltage has increased the efficiency of the converter increases as seen from Figure 14. The loss bifurcation among the components is presented in Figure 15. The losses in the system are determined using PLECS software. The maximum power loss occurs in the diodes (47%) as concluded from the same figure. The losses in the switches (S_1 and S_2) is close to 19%. The total losses in inductors and capacitors are 20% and 14% respectively.

VII. CONCLUSION

In this study, a non-pulsating continuous input current step-up DC/DC converter is NPIC. The operating principle and theoretical analysis in both CCM and DCM are discussed in detail. A shared connection between the input source and the load, non-pulsating nature of the input current of the NPIC converter makes it suitable for PV applications and energy storage systems. The converter can achieve a boosting factor of 8.88 at a gate pulse of 40%. From experimental results, it is verified that the voltage stress on the semiconductor devices is less than V_o. The efficiency of the converter is high but decreases at high power output. This converter can be easily employed for applications up to 500 W. Based upon the comparative analysis of the voltage gain per devices count, the converter has a significant voltage gain(G) per device (N_L, N_S, N_D and N_C) count over similar structures. The proposed converter is suitable for low and medium power applications. In the absence of galvanic isolation, the efficiency reduces at high power levels. The targeted power level is up to 500 W without cascading the converter or using the multilevel structure. The hardware prototype of a maximum power rating of 200W was tested for power ratings for efficiency analysis and the maximum efficiency was observed to be 94.5%. It was also observed as the input voltage is decreased the efficiency gets lower at the same power rating due to more conduction losses. The converter performance under dynamic conditions was found to be good and the experimental results fit well with the theoretical results. According to the performance of the converter, the converter can be a suitable candidature for high voltage renewable energy applications and grid-tied PV systems.

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SHAHRUKH KHAN (Student Member, IEEE) is currently pursuing the B.Tech. degree with the Department of Electrical Engineering, Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University (AMU), Aligarh, India. He has published and presented research articles on power electronic dc–dc converters in international conferences and reputed journals. His research interests include the design and control of power electronic converters, interleaved converters, and maximum power point techniques algorithms. He has won the Best Paper Award in one of his proceedings. He has reviewed various proceedings in IEEE international conferences and IEEE Access journal. He is the Honorary Secretary of IEEE Student Branch, AMU, for the session 2021–2022.

MOHAMMAD ZAID (Member, IEEE) received the degree and master's degree from the Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University (AMU), Aligarh, India. He is currently working as an Assistant Professor with the Department of Electrical Engineering, ZHCET, AMU. He is also a Branch Counselor of the IEEE Student Branch of the College. He has published research articles in the fields of dc/dc converters, multilevel inverters, and DG placement. His current research interest includes developing new topologies of high-gain dc/dc converters for renewable energy applications.

MOHAMMAD MUKTAFI ALI KHAN received the bachelor's degree from Jamia Millia Islamia and the master's degree from Maharishi Dayanand University. From 2003 to 2013, he worked as an Electrical Design Engineer with Mabless Power Engineers Pvt. Ltd. Since 2015, he has been working as a Technical Assistant with the Department of Electrical Engineering, Aligarh Muslim University. He has published research articles on Flyback dc–dc converter and fuzzy logic controller. He is currently working on regenerative braking system for electric vehicles and multilevel inverter.

ADIL SARWAR (Senior Member, IEEE) received the B.Tech., M.Tech., and Ph.D. degrees from Aligarh Muslim University, Aligarh, India, in 2006, 2008, and 2012, respectively. From 2012 to 2015, he was associated with the Electrical Engineering Department, Galgotia College of Engineering and Technology, Greater Noida, India. Since 2015, he has been working with the Department of Electrical Engineering, Aligarh Muslim University. He has published more than 50 research papers in international journals and conferences. He is also working on world-bank sponsored research projects. He is a Life Member of the Systems Society of India. He has contributed a chapter in *Power Electronics Handbook* (4ed. Edited by M. H. Rashid).