

Design of Drain-Extended MOS Devices Using RESURF Techniques for High Switching Performance and Avalanche Reliability

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ABSTRACT The drift region of conventional drain extended NMOS (DeNMOS_C) is engineered to reduce gate charge for high performance and to enhance avalanche ruggedness for reliability in switching applications. Reduced-surface-field (RESURF) techniques, including surface implant (P-Top), split-gate (SG), and shallow trench isolation (STI), with an optimum doping implant of the drift region, are presented to improve the on-state safe operating area (SOA) and hot carrier stress (HCS) reliability of DeNMOS after the gate charge reduction. It is shown that under unclamped inductive switching (UIS) conditions, the avalanche ruggedness of optimized devices is improved, whereas DeNMOS_C shows high susceptibility towards thermal runaway and device failure due to electrothermal effects. Switching performance shows a reduction of up to 46% in total gate charge (Q_g) and more than 65% in gate-to-drain coupling charge (Q_{gd}). Moreover, the highest improvement achieved in switching delay is 34%. The high-frequency figure of merits such as FoM1 ($R_{ON} \times Q_{gd}$) and FoM2 ($R_{ON} \times Q_g$) show significant improvement of up to 65% and 35%, respectively. The tradeoff in the DC figure of merits FoM3 (V_{BD}/R_{ON}) and Baliga-FoM (V_{BD}^2/R_{ON}) are also analyzed. Comparative analysis of optimized DeNMOS structures indicates that split gate DeNMOS without STI shows a minimum degradation of DC performance and the most significant improvement in high-frequency performance and switching reliability.

INDEX TERMS Drain extended NMOS (DeNMOS), figure of merit (FoM), gate charge (Q_g), gate-to-drain charge (Q_{gd}), reduced-surface-field (RESURF), switching performance, switching reliability.

I. INTRODUCTION

Drain Extended MOSFET (DeMOS) is extensively used as a high voltage device in SoC and integrated circuit designs. It finds application in interface and I/O circuit design due to its high voltage blocking capability and integration with advanced CMOS processes [1]–[4]. The analytical study of CMOS compatible reduced-surface-field (RESURF) based STI DeNMOS and configurations of high-voltage devices using standard 5V CMOS technology are presented in [1] and [2], respectively. Applications of DeNMOS in CMOS level shifter [3] and RFIC [4] require high voltage capability and high-speed transient switching characteristics. For switching performance analysis, a power device gate charge (Q_g) is an industry-standard metric. A low gate charge value

gives high switching performance by reducing switching loss and delay. Multiple gate charge optimization techniques for lateral power MOSFETs are discussed earlier [5]–[10]. Polysilicon gate layout and doping optimization to reduce total gate charge (Q_g) and gate-to-drain coupling charge (Q_{gd}) are discussed in [5]–[7]. In recent works, super-junction and split gate topology achieved a superior trade-off in on-resistance and Q_g [8]. Schottky contact [9] and low-k dielectric in trench gate MOSFET [10] significantly improved the switching figure of merit and dynamic performance by reducing the gate charge.

This work shows that the presence of a long gate-to-drain overlap length in conventional drain extended NMOS (DeNMOS_C) results in a significant rise of Q_g and Q_{gd} . However, in the absence of gate-to-drain overlap, a suitable RESURF technique should be applied to improve the on-state safe operating area (SOA). Earlier work on lateral power

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devices used RESURF based drift region engineering for an improved tradeoff between on-resistance (R_{ON}) and off-state breakdown voltage (V_{BD}) [11]–[13]. For example, a super-junction with a trench oxide layer achieved high V_{BD} by modulating the bulk electric field and low R_{ON} by creating a path for the electron current in a forward conduction state [14]. Similarly, field-shaping methods and the role of drift parameters to improve R_{ON} and V_{BD} are discussed in [15]–[17].

This work investigates multiple RESURF techniques such as the surface implant, split-gate, and shallow trench isolation (STI) in the drift region to ensure on-state SOA remains the same after the gate charge reduction. DeNMOS with the RESURF implant can significantly improve the breakdown voltage by reducing the surface field and is reported widely [18]–[20]. Application of the grounded field plate is another widely used RESURF technique. Source connected split-gate over the drift region act as a field plate to modulate the surface field [21], [22]. STI placed below the gate edge acts as RESURF to modulate the surface field and improve the gate oxide reliability [23]. STI enhances the gate edge reliability by shifting the peak electric field into the trench [24], [25].

Transient switching reliability becomes critical when these devices turn off from on-state under unclamped inductive switching (UIS) conditions. Electrothermal analysis for the unified study of SOA and UIS behavior of LDMOS was reported earlier [26]. We present a detailed investigation of the switching avalanche reliability of optimized DeNMOS structures using electrothermal simulations to explain the time evolution of bipolar triggering, space charge modulation, and lattice heating. Simulation results show that DeNMOS with lower avalanche ruggedness experience self-heating induced bipolar triggering and space charge modulation, resulting in current crowding and device failure due to increased lattice temperature. It is also shown that optimized devices achieved higher avalanche ruggedness than DeNMOS_C, thereby improving the device reliability in switching applications.

In this paper, section II presents different DeNMOS structures using various RESURF techniques and their simulation setup. Then, section III discusses the gate charge optimized DeNMOS design steps using drift region layout and doping optimization. Finally, we present an analysis of avalanche behavior and switching performance for all the optimized DeNMOS in section IV, followed by a conclusion in section V.

II. DeNMOS STRUCTURE AND SIMULATION SETUP

This work uses a well-calibrated process file to simulate the conventional DeNMOS (DeNMOS_C) using triple well CMOS process technology, shown in Fig. 1(a). The structure comprises an extended lightly doped drain known as the N-drift region with a gate-to-drain overlap length (L_{OV}) of 200 nm to modulate the surface field. It has a gate oxide of ~ 2 nm and uses n-well and p-well in the standard CMOS process as N-drift and P-body regions. The junction of P-body

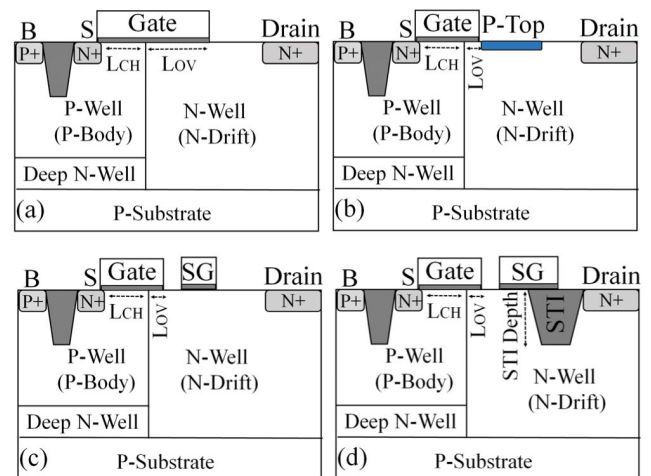


FIGURE 1. DeNMOS structures (a) Conventional (DeNMOS_C) (b) with P type surface implant near gate edge (P-Top) (c) with Split gate (SG) without STI (SG_NonSTI) (d) with Split gate and STI of varying depths: 150 nm (SG_STI_150), 250 nm (SG_STI_250) and 350 nm (SG_STI_350). Source-to-drain pitch of all the structures are same. B is Body and S refers to Source contact.

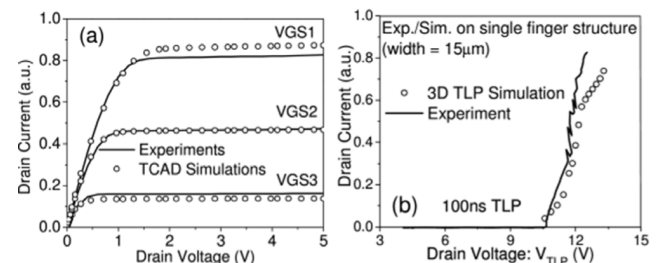


FIGURE 2. Calibration of models used in TCAD simulations for DeNMOS devices (a) I-V characteristics (b) breakdown behavior [11].

and N-drift is the edge of intrinsic MOS with a channel length (L_{CH}) of 200 nm. Fig. 2 shows the calibration of DeNMOS_C [11]. The DeNMOS_C structure is further modified using different RESURF techniques in the drift region, and its L_{OV} is scaled to 50 nm to reduce its gate length. The DeNMOS designs shown in Figs. 1(a)–1(d) have the same source to drain pitch, L_{CH} , and other layout parameters except for drift regions. Modified DeNMOS with different drift region designs has been investigated and compared with the DeNMOS_C.

Table 1 lists various DeNMOS drift region layout designs for different RESURF techniques used in this work. In extended-gate DeNMOS_C, a strong gate-to-drain coupling results in the degradation of switching performance. Hence, L_{OV} is reduced to 50 nm to enhance switching performance. P-Top DeNMOS shown in Fig. 1(b) uses a P-type pocket with optimum doping and dimension near the gate edge. Surface implant using a P-type pocket near the gate edge is an effective RESURF technique. However, the presence of P-Top can significantly degrade R_{ON} . Source connected split-gate (SG) DeNMOS labeled as SG_NonSTI is shown in Fig. 1(c), ensures RESURF at high drain voltage, while R_{ON} degradation is minimal at low drain voltage.

TABLE 1. DeNMOS structures parameters and layout.

Device	L_{OV} (nm)	Drift Region Layout Design
DeNMOS_C	200	Extended gate over drift region
P-Top	50	P type pocket near gate edge
SG_NonSTI	50	Split gate (SG) without STI
SG_STI_150	50	SG with STI of depth 150 nm
SG_STI_250	50	SG with STI of depth 250 nm
SG_STI_350	50	SG with STI of depth 350 nm

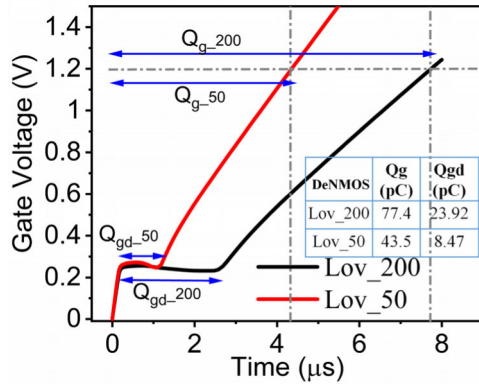


FIGURE 3. Gate charge waveform i.e., gate voltage versus time plot when a constant current (10 μ A) forced into the gate electrode at a drain voltage of 5 V [6] is plotted for the conventional DeNMOS with $L_{OV} = 200$ nm and gate scaled DeNMOS with $L_{OV} = 50$ nm.

SG_NonSTI has a source connected SG of 100 nm length considering high field effects near the SG edge. The distance between the active gate edge and SG is critical, and hence an optimum value is chosen without influencing the static characteristics [27]. Fig. 1(d) shows SG_STI DeNMOS with STI to suppress high field-effect near the SG edge. SG length was extended from 100 nm to 250 nm to sufficiently overlap over the STI region. Furthermore, we also varied the STI depth as 150 nm, 250 nm, and 350 nm to study its impact on device performance. All 2-D device simulations in this work are performed using the Sentaurus Device TCAD simulator [28].

The hydrodynamic carrier transport model is used to perform electrical simulations. Shockley-Read-Hall and Auger recombination models are included considering carrier generation-recombination. In addition, doping-dependent mobility models, high-field mobility saturation, and interface field-induced mobility degradation models are used for the simulation. Finally, the dynamic avalanche ruggedness of all the DeNMOS structures is compared using electrothermal simulations under unclamped inductive switching.

III. DeNMOS DESIGN AND OPTIMIZATION

A. IMPACT OF GATE CHARGE OPTIMIZATION

Reduction of gate length and gate to drain coupling can minimize DeNMOS gate charges Q_g and Q_{gd} . The gate charge waveforms shown in Fig. 3 show that scaling the L_{OV} for conventional DeNMOS from 200 nm to 50 nm can reduce Q_g and Q_{gd} by more than 40% and 60%, respectively. This

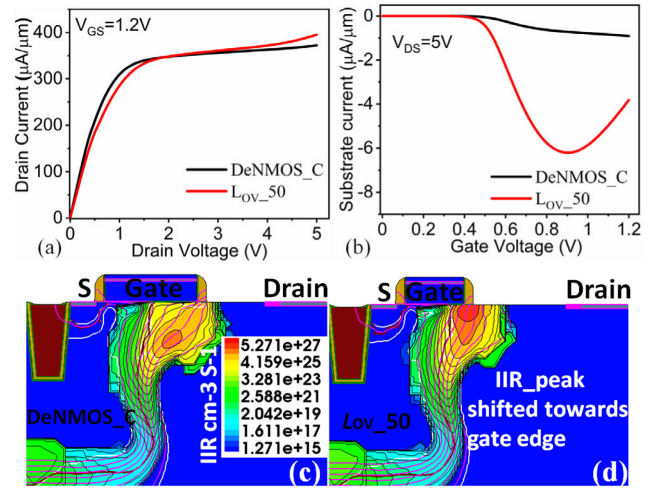


FIGURE 4. Comparison of DeNMOS_C ($L_{OV} = 200$ nm) and gate overlap length scaled DeNMOS ($L_{OV} = 50$ nm) (a) Output characteristic (b) Substrate current variation with gate voltage. Impact ionization rate (IIR) contour plot with potential lines for (c) DeNMOS_C (d) L_{OV_50} , at $V_{GS} = 1.2V$ and $V_{DS} = 5V$.

significant reduction of Q_g and Q_{gd} can enhance device switching speed and reduce switching losses [6]. However, scaling the L_{OV} degrades device R_{ON} , output resistance (R_{OUT}), on-state SOA, and hot carrier stress (HCS) reliability due to high avalanche generation at P-body/N-drift junction near gate edge. The absence of the extended gate field plate effect, which can disperse the surface potential lines, gives such design challenges. After L_{OV} scaling, L_{OV_50} DeNMOS in Fig. 4(a) shows a step increase in drain current at high drain voltage, which degrades on-state SOA. Furthermore, a high substrate current peak in L_{OV_50} DeNMOS [Fig. 4(b)] results in substrate current induced body effect (SCBE) [29], which is responsible for the rise of drain current in the saturation region. From Figs. 4(c) and 4(d), it is observed that increased potential line crowding results in a high field-effect near the gate edge in the absence of an extended gate. A high electric field near the gate edge increases the impact ionization rate (IIR) near the Si/SiO₂ interface in L_{OV_50} , reducing gate oxide reliability. Hence, there is a need to re-engineer the drift region of L_{OV_50} DeNMOS to enhance device SOA and reliability without compromising device transient switching performance.

B. DRIFT REGION LAYOUT OPTIMIZATION

As discussed in the previous section, the drift region surface experiences potential line crowding when the extended gate length (L_{OV}) is scaled from 200 nm to 50 nm [see L_{OV_50} in Fig. 4(d)]. L_{OV} scaling thus degrades on-state SOA because of high IIR near the gate edge. The presence of an extended gate in DeNMOS_C can effectively modulate the surface potential lines and suppress peak IIR by shifting its location away from the surface into the bulk. The extended gate generates a uniformly distributed vertical field that overlaps with the lateral field at high drain voltage and helps in modulating the surface field [18]. As shown in Figs. 5(a)-5(b), an increase

in gate overlap reduces the surface electric field near the P-body/N-drift junction. Moreover, depletion of the extended gate edge shifts the current path from the surface into the bulk, as shown in Fig. 5(d), while L_{OV_50} [Fig. 5(c)] shows high surface current density. In conjunction with reduced surface current density, the modulated electric field lowers the IIR near the gate edge and shifts peak IIR into the bulk [Fig. 4(c)], thereby improving on-state SOA [Fig. 4(a)].

Implementation of RESURF techniques like P-Top, split gate, and STI can modulate the surface field to reduce IIR and improve on-state SOA after L_{OV} scaling. Figs. 6(a)-6(f) shows the IIR contour plots for DeNMOS_C and layout-optimized devices. Like DeNMOS_C, layout-optimized devices after L_{OV} scaling can effectively suppress IIR and shift its peak away from the surface. Fig. 6(b) shows P-Top DeNMOS with a surface implant near the gate edge. Inserting a P-type region near the gate edge over the silicon surface can cut the lateral electric field and spread the surface potential lines near the gate edge, which helps in mitigating surface IIR. Dimension, doping, and location of P-Top are instrumental in defining the electric field profile within the drift region [20]. SG_NonSTI in Fig. 6(c) uses a source-connected split-gate (SG) to exert the field plate effect over the drift region and can effectively modulate the surface field. However, the edge of both the active gate and SG is prone to high field-effect due to potential line crowding, resulting in high IIR near the active gate edge. Therefore, the length of the split gate and its distance from the active gate should be minimum according to device technology specifications. Figs. 6(d)-6(f) shows the IIR plot for all the DeNMOS structures with the split gate and STI of different depths. STI with a low dielectric constant material like SiO_2 increases the potential drop in the drift region, which thus improves the P-body/N-drift junction breakdown voltage and gate oxide reliability near the gate edge. In SG_STI_150 [Fig. 6(d)], smaller STI depth raises the electric field near the STI edge towards the source, leading to IIR near the STI edge. An increase in STI depth relaxes the electric field at the STI/N-drift interface, reducing the IIR near the STI sidewall, as indicated in Figs. 6(e)-6(f). Drift region engineering using various RESURF techniques thus enhances SOA for all layout optimized devices as shown in output characteristics in Fig. 6(g), while charge accumulation is also greatly reduced after gate-to-drain overlap length scaling, which thus improves the switching performance.

C. DRIFT REGION DOPING OPTIMIZATION

RESURF techniques to engineer drift regions can effectively enhance on-state SOA after L_{OV} scaling, as discussed in the previous section. However, the high field at the active gate edge increases IIR near the P-body/N-drift junction after RESURF optimization. The rise of IIR near the P-body/N-drift junction results in the generation of the hot carriers near the intrinsic MOS channel edge, which degrades long-term reliability due to HCS [21], [24]. Therefore, drift region doping is optimized for each structure to reduce the

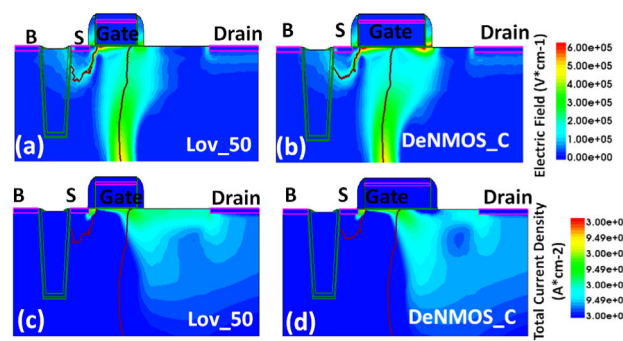


FIGURE 5. Electrical field distribution for (a) L_{OV_50} (b) DeNMOS_C, and Total current density distribution of (c) L_{OV_50} (d) DeNMOS_C, at $V_{DS} = 5 \text{ V}$ and $V_{GS} = 1.2 \text{ V}$.

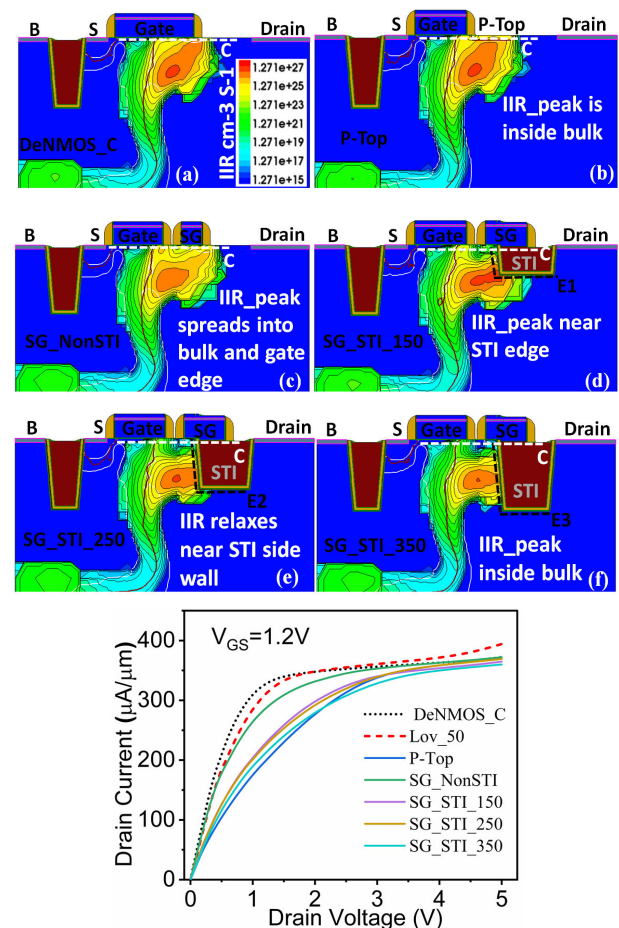


FIGURE 6. Contour plot of Impact Ionization rate (IIR) ($\text{cm}^{-3}\text{s}^{-1}$) and its peak location at $V_{DS} = 5 \text{ V}$ and $V_{GS} = 1.2 \text{ V}$ for (a) DeNMOS_C (b) P-Top (c) Split Gate NonSTI (SG_NonSTI), SG_STI with different STI depths (d) SG_STI_150, (e) SG_STI_250, (f) SG_STI_350. (g) Output characteristics showing improvement in SOA after layout optimization.

IIR at Si/SiO₂ interface near the P-body/N-drift junction and STI sidewall. Dose (D) and energy (E) of doping implants are analyzed to optimize the net charge within the drift region. Figs. 7(a)-7(h) shows the IIR plot near Si/SiO₂ interface across cutline C, E1, E2, and E3 depicted in Fig. 6. E1, E2, and E3 cutline correspond to the Si/SiO₂ interface at the

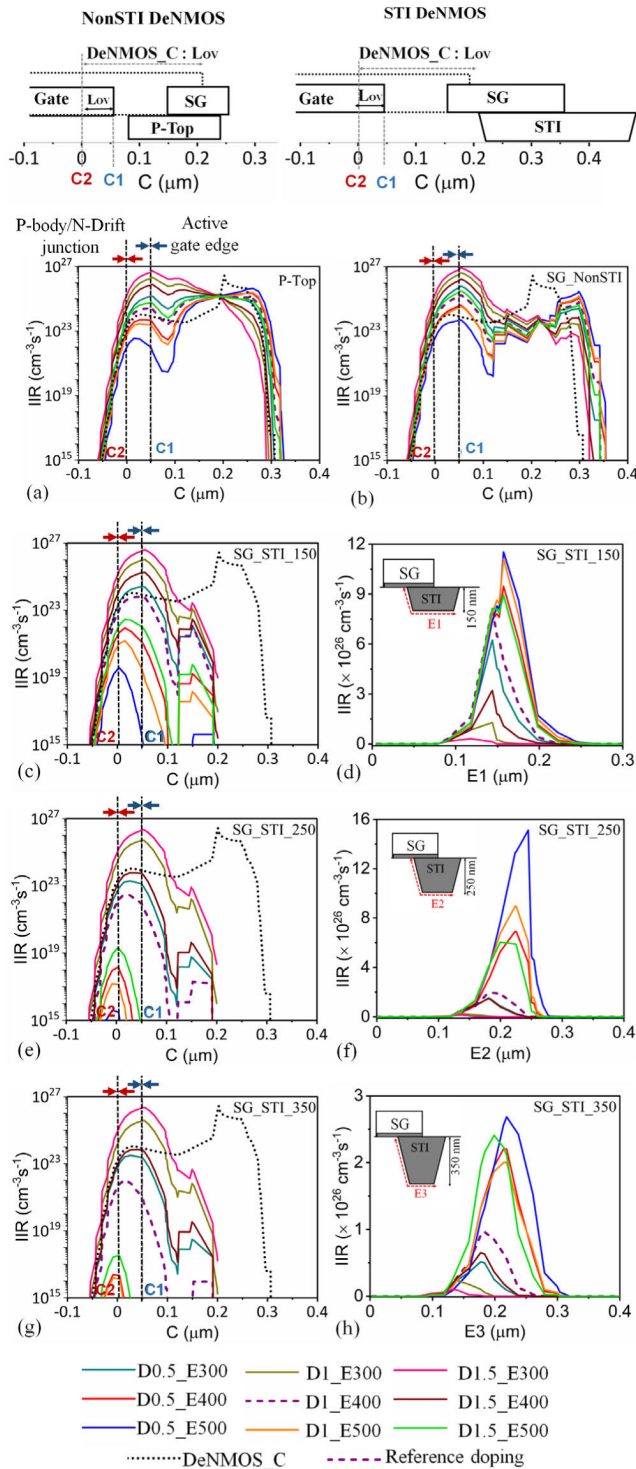


FIGURE 7. Impact Ionization Rate (IIR) near lateral Si/SiO₂ interface across cutline C (refer to Fig. 6) for (a) P-Top (b) SG_NonSTI (c) SG_STI_150 (e) SG_STI_250 and (g) SG_STI_350. IIR near slanted Si/SiO₂ interface across cutline (d) E1 for SG_STI_150, (f) E2 for SG_STI_250 and (h) E3 for SG_STI_350. Drift region doping dose and energy are varied such that, Dose (D) is 0.5×10^{13} , 1×10^{13} , and 1.5×10^{13} in cm^{-2} and Energy (E) is 300, 400 and 500 in KeV. Reference doping dose is $1 \times 10^{13} \text{ cm}^{-2}$ and energy is 400 KeV (labelled as D1_E400). All curves are plotted at DC bias of $V_{DS} = 5 \text{ V}$ $V_{GS} = 1.2 \text{ V}$. Surface IIR rate for all the cases is compared with DeNMOS_C. Location of split gate, P-Top and STI with respect to cutline is indicated at top for NonSTI and STI DeNMOS devices.

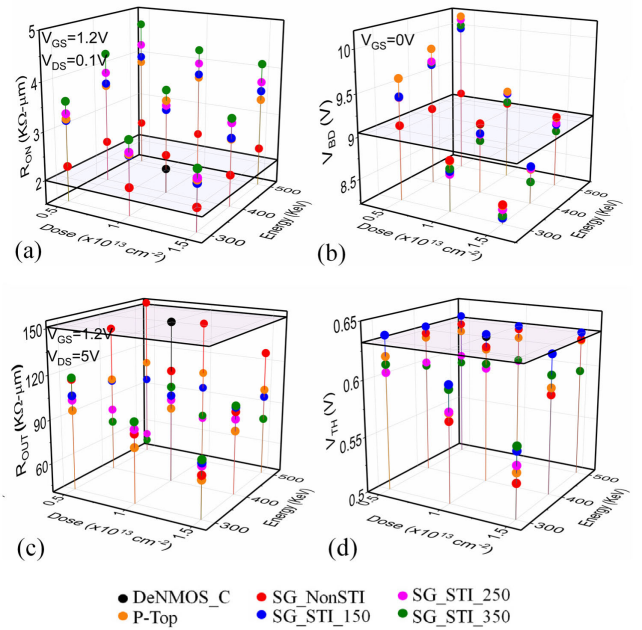


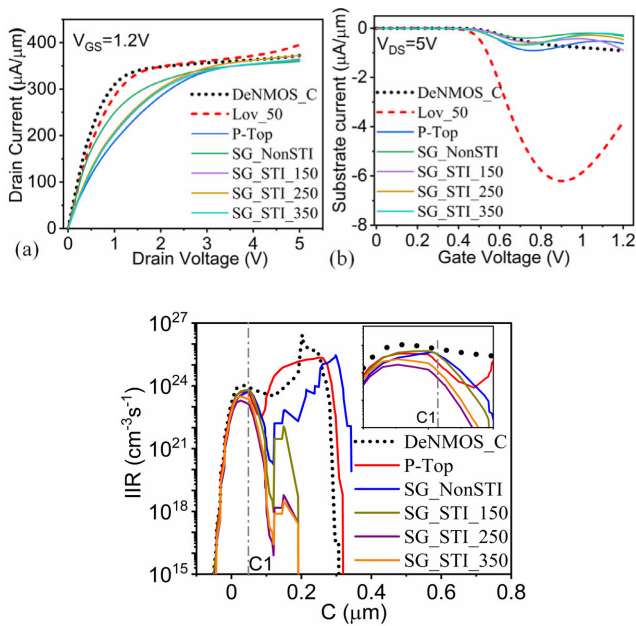
FIGURE 8. DC electrical characteristics of all the DeNMOS structure for different combinations of drift region implants doping dose and energy (a) ON resistance (b) OFF state breakdown voltage (c) Output Resistance (d) Threshold voltage. Reference doping for all layout modified DeNMOS is same as DeNMOS_C doping and corresponds to a doping dose of $1 \times 10^{13} \text{ cm}^{-2}$ and energy of 400 KeV (D1_E400).

STI sidewall, whereas C is the surface cutline representing Si/SiO₂ below the gate. Drift region doping of the DeNMOS_C is taken as the reference and labeled as D1_E400 for implantation dose (D) of $1 \times 10^{13} \text{ cm}^{-2}$ and energy (E) of 400 KeV. A decrease in doping dose and increase of doping energy (e.g., D0.5_E500) reduces the net doping of the drift region. Reduction of the drift region doping decreases IIR near the P-body/N-drift junction and increases it near the drain [Figs. 7(a)-7(b)]. Similarly, in STI-based DeNMOS, reduction in doping reduces surface IIR and increases peak IIR inside the bulk near the STI wall [Figs. 7(c)-7(h)].

The impact of the drift region doping dose and energy on DC electrical parameters for all the devices is shown in Figs. 8(a)-8(d). A horizontal reference cut-plane depicts R_{ON} , R_{OUT} , V_{BD} , and threshold voltage (V_{TH}) of the DeNMOS_C. From Fig. 8(a), all the modified DeNMOS structures have higher R_{ON} than DeNMOS_C as surface charge accumulation is reduced due to L_{OV} scaling. In Fig. 8(b), off-state breakdown voltage characteristics show that drift region layout and doping optimization have little impact on device V_{BD} , which varies within the acceptable range of 8V to 10V. Output resistance (R_{OUT}) is defined as the reciprocal of the slope of drain current at a given bias condition in output characteristics. A high value of R_{OUT} indicates that the saturation current is less dependent on the drain voltage. All the optimized structures show a reduction in R_{OUT} except for SG_NonSTI, as shown in Fig. 8(c). Optimum doping corresponding to each structure is selected such that the IIR remains smaller

TABLE 2. DC parameters of DeNMOS after layout and doping optimization.

Device	Dose-Energy	R_{ON} (K Ω - μ m)	V_{BD} (V)	R_{OUT} (K Ω - μ m)	V_{TH} (V)
DeNMOS_C	Reference	2.02	9.05	151	0.63
P-Top	D0.5 E400	3.59	8.93	106	0.63
SG_NonSTI	D0.5 E500	2.42	9.18	154	0.63
SG_STI_150	D1 E400	3.28	8.64	101	0.63
SG_STI_250	D0.5 E300	3.33	8.71	102	0.61
SG_STI_350	D0.5 E300	3.58	9.87	118	0.61

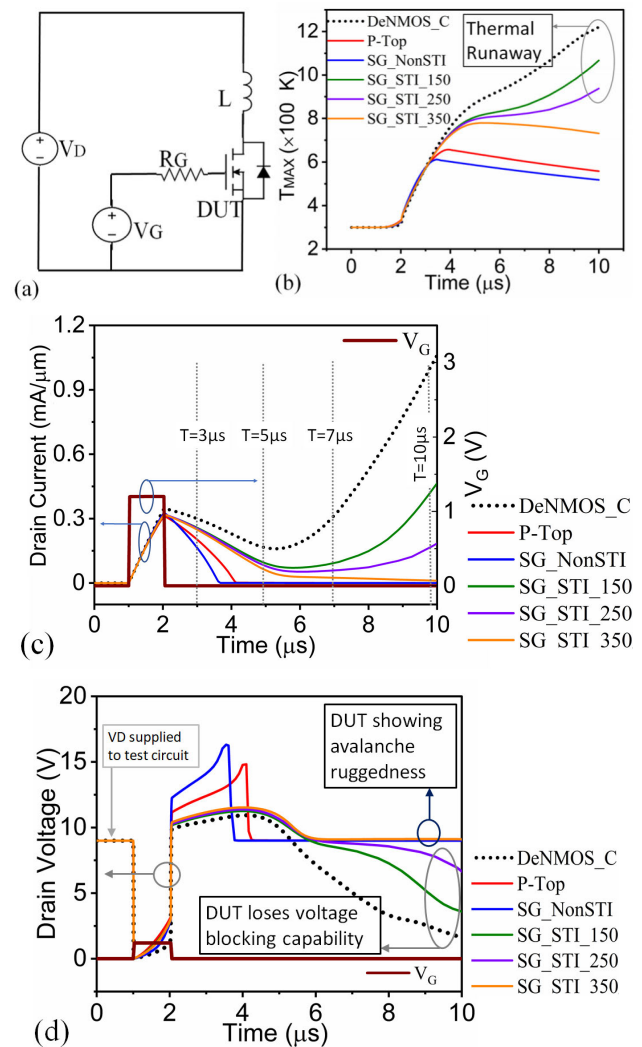
**FIGURE 9. Plots comparing optimized DeNMOS structures for (a) Output characteristics (b) Substrate current (c) Impact ionization rate (IIR) (corresponding cutlines C as shown in Fig. 6), at a DC bias of $V_{DS} = 5$ V and $V_{GS} = 1.2$ V.**

than that of DeNMOS_C at Si/SiO₂ interface near P-body/N-drift junction, and the tradeoff in DC parameters is minimum. Table 2 shows the selected doping dose and energy corresponding to each DeNMOS structure and its DC parameters.

IV. SIMULATION RESULTS AND COMPARISON

A. AVALANCHE BEHAVIOUR ANALYSIS

DC characteristics of all the optimized DeNMOS structures are compared and shown in Figs. 9(a)-9(c). Doping optimized devices show similar on-state SOA as layout optimized devices with a slight variation in R_{ON} , as shown in output characteristics in Fig. 9(a). Substrate current responsible for the substrate current induced bias effect (SCBE) at high drain voltage is suppressed for all the optimized devices, as shown in Fig. 9(b). IIR for all the devices is plotted across cutline C (Fig. 6), near the Si/SiO₂ interface, as shown in Fig. 9(c). IIR at the active gate edge (C1) is reduced for all the selected optimized structures compared to DeNMOS_C. Lower IIR near P-body/N-drift junction improves HCS reliability near the intrinsic MOS channel edge. After L_{OV}

**FIGURE 10. (a) Test circuit for Unclamped Inductive Switching (UIS) waveforms for (b) Maximum junction temperature (c) Drain current and (d) Drain voltage when device is turned OFF from ON state.**

scaling, implementation of drift region optimization techniques resulted in the desired on-state SOA and increased HCS reliability.

The dynamic avalanche reliability of all the DeNMOS structures under unclamped inductive switching (UIS) conditions is analyzed using electrothermal 2-D TCAD simulations [30]. Figs. 10(a)-10(d) shows the UIS test circuit and its corresponding waveforms. The gate electrode receives a 1.2V pulse of finite duration, and V_D is provided with a voltage close to the breakdown voltage of DUT. During the on-state of DUT, the drain current is ramped up as a function of supply voltage V_D and load inductor L . Drain current reaches its peak when the DUT is turned off, as shown in Fig. 10(c). In the absence of a freewheeling diode across inductor L , the inductor current starts discharging through the internal body diode of DUT as there is no inversion channel in the absence of gate supply. Fig. 10(d) shows an abrupt rise of drain voltage for devices with higher avalanche ruggedness.

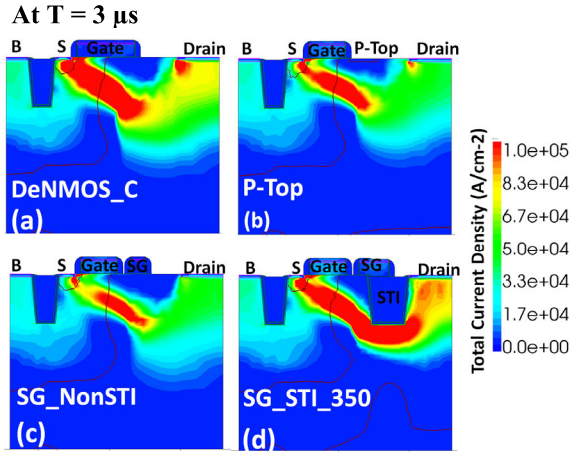


FIGURE 11. Presence of strong parasitic NPN BJT at $T=3 \mu s$ in (a) DeNMOS_C (b) P-Top (c) SG_NonSTI (d) SG_STI_350.

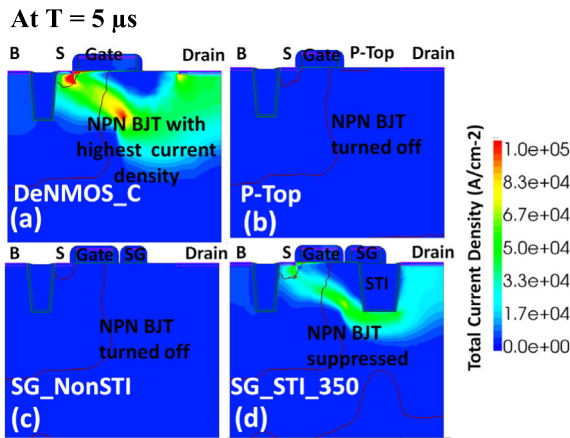


FIGURE 12. Suppression of parasitic NPN BJT at $T=5 \mu s$ in (a) DeNMOS_C (b) P-Top (c) SG_NonSTI (d) SG_STI_350.

In contrast, DUTs with low avalanche ruggedness lose their voltage blocking capability and an exponential rise of drain current [Fig. 10(c)] and lattice temperature [Fig. 10(b)] is observed with time.

DeNMOS_C shows the highest susceptibility towards thermal runaway [Fig. 10(b)] and eventually device failure at a given UIS condition. The thermal runaway at longer times corresponds to an exponential rise of temperature and results in device failure due to excessive heating. P-Top, SG_NonSTI, and SG_STI_350 show avalanche reliability with reduced lattice heating, whereas junction temperature rises for SG_STI_150 and SG_STI_250. The exponential rise in temperature is due to current crowding and filamentation near the drain after space charge modulation [31]. To demonstrate how different physical behavior like parasitic NPN BJT triggering and lattice heating of DUT evolve with time under UIS conditions, we investigate contour plots of DeNMOS_C, P-Top, SG_NonSTI, and SG_STI_350 to explain the dynamics of parasitic NPN BJT triggering and thermal runaway.

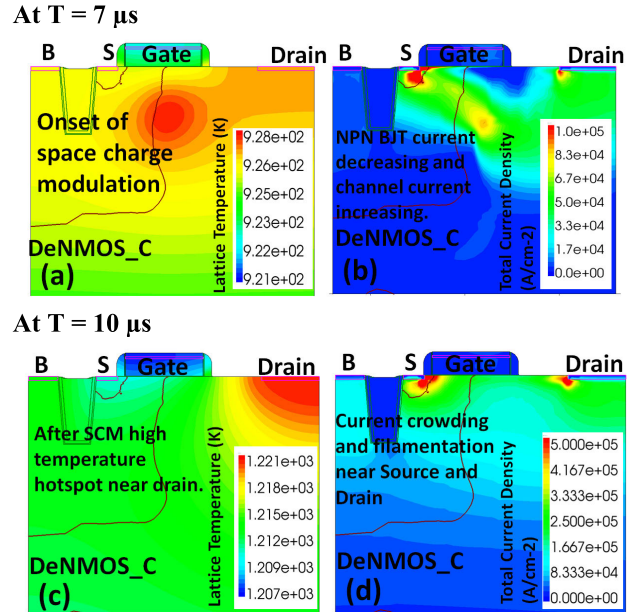


FIGURE 13. Shift of high temperature hot-spot from P/N junction towards drain of DeNMOS_C in (a) and (c). (b) Current density of parasitic NPN BJT and (d) High current density due to current crowding and filamentation.

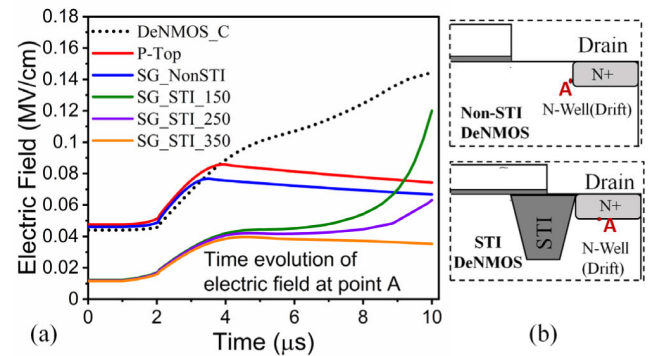


FIGURE 14. (a) Evolution of electric field near drain diffusion at point A (N+/N-well interface). (b) Location of point A in NonSTI (DeNMOS_C, P-Top, SG_NonSTI) and STI (SG_STI_150, SG_STI_250, SG_STI_350) devices.

1) DYNAMICS OF BIPOLAR TRIGGERING

After the DUT is turned off, its drain voltage rises to support the large drain current, as shown in Fig. 10(d). High drain voltage results in avalanche-generated holes within the DUT, which lowers the barrier across the source substrate junction and triggers parasitic NPN BJT. From Figs. 11(a)-11(d), it is observed that strong bipolar is present in all the devices at time $T=3 \mu s$ [Fig. 10(c)]. However, at time $T=5 \mu s$ [Fig. 10(c)] parasitic bipolar of SG_NonSTI and P-Top is entirely switched off, while SG_STI_350 shows a weaker parasitic bipolar effect than DeNMOS_C [Figs. 12(a)-12(d)]. The delay in avalanche degradation is responsible for a large parasitic bipolar current at longer times. An increase of avalanche degradation time raises the lattice temperature, and hence we observe the highest junction temperature in the case of DeNMOS_C [Fig. 10(b)].

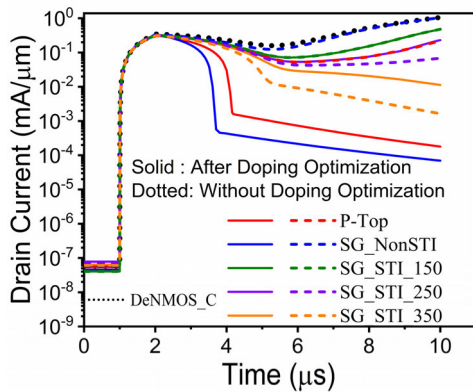


FIGURE 15. Comparison of UIS waveform drain current for RESURF optimized DeNMOS structures with and without doping optimization.

2) DYNAMICS OF THERMAL RUNAWAY

Devices DeNMOS_C, SG_STI_150, and SG_STI_250 show a thermal runaway, whereas the maximum junction temperature of P-Top, SG_NonSTI, and SG_STI_350 starts decreasing at longer times, as shown in Fig. 10(b). The exponential rise of lattice temperature with time due to space charge modulation and subsequent current filamentation is explained using DeNMOS_C, as shown in Figs. 13(a)-13(d). The NPN BJT of DeNMOS_C is weaker at $T=7 \mu s$ [Fig. 13(b)] compared to time $T=5 \mu s$ [Fig. 12(a)]. However, the drain current of DeNMOS_C is increasing at $T=7 \mu s$ [Fig. 10(c)] instead of decreasing with a reduced current density of NPN BJT [Fig. 13(b)]. The rise of the DeNMOS_C drain current after $T=5 \mu s$ results from lattice heating-induced threshold voltage degradation, which turns on the MOS channel. High drain current eventually results in space charge modulation [Fig. 13(a)], which starts shifting peak electric field and lattice temperature hotspots towards the drain [Fig. 13(c)]. The electric field near drain diffusion (location A at N^+/N -well interface shown in Fig. 14(b)) is plotted for all the devices in Fig. 14(a). The rise of the electric field at point A results in avalanche generation of holes which triggers parasitic NPN BJT again, hence for DeNMOS_C, SG_STI_150, and SG_STI_250, NPN regenerative feedback mechanism is observed. Eventually, the rise of lattice temperature and an electric field near drain diffusion results in an exponential rise of drain current, and at $T=10 \mu s$ non-uniform current distribution results in current filamentation near both source and drain [Fig. 13(d)] [31].

It should be noted that drift region layout optimization can improve the switching performance by reducing the gate charge. However, doping optimization plays a significant role in improving avalanche reliability in DC and transient conditions. From Fig. 15, we observe that P-Top and SG_NonSTI avalanche ruggedness is low, and their drain current increases exponentially without doping optimization. Whereas the presence of STI has improved turn-off avalanche reliability when compared to DeNMOS_C. The presence of STI suppresses the IIR, which reduces the avalanche degradation time and improves the avalanche ruggedness.

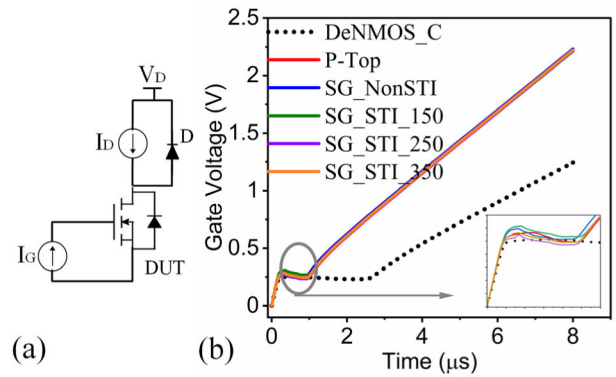


FIGURE 16. (a) Test circuit to calculate the gate charge (b) Gate charge waveform of all the DeNMOS after drift region optimization when a constant current of $10 \mu A$ forced into gate electrode at $V_D = 5 V$.

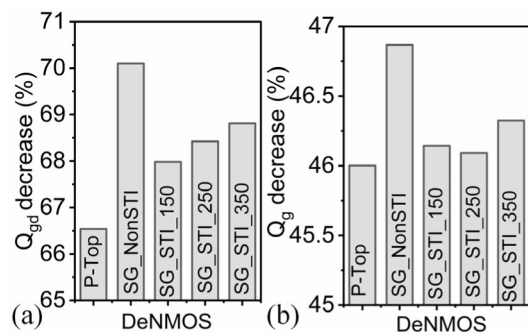


FIGURE 17. Percentage reduction in (a) Gate to drain coupling charge Q_{gd} (b) Total gate charge Q_g , with respect to Q_{gd} and Q_g of DeNMOS_C.

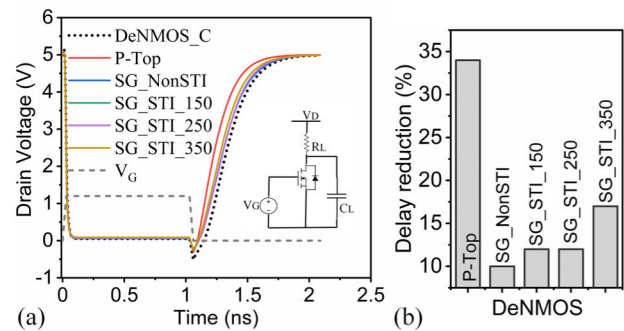


FIGURE 18. (a) Switching delay waveform for inverter circuit shown in inset (b) Percentage reduction in switching delay of optimized devices.

After doping optimization, reduction in doping dose and increased doping energy enhanced the avalanche reliability of P-Top and SG_NonSTI, whereas the reduction of doping energy lowered the same for SG_STI_250 and SG_STI_350.

B. SWITCHING PERFORMANCE ANALYSIS

Gate charge is a critical parameter that evaluates the switching speed and losses of the transistor. The gate charge characteristics [6] are simulated using the test circuit depicted in Fig. 16(a). The simulation uses 10^4 cells connected in

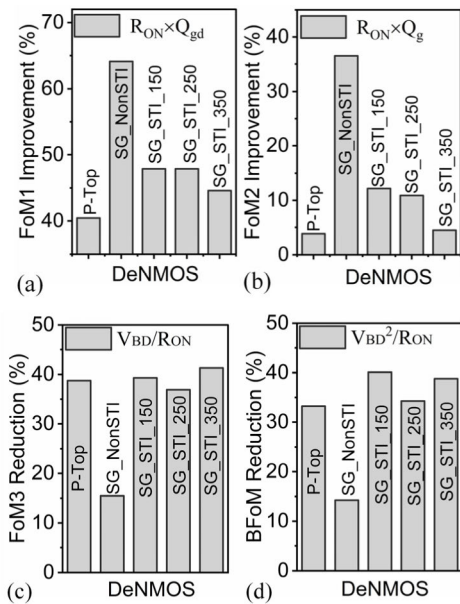


FIGURE 19. Percentage improvement in (a) $FoM1 = R_{ON} \times Q_{gd}$ (b) $FoM2 = R_{ON} \times Q_g$ and Percentage reduction of (c) $FoM3 = V_{BD}/R_{ON}$ (d) Baliga FoM (BFoM) = V_{BD}^2/R_{ON} , with respect to DeNMOS_C.

parallel and a 10 μ A current source connected to the gate. In Fig. 16(b), the gate charge waveform shows a significant reduction of Q_g and Q_{gd} for all optimized devices compared to DeNMOS_C. Q_g is the total gate current multiplied by charging time at $V_{GS} = 1.2V$, while Q_{gd} corresponds to the product of total gate current and period for which gate voltage remains constant in Fig. 16(b) [32]. The SG_NonSTI has the lowest Q_{gd} (7.14 pC), which is a reduction of more than 70% compared to DeNMOS_C (23.88 pC), while other devices show a reduction in the range of 66.5% to 68% [Fig. 17(a)]. SG_NonSTI also shows the lowest Q_g (41.13 pC), which is 46.9% [Fig. 17(b)] reduction compared to DeNMOS_C (77 pC).

Transient switching delay waveform is plotted for all the devices using the inverter circuit shown in the inset of Fig. 18 (a). The gate is subjected to a 1.2 V voltage pulse with a rise and fall time of 100 ps. Fig. 18(a) depicts the output voltage waveform across load C_L . The switching delay has improved for all the optimized devices in the range of 10% to 34% [Fig. 18(b)], with the P-Top device showing the lowest propagation delay. The improvement in switching delay is a result of the reduced Q_g and Q_{gd} of optimized devices. P-Top gives the lowest switching delay as it has lower drain-to-source coupling than devices using a source-connected split gate.

The figure of merit (FoM) of a power device is dependent on R_{ON} , V_{BD} , Q_g , and Q_{gd} . We have calculated the high-frequency figure of merit FoM1 ($R_{ON} \times Q_{gd}$) and FoM2 ($R_{ON} \times Q_g$) for transient performance [33]. The smaller the value of FoM1 and FoM2 better will be the switching performance. FoM3 (V_{BD}/R_{ON}) and Baliga-FoM (V_{BD}^2/R_{ON}) are DC figures of merit, where the higher the value better will be device conduction efficiency [34]. With the least

R_{ON} degradation and a significant reduction in both Q_g and Q_{gd} , SG_NonSTI shows the greatest improvement in FoM1 and FoM2 [Figs. 19(a) and 19(b)]. Large R_{ON} in P-Top and STI-based DeNMOS has reduced the percentage improvement in their FoM1 and FoM2 compared to SG_NonSTI. Although an increase in R_{ON} has resulted in the degradation of FoM3 and BFoM of optimized devices [Figs. 19(c) and 19(d)], in the case of high-speed switching applications, switching losses are much higher than conduction losses. Hence, significant improvement in FoM1 and FoM2 will outperform reduction in DC figure of merits as switching performance at high-speed switching applications is greatly improved.

V. CONCLUSION

This work presents a comprehensive comparative investigation of various RESURF techniques to optimize DeNMOS_C for high performance and avalanche reliability in switching applications. The on-state SOA of the gate charge optimized DeNMOS is enhanced using RESURF, whereas doping optimization of the drift region improved on-state HCS and switching reliability of optimized structures compared to DeNMOS_C. We investigated three structures of DeNMOS: P-Top, SG_NonSTI, and SG_STI (with STI depth of 150 nm, 250 nm, and 350 nm). Electrothermal simulations under the UIS test condition show improved dynamic avalanche ruggedness and switching reliability of optimized structures compared to DeNMOS_C. Moreover, all the optimized structures showed a reduction of Q_g (46% to 46.8%), Q_{gd} (66.5% to 70%), and switching speed (10% to 34%) compared to DeNMOS_C. In addition, the high-frequency figure of merit FoM1($R_{ON} \times Q_{gd}$) shows 40% to 65% improvement, and FoM2 ($R_{ON} \times Q_g$) shows 5% to 35% improvement for optimized devices. The presence of STI has shown improvement in on-state and switching avalanche reliability, while optimized P-Top shows the lowest switching delay. Furthermore, compared to other optimized structures, SG_NonSTI shows the best FoM1, FoM2, and the lowest degradation of FoM3 (V_{BD}/R_{ON}) and Baliga-FoM (V_{BD}^2/R_{ON}) with the highest switching reliability. Thus, it can be concluded that the use of RESURF techniques and drift region doping optimization can significantly enhance the switching performance and reliability of DeNMOS while also avoiding the severe concerns of on-state SOA and HCS reliability.

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