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A Random Modulation Spread-Spectrum Digital PWM for a Low System Clock Digital Buck Converter

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ABSTRACT The need for a high-efficiency power system has emerged since many IoT devices are mainly operated by batteries. A power system with analog control can have a high control bandwidth, but it is relatively vulnerable to noise disturbances and may suffer from control problems. On the other hand, a digitally controlled power system has high reliability and great controllability at the expense of switching noise and EMI issues. To implement a digitally controlled PWM with high resolution and low EMI, this study proposes a random carrier frequency modulation with dithered duty cycle method, where wide spectrum dithering and random modulation of spread spectrum PWM are tightly integrated. The proposed system was not only able to suppress voltage ripples, but also possible to minimize the occurrence of dependent frequencies due to the fixed dithering pattern. The spectrum of the output voltage showed that the switching frequency component was reduced by about 6.1 dB and the output voltage ripples were also reduced compared to the existing PWM techniques.

INDEX TERMS Digitally controlled buck converter, spread spectrum, dithering, pulse-width modulation.

I. INTRODUCTION

As the demand and interest on the Internet of Things (IoT) spread widely in industries, studies on power systems suitable for specific applications are being actively conducted. Particularly, in terms of harvesting energy IoT devices for a sensor network, the importance of low-power and high-efficiency DC power converters has been further highlighted due to their dependence on the secondary battery with a limited capacity [1].

The analog Switching Mode Power Supply (SMPS) which converts electricity through power switch has a wide control bandwidth. However, since its analog components are relatively sensitive to environmental effects such as the changes of the ambient temperature, the analog system

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could have unstable control issues due to the altered system characteristics. By implementing the power system digitally, the enhanced control stability becomes possible because of the durability of the digital system. Furthermore, as it is relatively easy to implement the complicated nonlinear digital control system compared to the analog counterpart, studies that focus on a power system that is digitally controlled partly or entirely are increasing [2].

For a digitally controlled power system, a limit cycle issue can be induced if the resolution of PWM is lower than that of the ADC [3]. A simple solution for that issue in the digital power system is to build a high resolution PWM by using a high frequency clock, but it accompanies high power consumption, which may not meet the low-power design requirements of IoT devices. Delay line PWM method [4], hybrid PWM method [5], and PWM method using dithering [6] have been developed as high-resolution PWM methods with a low

system clock. However, delay line PWM and hybrid PWM methods have linearity issues and increase in the chip area. The PWM dithering technique is a simple method to implement high-resolution PWM without additional circuitry, but it can cause EMI problems to other circuitry [7].

Beside PWM dithering, the SMPS is often blamed as a EMI source because of its switching nature. Particularly, for a wireless IoT device, communication failures due to EMI could be significant. A PCB layout optimization [8] or an external EMI filter [9] can reduce EMI. However, these methods require additional components, manufacturing costs and increased PCB area, so they are not appropriate for small IoT devices. Therefore, various approaches to reduce EMI by controlling switching time, called spread spectrum techniques have been studied [10], [11]. The spread spectrum approaches prevent EMI by randomly spreading the switching frequency concentrated in a single frequency over a wide range. Recently, many studies have been conducted to spread the switching frequency randomly and uniformly using a chaos signal, which is a nonlinear random signal [12]. The implementation of a chaotic signal generating circuit is relatively simple for the analog system. However, the implementation of the digital chaos circuit is more complicated, and a rather inaccurate chaos signal is generated due to quantization errors [13]. A digital random modulation method can generate random numbers by using a pseudo-random generator such as a linear feedback shift register in a digital system. In addition, parameters such as scattered frequency ranges and random number seeds can be easily redefined in a digital system. Random modulation methods such as RCFMFD (Random Carrier-Frequency Modulation with Fixed Duty cycle), which also scatter the carrier wave (period) of the PWM signal, can reliably reduce EMI, but even in a system with a high resolution PWM, it presents a higher voltage ripple than normal PWM in a steady-state because of the constantly changing switching frequency [14]. Therefore, applying a random modulation method to a digital PWM system with low PWM resolution is more challenging.

To satisfy the power system requirements of IoT devices such as the low system clock for low power and the low EMI requirement, we propose a Random Carrier Frequency Modulation Dithered Duty-cycle method that is the incorporation of a random modulation spread spectrum technique based on RCFMFD and a dithering technique for the low resolution digital PWM in order to reduce EMI caused by switching frequency and dithering. The entire power converter system is depicted in Fig. 1. The proposed method satisfies the conditions for limit-cycle prevention with a low system clock, has a low voltage ripple, and reduced EMI by approximately 9 dB compared to the existing standard PWM scheme.

Chapters 2 and 3 of this paper describe a random modulation method for spread-spectrum and a PWM resolution extension and EMI reduction method, respectively. Chapter 4 discusses the experimental results of the proposed system, and Chapter 5 addresses the conclusion of this paper.

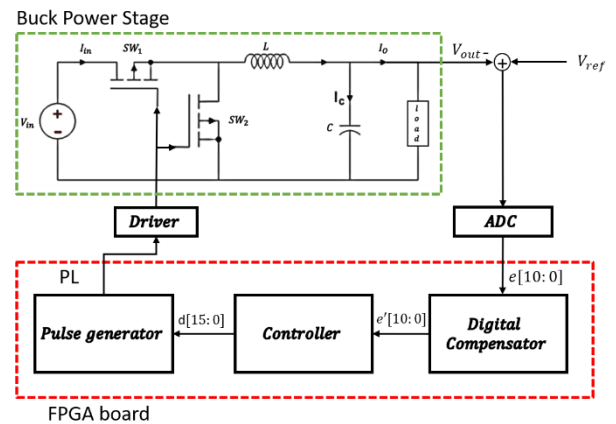


FIGURE 1. Block diagram of the proposed digital buck converter.

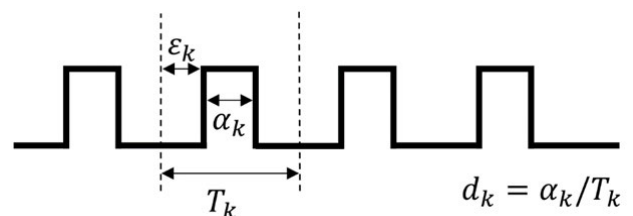


FIGURE 2. Parameters of random modulation-based PWM.

II. RANDOM MODULATION BASED SPREAD SPECTRUM METHODS FOR REDUCING EMI

The conventional PWM control-based SMPS uses a fixed switching period, and thus, power is concentrated on the switching frequency and its harmonic components. Therefore, the EMI problem has emerged as the power semiconductors become smaller and use high switching frequencies. An external EMI filter, which decreases EMI by adding a low-pass filter that can suppress harmonics in the SMPS's output, increases the system area and requires additional components, thus being unsuitable for small IoT devices. Since the cause of EMI of a buck converter is essentially affected by a constant switching frequency, studies taking the approach of the PWM switching control-based method to reduce EMI have emerged [15]–[18]. These methods randomly spread the constant PWM frequency across multiple frequency bands, reducing the peak level of a specific frequency and power spectral density (PSD).

Existing switching-based EMI reduction methods focus on chaos modulation methods and random modulation methods. The chaos modulation method presents the highest EMI reduction rate among spread spectrum methods, while the random modulation method is suitable for digital power systems because it is possible to implement a random number generator simply by using a linear feedback shift register in a digital system and exhibits an EMI reduction rate as much as chaotic modulation. Random modulation methods can be classified into four modulation methods [19].

The RPPM (Randomized Pulse Position Modulation) method is essentially similar to the PWM technique with a fixed switching period, but it controls by randomly selecting

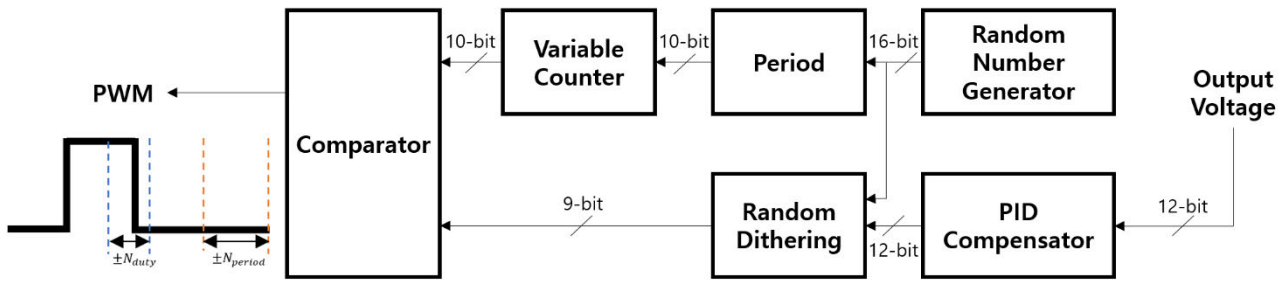


FIGURE 3. Structure of the proposed digital system.

the point at which the duty on-time starts. The RPWM (Random Pulse Width Modulation) technique randomly selects the pulse width while providing a constant average duty cycle. Unlike the RPPM and PRWM methods that use a fixed switching period, the RCFMVD (Random Carrier-Frequency Modulation with Variable Duty cycle) method controls the random switching period with a constant pulse width. Another method, the RCFMFD (Random Carrier-Frequency Modulation with Fixed Duty cycle), controls the switching period randomly while keeping the duty cycle constant. Although the random modulation method can reduce EMI by assuring the switching frequency, it has the disadvantage of generating low-frequency ripple, but the RCFMFD method is suitable for switching converters by providing a minimum voltage ripple among random modulation methods [20]. The characteristics of random switching schemes are summarized in the Fig. 2 and Table 1 [14].

TABLE 1. Characteristics of random switching schemes.

	T_k	α_k	ϵ_k	d_k
PWM	Fixed	Fixed	Zero	Fixed
RPPM	Fixed	Fixed	Rand.	Fixed
RPWM	Fixed	Rand.	Zero	Rand.
RCFMVD	Rand.	Fixed	Zero	Rand.
RCFMFD	Rand.	Rand.	Zero	Fixed

As the resolution of the ADC increases, the resolution of the output voltage of the buck converter increases as well, thereby enabling more precise control. However, if the resolution of the ADC is higher than the PWM resolution, the limit cycle issue occurs in which the output voltage ripple appears in the steady state because the exact duty cycle control amount cannot be satisfied. For this reason, methods such as PLL and dithering have been proposed for stable output voltage control of SMPS for implementing high-resolution DPWM at a low system clock.

III. HIGH RESOLUTION PWM WITH LOW EMI

Random modulation methods present a higher EMI suppression rate than other EMI reduction methods, but they exhibit

high output voltage ripple in a steady-state for the switching frequency that changes every time. Hence, to apply a random modulation method to the digital power converter in the IoT with a low system clock, a high-resolution spread-spectrum method that can handle limit cycle issues is required to suppress unstable power supply. Therefore, in this paper, Random Carrier Frequency Modulation with Dithered Duty cycle (RCFMDD), which is a structure where spread-spectrum and PWM dithering are tightly combined as shown in Fig. 3, is proposed to satisfy the above requirements.

A. RANDOM DITHERING

If an 11-bit ADC is used to control the buck converter with a switching frequency of 100 kHz, a PWM with at least 12-bit resolution is required to meet the limit-cycle prevention conditions. However, to implement a counter for 12-bit PWM, a system clock above 409.6 MHz is necessary, thus increasing a power cost, which is not suitable for the low power design requirements of IoT devices. Therefore, in this paper, we implemented a PWM with a 12-bit resolution operating with a 50 MHz system clock using a 3-bit dither for a 9-bit counter-based PWM.

The dithering technique has the advantage that high-resolution PWM can be implemented without additional circuits; in contrast, there is a disadvantage in that voltage ripple of harmonic frequency is additionally generated due to the fixed dithering pattern, which adversely affects EMI. In the proposed method, dithering patterns are output in random order during the 3-bit dithering period of eight cycles, thereby minimizing the occurrence of fixed frequencies due to dithering.

In this system, we propose a spread-spectrum-based dithered PWM to suppress the occurrence of limit cycle and EMI in a digital system using an ADC with 11-bit resolution and a low system clock. The structure of the proposed system is shown in Fig. 4.

The proposed system generates the dithered duty cycles and the frequency-shifted period. The dithering part consists of a 3-bit counter for shifting out the dithered pattern, a crossbar that randomly mixes the dithering pattern, and an adder that adds a 1-bit dither bit output from the crossbar to the 9-bit duty cycle of PWM. With low 3 bits of the 12-bit full resolution duty cycle, the number of 1s and 0s of the

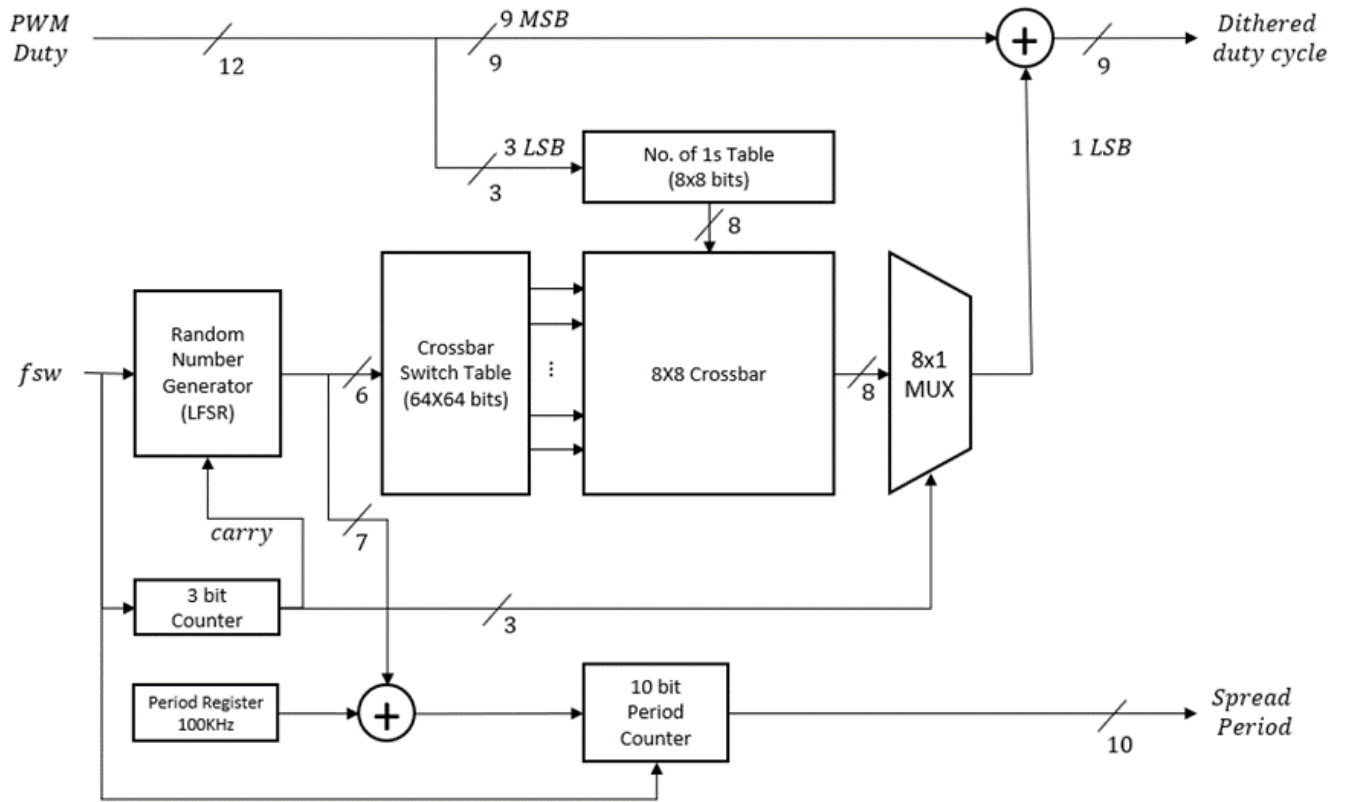


FIGURE 4. Structure of the proposed system.

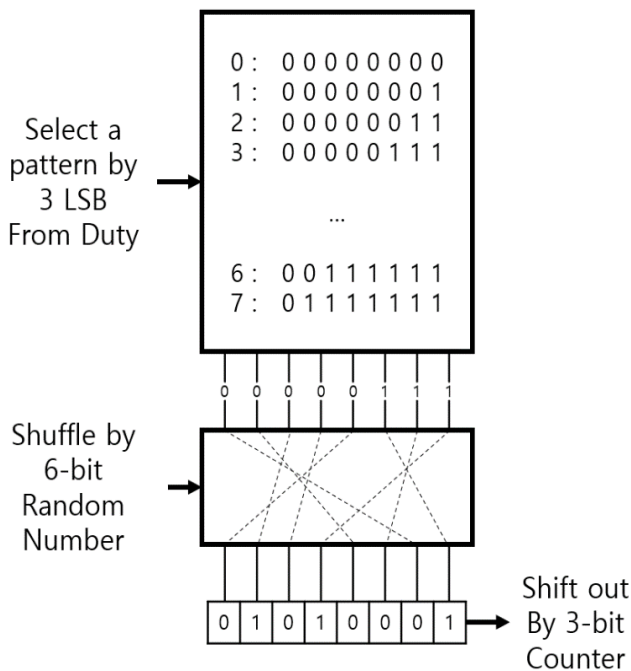
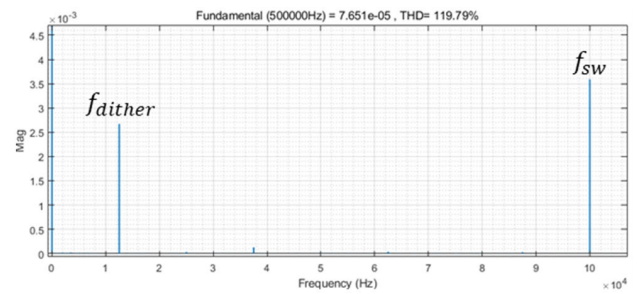
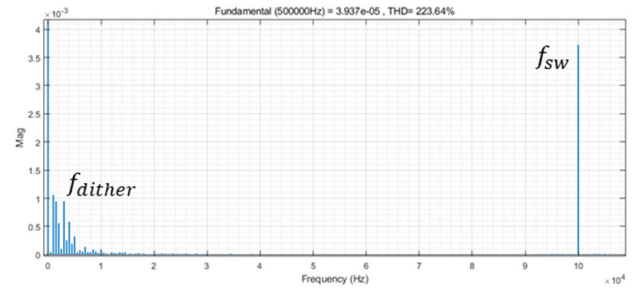


FIGURE 5. Proposed random dithering structure.



(a) Fixed dither pattern



(b) Random dither pattern.

FIGURE 6. Comparison of FFT results of conventional dithering and random dithering methods.

dithering pattern are selected, and the crossbar is set with the value obtained through the random number generator so that the eight input patterns of 1s and 0s can be mixed and output in a random order. With the 3-bit counter, 8 bits of the

mixed dithering pattern are sequentially output one at every PWM switching period and added to the PWM comparison value, thereby finally generating the dithered duty cycle. It is

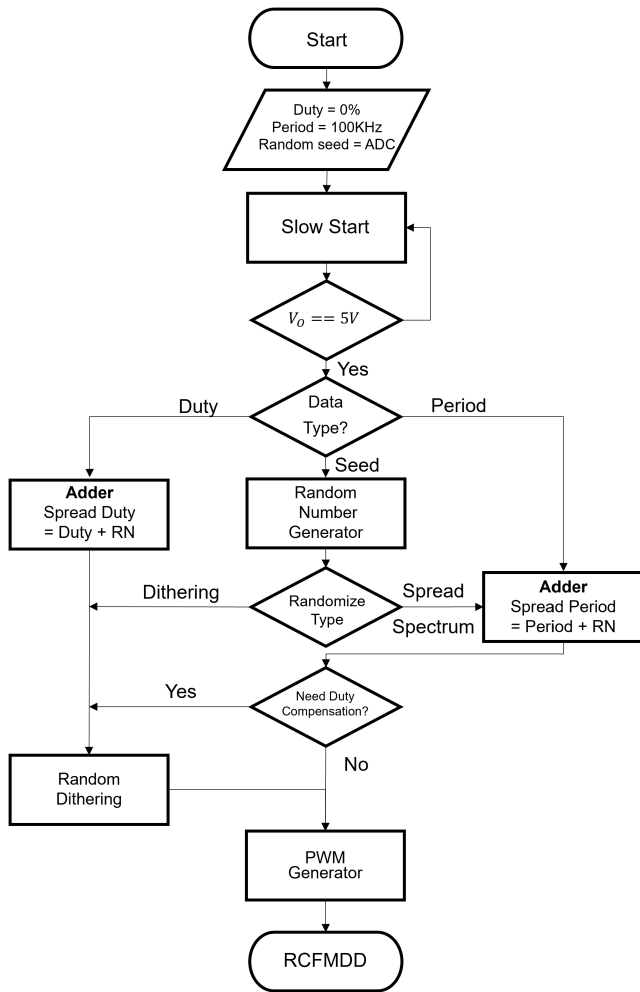


FIGURE 7. A flowchart of the proposed method.

necessary to implement a random number generator to randomly change the bit order of the dithering pattern. Therefore, in this paper, a pseudo-random number is generated using a 16-bit Linear Feedback Shift Register (LFSR). The random number generated by the LFSR is also used to determine the new period which spreads the main switching frequency.

Fig. 5 presents an example of how to implement the proposed 3-bit random dithering pattern. In the figure, the lower 3-bit of the 12-bit high-resolution duty cycle is received, and an 8-bit pattern containing 1 as much as that value is constituted. With the random value obtained through the random number in the figure, an 8-bit pattern is mixed to form an output dither pattern. This 8-bit output pattern is sequentially added to the PWM duty bit by bit by a 3-bit counter to generate PWM. For the convenience of implementation in the FPGA, the part generating the random dithering pattern is implemented as one large look-up table (LUT) in this study. In this case, the size of the LUT becomes 12 bits including the lower 3 bits of the original PWM duty, 6 bits of a random number, and 3 bits counter, thus becoming 4 kbits.

In Fig. 6, the output voltage for each method is compared with the spectrum through fast Fourier transform. A 12.5 kHz

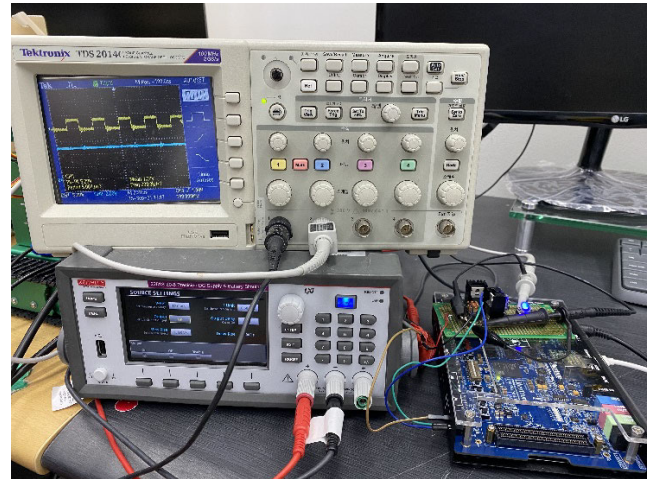
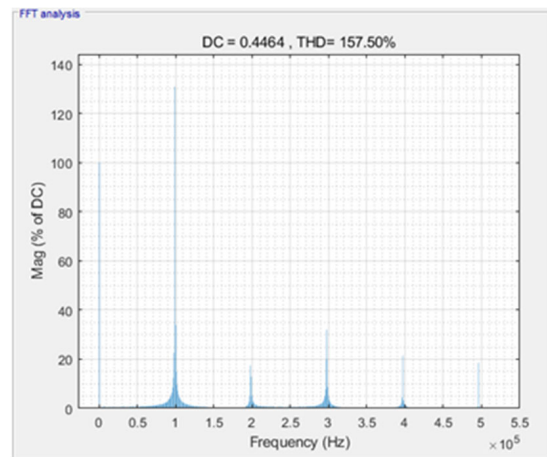
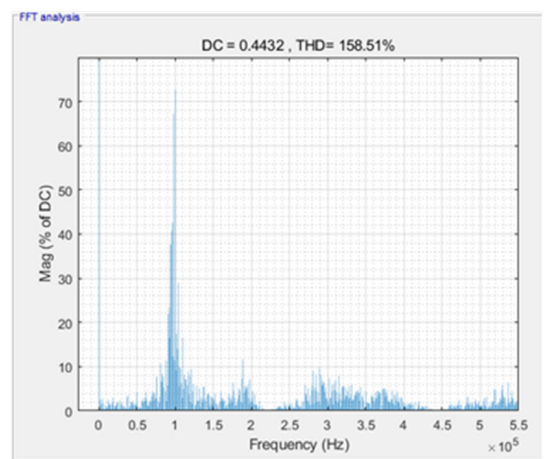


FIGURE 8. Photo of experiment environment.



(a) Standard PWM



(b) A proposed system

FIGURE 9. FFT results of standard PWM and proposed system.

frequency is generated due to a fixed dither pattern in the conventional dither method, but it is smeared when the random dithering method is applied.

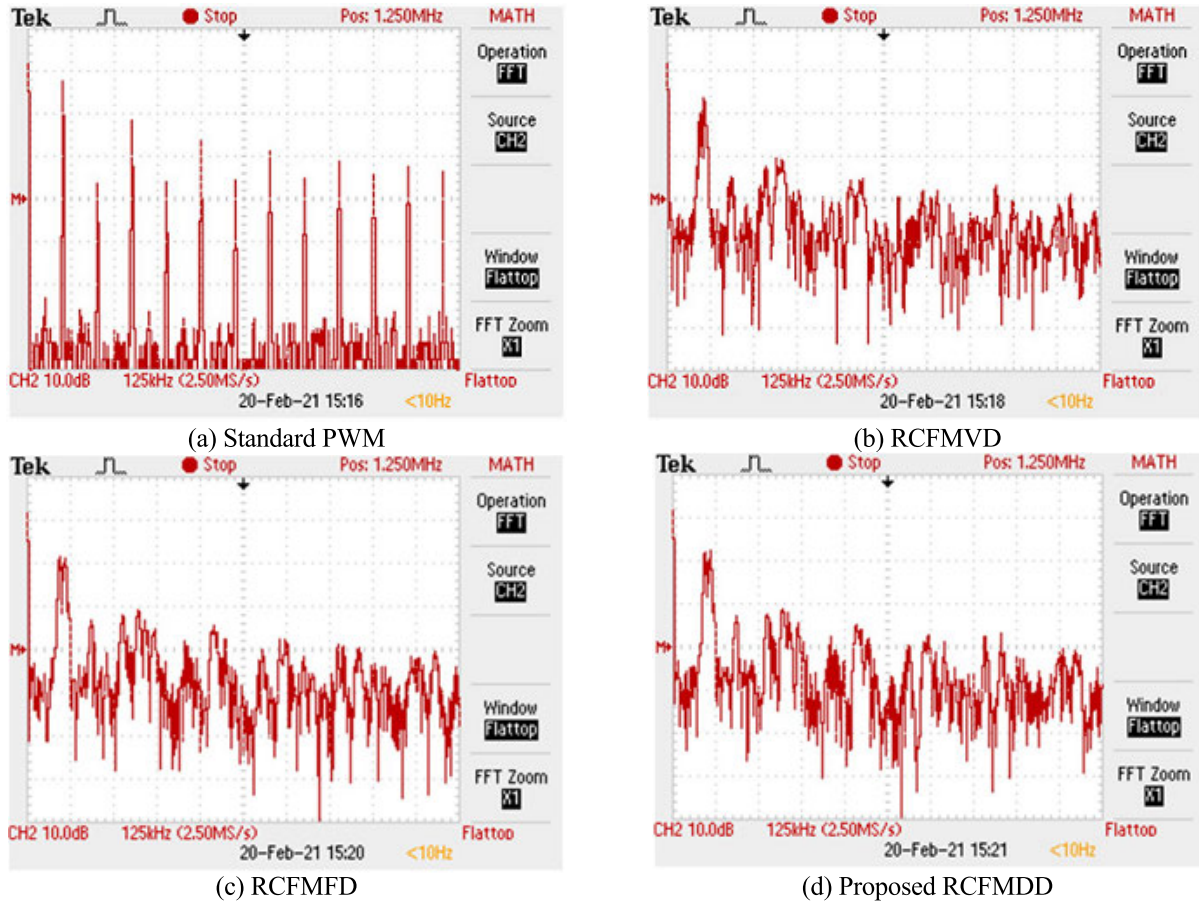


FIGURE 10. FFT results of standard PWM and proposed system.

B. RANDOM CARRIER FREQUENCY MODULATION WITH DITHERED DUTY-CYCLE

As explained earlier, the fixed switching frequency of the buck converter generates high EMI, and the dithering method for implementing high-resolution PWM is also the main cause of EMI. RCFMFD, which is one of the random modulation methods, maintains a constant duty cycle while randomizing the PWM period and the corresponding on-time duration. If the randomness level of the RCFMFD increases, the spreading range of the switching frequency is increased and the PSD of each frequency component is lowered, but the low frequency noise can degrade the performance. To resolve the noise issues, the difference between the minimum or maximum frequency of the spreading switching frequency and the switching frequency is designed to be $\pm 1/3$ of the existing switching frequency as shown in Equation 2. In the proposed method, the randomness level is set to 0.25 empirically while satisfying the condition of the equation.

$$Randomness\ level = \frac{T_{sw,max} - T_{sw,min}}{T_{sw}} \tag{1}$$

$$(T_{sw,max} - T_{sw}) < T_{sw}/3, (T_{sw} - T_{sw,min}) < T_{sw}/3 \tag{2}$$

Fig. 7 presents a flow chart of the proposed method. The controller starts in PWM mode and it switches to the dithered

RCFMFD state and operates when it reaches the steady state. The proposed method primarily determines a duty value with the resolution for 12-bit resolution through the PID controller. After generating a random carrier for the spread spectrum technique using a 16-bit LFSR with an initial ADC value as a seed, the duty is compensated for the random carrier so that it has a fixed duty cycle. Finally, the RCFMDD signal is decided by selecting the lower 3-bit of the 12-bit PWM duty and a random dither pattern with a random number and adding the output 1-bit dither bit with the upper 9-bit of the 12-bit PWM duty.

IV. EXPERIMENTAL RESULTS

An experimental digital buck converter with the proposed RCFMDD was physically implemented with the specification described in Table 2. To see the effect of the various frequency ranges the LC filter of the analog power stage is designed for 100kHz and fixed. EMI reduction effect due to the spread spectrum of the proposed circuit was verified in the stable area of the fixed load so that there is no problem with the current. We configured the experimental environment as shown in Fig. 8. As the FPGA board, which is a ZedBoard with a ZYNQ7Z020 FPGA chip, is the digital controller. In the digital system, an ADC with 11-bit resolution is used

TABLE 2. Designed digital buck converter specifications.

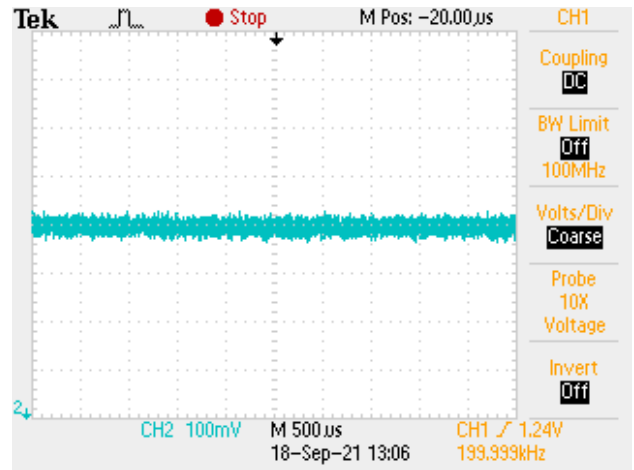
Parameter	Description	Value
Vin	Input voltage	12V
Vo	Output voltage	5V
L	Inductance	220uH
C	Capacitance	22uF
Fsw	Switching Frequency	88.8 ~ 114.4kHz
Io	Output current	1A
N_ADC	ADC resolution	11-bit
N_PWM	PWM resolution	9-bit
N_dither	The number of dither bit	3-bit
N_eff.pwm	Efficiency bits size	12-bit
clk	System clock	50MHz

to measure the analog output voltage of the buck converter. The dithering part in the system is implemented as a single look-up table for the simplicity of the FPGA design. The proposed system operates with the load current range of 1A or less, and controls the buck converter with the switching frequency range of 88.8kHz ~ 114.4kHz.

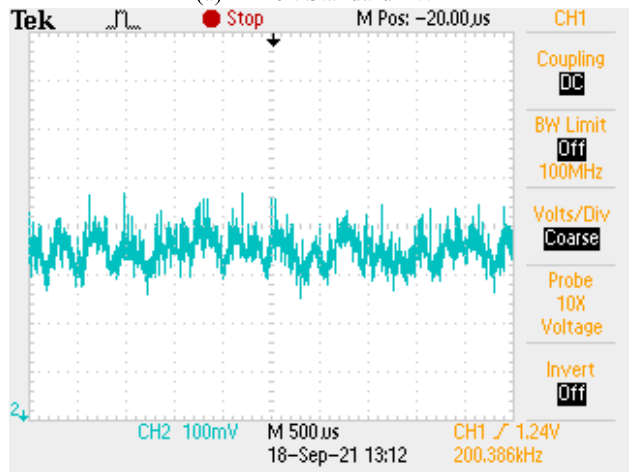
The digital buck converter with the proposed RCFMDD was also implemented and simulated to compare with existing spread spectrum digital buck converters in the MATLAB 2018a and Modelsim 10.1a.

In the spectrum of the conventional PWM, the switching frequency of 100 kHz and harmonics are concentrated. However, as a result of applying the proposed technique, the switching frequency and the peak level at the harmonics decrease as the switching frequency and harmonics are randomly spread over a specific frequency range as shown in Fig. 9(b).

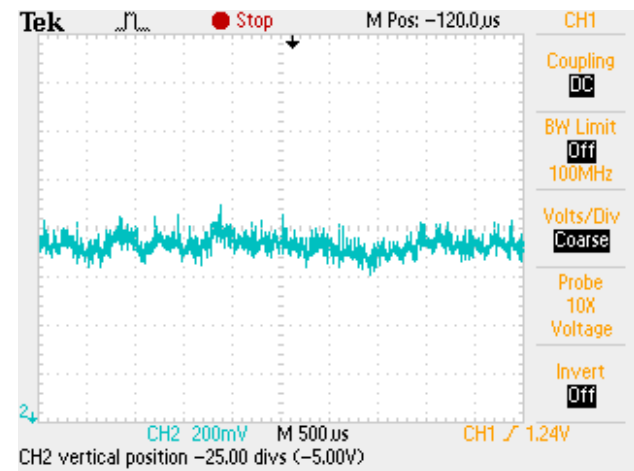
The output spectrums of standard PWM, RCFMVD, RCFMFD, and the proposed RCFMDD are compared in Fig. 10. Fig. 10 shows the spectrums of the MATLAB simulation output of the existing PWM system and that of the proposed RCFMDD system in the simulation. The simulation result is used for Fig. 10 to show the spectrum without the effect of noise in the real system. While the 12-bit PWM for the 100kHz buck converter requires 400Mhz system clock, the proposed RCFMDD shows equivalent control resolution with 50Mhz system clock with the dithering technique designed for spread spectrum operation. The proposed system reduces EMI comparable to the conventional techniques with low system clock frequency. Although there was a difference in the amount of reduction among the random modulation techniques, it was confirmed that a significant amount of power was reduced at the switching frequency and harmonics. The RCFMFD, which spreads frequencies while having a fixed duty ratio, showed the lowest EMI reduction rate, and RCFMVD with random period and random duty ratio showed the highest EMI reduction rate. The proposed RCFMDD,



(a) 12-bit Standard PWM



(b) 9-bit RCFMFD



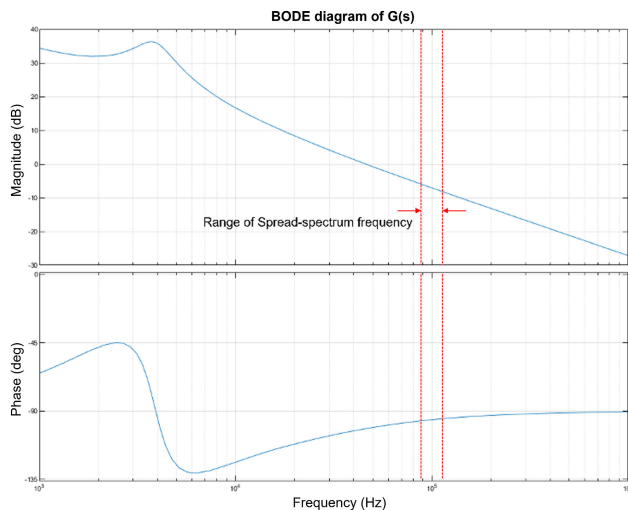
(c) Proposed RCFMDD

FIGURE 11. Output voltage ripple comparison of Standard PWM, RCFMVD, RCFMFD, and RCFMDD.

which has only 1/8 PWM resolution compared to other methods, takes an intermediate step between the two methods,

TABLE 3. Comparison result of each scheme.

	F_{sw} Suppressing	Voltage Ripple
Standard PWM	-	47mV
RCFMFD	6.5dB	228mV
Proposed system	6.1dB	121mV

**FIGURE 12.** A bode plot of proposed system.

showed the second highest EMI reduction despite of its very low PWM frequency.

Although EMI could be sufficiently reduced with the existing random modulation technique, additional voltage ripple occurs due to the limit cycle phenomenon in a low system clock environment. Fig. 11 shows the comparison of the output voltage ripple of each standard PWM, RCFMVD, RCFMFD, and the proposed system RCFMDD when using 11-bit ADC resolution in a digital system using a 50MHz system clock. As a result of comparing the maximum output voltage ripple for 0.5ms in the steady state, the standard PWM with 12-bit resolution, conventional random modulation techniques and proposed system due to the low system clock showed a ripple of 40mV, 220mV, 120mV, respectively as in Table 3.

Fig. 12 is a bode plot using PID coefficients in a stable buck state for a fixed load. As shown in the figure, it is stable in the frequency band for spread spectrum. As it is a gain region, it showed stable output (Fig. 11(c)) even in a dynamic state.

V. CONCLUSION

In this paper a digitally controlled DC-DC buck converter for IoT devices, in which low EMI with high resolution, is proposed. By combined the dithering technique and the random frequency modulation technique tightly, the proposed method not only decreases the EMI problems of the digital PWM but also increase the PWM resolution without suffering from

the harmonics due to the dithering. The experimental results show that the switching frequency is reduced about 6.1dB comparing to the standard PWM and the voltage ripples are smaller than those of the conventional spread spectrum techniques such as RCFMFD. Since the GaN power system operates with very high system frequency, those system can have significant benefit with the proposed technique to reduce EMI with relatively lower system clock frequency. As a future study, we will continue to study the performance of the buck itself as well as the improvement of the digital control system for EMI reduction.

REFERENCES

- [1] T. Wu, Y. Huang, and T. Lin, "Multi-function high-power converters for smart-grid applications," in *Proc. E S Web Conf.*, vol. 69, p. 01007, Jan. 2018, doi: [10.1051/e3sconf/20186901007](https://doi.org/10.1051/e3sconf/20186901007).
- [2] J. Kaczmarek and R. Suszynski, "Digital control buck converter—Reducing the impact of load change on the output voltage," in *Proc. 24th Int. Conf. Mixed Design Integr. Circuits Syst. (MIXDES)*, Jun. 2017, pp. 479–483, doi: [10.23919/MIXDES.2017.8005258](https://doi.org/10.23919/MIXDES.2017.8005258).
- [3] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003, doi: [10.1109/TPEL.2002.807092](https://doi.org/10.1109/TPEL.2002.807092).
- [4] Z. Zhang, S. Xu, F. Yao, G. Xie, and X. Cheng, "A 30MHz delay-line-based buck converter with 5.7%–94.8% switching duty cycle," in *Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS)*, Nov. 2019, pp. 53–56, doi: [10.1109/APCCAS47518.2019.8953135](https://doi.org/10.1109/APCCAS47518.2019.8953135).
- [5] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003, doi: [10.1109/TPEL.2002.807121](https://doi.org/10.1109/TPEL.2002.807121).
- [6] A. Peterchev, "Digital control of PWM converters: Analysis and application to voltage regulation modules," Dept. Elect. Eng. Comput. Sci., Univ. California Berkeley, Berkeley, CA, USA, Tech. Rep. UCB/EECS-2006-146, Nov. 2006.
- [7] O. Ibrahim, N. Yahaya, and N. Saad, "Design and implementation challenges of digital controlled DC-DC converters," *J. Mech. Continua Math. Sci.*, Mar. 2018, doi: [10.26782/jmcms.2019.03.00004](https://doi.org/10.26782/jmcms.2019.03.00004).
- [8] A. Bhargava, D. Pommerenke, K. W. Kam, F. Centola, and C. W. Lam, "DC-DC buck converter EMI reduction using PCB layout modification," *IEEE Trans. Electromagn. Compat.*, vol. 53, no. 3, pp. 806–813, Aug. 2011, doi: [10.1109/TEMC.2011.2145421](https://doi.org/10.1109/TEMC.2011.2145421).
- [9] A. Majid, J. Saleem, H. B. Kotte, R. Ambatipudi, and K. Bertilsson, "Design and implementation of EMI filter for high frequency (MHz) power converters," in *Proc. Int. Symp. Electromagn. Compat. (EMC Eur.)*, Sep. 2012, pp. 1–4, doi: [10.1109/EMCEurope.2012.6396738](https://doi.org/10.1109/EMCEurope.2012.6396738).
- [10] R. Gamoudi, D. E. Chariq, and L. Sbita, "A review of spread-spectrum-based PWM techniques—A novel fast digital implementation," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10292–10307, Dec. 2018, doi: [10.1109/TPEL.2018.2808038](https://doi.org/10.1109/TPEL.2018.2808038).
- [11] O. Trescases, G. Wei, A. Prodic, and W. T. Ng, "An EMI reduction technique for digitally controlled SMPS," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1560–1565, Jul. 2007, doi: [10.1109/TPEL.2007.901911](https://doi.org/10.1109/TPEL.2007.901911).
- [12] V. Nguyen, H. Huynh, S. Kim, and H. Song, "Active EMI reduction using chaotic modulation in a buck converter with relaxed output LC filter," *Electronics*, vol. 7, no. 10, p. 254, Oct. 2018, doi: [10.3390/electronics7100254](https://doi.org/10.3390/electronics7100254).
- [13] T. Karimov, D. Butusov, V. Andreev, A. Karimov, and A. Tutueva, "Accurate synchronization of digital and analog chaotic systems by parameters re-identification," *Electronics*, vol. 7, no. 7, p. 123, Jul. 2018, doi: [10.3390/electronics7070123](https://doi.org/10.3390/electronics7070123).
- [14] K. K. Tse, H. Chung, S. Hui, and H. So, "A comparative investigation on the use of random modulation schemes for DC/DC converters," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 253–263, May 2000, doi: [10.1109/41.836340](https://doi.org/10.1109/41.836340).
- [15] J. Wu, C. Mu, C. Yang, and C. Tsai, "Digitally controlled low-EMI switching converter with random pulse position modulation," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2009, pp. 341–344, doi: [10.1109/ASSCC.2009.5357164](https://doi.org/10.1109/ASSCC.2009.5357164).

- [16] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI reduction in switched power converters using frequency modulation techniques," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 569–576, Aug. 2005, doi: [10.1109/TEMC.2005.851733](https://doi.org/10.1109/TEMC.2005.851733).
- [17] D. Trevisan, P. Mattavelli, and S. Saggini, "Random switching frequency in a synchronous-asynchronous digital voltage-mode control for DC-DC converters," in *Proc. Ph.D. Res. Microelectron. Electron.*, Jun. 2006, pp. 53–56, doi: [10.1109/RME.2006.1689894](https://doi.org/10.1109/RME.2006.1689894).
- [18] K. K. Tse, H. S.-H. Chung, S. Y. Huo, and H. C. So, "Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 399–410, Mar. 2000, doi: [10.1109/63.838113](https://doi.org/10.1109/63.838113).
- [19] J.-Y. Lin, Y.-C. Hsu, and Y.-D. Lin, "A low EMI DC-DC buck converter with a triangular spread-spectrum mechanism," *Energies*, vol. 13, no. 4, p. 856, Feb. 2020, doi: [10.3390/en13040856](https://doi.org/10.3390/en13040856).
- [20] M. Faisal, J. Yousaf, and W. Nah, "Effect of random modulation switching schemes on harmonics and CE levels of a buck converter," in *Proc. Int. SoC Design Conf. (ISOCC)*, Oct. 2019, pp. 208–209, doi: [10.1109/ISOCC47750.2019.9027744](https://doi.org/10.1109/ISOCC47750.2019.9027744).



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