IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received October 1, 2021, accepted November 1, 2021, date of publication November 8, 2021,
date of current version November 18, 2021.

*Digital Object Identifier 10.1109/ACCESS.2021.3126457*

# Quantitative Feedback Theory Control to Improve Stability in DC Catenary Feeding Traction and Auxiliary Drives

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This work was supported in part by the Comunidad de Madrid under Grant IND2018/IND-9493 and in part by the Agencia Estatal de Investigación (AEI) and the European Regional Development Fund (ERDF) under Grant DPI2017-88505-C2-2-R.

**ABSTRACT** The progressive electrification of railways involves an increasing number of power electronic converters connected to the railway catenary, which may compromise its stability. Both the converter for traction and the converter for auxiliary power systems (APS) behave as constant power loads (CPL) and interact negatively with the catenary impedance producing voltage instability. This article applies quantitative feedback theory (QFT) to design an ac voltage controller for the APS converter that shapes the dc input admittance of the converter by performing only ac side-control without a dc-side feedback loop. The QFT enables to design a low order controller that satisfies multiple performance specifications in systems with high uncertainty as is the case of the train system. The proposed control guarantees catenary stability while ensuring ac output voltage reference tracking and providing robustness to unmodeled uncertainties. As an additional contribution, the article presents an algorithm for including input admittance specifications in the QFT design process. The proposed control has been evaluated on an experimental platform that recreates the train system. Experimental results show that the controlled system meets railway standards and correctly shapes the specified dc input impedance.

**INDEX TERMS** Admittance shaping, constant power loads, dc catenary line, quantitative feedback theory, railway electrification, robust control, voltage control.

## NOMENCLATURE

| | |
|---|---|
| $C$ | Capacitor of the output filter in the APS. |
| $C_F$ | Shunt capacitor of the LC filter between catenary and PCC. |
| $\hat{d}_{dq}$ | APS dq-axis small-signal duty cycles. |
| $D_{dq}$ | Operating point of $\hat{d}_{dq}$. |
| $f_g$ | Fundamental frequency of the APS ac output voltage, $v_C$. |
| $f_s$ | Sampling frequency. |
| $\mathbf{G_{VDdq}}(s)$ | Matrix of open-loop transfer functions. |
| $\mathbf{G_{VVdq}}(s)$ | Matrix of transfer functions between $\hat{v}_{Cdq}$ and $\hat{v}_{PCC}$. |
| $\mathbf{G_{IDdq}}(s)$ | Matrix of transfer functions between $\hat{i}_I$ and $\hat{d}_{dq}$. |
| $\hat{i}_I$ | APS small-signal dc input current. |
| $\hat{i}_{Odq}$ | APS dq-axis small-signal ac output current. |
| $I_{Odq}$ | Operating point of $\hat{i}_{Odq}$. |
| $\mathbf{K_{dq}}(s)$ | APS dq-axis voltage controller. |
| $L$ | Inductance of the output filter in the APS. |
| $L_{CAT}$ | Inductive term of the catenary impedance. |
| $LC_d(s)$ | Admittance bounds. |
| $Le_{CAT}$ | Distance between the train and the feeding substation. |
| $L_F$ | Inductance of the LC filter between catenary and PCC. |

The associate editor coordinating the review of this manuscript and approving it for publication was Mohammad Alshabi.

| | |
|---|---|
| $M_{p_u}$ | Maximum overshoot for $T_{R_u}(s)$. |
| $\omega_g$ | Angular frequency of $v_C$. |
| $\omega_{n_u}$, $\omega_{n_l}$ | Natural frequency for $T_{R_u}(s)$ and $T_{R_l}(s)$, respectively. |
| $P_{CPL}$ | Power consumed by the traction converter. |
| $R_{CAT}$ | Resistive term of the catenary impedance. |
| $R_L$ | Parasitic winding resistance of $L$. |
| $R_{LF}$ | Parasitic winding resistance of $L_F$. |
| $S_d$ | Sensitivity function. |
| $\sigma_u$, $\sigma_l$ | Damping ratio for $T_{R_u}(s)$ and $T_{R_l}(s)$, respectively. |
| $T_d(s)$ | Tracking transfer function. |
| $T_{Ru}(s)$, $T_{Rl}(s)$ | Upper and lower limit of $T_d(s)$. |
| $t_{s_u}$, $t_{s_l}$ | Minimum and maximum settling time. |
| $V_{CAT}$ | DC catenary voltage. |
| $v_c$ | APS ac output voltage |
| $\hat{v}_{Cdq}$ | APS dq-axis small-signal ac output voltage. |
| $V_{Cdq}$ | Operating point of $\hat{v}_{Cdq}$. |
| $\hat{v}_{PCC}$ | Small-signal PCC or APS input voltage. |
| $V_{PCC}$ | Operating point of $\hat{v}_{PCC}$. |
| $Y_{APSdq-C}(s)$ | Closed-loop APS input admittance. |
| $Y_{APSdq-O}(s)$ | Open-loop APS input admittance. |
| $Y_{LO}$ | Auxiliary load admittance. |
| $YC_{APS-C}$ | Curve between the permitted and not permitted admittance regions. |
| $Z_{APS-C}$ | Closed-loop input impedance of the APS. |
| $Z_{CPL}$ | CPL impedance modeling the traction converter. |
| $Z_{FCAT}$ | Output impedance of the LC filter and the catenary. |
| $Z_{LO}$ | Auxiliary load impedance. |
| $Z_S$ | Output impedance seen from the APS. |

## I. INTRODUCTION

Rail is one of the most sustainable modes of transport thanks to its growing electrification and the increasingly use of renewable energy sources [1]. For that reason, it is set to become a key player in reducing transport emissions. In Europe, for example, railway is mostly electrified and represents only 0.5 % of the greenhouse gas emissions of all modes of transport, while it transports 11.2 % of freight and 6.6 % of passengers [2]. Electrification leads to an increase in the presence of power electronics converters that are connected to the catenary. Typically, the train is equipped with converters for traction and converters to supply auxiliary systems. These converters are connected to an ac or dc catenary at a point of common connection (PCC). Although the presence of ac catenaries is predominant in modern high-speed corridors and common in long distance railways with heavy traffic [3], dc catenaries are still prevailing in short and medium distance railway systems and urban rail transport (light rails, tramways or metros) [4], [5] and constitute 47.3 % of railway lines around the World [6].

The interaction between the catenary and the controlled power electronics converters can cause oscillations in the catenary voltage [7]. This problem is inherent to the application and is caused by the fact that a voltage-controlled converter behaves as a constant power load (CPL) in some frequency ranges [8]. A CPL is equivalent to a small-signal negative resistance, since an increase in the voltage implies a decrease in the current and vice versa in order to keep constant power [9]. In this case, the auxiliary voltage-controlled converter or auxiliary power system (APS) behaves as a CPL because its main objective is to keep a regulated ac voltage [10]. Given the static nature of its load, keeping a stationary ac voltage (50 Hz and 400 V) implies consuming a constant power. A torque control is applied to the traction converters, but as the speed varies slowly, it can be considered also as a CPL [11]. These catenary voltage fluctuations compromise stability and can lead to a voltage drop on the railway line, which has a negative economic impact. Not considering the problem during the design stage may result in additional costs due to on-site adjustment of the APS by a team of engineers, the possibility of rejection of the equipment by the customer or having to oversize the LC filter capacitor [12]. This stability problem has been studied extensively in trains with ac catenary [13]–[17] and less widely in railway systems with dc catenary [18]–[20] on which this work focuses.

Figure. 1 presents the block diagram of the dc railway system under study. The dc catenary or dc overhead line is generated by the substation, which has traditionally used a 12-pulse rectifier to perform the ac-dc conversion [6], [21]. The catenary feeds a power-controlled traction converter and a voltage-controlled auxiliary power system (APS) converter through an LC filter. The functions of the filter include filtering ac components in the PCC and preventing the transmission of voltage peaks in the catenary to the converters. As mentioned above, the CPL behavior of both converters have a negative impact on the PCC stability. The LC-filter capacitance can be designed to ensure system stability, but usually the design only takes into account the connection of the traction converter. For this reason, the connection of the auxiliary systems can still cause undesirable oscillations in the PCC.

The frequency of the PCC oscillation is variable, because it depends on resonance frequency of the LC filter. The resonance frequency is also a function of the catenary impedance which varies with the position of the train along the catenary. The rail catenary is divided into sections of several kilometers, with each substation, feeding two adjacent sections. The greater the distance of the train from the substation feeding the catenary section, $Le_{CAT}$, the greater the inductive-resistive impedance of the catenary, $L_{CAT}$ and $R_{CAT}$. The LC-filter resonance frequency decreases as catenary inductance increases, so it may conflict with the low-frequency CPL behavior [8], [12] of the converters and destabilize the system.

Different approaches have been proposed to improve catenary stability, being possible to classify them in two

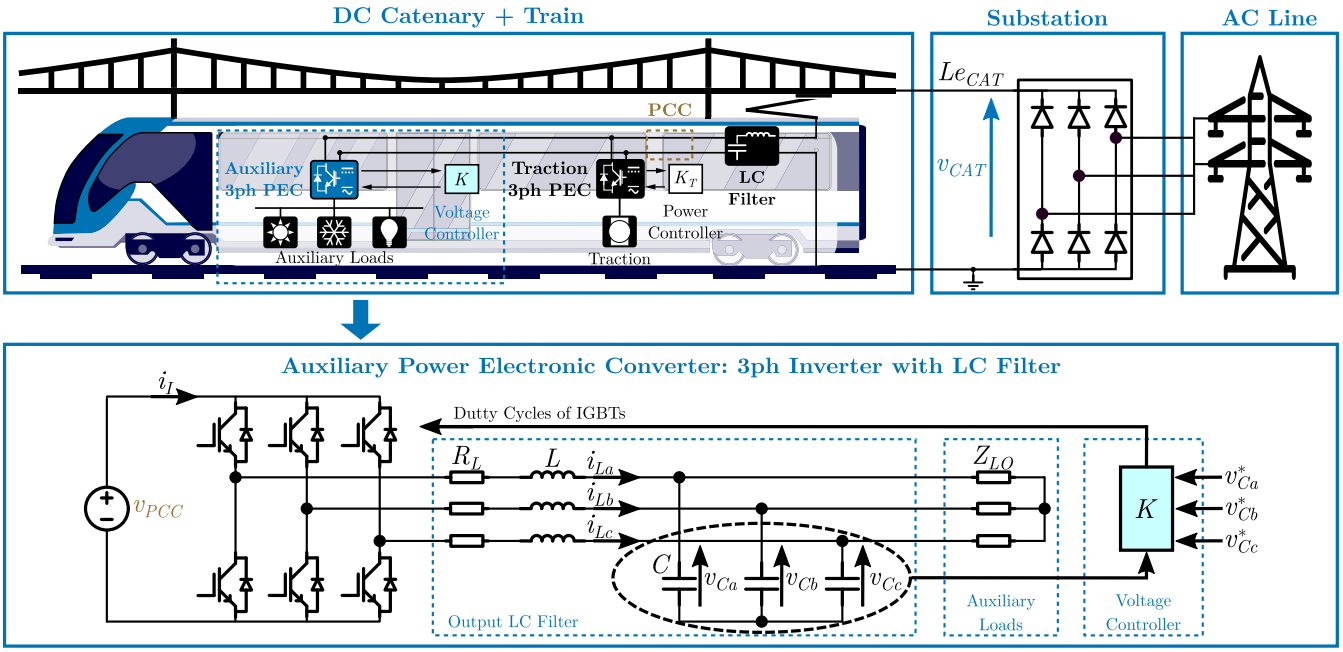


**FIGURE 1.** DC railway system. The dc catenary is generated by the substation through an LC filter. Two power electronics converters (PECs) are connected to the PCC: the power-controlled traction converter and the voltage-controlled auxiliary converter which is a three-phase inverter with LC output filter. The $K$ voltage control regulates $v_C$ to track $v_C^*$.

main categories. The first group consists of adding passive components to the system and includes both passive damping [22]–[24] and adding more capacitance to the LC filter [12]. The second approach is based on modifying the control of the converters. It includes two main methods: active damping [19], [20], [22], [25], [26] and input-admittance shaping [13], [18], [27], [28] of the auxiliary converter to meet an impedance-based stability criteria (such as Middlebrook [29], Opposing Argument [30], Gain Margin Phase Margin (GMPM) [31] or Energy Source Analysis Consortium (ESAC) [32] criteria). In general, the control-based approach is preferred because adding passive components increases the cost and weight of the train.

This article proposes a voltage control for the auxiliary converter based on the use of the Quantitative Feedback Theory (QFT) [33] to shape the dc input admittance/impedance of the converter. The main objective of the proposed design is to shape the input admittance of the converter to meet an impedance-based stability criterion to ensure stability in the catenary. In addition, the converter must regulate its ac output voltage and be robust to non-modeled uncertainties. QFT control makes it possible to synthesize a simple, low-order, maximum-bandwidth controller that satisfies multiple specifications in uncertain systems [34].

In this paper, the QFT controller is designed to meet three performance specifications (input admittance, reference tracking and relative robustness [35]) ensuring stable and correct system operation over the full range of variation of catenary inductance, catenary voltage and auxiliary load.

The main contribution of the proposed control is to shape the dc input admittance of the auxiliary converter to guarantee catenary stability, while ensuring perfect reference tracking of the ac output voltage and offering robustness to non-modeled uncertainties. A thorough search of the relevant literature yielded no related literature on shaping the dc input impedance by performing only ac-side control with no dc-side feedback loop. Another contribution of the article is to propose an algorithm to include input admittance specifications in the QFT design process. The proposed algorithm uses the opposing argument criteria, but it can be modified to use any other impedance-based stability criterion.

The rest of this article is organized as follows. Section II briefly describes the methodology of the QFT-based design process. Section III presents the modeling of the system and its uncertainties. Section IV defines the performance specifications and determines the bounds in which the QFT design is based. Section V describes the steps of the QFT design considering the modeled dc rail system and the proposed specifications. Section VI deals with the verification of the design QFT controller. In Section VII, the performance of the proposed controller is evaluated in an experimental setup. Finally, Section VIII concludes the article.

## II. QFT DESIGN PROCESS IN A NUTSHELL

Quantitative-feedback theory (QFT) control belongs to the so-called robust control techniques and was first formally formulated by Horowitz and Sidi in 1972 [36]. Since then, it has been used in diverse fields such as aerospace applications [37], [38] or mechatronics [39], [40]. A few examples are found in the fields of power electronics [41]–[43] and power systems [44], [45].

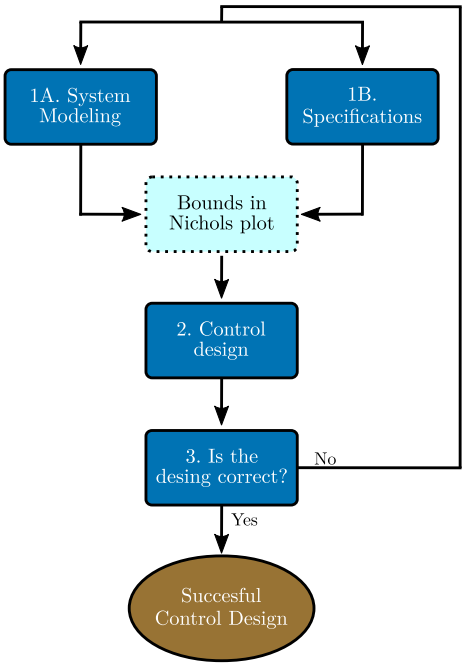


**FIGURE 2.** QFT design process at a glance.

QFT technique simultaneously reduces the effects of plant uncertainty and satisfy performance specifications through feedback [46]. The uncertainty model of the plant $G(j\omega)$ (see Section III) and its frequency and time specifications (see Sections IV-A,IV-B,IV-C) define a set of curves in the Nichols charts, known as bounds (see Section IV-D), which are used as a guide to obtain the open-loop transfer function, $L(j\omega) = K(j\omega) \cdot G(j\omega)$. The bounds delimit the permitted and not permitted values that $L(j\omega)$ can take.

After defining the bounds, the synthesis or loop shaping of the controller $K(j\omega)$ is essentially visual and performed on the Nichols chart (see Section V). The designer introduces gain, zeros and poles into $K(j\omega)$ to make the open-loop function $L(j\omega)$ lie near its bounds at each frequency to obtain an optimal controller [34]. After designing a controller, it must be validated by analyzing the frequency- and time-domain performance (see Section VI).

Fig. 2 shows the main steps of the QFT design that will be described in detail applied to the converter control design in the following sections.

## III. SYSTEM MODELING

### A. DYNAMIC MODELING

A critical factor for system stability is the interaction between the closed-loop input impedance of the APS $Z_{APS-C}$ and the output impedance that it sees toward the catenary $Z_S$. Both impedances can be obtained analyzing the small-signal model of the system presented in Fig. 3.

The small-signal model in synchnonous-reference frame ($dq$-axes) presented in Fig. 3.(a) is derived from modeling the components of the system represented in Fig. 1. The diagram of the dc railway system shows that the ac transmission line feeds the dc catenary voltage $V_{CAT}$ through the substation, which consists of a three-phase transformer and a 12-pulse rectifier. From the point of view of the train, the catenary can be modeled as an ideal voltage source with and equivalent series RL impedance, $L_{CAT}$ and $R_{CAT}$. The LC filter between the catenary and the PCC is modeled considering the parasitic winding resistance $R_{LF}$ in the filter inductance $L_F$ and an ideal shunt capacitor $C_F$. The traction converter connected to the PCC is modeled as a CPL [12] in which an impedance $Z_{CPL}$ consumes a constant power $P_{CPL}$. Modeling the traction converter as a CPL with infinite bandwidth assumes the worst case in terms of stability and challenges the proposed control for the auxiliary converter.

The APS is depicted in detail in Fig. 1. It consists of a voltage-controlled three-phase inverter with an LC output filter, $C$ and $L$, in which the inductance winding resistances $R_L$ are considered as parasitic elements. In this paper, only a resistive load $Z_{LO}$ is going to be considered as auxiliary load. The $dq$-axes small-signal model of the APS comprises a dc small-signal circuit and two coupled ac small-signal circuits [47] as shown in Fig. 3.

The output impedance $Z_S$ seen by the APS consists of the parallel of the CPL with the impedance network formed by the catenary and the LC filter.

In this type of systems, the design of $C_F$ is made in order to ensure stability under the assumption that only the traction converter is connected to the PCC. Therefore, the connection of the APS to the PCC can be a potential source of instabilities.

The small-signal model of the APS is a multiple-input-multiple-output (MIMO) system with 2 inputs (the duty cycles $\hat{d}_d$ and $\hat{d}_q$), 3 outputs (the input current $\hat{i}_I$ and the output voltages $\hat{v}_{Cd}$ and $\hat{v}_{Cq}$) and 3 input disturbances (the output currents $\hat{i}_{Od}$ and $\hat{i}_{Oq}$ and the input voltage $\hat{v}_{PCC}$). Fig. 3.(b) and 3.(c) show the block diagrams of the input-output dynamical models for input current $\hat{i}_I$ and output voltages $\hat{v}_{Cdq}$, respectively. The diagrams include the voltage controller $\mathbf{K_{dq}}(s)$. These models help to determine the closed-loop input admittance that will be one of the specifications in the control design.

The relationship between the $dq$-axes output voltage $\hat{v}_{Cdq}$ with the $dq$ components of the duty cycle $\hat{d}_{dq}$ is modeled in small signal as the matrix of open-loop transfer functions

$$\mathbf{G_{VDdq}}(s) = \frac{\hat{v}_{Cdq}(s)}{\hat{d}_{dq}(s)} = \begin{bmatrix} \frac{A^2}{A^2+B^2} & \frac{B}{A^2+B^2} \\ \frac{-B}{A^2+B^2} & \frac{A^2}{A^2+B^2} \end{bmatrix}, \quad (1)$$

where $A$ and $B$ are transfer functions given by

$$A(s) = \frac{-\omega_g LC + (sL + R_L)(sC + Y_{LO}) + 1}{V_{PCC}}, \quad (2)$$

$$B(s) = \frac{\omega_g L(sC + Y_{LO}) + \omega_g C(sL + R_L)}{V_{PCC}}, \quad (3)$$

in which $\omega_g$ is the angular frequency of the APS output voltage $v_C$ and $Y_{LO} = Z_{LO}^{-1}$ is the load admittance.

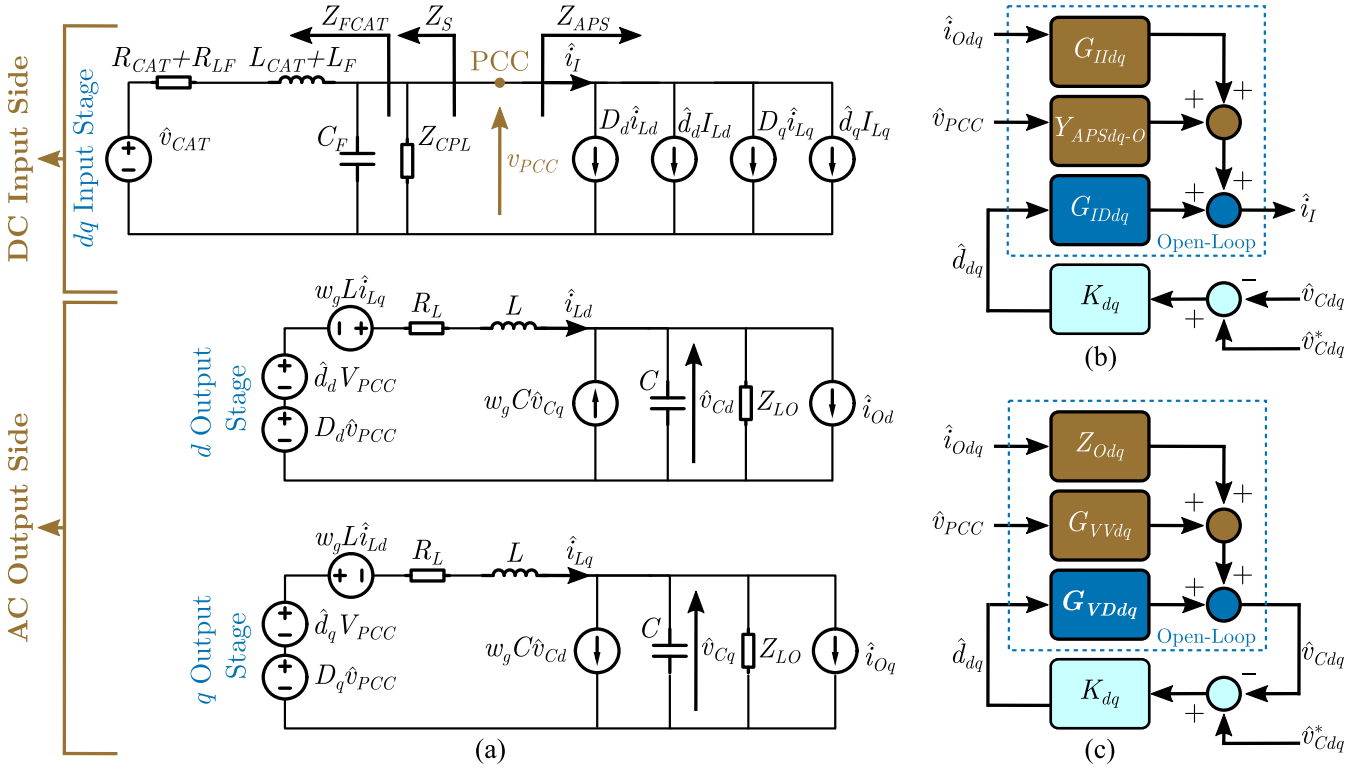


**FIGURE 3.** (a) *dq*-axes small-signal model of the voltage-controlled converter assuming CPL and including the model of the dc catenary. (b) *dq*-axes small-signal MIMO system considering the input current dynamic. (c) *dq*-axes small-signal MIMO system considering the output voltage dynamic.

The relationship between the PCC voltage $\hat{v}_{PCC}$ and the input current $\hat{i}_I$ is the open-loop input admittance

$$Y_{APSdq-O}(s) = \frac{\hat{i}_I(s)}{\hat{v}_{PCC}(s)} = D_d^2 Y_{Ldd} + D_q D_d (Y_{Lqd} + Y_{Ldq}) + D_q^2 Y_{Lqq}, \tag{4}$$

with

$$Y_{Ldd}^{-1} = Y_{Lqq}^{-1} = R_L + sL + \frac{sC + Y_{LO}}{(sC + Y_{LO})^2 + \omega_g^2 C^2}, \tag{5}$$

$$Y_{Ldq}^{-1} = -Y_{Lqd}^{-1} = -\omega_g L + \frac{\omega_g C}{(sC + Y_{LO})^2 + \omega_g^2 C^2}. \tag{6}$$

The operating point of the duty cycle is given by

$$D_d = \frac{-\omega_g L(I_{Oq} + \omega_g C V_{Cd}) + R_L(I_{Od} - \omega_g C V_{Cq}) + V_{Cd}}{V_{PCC}}, \tag{7}$$

$$D_q = \frac{\omega_g L(I_{Od} - \omega_g C V_{Cq}) + R_L(I_{Oq} + \omega_g C V_{Cd}) + V_{Cq}}{V_{PCC}}, \tag{8}$$

where $V_{Cd}$ and $V_{Cq}$ are the operating points of the output voltage $\hat{v}_{Cdq}$ and

$$I_{Od} = V_{Cd} Y_{LO}, \tag{9}$$

$$I_{Oq} = V_{Cq} Y_{LO}. \tag{10}$$

The transfer matrix that relates the input current $\hat{i}_I$ with the duty cycle $\hat{d}_{dq}$ is

$$\mathbf{G_{IDdq}}(s) = \frac{\hat{i}_I(s)}{\hat{d}_{dq}(s)} = \begin{bmatrix} G_{IDd} & G_{IDq} \end{bmatrix}, \tag{11}$$

defining

$$G_{IDd} = V_{PCC}(2D_d Y_{Ldd} + D_q Y_{Lqd} + D_q Y_{Ldq}), \tag{12}$$

$$G_{IDq} = V_{PCC}(2D_q Y_{Lqq} + D_d Y_{Lqd} + D_d Y_{Ldq}). \tag{13}$$

The relationship between the PCC voltage $\hat{v}_{PCC}$ and the *dq*-axes output voltage $\hat{v}_{Cdq}$ is given by the transfer matrix:

$$\mathbf{G_{VVdq}}(s) = \frac{\hat{v}_{Cdq}(s)}{\hat{v}_{PCC}(s)} = \begin{bmatrix} \frac{AD_d + BD_q}{V_{PCC}(A^2 + B^2)} \\ \frac{AD_d - BD_q}{V_{PCC}(A^2 + B^2)} \end{bmatrix} \tag{14}$$

where $A$ and $B$ are given by (2) and (3).

The APS closed-loop admittance can be obtained from Fig. 3.(b) and 3.(c) as follows:

$$Y_{APS-C}(s) = Y_{APS-O} - \mathbf{G_{IDdq}}(\mathbf{I} + \mathbf{K_{dq}}\mathbf{G_{VDdq}})^{-1}\mathbf{K_{dq}}\mathbf{G_{VVdq}} \tag{15}$$

The output impedance $Z_S(s)$ is defined as the parallel of the CPL impedance $Z_{CPL}$ and the output impedance seen toward the catenary $Z_{FCAT}(s)$:

$$Z_S(s) = Z_{CPL} // Z_{FCAT}(s), \tag{16}$$

**TABLE 1. Main parameters for the control design.**

| Variable | Symbol | Value |
|---|---|---|
| PCC voltage | $V_{PCC}$ | $650-1000$ V |
| LC-filter capacitor | $C_F$ | 23 mF |
| LC-filter inductance | $L_F$ | 0.22 mH |
| LC-filter resistance | $R_{LF}$ | 11 mΩ |
| Train position | $Le_{CAT}$ | $0-4$ km |
| Catenary resistance per km | $R_{CAT}$ | 51 mΩ/km |
| Catenary inductance per km | $L_{CAT}$ | 1.5 mH/km |
| CPL power | $P_{CPL}$ | 300 kW |
| $d$-axis output voltage reference | $v^*_{Cd}$ | 326 V |
| Output LC-filter capacitor | $C$ | 40 $\mu$F |
| Output LC-filter inductance | $L$ | 3.4 mH |
| Output LC-filter resistance | $R_L$ | 47.4 mΩ |
| Auxiliary load | $Z_{LO}$ | $3.2-\infty$ Ω |
| Output-voltage radial frequency | $\omega_g$ | $2\pi 50$ rad/s |
| Sampling frequency | $f_s$ | 10 kHz |
| Switching frequency | $f_{sw}$ | 5 kHz |

with

$$Z_{CPL} = -\frac{V_{PCC}^2}{P_{CPL}}, \tag{17}$$

$$Z_{FCAT}(s) = \frac{sL_T + R_T}{s^2 L_T C_F + sC_F R_T + 1}, \tag{18}$$

being $L_T = L_F + L_{CAT}$ and $R_T = R_{LF} + R_{CAT}$.

### B. UNCERTAINTY MODELING

The plant model of the railway system under study is affected by a variety of uncertainties. First, the European standard for railway applications allows that the PCC voltage can vary from $v_{PCC} = 650\ V$ to $v_{PCC} = 1000\ V$ [48]. Second, the APS load condition can change from no load to $Z_{LO} = 3.2\ \Omega$. Finally, the position of the train along the catenary can vary from $Le_{CAT} = 0\ km$ to $Le_{CAT} = 4\ km$, which implies a variability $R_{CAT}$ and $L_{CAT}$.

The parameters listed in Table 1 has been used to analyze the system uncertainty. Both PCC voltage uncertainty and load uncertainty result in uncertainty in $\mathbf{G_{VDdq}}$. Uncertainty in $V_{PCC}$ also results, together with uncertainty in $Le_{CAT}$, in variability in the output impedance $Z_S$ as it can be observed in Fig. 4.

The QFT technique works with a set of frequencies of interest that are determined by inspecting the frequency response of the plants resulting from considering the range of uncertainty.

- Low frequencies for tracking and robustness specifications. The fundamental frequency of the $abc$-axes output voltage is $f_g = 50$ Hz, but when applying the Park transformation, the fundamental $dq$-axes components are dc (that is 0 Hz). A frequency very close to 0 is selected: $F_1 = 10^{-5}$ Hz.
- Medium frequencies for admittance and robustness specifications. Fig. 4 shows that resonance of $Z_S$ is between 12.2 Hz and 70.5 Hz. For this reason, a set of frequencies around those values is selected: $F_2 = (12, 12.2, 12.5, 70, 70.5, 71)$ Hz.

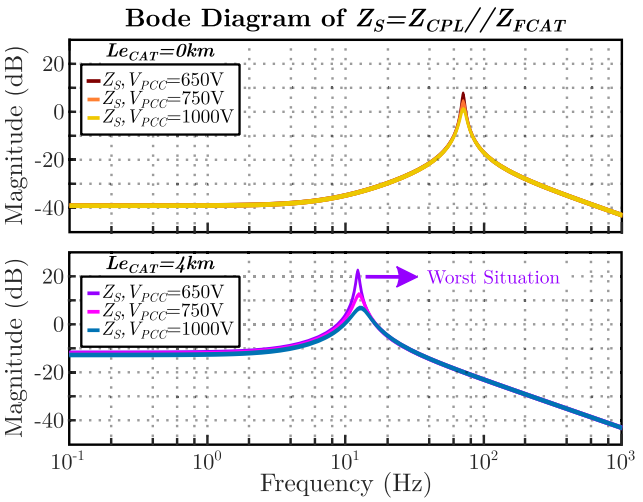


**FIGURE 4. Bode diagram of $Z_S(s) = Z_{CPL}//Z_{FCAT}(s)$ according to the distance between train and substation $Le_{CAT}$ and the PCC voltage $V_{PCC}$. The worst case occurs with maximum distance and minimum voltage ($Le_{CAT} = 4km$ and $V_{PCC} = 650V$) as the resonance peak of $|Z_S|$ is maximum.**

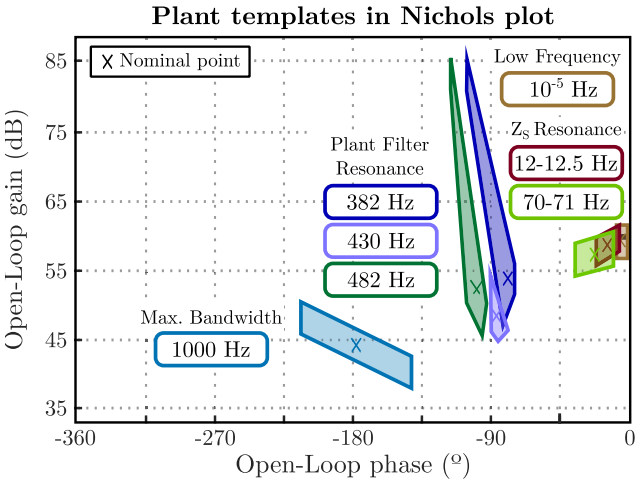


**FIGURE 5. Plant templates of $G_{VDdq1,1}(s)$ for frequencies of interest. The nominal point for each frequency is mark with a cross.**

- High frequencies for maximum bandwidth and robustness specification. The nominal plant resonance is at 430 Hz. Besides, the maximum bandwidth is limited by the sampling frequency $BW_{max} = f_s/6$, so $BW = 1.6$ kHz. For these reasons, the selected set of high frequencies is $F_3 = (382, 430, 482, 1600)$ Hz.

The plant uncertainties are projected as QFT templates in the Nichols chart as shown in Fig. 5. The crosses represent the nominal plant at the frequencies of interest. The colored regions represent the model uncertainty.

Figure 6 shows the Nyquist diagram of $Z_{FCAT}/Z_{CPL}$ when only the CPL is connected to the catenary and for the worst conditions (maximum $Le_{CAT}$ and minimum $V_{PCC}$). It can be observed that the system is at the limit of stability under these conditions. If the APS control is designed to guarantee

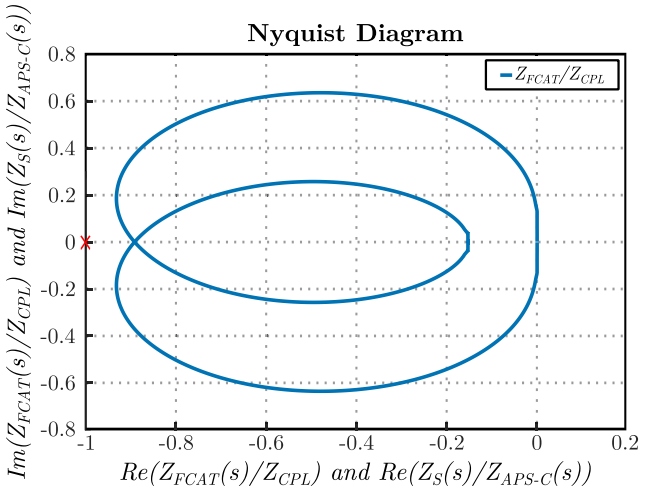


**FIGURE 6.** $Z_{FCAT}(s)/Z_{CPL}(s)$ for the worst case (maximum distance $Le_{CAT}$ = 4 km and minimum voltage $V_{PCC}$ = 650 V).

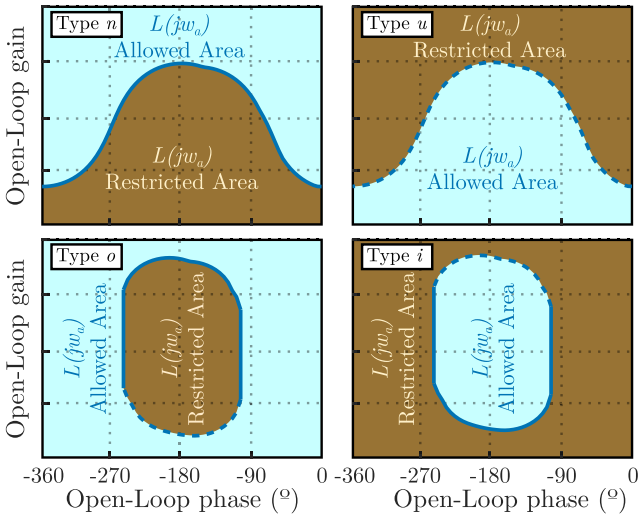


**FIGURE 7.** Types of bounds in Nichols chart. The bound delimits the value that the open-loop function $L(j\omega_a)$ can take for a given frequency $\omega_a$. The blue area represents permitted values, while the brown area shows restricted ones.

stability when the APS plugs in while the train is operating in this worst-case scenario, the rail system will be stable for any other situation.

## IV. SPECIFICATIONS AND BOUNDS

Unlike other robust control techniques, the QFT technique only needs to deal with the nominal plant to synthesize the control, since all model uncertainties are included in the QFT bounds [34]. The QFT bounds are curves on the Nichols chart resulting from the combination of the model uncertainties in the form of the QFT templates (Fig. 5) and the type of specification. There exists a QFT bound at each frequency of interest and for each type of specification. The intersection of all the bounds at a frequency $\omega_a$ determines the permitted values that the open-loop function $L(j\omega_a)$ can take at that frequency. Fig. 7 shows the four possible types of bounds ($n$, $u$, $o$ and $i$).

Three types of specifications are considered for designing the controller:

- Reference tracking, in which the objective is to track the voltage reference with zero steady-state error. As it was mentioned in subsection III-B, the fundamental components are dc signals in $dq$-axes.
- Input admittance, which is the main objective in order to solve the problem under study. The aim is to obtain a closed-loop input admittance of the inverter that meets the opposing argument criterion.
- Relative robustness, which aims to ensure that the designed control is robust to non-modeled uncertainties.

The three specifications are described in the following subsections.

The QFT bounds considering tracking and robustness specifications are obtained by using the QFT toolbox for Matlab [49]. The algorithm to obtain the QFT bounds from the input admittance specification is presented in this article.

### A. TRACKING SPECIFICATION

For tracking performance considering low frequencies $F_1$, it is desired that the settling time of the response of the controlled APS be between a minimum $t_{s_u}$ and a maximum $t_{s_l}$. The tracking specification is defined by constraining the tracking transfer function $T_d(s)$ between an upper limit $T_{Ru}(s)$ and a lower limit $T_{Rl}(s)$ :

$$|T_{Rl}(s)| \leq |T_d(s)| \leq |T_{Ru}(s)|, \tag{19}$$

where

$$|T_d(s)| = \left| \frac{K_{dq,(1,1)}(s)G_{VDdq,(1,1)}(s)}{1 + K_{dq,(1,1)}(s)G_{VDdq,(1,1)}(s)} \right| \tag{20}$$

The upper restriction $T_{Ru}(s)$ is chosen to meet a minimum settling time $t_{s_u}$ and a maximum overshoot $M_{p_u}$. From these two specifications, the dynamic behavior of a second-order system can be described in terms of its natural frequency $\omega_{n_u}$ and damping ratio $\zeta_u$ [50]. It is advisable to relax the tracking condition at high frequencies, since the plant variability is higher than at low frequencies [34], so a zero is added a decade in frequency above $\sigma_u = \zeta_u\omega_{n_u}$, that is $a = 10\sigma_u$. $T_{Ru}(s)$ is modeled as

$$T_{Ru}(s) = \frac{(\frac{\omega_{nu}^2}{a})(s+a)}{s^2 + 2\zeta_u\omega_{n_u}s + \omega_{n_u}^2}. \tag{21}$$

The lower restriction $T_{Rl}(s)$ is defined as a critically damped system ($\zeta_l = 1$) with a settling time $t_{s_l} = 4/\sigma_l$ where $\sigma_l = \omega_{n_l}$. It is also desirable to relax the tracking condition at high frequencies, but in this case a pole is added a decade above $\sigma_l$. $T_{Rl}(s)$ is then given by:

$$T_{Rl}(s) = \frac{10\sigma_l^3}{(s+\sigma_l)^2(s+10\sigma_l)}. \tag{22}$$

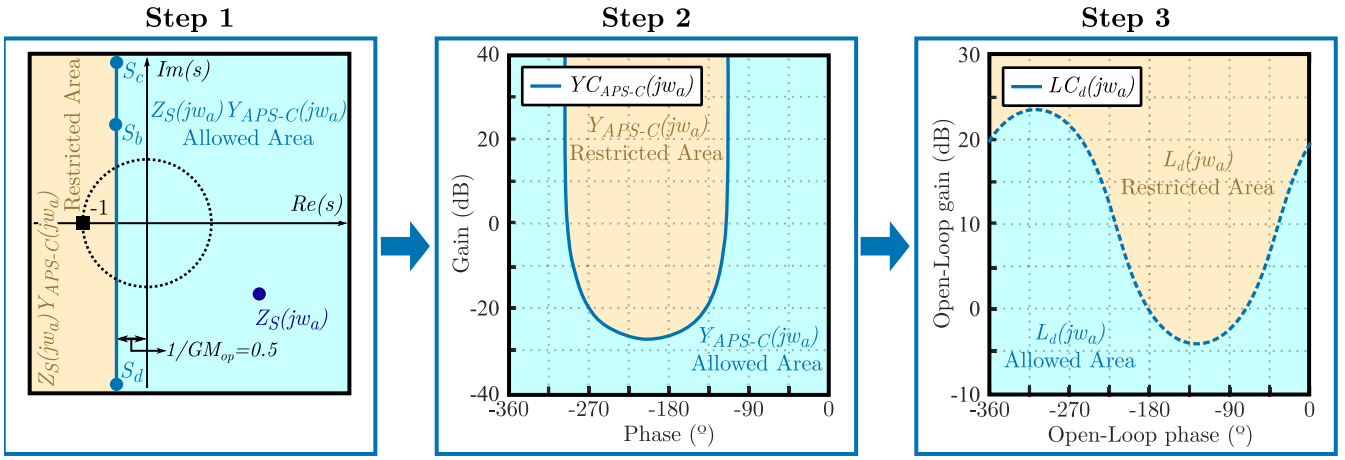


**FIGURE 8.** Procedure to obtain the admittance bound for a frequency $\omega_a$ by means of the opposing argument criterion with gain margin $GM_{op} = 0.5$. To use another impedance-based stability criterion, just modify step 1. These steps need to be repeated for all study frequencies, in this case for $F_2$.

### B. INPUT ADMITTANCE SPECIFICATION

The proposed solution is based on shaping the input admittance of the APS to meet the opposing-argument criterion [30] and ensure stability at the PCC. For that reason, an input admittance specification must be introduced in the QFT design. The algorithm that obtains the bounds for the input admittance specification is one of the main contributions of this article.

The specification is set in closed-loop, $Y_{APSdq-C}(s)$, so the algorithm must transfer it to open-loop to generate the corresponding admittance bounds, $LC_d(s)$.

The variability in $V_{PCC}$ (650 V, 750 V and 1000 V), $Z_{LO}$ (3.2 Ω, 6.4 Ω and ∞ Ω) and $Le_{CAT}$ (0 km and 4 km) supposes 18 different combinations of parameters, while the number of frequencies of interest $F_2$ is 9. Therefore, there are $18 \cdot 9$ admittance bounds. The process is illustrated in Fig. 8 at, for example, a frequency of 12 Hz ($\omega_a = 75.4$ rad/s) and with $v_{PCC} = 650$ V, $Z_{LO} = 3.2$ Ω and $Le_{CAT} = 4$ km. The process must be repeated for each combination of parameters and $F_2$ frequencies. It consists of the following steps:

- Step 1: Since the opposing-argument criterion is used, the desired gain margin for $Z_S(s)Y_{APS-C}(s)$ must be defined. In this case, $GM_{op} = 6$ dB. The following restriction must be complied at $\omega_a$:

$$Re(Z_S(j\omega_a)Y_{APS-C}(j\omega_a)) > (-1/GM_{op}) \quad (23)$$

- Step 2: The curve between the permitted and not permitted admittance regions, $YC_{APS-C}(j\omega_a)$ is given by

$$YC_{APS-C}(j\omega_a) = \frac{S_b}{Z_S(j\omega_a)} \quad (24)$$

  where $S_b$ goes from $S_c$ to $S_d$, which are complex numbers with real part $\mathrm{Re}(S_c) = \mathrm{Re}(S_d) = GM_{op}^{-1}$ and imaginary part $\mathrm{Im}(S_c) \to \infty$ and $\mathrm{Im}(S_d) \to -\infty$.
- Step 3: Taking into account (15), the bound in open-loop for $\omega_a$ is calculated as $LC_d(j\omega_a) = f(Y_{APS-C}(j\omega_a))$.

### C. RELATIVE ROBUSTNESS SPECIFICATION

The sensitivity function $S_d = (1 + K_{dq,(1,1)}G_{VDdq,(1,1)})^{-1}$ is a good indicator of robustness, being its maximum peak an inverse indicator of the system stability [35]. A typical maximum value of $|S_d|_{max} = 6$ dB is chosen for all the frequencies of interest ($F_1, F_2, F_3$). It provides to the controlled system with at least a phase margin $PM = 30°$ and a gain margin $GM = 6$ dB, which are acceptable figures of robustness.

### D. RESULTING BOUNDS IN NICHOLS CHART

The Matlab toolbox [49] and the proposed algorithm are used to obtain the bounds for each frequency of interest according to the QFT templates and the chosen specifications. The intersection of all the bounds results in the limiting curve for each frequency in ($F_1, F_2, F_3$). The Nichols chart that includes the bounds at each frequency (marked by a circle) and the nominal plant (black solid line) of the uncontrolled system is presented in Fig. 9.(a), in which the most restrictive bounds are of type $n$ and $u$, corresponding respectively to the tracking and admittance specification. The design process of the voltage controller starts from this Nichols diagram.

## V. QFT CONTROLLER DESIGN PROCEDURE

The QFT design procedure of the voltage controller is essentially a visual process, in which the designer introduces gain, poles and zeros into the controller transfer function to make the open-loop gain meet the bounds obtained in the previous step and shown in Fig. 9.(a). As mentioned above, there is an additional specification that limits the bandwidth to $BW = f_s/6 = 1.6$ kHz. Fig. 9 illustrates the steps of the design procedure that consist of:

- Step 1: An integrator is added to the controller for tracking the dc voltage reference, $K_1(s) = \frac{1}{s}$. It increases the gain and decreases 90° the phase at frequency $F_1$.
- Step 2: A notch filter is added at 12 Hz, $K_2(s) = \frac{s^2+30.84s+5944}{s^2+254.3s+5944}$. It reduces the gain and increase the phase at medium frequencies $F_2$.

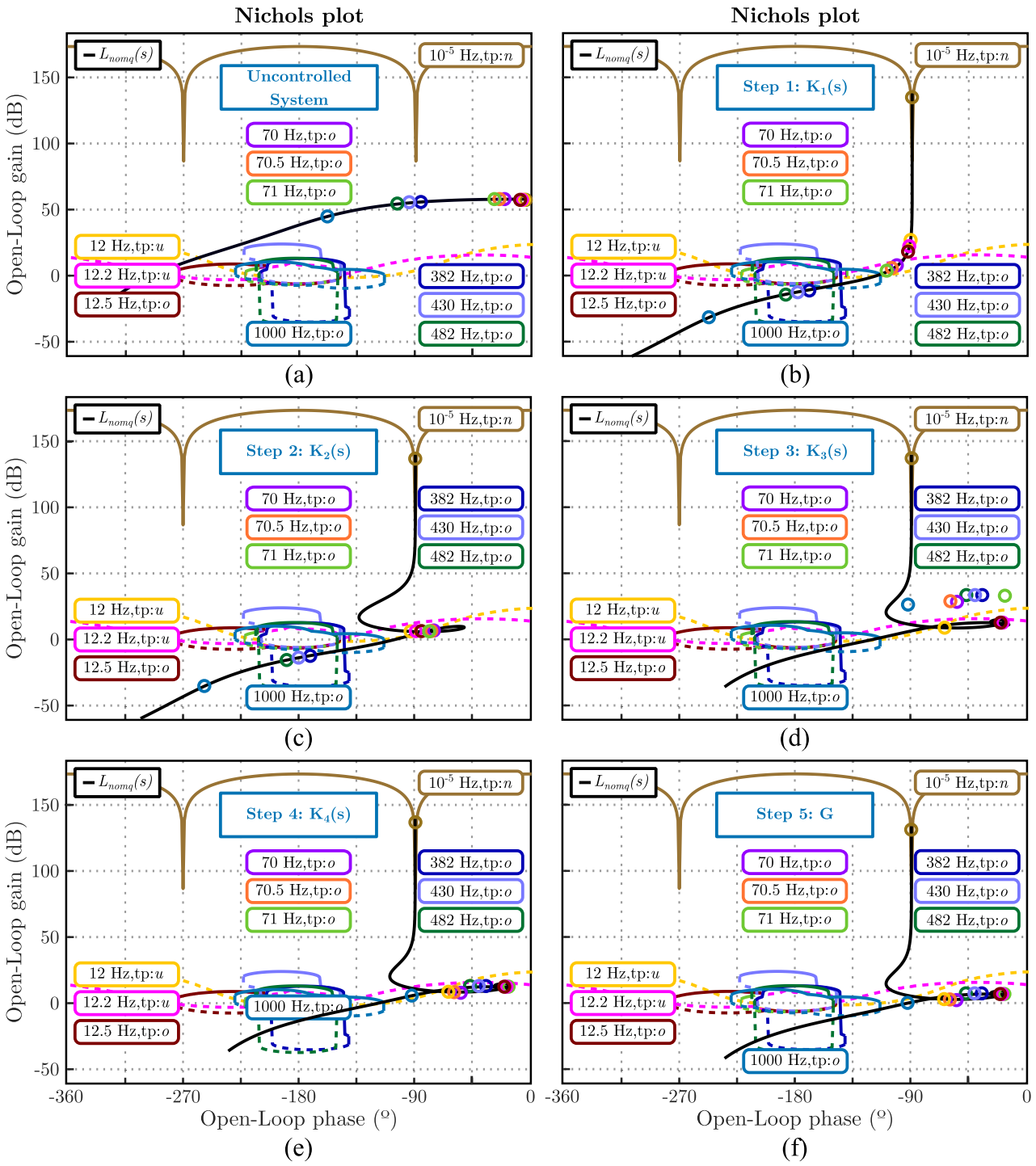


**FIGURE 9.** Step-by-step QFT design process. Each frequency (marked by a circle) and its corresponding bound are painted with the same color. Black line represents the $d$-axis nominal plant, that is $L_{d,nom}(s) = K_d(s) \cdot G_{VDdq_{1,1}}(s)$ with $V_{PCC} = 750$ V and $Z_{LO} = 6.4\ \Omega$.

- Step 3: Three poles at 100 rad/s and three zeros at 70 rad/s are included into the controller, $K_3(s) = \frac{(s+70)^3}{(s+100)^3}$. They increase the phase at frequencies $F_2$ but with almost no reduction in gain, thus the bandwidth keeps constant.
- Step 4: Three zeros are added to increase the gain at frequency 1600 Hz. In addition, two poles are included to make the controller strictly causal. $K_4(s) = \frac{(s+1000)(s+750)(s+10^4)}{(s+10^5)(s+2\cdot10^4)}$.
- Step 5: Finally, the gain is adjusted to achieve the desired bandwith of 1600 Hz, $G = 4078$.

The resulting $dq$-axes voltage controller is

$$\mathbf{K_{dq}}(s) = \begin{bmatrix} K(s) & 0 \\ 0 & K(s) \end{bmatrix}, \tag{25}$$

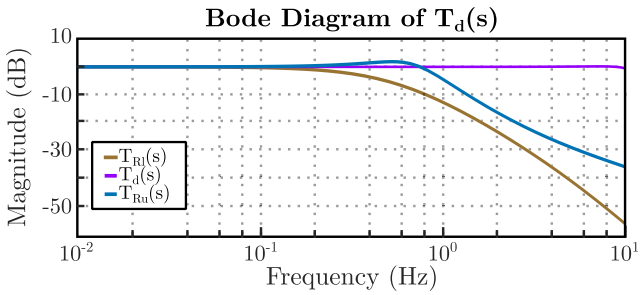


**FIGURE 10.** Complementary sensitivity function $T_d(s)$ considering all the rank of variability of $V_{PCC}$ and $Z_{LO}$ and upper and lower limits, $T_{Ru}(s)$ and $T_{Rl}(s)$ respectively. At low frequencies, $T_d(s)$ is equal for all the rank of variability.

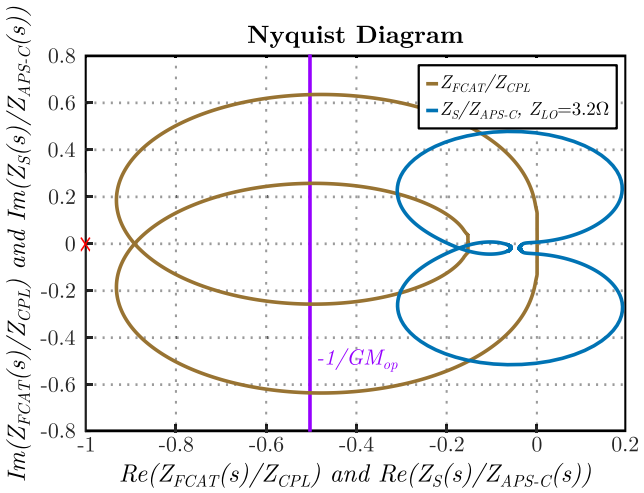


**FIGURE 11.** Comparing $Z_{FCAT}(s)/Z_{CPL}(s)$ and $Z_S(s)/Z_{APS-C}(s)$ for the worst case (maximum load $Z_{LO} = 3.2\ \Omega$, maximum distance $Le_{CAT} = 4$ km and minimum voltage $V_{PCC} = 650$ V). Unlike $Z_{FCAT}(s)/Z_{CPL}(s)$, $Z_S(s)/Z_{APS-C}(s)$ meets opposing-argument criterion.

where

$$K(s) = GK_1(s)K_2(s)K_3(s)K_4(s). \tag{26}$$

## VI. THEORETICAL AND SIMULATION VERIFICATION

The QFT design process ends by verifying that the controller meets the different specifications through theoretical analyses and simulation. In case of the controller does not meet the requirement, the design process would be repeated after modifying the QFT design specifications.

### A. THEORETICAL VERIFICATION

The tracking specification described in subsection IV-A is verified by analyzing the $d$-axis complementary sensitivity function $T_d(s)$. Considering all the rank of variability of the PCC voltage $V_{PCC}$ and of the load $Z_{LO}$, Fig. 10 shows that $T_d(s)$ meets the specifications and is between the limits $T_{R_u}(s)$ and $T_{R_l}$ at low frequencies where the tracking specification is defined.

The input admittance specification described in IV-B is the most important objective to be met by the voltage control proposed in this article. Fig. 11 presents a

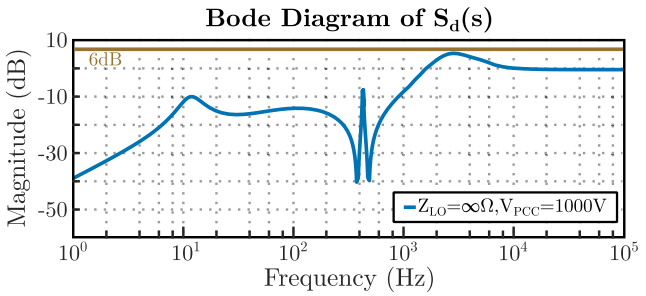


**FIGURE 12.** Sensitivity function for the worst case ($Z_{LO} = \infty\ \Omega$ and $V_{PCC} = 1000$ V).

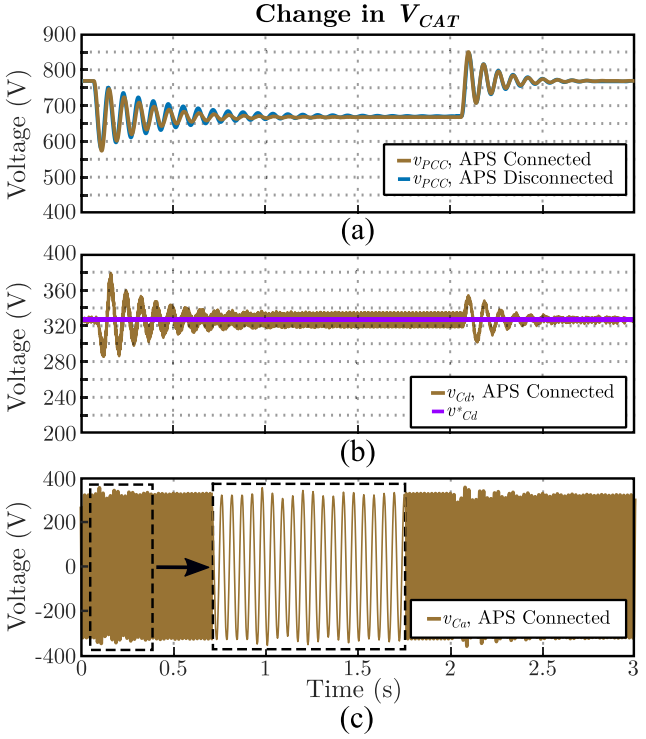


**FIGURE 13.** Comparison of the effect on $V_{PCC}$ of catenary voltage $V_{CAT}$ steps with and without the APS considering the worst case (maximum load $Z_{LO} = 3.2\ \Omega$ and maximum distance $Le_{CAT} = 4$ km). Catenary voltage steps from $V_{CAT} = 750$ V to $V_{CAT} = 650$ V at $t = 0.1$ s and from $V_{CAT} = 650$ V to $V_{CAT} = 750$ V at $t = 2$ s. (a) PCC voltage with and without APS, (b) $d$-axis output voltage with APS and (c) phase-a output voltage with APS.

comparison between the frequency response when the APS is not connected ($Z_{FCAT}/Z_{CPL}$) and when the APS is operating ($Z_S(s)/Z_{APS}(s)$) with the maximum auxiliary load ($Z_{LO} = 3.2\ \Omega$). The worst case has been considered (maximum distance, $Le_{CAT} = 4$ km, and minimum PCC voltage, $V_{PCC} = 650$ V). Fig. 11 shows that the designed controller meets the opposing-argument criterion for the input admittance/impedance, $Re(Z_S(s)Y_{APS-C}(s)) > -1/GM_{op}$.

Finally, Fig. 12 verifies that the maximum value of the sensitivity function is lower than the maximum specified in subsection IV-C, $|S_d|_{max} \leq 6$ dB. The maximum value of $S_d$ is given for no load ($Z_{LO} = \infty\ \Omega$) and maximum voltage ($V_{PCC} = 1000$ V).

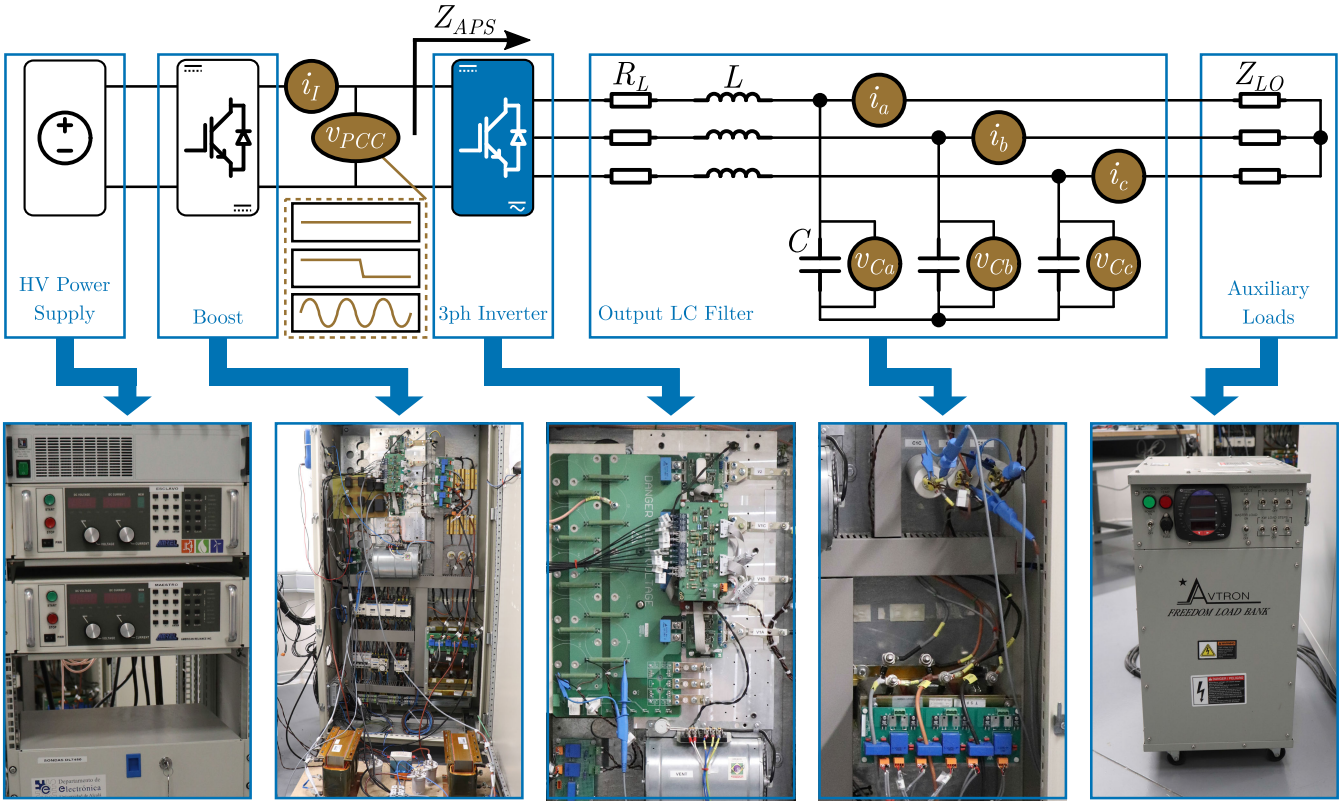


**FIGURE 14.** Experimental setup.

### B. SIMULATION RESULTS

Fig. 13 shows the system response to steps in the catenary voltage $V_{CAT}$. The negative impedance of the CPL is higher as the PCC voltage is lower. Therefore, the test is performed by setting the catenary voltage steps within a minimum range (650 V - 750 V) to assume the worst case. In addition, an auxiliary power load connected to the APS close to zero ($Z_{LO} = \infty\ \Omega$) is equivalent to assuming that the APS is disconnected from the system for the $V_{PCC}$ stability. Hence, the system has been evaluated assuming maximum auxiliary power load ($Z_{LO} = 3.2\ \Omega$).

Fig. 13.(a) shows the PCC voltage response to catenary voltage steps with and without the APS operating. Two catenary voltage steps has been tested: from $V_{CAT} = 750$ V to $V_{CAT} = 650$ V at $t = 0.1$ s and from $V_{CAT} = 750$ V to $V_{CAT} = 650$ V at $t = 2$ s. It can be observed that in both cases the PCC voltage oscillates in a underdamped way but stable, being the response with the APS opearting with full load slightly better than with only the CPL connected to the PCC. Fig. 13.(b) shows how the controlled output voltage $V_{C_d}$ tracks the output voltage reference $V^*_{C_d}$ with an underdamped transitory after the $V_{CAT}$ steps. Fig. 13.(c) shows how the a-phase output voltage is still correctly regulated after the voltage steps.

## VII. EXPERIMENTAL RESULTS

The proposed approach is experimentally evaluated with two different objectives. First, it is evaluated that the system complies with the european railway standards EN 50533 [51] and EN 61287 [10] under load changes and input voltage variations. Second, it is verified that the controlled inverter presents the modeled input impedance.

The experimental tests are carried out in the experimental setup shown in Fig. 14 whose main parameters are listed in Table 2. It consists of the following components:

- A dc voltage source based on 2 parallel-connected programmable dc power supplies.
- A boost dc/dc converter to emulate the dc catenary. The converter allows adding sinusoidal disturbance in the PCC for identifying the input impedance of the inverter and emulating the voltage jumps that usually occur in the catenary.
- A three-phase inverter acting as the railway auxiliary converter. It consists of a three-phase two-level voltage-source converter with an LC output filter.
- A programmable resistive load that emulates the auxiliary loads.

### A. PERFORMANCE TEST

The first series of experiments is intended to test whether the proposed controller meets railway standards EN 50533 and EN 61287. The standards specify that the converter output must be regulated at a line rms voltage of 400 V and frequency 50 Hz under load and input voltage variations within the power and input voltage ranges of the converter.

**TABLE 2. Main parameters of the experimental setup.**

| Variable | Symbol | Value |
|---|---|---|
| PCC voltage | $V_{PCC}$ | $650 - 800$ V |
| $d$-axis output voltage reference | $v^*_{Cd}$ | 326 V |
| Output LC-filter capacitor | $C$ | 40 $\mu$F |
| Output LC-filter inductance | $L$ | 3.4 mH |
| Output LC-filter resistance | $R_L$ | 47.4 m$\Omega$ |
| Auxiliary load | $Z_{LO}$ | $0 - 17.8$ $\Omega$ |

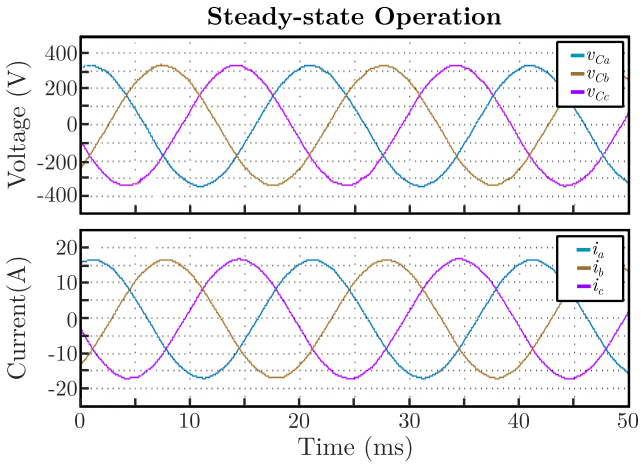


**FIGURE 15.** Output voltage $v_{C,abc}$ and current $i_{O,abc}$ in steady-state operation with an 8-kW load and an input voltage of 750 V.

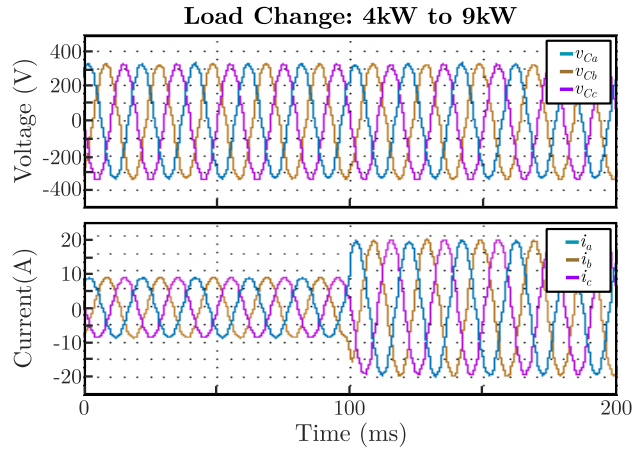


**FIGURE 16.** Output voltage $v_{C,abc}$ and current $i_{O,abc}$ when the load changes from 4 kW to 9 kW with an input voltage of 750 V.

Fig. 15 shows the results when the inverter is operating in steady state with an input voltage $V_{PCC} = 750$ V and feeds an 8 kW load. The total harmonic distortion in the voltage is $THD_v = 2.5$ %, lower than 8 % established in section 4.4 of the standard EN 50533 for linear loads.

Fig. 16 and Fig. 17 show how the controller regulates undisturbed the output voltage in case of load jumps, in compliance with section 4.8 of the standard EN 50533 for power steps. In Fig. 16, the controlled inverter perfectly responds in case of a load step from 4 kW to 9 kW without appreciating any variation in the output voltage. A similar response is

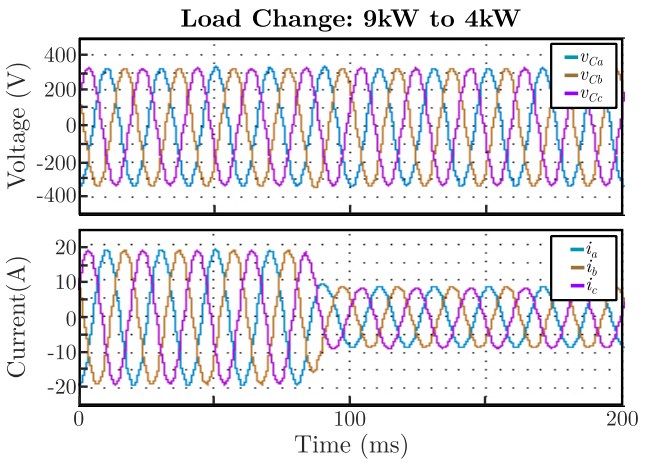


**FIGURE 17.** Output voltage $v_{C,abc}$ and current $i_{O,abc}$ when the load changes from 9 kW to 4 kW with an input voltage of 750 V.

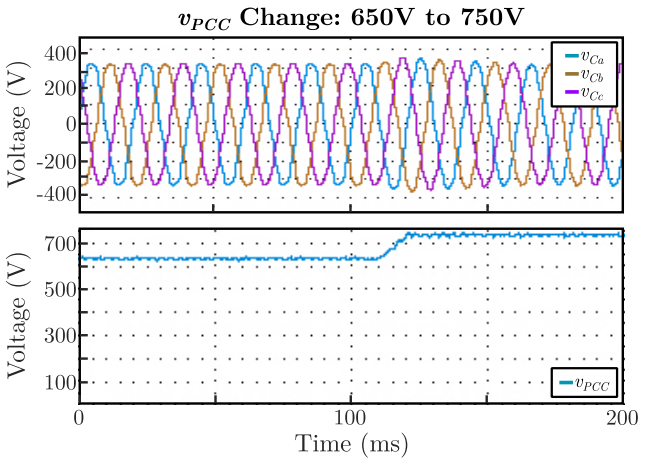


**FIGURE 18.** Output voltage $v_{C,abc}$ and PCC voltage $v_{PCC}$ for an input voltage step from 650 V to 750 V.

obtained with a load step from 9 kW to 4 kW as presented in Fig. 17. In both cases it can be observed that the variation in the output voltage is practically negligible, clearly complying with the standard, which establishes up to 40 % of permissible variation with respect to the rated value in the event of power steps from 0 % to 100 %.

Finally, Fig. 18 and Fig. 19 show as the output voltage reaches the nominal value after an input voltage step from 650 V to 750 V and from 750 V to 650 V, respectively. In both cases, the output voltage returns to nominal ratings in less of 100 ms that is maximum time specified in section 4.5.3.20 of the standard EN 61287 after an input voltage step.

Similar results in terms of time domain specifications could be obtained with a traditional controller such as a PI structure. However, due to its low order, it would not be able of shaping the dc input admittance to comply with impedance-stability criteria. More complex traditional control structures could shape this admittance but dealing with a high complex design process that could result in a high-order

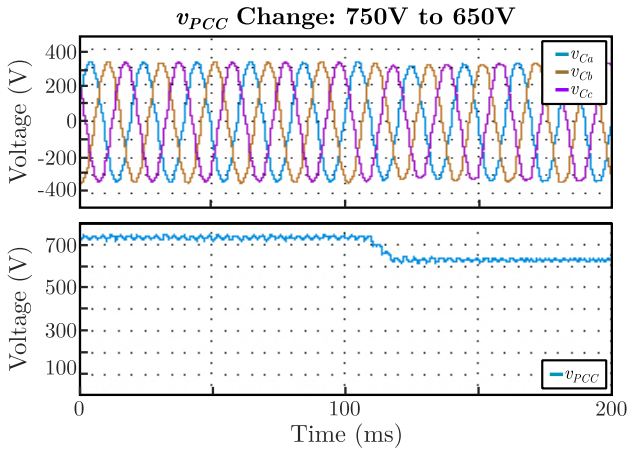


**FIGURE 19.** Output voltage $v_{C\_abc}$ and PCC voltage $v_{PCC}$ for an input voltage step from 750 V to 650 V.

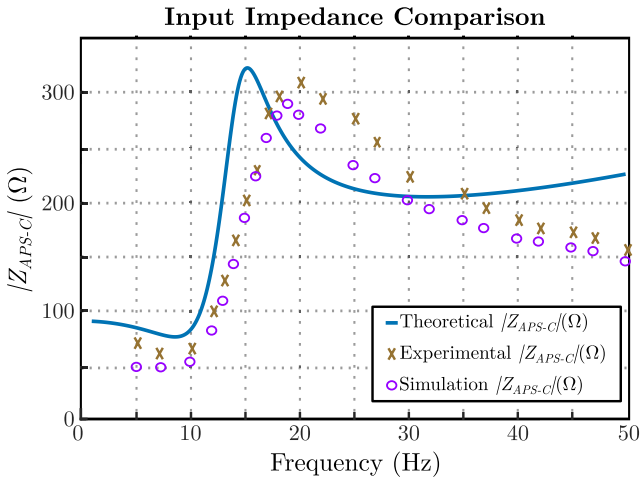


**FIGURE 20.** Comparison among the obtained closed-loop input impedances $|Z_{APS-C}|$: theoretical (solid blue line), in simulation (purple circles) and experimental (brown crosses).

controller considering the multiple specifications and the uncertain model.

### B. INPUT IMPEDANCE VERIFICATION

The input impedance of the inverter $Z_{APS}$ must meet both the opposing argument criterion defined in Section IV with respect to the catenary output impedance $Z_S$ and a gain margin $GM_{op}$ lower than 6 dB. That implies a high value of the input impedance at 12 Hz, where the resonance of the input LC filter is maximum.

The experimental identification of the input impedance is made considering a frequency sweep $f_d = [5 - 50]$ $Hz$ and a power load of 8 kW. The boost dc/dc converter that emulates the catenary adds a constant-amplitude sinusoidal disturbance with frequency $f_d$ to the dc voltage. The PCC voltage $V_{PCC}$ and the inverter input current $i_I$ are acquired using an oscilloscope and then analyzed by applying an FFT algorithm to obtain their harmonic spectrum. The impedance at frequency $f_d$ is given by dividing the magnitude of the PCC voltage by the magnitude of the input current at frequency $f_d$, $Z_{APS}(f_d) = |v_{PCC}(f_d)| \,/\, |i_I(f_d)|$.

Fig. 20 shows a comparison among the theoretical frequency-shaped impedance (solid blue line) and the obtained in simulation (purple circles) and experimentally (brown crosses). Results successfully comply with impedance restrictions inherited from impedance criteria. A small deviation in module can be observed in certain frequencies due to model mismatching and measurement noise.

## VIII. CONCLUSION

This article has addressed the stability problem in railway catenary with CPL behaving converters connected to their PCC. The approach consists in the QFT-based design of a voltage controller for the APS converter that ensures stability at the PCC of the catenary by meeting an impedance-based stability criterion. The proposed QFT voltage controller shapes the dc input admittance of the APS converter without a feedback loop on the dc side while tracking the ac output voltage reference and provides robustness to unmodeled uncertainties. To meet these three specifications at the same time will be not possible applying a classical PI controller due to its lack of controller order that reduces the design degrees-of-freedom below the needed to meet impedance-criteria or forcing to severely reduce tracking performance. More complex classical control approaches could deal with the design but at the cost of a cumbersome design process and resulting in high-order controllers. QFT proves to be a powerful tool in the design of controllers with multiple specifications and high variability in plant parameters. Additionally, this paper has provided an algorithm to include in the QFT the input admittance specification to meet impedance-based stability criteria. Experimental results have verified that the proposed QFT voltage controller complies with the European railway standards and that correctly shapes the specified dc input impedance.

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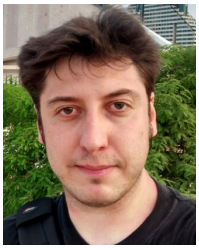

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