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Dual-Mode Supply Modulator IC With an Adaptive Quiescent Current Controller for Its Linear Amplifier in LTE Mobile Power Amplifier

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ABSTRACT This article presents a hybrid envelope tracking (ET) supply modulator (SM) integrated circuit (IC) based on a Class-AB linear amplifier (LA) with supply voltage and temperature insensitive quiescent current. For ET mode, to further improve efficiency of the ET-SM, the supply voltage of the LA can be modulated using an additional dc-dc converter according to the average output power. An adaptive quiescent current controller for the LA of the ET-SM is proposed to maintain its quiescent current for large variations in voltage and temperature. Due to the insensitive quiescent current over the voltage of the LA, the supply voltage to the LA can be controlled in a wider range for the average output power, which allows the power amplifier (PA) in the ET mode to have a greater improvement in efficiency. The size of the output stage of the LA is also discretely reconfigured using 3-bit digital control to reduce the power consumption of the LA according to the output power level. For the low average output power levels, the operation mode is changed to APT mode, which supplies a reduced dc voltage according to the reduced average output power to the PA. The proposed SM, dc/dc converter and PA ICs were designed and implemented using CMOS processes for 0.9 GHz LTE application. Using an LTE uplink signal with a signal bandwidth of 5 MHz and a PAPR of 7.5 dB, a PAE of 38.4% at an average output power of 24.0 dBm was obtained under an ACLR of −30.0 dBc for the overall ET-PA. At a 6 dB back-off for the average output power, a PAE of 24.6% was achieved using the ET mode. A maximum PAE improvement of 8.0% point using the proposed SM IC was achieved compared to the stand-alone PA.

INDEX TERMS Power amplifier integrated circuit, supply modulator, envelope tracking, average power tracking, dual-mode power amplifier.

I. INTRODUCTION

Since power amplifiers (PAs) consume large amount of power in RF front-end, they require high-efficiency characteristics. High-efficiency PAs can save the battery life of mobile devices, which can lead to enhanced user convenience. Since recent communication standards also require very high linearity characteristics, PAs should operate at large back-off power levels to comply to the linearity requirements. Furthermore, when the device is located near the base station, the output power can be backed off to lower the power consumption. As the back-off increases, the efficiency of the PA rapidly decreases. Accordingly, efficiency improvement in the wide output power range becomes more and more interested.

Supply modulator (SM) is an auxiliary circuit for reducing the dc power dissipation of the PA by modulating the

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supply voltage of the PA according to the envelope or the average power of the RF signal. Supply modulation techniques, such as envelope tracking (ET) [1]–[31], dynamic supply switching (DSS) [32], and average power tracking (APT) [34], have been widely used to improve the efficiency of PAs. The ET-PA has a large efficiency improvement in high output power region, but the amount of efficiency improvement decreases in the low output power region due to the low efficiency of the linear amplifier (LA). Though the APT-PA has little efficiency improvement in the high output power region, it can have even higher efficiency than that of the ET-PA in the low output power region due to the highly efficient dc-dc converter for the APT operation. Therefore, dual-mode supply modulation techniques adopting the ET and APT modes have been reported to have improved efficiency of the PA in wider output power range [9]–[11].

The SM presented in [9] adopts the ET and APT modes to optimize the efficiency of the PA at both low and high output power ranges. The size of the switching amplifier (SA) was also changed according to the operation mode to optimize the efficiency. In [10], [11], a buck-boost converter was adopted to supply a voltage to the linear amplifier (LA) in the ET mode and to directly supply its output to the PA in the APT mode for dual-mode operation. Efficiency of the SM was maintained over 80% in spite of wide variation of the battery voltage.

The hybrid ET-SM includes an LA that steadily consumes power even when the output power of the SM is decreased from the peak. Hence, the efficiency of the SM can be seriously degraded, particularly when the average output power is backed off. To address this issue, supply voltage of the LA can be reduced as the average power is reduced [12]–[14]. In [12], a method of switching the supply voltages from 5 to 2.5 V was proposed to improve its efficiency in the low output power region. An additional operational transconductance amplifier (OTA) for a supply voltage of 2.5 V was designed to maintain the Class-AB bias of the output stage. However, this method can increase complexity of the circuit. In [13], envelope voltage with reduced bandwidth is supplied to the LA using a second SA. As a result, the efficiency of the LA can be improved by reducing the power dissipation of PMOS and NMOS switches of the output stage.

Supply voltage of the LA can be reduced according to the average output power using an additional dc-dc converter [14]. A voltage-independent structure for maintaining the Class-AB operation condition of the LA was also introduced. In [15], an accurate quiescent current controller for the 3-stage LA to protect the LA bias condition from the process and supply voltage variations was proposed. However, the proposed circuit allows only a narrow range of the supply voltage variation (from 3.5 to 3.7 V) for the LA. In addition, the quiescent current of the LA is still sensitive to temperature changes. Previous studies, including [9]–[15], still have not presented compensation method for changes of the quiescent current in response to the temperature variation.

This article presents a dual-mode supply modulator IC using a supply voltage and temperature insensitive LA. To enhance the efficiency of the ET-PA, the supply voltage to the LA is modulated according to the average output power level using a dc-dc converter. An adaptive quiescent current controller is also included in the LA to minimize the quiescent current variation of the LA for large variations of supply voltage and temperature. With this controller, the LA can operate even with very low supply voltage, which allows the SM to have high efficiency in the wider output power range. The output stage of the LA should be designed with a sufficient width of the transistor to handle its large peak current. However, when the output power of the SM is reduced, a large transistor width having large quiescent current can degrade efficiency of the LA. For the proposed LA, the output stage is designed to be reconfigurable according to the output power for additional efficiency improvement. A 3-bit digital control is adopted to reconfigure the output stage to reduce the dc power dissipation at the low output power region. As the output power gets even lower, the LA and SA are turned off and the PA is supplied by the dc-dc converter for the APT operation. This article is an extended version of the previous work [24]. The essential analysis based on dc and envelope simulations for the proposed adaptive controller is newly included. In addition, the topologies and efficiency improvement mechanism of the reconfigurable output stage and the CMOS PA are described. More measurement data are included. The comparison table is updated including more performances and features of this work and the related works.

For verification, the SM, dc-dc converter and PA ICs were implemented using CMOS processes. An off-chip balun was adopted for the output matching network of the two-stage differential PA. Simulated and experimental results will be presented and compared to the previous works examining this topic.

II. ANALYSIS AND DESIGN OF DUAL-MODE SUPPLY MODULATOR IC

A. DUAL-MODE OPERATION WITH ENHANCED LA

Fig. 1 shows schematic diagrams to illustrating the dual-mode operation, with the ET mode in (a) and the APT mode in (b). For the ET mode, the LA and SA are connected in parallel for the hybrid SM. The SM amplifies an envelope voltage of the input RF signal (V_{ENV}). The high frequency current from the LA and the low frequency current from the SA are combined and supplied to the PA. As a result, the supply voltage of the PA is dynamically modulated in the time domain. Efficiency of the SM-PA (η_{SM-PA}) is obtained as follows.

$$\eta_{SM-PA} = \eta_{SM} \cdot \eta_{PA} \tag{1}$$

where η_{SM} and η_{PA} are the efficiencies of SM and PA, respectively. To increase η_{SM-PA}, η_{PA} needs to be increased by effectively modulating the PA supply voltage and η_{SM} needs to be increased through improving efficiency of the LA or SA.

At the maximum average output power of the PA, the SM generates V_{pa} which has a voltage swing with a range of from

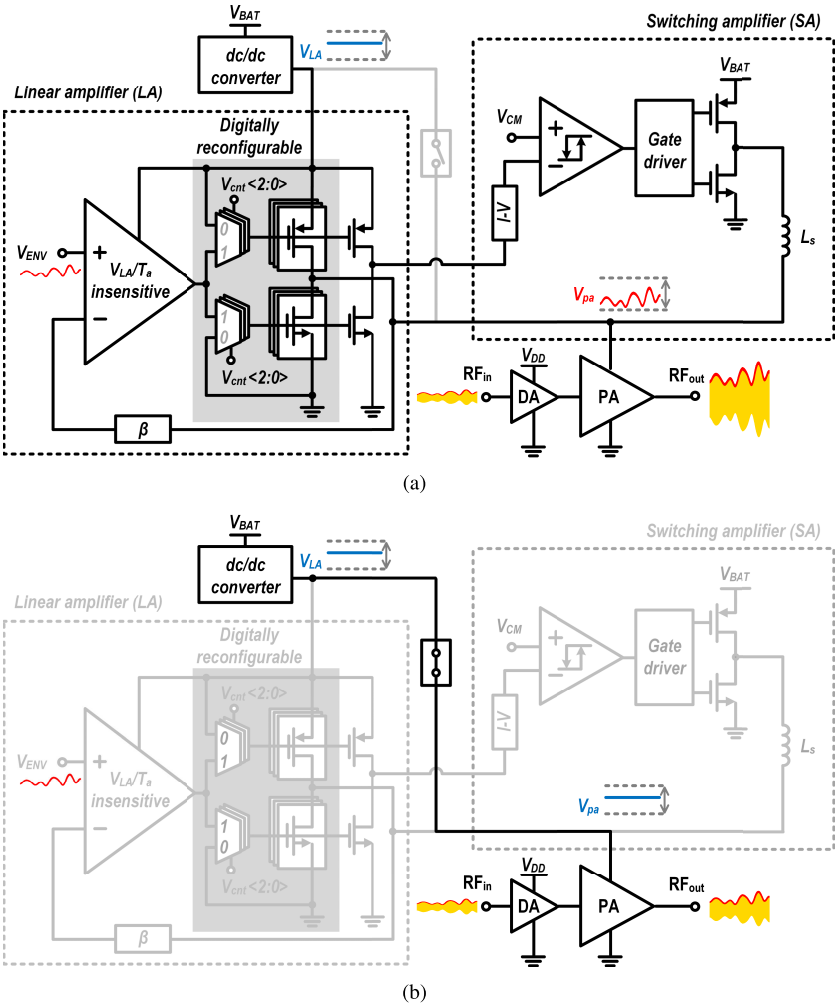


FIGURE 1. Diagrams for the dual-mode operation for the SM-PA: (a) ET mode, (b) APT mode.

the offset voltage (about 0.5 V) to $V_{pa,peak}$ (generally V_{BAT}-0.3 V) [16]. At the average output power back-off region, the V_{pa} swing is reduced by controlling the V_{ENV}. However, the efficiency of LA having a reduced voltage swing of V_{pa} decreases, which degrades the efficiency of the ET-PA. Since the ET mode cannot maintain its capability of efficiency improvement in a wide output power range, the operation mode needs be switched to the APT mode. To mitigate the efficiency degradation of the ET mode, the supply voltage of the LA (V_{LA}) can be reduced to improve the efficiency of the LA as the average output power back-off (P_{OBO}) increases. A dc-dc converter can be used to generate the variable voltage (V_{LA}).

To make the V_{LA} modulation wider and more effective, the LA is required to have a normal operation in a V_{LA} range as wide as possible. In addition, temperature (T_a) variation also affects the LA performances. The proposed LA was designed to maintain its quiescent current ($I_{q,LA}$) over wide ranges of V_{LA} and T_a. In the section II-B, the transistor-level schematics and the simulation results will be presented. The output stage of the LA is designed to be discretely reconfigurable according to the output power level. As the output power of the PA decreases, the size of the output stage is reduced by using the digital control signal of V_{cnt} to reduce the power consumption of the LA. This will be further explained in the section II-C.

The SA includes a hysteresis comparator, an anti-shoot through gate driver, and power switches. The comparator determines increase or decrease for the output current of the SA through the reference signal from the LA. When the output current needs to be increased, the gate driver turns PMOS on. While the output current needs to be decreased, it turns NMOS on. To prevent the shoot-through current for the power switches, the gate driver provides a short delay between the turn-on transitions.

For the further lower output power region, both LA and SA are turned off, and the output voltage of the dc-dc converter is directly supplied to the PA, as illustrated in Fig. 1(b). Using a highly efficient dc-dc converter, the V_{pa} can be modulated according to the average output power. In the very low output

power region, it is expected that the efficiency of the APT-PA can exceed that of the ET-PA.

Fig. 2 shows the expected efficiency curves according to the output power of the PA: (a) SM and (b) SM-PA. By applying the V_{LA} modulation and output stage reconfiguration techniques, the proposed ET-SM with the improved LA can have higher efficiency at the output power back-off levels than the conventional ET-SM has. Based on the dual-mode operation, efficiency of the SM-PA can be improved in all output power regions compared to that of the stand-alone PA, as shown in Fig. 2(b). Due to the improved efficiency of the proposed ET-SM, the power region for the ET mode can be further extended. As a result, higher efficiency characteristics can be obtained around at the mid-power region.

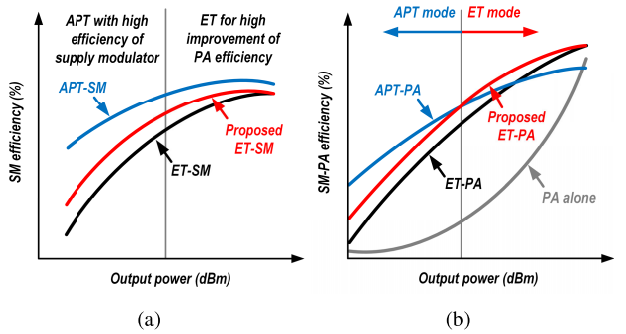


FIGURE 2. Efficiency curves according to the output power of the PA: (a) SM and (b) SM-PA.

Table 1 summarizes the configurations of the SM according to the P_{OBO}. $W_{l,p}$ and $W_{l,n}$ are the widths of the PMOS and NMOS for the output stage of the LA, respectively. As P_{OBO} increases from 0 to 6 dB, V_{LA} and W_l are gradually decreased to reduce the power consumption of the LA. For a P_{OBO} of no less than 7 dB, all 3 bits of V_{cnt} are set as 'L' to turn off the LA for APT mode operation.

TABLE 1. Configurations of the SM according to the output back-off levels.

P_{OBO} (dB)	V_{LA} (V)	V_{cnt} <2>	V_{cnt} <1>	V_{cnt} <0>	$W_{l,p}$ (μm)	$W_{l,n}$ (μm)	Mode
0	V_{BAT}-0.1	H	H	H	11,900	5,950	ET
1	V_{BAT}-0.2	H	H	L	10,200	5,100	ET
2	V_{BAT}-0.3	H	L	H	8,500	4,250	ET
3	V_{BAT}-0.4	H	L	L	6,800	3,400	ET
4	V_{BAT}-0.5	L	H	H	5,100	2,550	ET
5	V_{BAT}-0.6	L	H	L	3,400	1,700	ET
6	V_{BAT}-0.7	L	L	H	1,700	850	ET
>7	<V_{BAT}-0.8	L	L	L	X	X	APT

B. LA INSENSITIVE TO SUPPLY VOLTAGE AND TEMPERATURE

To make the LA work properly, the $I_{q,LA}$ of the LA output stage should be maintained according to the wide V_{LA} variation. If it is changed to be larger than the optimized $I_{q,LA}$, efficiency of the LA decreases. Or if it becomes smaller, the envelope cannot be linearly amplified, which can result in distortion in V_{pa}. This section will explain the design of the LA which is insensitive to V_{LA} and T_a variations.

Fig. 3 shows a schematic of the proposed V_{LA} and T_a insensitive LA consisting of the input, buffer, and output stages. The input stage consists of the complementary N-P differential pairs for constant-g_m and has a folded cascode structure with high gain. The buffer stage is designed with two source followers biased with I_b to drive a large output stage. I_b is the bias current which is independent of V_{LA} and T_a. The output stage is composed of Class-AB common-sources for rail-to-rail output swing and high-efficiency characteristics.

While V_{LA} changes, the potential of the sources of the buffer stage changes. In addition, the drain-to-source voltage of the transistors in the buffer stage is changed for T_a variation. These two variations change the gate-to-source dc voltage of the output stage, which can lead to a change in $I_{q,LA}$. As the V_{LA} is decreasing or the T_a is increasing, $I_{q,LA}$ decreases, which indicates that the bias state of the output stage shifts from Class-AB to -B. Since the output stage having low $I_{q,LA}$ cannot linearly amplify the envelope, V_{pa} can be distorted. The LAs in the previous literatures [13], [14] used a floating Class-AB control circuit in which PMOS and NMOS are connected in parallel to maintain the bias state of the output stage. Based on these works, a design including the V_{LA} sensing and Ta compensation circuits is proposed in this work. As a result, the $I_{q,LA}$ can be maintained over wide ranges of both V_{LA} and T_a.

Fig. 4 shows a schematic of the proposed adaptive quiescent current controller. $M_{s,p}$ and $M_{s,n}$ are stacked with a diode-connected transistor to sense the varying V_{LA}. $M_{f,p}$ and $M_{f,n}$ are connected in parallel and inserted between the source terminals of the buffer stage. These two transistors constitute a floating current source which adjusts the biasing current of the buffer stage. For a constant current I_b, $I_{X,P}$ and $I_{X,N}$ satisfy the following relationship with I_Y which is the dc current flowing through the floating current source.

$$I_{X,P} = I_{X,N} = I_b - I_Y, \tag{2}$$

which indicates that $I_{X,P}$ and $I_{X,N}$ decrease as I_Y increases. For variation in V_{LA} and T_a, I_Y can be controlled to adjust $I_{X,P}$ and $I_{X,N}$.

Fig. 5 shows the simulated dc voltages and currents of an adaptive $I_{q,LA}$ controller according to V_{LA}. The gates of $M_{s,p}$ and $M_{s,n}$ are connected to ground and V_{LA}, respectively. A V_{LA} decrease reduces the magnitudes of their gate-to-source voltages and increases each of the drain-to-source voltages ($V_{SEN,P}$ and $V_{SEN,N}$). This also leads to an increase of I_Y which is the current of the floating current source. From (2), increasing I_Y leads to decreasing $I_{X,P}$ and $I_{X,N}$. In the case without the $I_{q,LA}$ controller, $I_{X,P}$ and $I_{X,N}$ are constant. Then, the source-to-gate dc voltage of PMOS ($V_{SG,P}$) and the gate-to-source dc voltage of NMOS ($V_{GS,N}$) in the

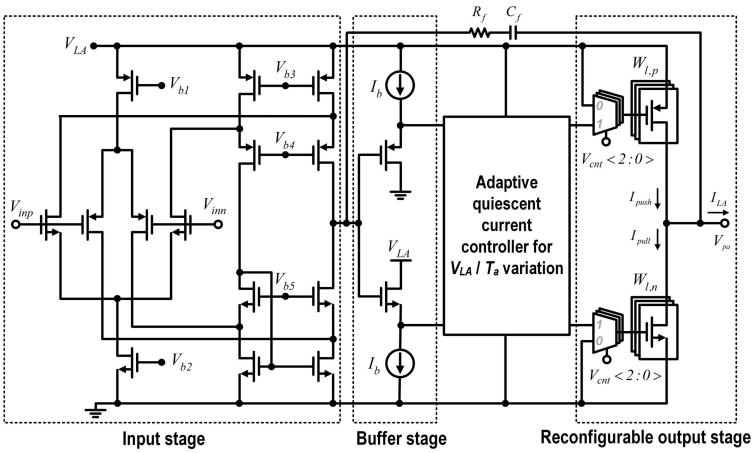


FIGURE 3. Schematic of the proposed supply voltage and temperature insensitive LA.

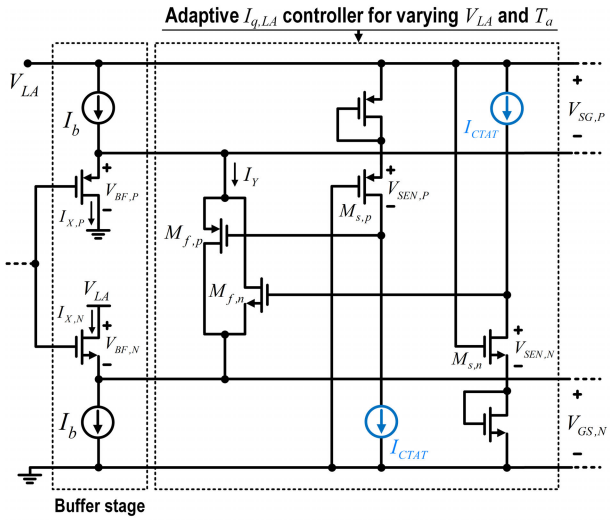


FIGURE 4. Schematic of the proposed adaptive quiescent current controller.

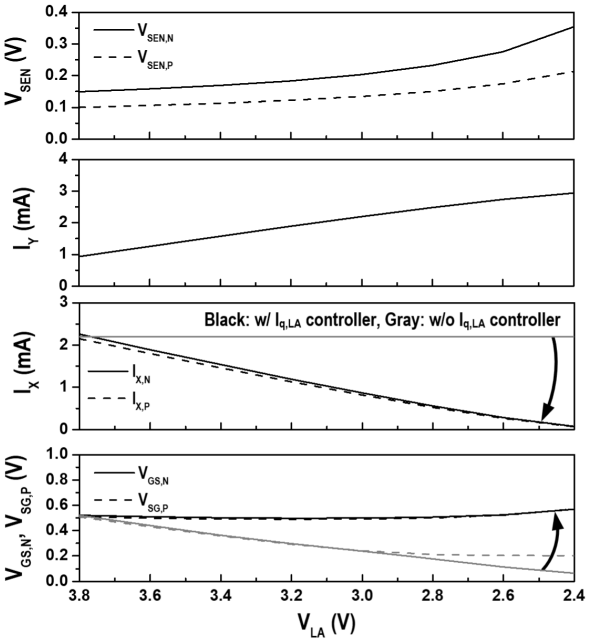


FIGURE 5. Simulated dc voltages and currents of an adaptive $I_{q,LA}$ controller according to V_{LA}.

output stage are written as follows.

$$V_{SG,P} = V_{LA} - V_{BF,P}, \tag{3}$$

$$V_{GS,N} = V_{LA} - V_{BF,N}, \tag{4}$$

where $V_{BF,P}$ and $V_{BF,N}$ are the source-to-drain dc voltage of PMOS and the drain-to-source dc voltage of NMOS in the buffer stage, respectively. To maintain the $I_{q,LA}$ of the output stage, $V_{SG,P}$ and $V_{GS,N}$ need to be constant. In other words, when the V_{LA} decreases, $V_{BF,P}$ and $V_{BF,N}$ need to be decreased at the same rate, as indicated in (3) and (4). By optimizing the negative slopes of $I_{X,P}$ and $I_{X,N}$ for decreasing V_{LA}, the rates of decrease of $V_{BF,P}$ and $V_{BF,N}$ can be almost identical to that of V_{LA}. As a result, the changes in $V_{SG,P}$ and $V_{GS,N}$ are reduced from 0.3 and 0.46 V to 0.06 and 0.05 V, respectively.

If the buffer stage and the floating current source are temperature-sensitive, $I_{q,LA}$ can also vary. To compensate for the temperature variation, the bias currents of the sensing transistors ($M_{s,p}$, $M_{s,n}$) were be generated by a complementary to absolute temperature (CTAT) current generator [36]. The slope of I_{CTAT} for T_a compensates for the variation in $I_{q,LA}$ according to the temperature.

Fig. 6 shows the simulated dc voltages and currents of the adaptive $I_{q,LA}$ controller according to T_a. When the T_a varies from −40 to 85 °C, I_{CTAT} varies from 161 to 76 μA. The slope of I_{CTAT} derives the slope of I_Y from the changes in $V_{SEN,P}$ and $V_{SEN,N}$. From (2), the increase of I_Y causes decreases in $I_{X,P}$ and $I_{X,N}$, which in turn leads to decrease in $V_{BF,P}$ and $V_{BF,N}$. In the case without the $I_{q,LA}$ controller, $I_{X,P}$ and $I_{X,N}$ are designed to be constant. $V_{SG,P}$ and $V_{GS,N}$, which can be changed according to T_a, are compensated using

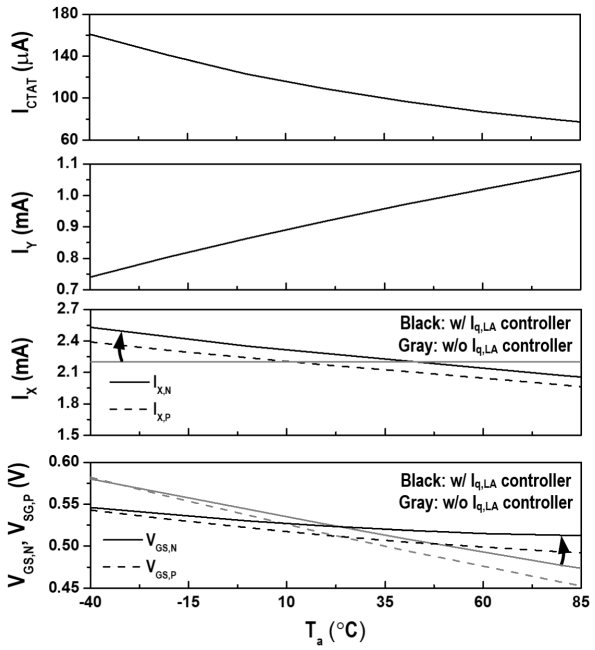


FIGURE 6. Simulated dc voltages and currents of the adaptive $I_{q,LA}$ controller according to T_a.

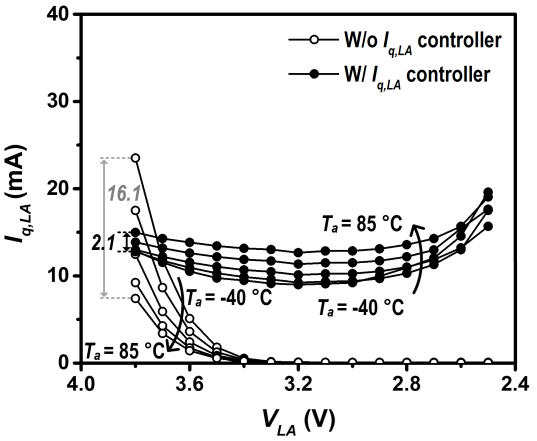


FIGURE 7. Simulated $I_{q,LA}$ with and without the adaptive $I_{q,LA}$ controller according to the V_{LA} and T_a variation.

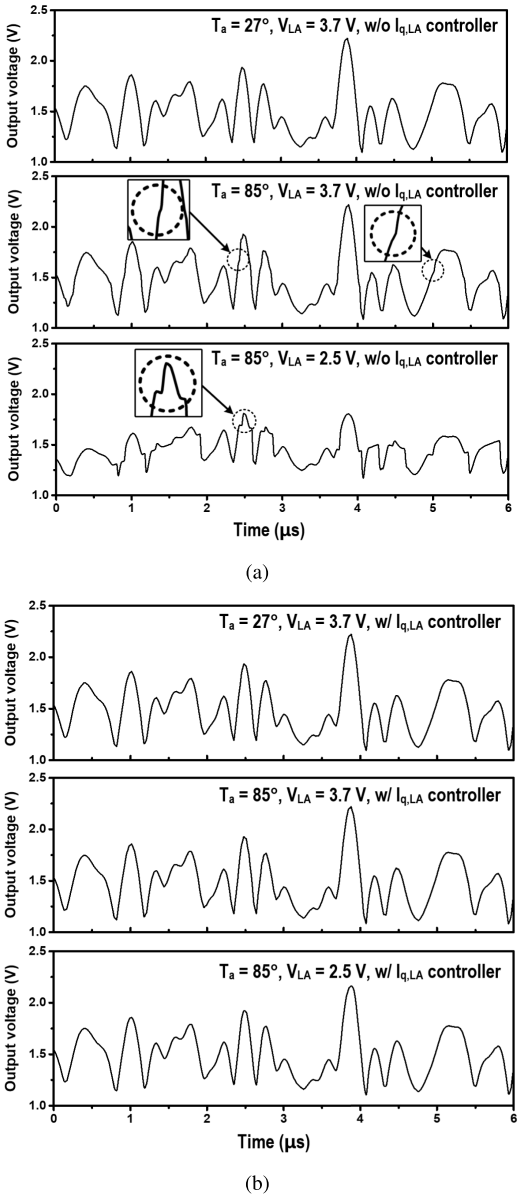


FIGURE 8. Simulated output voltage waveforms of the SM for variations in V_{LA} and T_a: (a) without $I_{q,LA}$ controller, (b) with $I_{q,LA}$ controller.

appropriately optimized slopes of $I_{X,P}$ and $I_{X,N}$. As a result, the changes in $V_{SG,P}$ and $V_{GS,N}$ are reduced from 0.14 and 0.12 V to 0.05 and 0.03 V, respectively.

Fig. 7 shows the simulated $I_{q,LA}$ with and without the adaptive $I_{q,LA}$ controller according to the various values of V_{LA} (3.8 to 2.5 V) and T_a (−40 to 85 °C). Without the adaptive $I_{q,LA}$ controller, $I_{q,LA}$ rapidly decreases as V_{LA} decreases and as T_a increases. If V_{LA} drops below 3.4 V, $I_{q,LA}$ decreases below 1 mA with serious nonlinear operation. In addition, if T_a changes from −40 to 85 °C at a V_{LA} of 3.8 V, $I_{q,LA}$ changes up to 16.1 mA. With an adaptive $I_{q,LA}$ controller, the variation remains within 5 mA when V_{LA} is lowered from 3.8 to 2.5 V. In addition, if T_a changes from −40 to 85 °C under a V_{LA} of 3.8 V, $I_{q,LA}$ only changes up to 2.1 mA. After applying the adaptive $I_{q,LA}$ controller, the $I_{q,LA}$ values are configured within the range of from 10 to 15 mA for large variations in V_{LA} and T_a.

Fig. 8 shows the simulated output voltage waveforms of the SM for variations in V_{LA} and T_a with and without the $I_{q,LA}$ controller. As shown in Fig. 8(a), without the $I_{q,LA}$ controller, the LA linearly amplifies the envelope with an $I_{q,LA}$ of 14 mA under a V_{LA} of 3.7 V and a T_a of 27 °C. When the T_a increases to 85 °C, the bias current of the LA is changed for deeper Class-AB having an $I_{q,LA}$ of 7.4 mA. Accordingly, some distortions on waveforms can be observed especially at the on/off transition time of PMOS and NMOS switches in the output stage. If V_{LA} is reduced to 2.5 V, the LA operates under Class-C condition. The output voltage becomes significantly

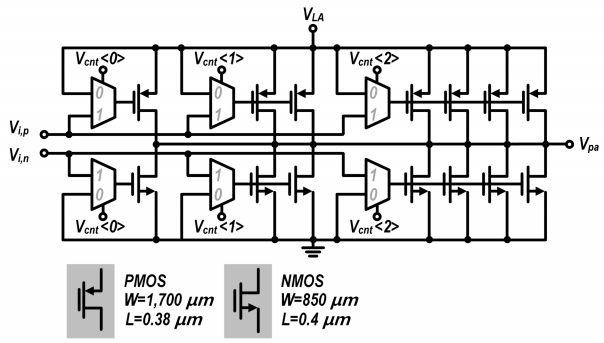


FIGURE 9. Schematic of the reconfigurable output stage of the LA.

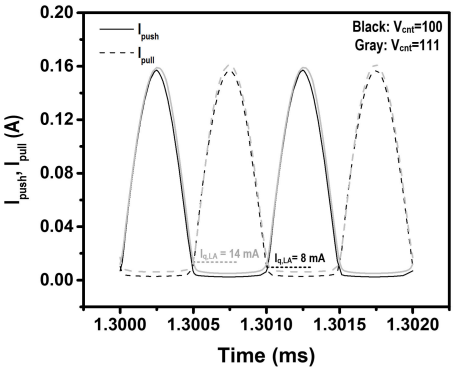


FIGURE 10. Simulated I_{push} and I_{pull} for cases of V_{cnt} set to 'HHH' and 'HLL.'

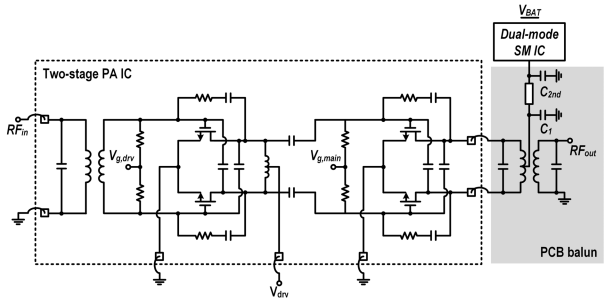
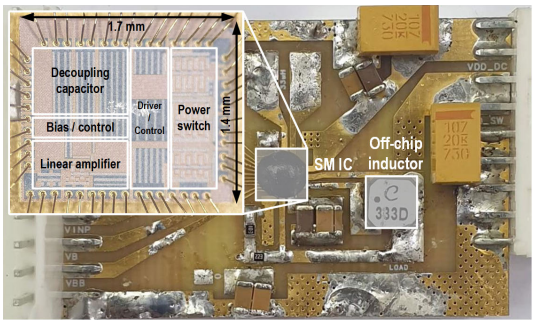


FIGURE 11. Schematic of two-stage CMOS PA IC with a dual-mode SM IC.

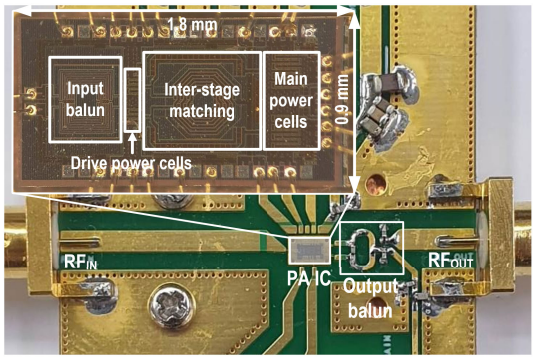
distorted compared to the input envelope. The peak-to-peak voltage swing is reduced and severe waveform distortion can be observed at the on/off transition time. A decrease in $V_{pa,peak}$ can reduce the output power and gain of the PA. The waveform distortion can worsen the linearity of the PA. As shown in Fig. 8(b), with the $I_{q,LA}$ controller, the output voltage waveforms of the LA are maintained for large variations in V_{LA} and T_a. Therefore, with the $I_{q,LA}$ controller, V_{LA} can be modulated without distortion for improved efficiency of the PA.

C. RECONFIGURABLE OUTPUT STAGE OF THE LA

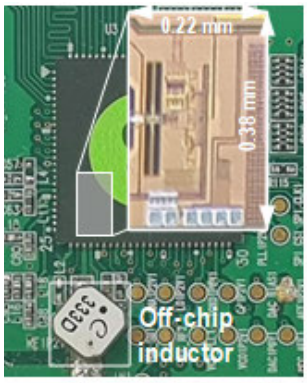
Fig. 9 shows the schematic of the reconfigurable output stage of the LA using 3-bit digital signal. The width and length of the unit PMOS are 1,700 and 0.38 μm, respectively, while



(a)



(b)



(c)

FIGURE 12. Photographs of the implemented ICs and evaluation boards: (a) dual-mode SM, (b) two-stage PA, and (c) dc-dc converter.

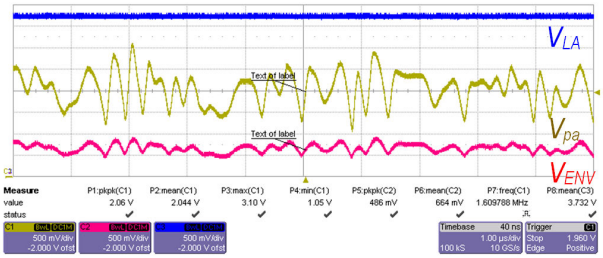
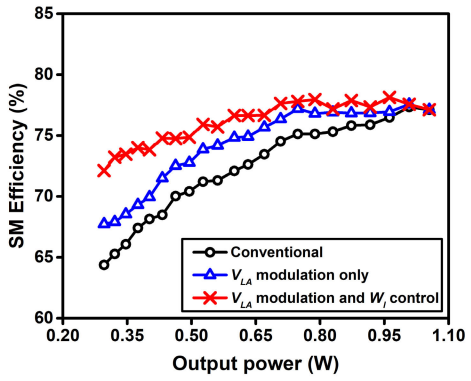
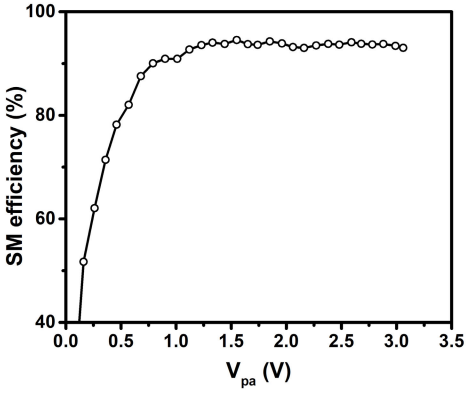


FIGURE 13. Measured waveforms from the implemented SM IC using the LTE signal.

those of the unit NMOS are 850 and 0.4 μm, respectively. The multiplexer connects the input signals of $V_{i,p}$ and $V_{i,n}$ to the gates of PMOS and NMOS when the selection signal is 'H.' If the selection signal is 'L,' the gate of PMOS is connected

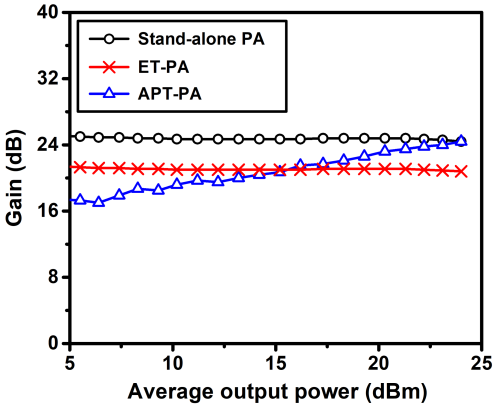


(a)

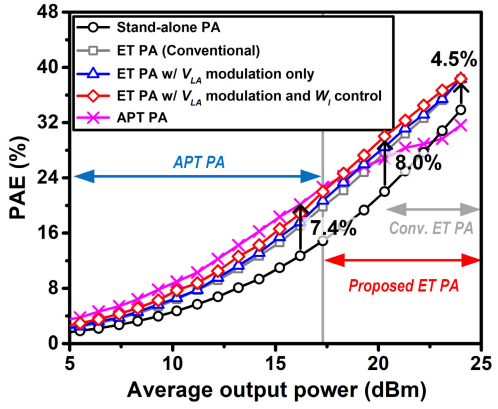


(b)

FIGURE 14. Measured SM efficiency: (a) ET mode using the LTE signal, (b) APT mode.



(a)



(b)

FIGURE 15. Measured performances of the stand-alone PA and the SM-PA using the LTE signal: (a) gain, (b) PAE.

to V_{LA} and the gate of NMOS is connected to ground to turn it off. The output stage is designed with a maximum PMOS width of 11.9 mm and an NMOS width of 8.95 mm to drive a current of over 400 mA. By using the 3-bit digital control signal of $V_{cnt}\langle 2{:}0\rangle$, 7 units of PMOS and NMOS can be discretely turned on/off.

Fig. 10 shows the simulated I_{push} and I_{pull} for cases of V_{cnt} set to 'HHH' and 'HLL' using a 1 MHz continuous wave as an input. The output stage set to have maximum width consumes a large $I_{q,LA}$ of 14 mA even with a Class-AB operation condition. As the output power of the SM decreases, the proportion of $I_{q,LA}$ in the dc power consumption of the SM increases. In the low output power region of the PA, there is also a reduction in the peak output current by the LA. Thus, the large-size output stage is not required any more. Accordingly, as the output power of the PA decreases, the size of the output stage can be reduced to decrease $I_{q,LA}$ using the proposed size reconfiguration technique.

III. IMPLEMENTATION OF SM WITH CMOS PA

A. SM WITH TWO-STAGE CMOS PA IC

Fig. 11 shows a schematic of the two-stage CMOS PA IC with the dual-mode SM IC for the 900 MHz frequency band. For high power gain, each stage has a differential structure with cross-coupled capacitors for both 1^{st} and 2^{nd} stages. In addition, RC feedback networks are also included to stabilize the PA. The input impedance is matched using an on-chip balun. For inter-stage matching, two series capacitors and one shunt inductor with a center tap are used. The output matching network is designed using a low-loss off-chip balun on a printed circuit board (PCB). The output of the SM is connected to the PA through the center tap in the primary turn of the balun. The 2^{nd} harmonic load impedance for the 2^{nd} stage is controlled by C_{2nd} and C_1.

B. IMPLEMENTATION

Fig. 12 shows photographs of the implemented ICs and evaluation boards: (a) dual-mode SM, (b) two-stage PA and (c) dc-dc converter. The SM and dc-dc converter ICs were fabricated using a 65 nm CMOS process. Their sizes are 1.7×1.4 and 0.22×0.38 mm^2, respectively. The PA IC was fabricated using a 180 nm CMOS process and its size is 1.8×0.9 mm^2. An off-chip balun was designed using a 4-layer FR4 PCB. The I/O pins of the SM and PA ICs were

TABLE 2. Performance summary and comparison to the previously reported SM-PAs.

Ref.	Freq. (MHz)	P_{out} (dBm)	PAE (%)			Gain (dB)	ACLR (dBc)	EVM (%)	V_{BAT} (V)	Process		Fetures
			0 dB OBO	6 dB OBO	10 dB OBO					SM	PA (Configuration)	
[3]	1.90	24.6	26.0	13.0*	7.0*	14.0*	N/A**	4.4	3.6	0.35-μm SiGe BiCMOS	0.35-μm SiGe BiCMOS (One-stage)	Fully integrated ET-PA in one chip
[4]	1.85	26.0	34.1	22.0*	12.5*	N/A	-34.2	2.8	5.0	0.18-μm CMOS	0.18-μm CMOS (One-stage)	Source/load harmonic control, off-chip output balun
[5]	1.88	24.2	38.6	24.0*	12.5*	24.6	N/A	3.6	3.4	0.13-μm CMOS	InGaP/GaAs HBT (Two-stage)	Doherty PA with envelope tracking carrier amplifier
[6]	1.70	28.5	36.6	28.0*	23.0	12.5*	-35.6	3.0	4.7	0.18-μm CMOS	0.18-μm CMOS (One-stage)	Source/load harmonic control, non-zero V_{ss} SM
[14]	1.71	27.0	40.0	27.0*	18.7	28.8	-35.3	3.23	5.0	0.18-μm CMOS	InGaP/GaAs HBT (Two-stage)	Multi-level LA supply tracking
[15]	0.90	28.5	41.1	27.0*	17.0*	N/A	N/A	N/A	3.6	0.18-μm CMOS	Commercial RF PA (N/A)	Delay-based hysteresis control, accurate quiescent current control
This work	0.90	24.0	38.4	24.6	16.3	20.8	-30.0	4.4	3.8	65-nm CMOS	0.18-μm CMOS (Two-stage)	Dual-mode with V_{LA} modulation, adaptive quiescent current control

*Graphically estimated, **not available,

directly connected to the pads on the evaluation board using bond wires for a chip-on-board assembly. The dc-dc converter was packaged using a QFN.

IV. MEASUREMENT RESULTS

Fig. 13 shows the measured waveforms from the implemented SM with a fixed V_{LA} of 3.7 V using the LTE signal. V_{BAT} of 3.8 V was supplied to the SM PA. V_{pa} is supplied to the PA for ET operation. Fig. 14(a) shows the measured efficiency of the SM in the ET mode using the LTE signal. For the conventional case, V_{LA} was fixed over the output power levels. As V_{LA} is modulated according to the output power level, the efficiency of the SM can be improved. When the output stage of the LA is reconfigured according to the output power level, the efficiency can be further improved. As a result, an output power of 1.06 W and an efficiency of 78.0% were achieved from the SM.

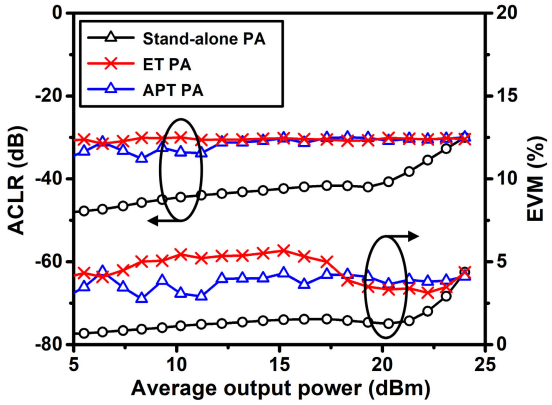
Fig. 14(b) shows the measured efficiency of the SM according to V_{pa} in the APT mode. The load of the SM was modelled using a 40 Ω resistor based on the dc supply voltage and current of the PA. The SM in the APT-mode has a maximum efficiency of 94.1% and the efficiency is maintained above 90.0% even when V_{pa} becomes 0.8 V.

Fig. 15(a) shows the measured gain of the stand-alone PA and the SM-PA using the LTE signal. The PAE of the SM-PA was calculated using the following equation,

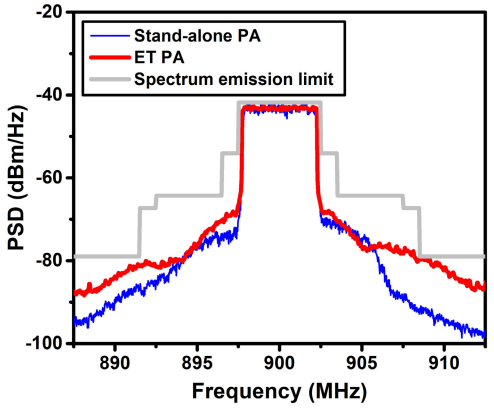
$$PAE = \frac{P_{out} - P_{in}}{P_{DC,dcdc} + P_{DC,SA} + P_{DC,DA}}, \quad (5)$$

where P_{out} and P_{in} are the output power and input power of the two-stage PA, respectively. $P_{DC,dc-dc}$ and $P_{DC,SA}$ are the dc power consumption of the dc-dc converter and the SA, respectively, while $P_{DC,DA}$ is the dc power consumption of the 1^{st} stage of the PA. Power gains of 20.8 and 24.4 dB of the ET- and APT-PAs were obtained at an average output power of 24.0 dBm, respectively. Fig. 15(b) shows the measured PAEs for the stand-alone PA, the conventional ET-PA, the ET-PA with V_{LA} modulation only, the ET-PA with both V_{LA} modulation and W_l control, and the APT-PA. By modulating V_{LA} in a wide output power range, the efficiency of the ET-PA was improved. In addition, by controlling W_l, efficiency was further improved. Compared to the stand-alone PA, PAE was improved by 4.5% point at an average output power of 24.0 dBm and by 8.0% point at 20.3 dBm, respectively.

Fig. 16 shows the measured performances of the SM PA using the LTE signal for ACLR and EVM in (a) and PSD in (b). An ACLR of −30.0 dBc and an EVM of 4.4% were obtained at an average output power of 24.0 dBm. As shown, the measured PSD complies with the LTE spectrum emission mask. Fig. 17 shows the measured signal constellation of the SM-PA using the LTE signal at an average output power



(a)



(b)

FIGURE 16. Measured performances of the SM-PA using the LTE signal: (a) ACLR, (b) PSD.

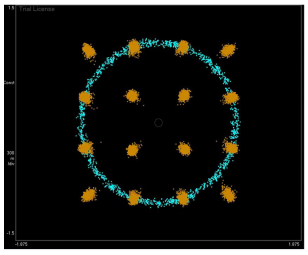


FIGURE 17. Measured signal constellation of the SM-PA using the LTE signal.

of 24.0 dBm. The performances described in this work are summarized and compared to those of the previously reported SM-PAs in Table 2.

V. CONCLUSION

This article presents a hybrid ET/APT supply modulator IC based on a Class-AB linear amplifier (LA) with supply voltage and temperature insensitive quiescent current for dual-mode operation. To further improve the efficiency, the supply voltage for the LA of the ET supply modulator can be modulated according to the average output power. To modulate the supply voltage for the LA in wider range, an adaptive quiescent current controller was proposed to maintain its quiescent current for large variations in voltage and temperature. In addition, the output stage of the LA was discretely reconfigured using 3-bit digital control to reduce the power consumption according to the output power level.

For verification of the proposed circuits and methods, a hybrid ET/APT supply modulator IC, a dc/dc converter, and a PA IC were designed and implemented using CMOS processes for the 0.9 GHz LTE application. Using an LTE uplink signal with a signal bandwidth of 5 MHz and a PAPR of 7.5 dB, a PAE of 38.4% at an average output power of 24.0 dBm was obtained under an ACLR of −30.0 dBc for the overall ET-PA. At a 6 dB back-off for the average output power, a PAE of 24.6% was achieved using the ET mode. It was experimentally demonstrated that the efficiency can be further improved using the proposed ET-PA, especially at the back-off power levels.

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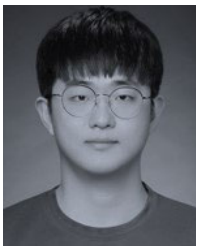

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