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A Hybrid Method for Three-Level T-Type Inverters to Eliminate Neutral Point Voltage Ripple and Control DC-Link Capacitors' Voltage for Separate MPPT

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ABSTRACT Nowadays, photovoltaic (PV) systems based on centralized topology with a three-level T-type ($3LT^2$) inverter are used to decrease investment costs and increase conversion efficiency. In this topology, the split capacitors of the DC-link can individually connected to PV arrays. Accordingly, DC-link capacitors' voltage should separately controlled to track PV arrays' maximum power point (MPP) voltage. However, the asymmetric control of capacitors' voltage causes line voltage to unbalance and output current to distort. In this paper, a hybrid method based on dipolar variable injection and zero-sequence voltage injection concepts is proposed to simultaneously control the DC-link capacitors' voltage of the $3LT^2$ inverter and eliminate their voltages ripple. In the presence of partial shading, the proposed method can control the capacitors' voltage of the DC-link to realize the separate MPP tracking while ensuring the balance of line voltages. Furthermore, the proposed method eliminates the voltage ripple on DC-link capacitors, inherently caused by the $3LT^2$ inverter, to improve the DC-link lifetime and the PV system reliability. The simulation studies and practical experiments have been performed, and their results prove the validity of the proposed method, whether the PF is unity or non-unity.

INDEX TERMS Three-level T-type ($3LT^2$) inverter, neutral point voltage (NPV) ripple elimination, separate maximum power point tracking (MPPT), dipolar modulation, zero-sequence voltage (ZSV) injection, photovoltaic (PV) system.

I. INTRODUCTION

Nowadays, there is growing attention to green energy sources since fossil fuels are non-renewable energy sources, and their consumption is the main contributor to global warming [1]. Among green energy sources, solar energy, harnessed by photovoltaic (PV) systems, has attracted much attention because the PV systems benefit simple installation capability, less required installation area, and noiseless operation in the electric power system [2].

Generally, as shown in Fig.1, PV systems can be categorized considering topology to 1) centralized topology, 2) multi-string topology, and 3) centralized topology with separated maximum power point tracking (MPPT) [3]. These topologies have been introduced considering the stage number of the power converters and the number of PV arrays or strings connected to the converters. The centralized topology includes a PV array connected to the AC power system through a one-stage power converter. Therefore, applying the centralized topology causes the investment cost to decrease and the power converter's efficiency to increase. However, this topology leads to MPPT degradation in a partially shaded PV system. It causes the overall efficiency of the PV system to decrease because all PV modules are controlled based on a common MPPT algorithm [4].

The multi-string topology comprises PV strings connected to an inverter through individual DC-DC converters. The multi-string topology improves the MPPT performance

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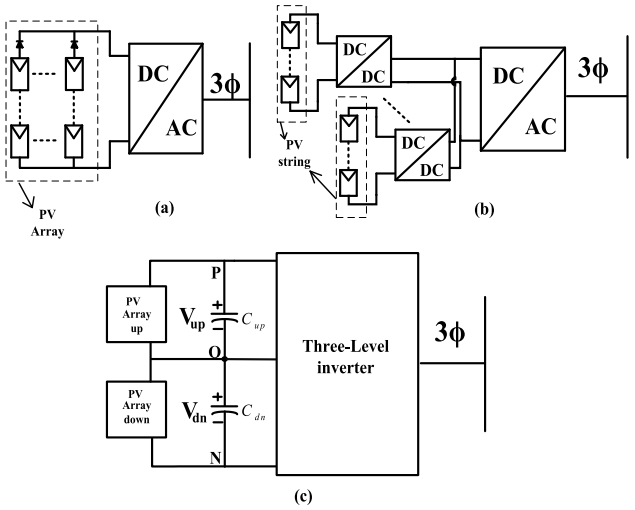

FIGURE 1. PV system topologies. (a) centralized topology. (b) multi-string topology. (c) centralized topology with separated MPPT.

compared to centralized since fewer modules operate based on a common MPPT algorithm. Nevertheless, when an equal number of PV modules are operated, the investment cost of the multi-string topology is higher than that of the centralized topology [5].

The centralized topology with the separated MPPT includes two PV arrays connected to the split capacitors of the three-level inverter's DC-link, although only a PV array should be connected to a three-level inverter's DC-link conventionally. Hereby, this topology merges the advantages of the centralized and the multi-string topologies. It decreases the investment cost and increases the conversion efficiency because it uses only one inverter as an interface between the PV arrays and the AC grid. Moreover, it causes the mismatch of the MPP of PV modules to have less effect on the energy harness since fewer modules operate based on a common MPPT algorithm [6].

In the above-mentioned topologies, utilization of a three-level inverter provides side-effective benefits such as lower voltage stress across switching devices, lesser total harmonic distortion (THD), smaller output filter requirement [7], [8]. Among three-level inverters, the three-level T-type ($3LT^2$) inverter is preferred due to efficiency-effective performance in the range of medium switching frequency and tens of kilowatt power [10] (note that the medium switching frequency and tens of KW power fulfill most of the PV application). Accordingly, the $3LT^2$ inverter is considered to be applied in centralized topology with separated MPPT in this paper.

The $3LT^2$ inverter provides exclusive features in operation, performance, and its structure conforms to centralized topology with separated MPPT. However, it inherently suffers from neutral point voltage (NPV) unbalancing. The NPV unbalancing includes NPV offset unbalancing and NPV ripple. The NPV offset unbalancing refers to voltage inequality of the up and down DC-link capacitors, while the voltage difference between the capacitors does not change with time. Conversely, The NPV ripple refers to zero-mean time-varying components of the DC-link capacitors' voltage [11].

The NPV offset unbalancing may be generated due to the manufactural difference between the DC-link capacitors, the inherent difference of switching device characteristics, and the modulation technique that the inverter operates based on. The unbalanced NPV offset leads to drawbacks such as switch breakdown and THD increase of output current [12]. Accordingly, the following approaches have been considered regarding the NPV offset unbalancing in previous works. 1) The up and down capacitor voltages are controlled to remove the NPV offset unbalancing [13]–[17]. Although this approach prevents unbalanced NPV offset drawbacks, it deteriorates MPPT performance in centralized topology with the three-level inverter. 2) The up and down capacitor voltages are asymmetrically controlled to cooperate with separated MPPT, and simultaneously the necessary measures are taken to avoid the drawbacks caused by unbalanced NPV offset [4], [6], [18], [19].

The NPV ripple is generated due to the modulation technique and operation condition of the $3LT^2$ inverter. The NPV ripple mainly consists of the AC component that oscillates with three multiple of the fundamental frequency. The amplitude of the NPV ripple depends on the output current, the power factor (PF), and the DC-link capacitors' size [16]. The NPV ripple shortens the lifetime of the inverter's DC-link capacitors, which, in turn, reduces the $3LT^2$ inverter lifetime [20]. Furthermore, the NPV ripple increases the THD of output current [21]. Accordingly, the suppression approach has been strictly followed regarding the NPV ripple in previous works [15], [22]–[26].

Noteworthy that the above-mentioned approaches to deal with the NPV offset unbalancing and ripple have been realized by proposing proper pulse width modulation (PWM) methods. The PWM methods are typically categorized into the space vector PWM (SV-PWM) and carrier-based PWM (CB-PWM) methods. However, the CB-PWM methods are preferred since they simplify the hardware implementation and shorten the execution time. Unipolar PWM and dipolar PWM are well-known types of CB-PWM methods [27].

The unipolar CB-PWM methods typically used zero-sequence voltage (ZSV) injection to balance the NPV offset and suppress the NPV ripple [14], [15], [22], [26]. Nevertheless, these methods are degraded due to overmodulation when the inverter operates at the non-unity PF. For example, the work in [22] calculates the proper ZSV that causes the neutral point current (NPC) to zero. Hereby, this method balances the NPV offset and eliminates NPV ripple while the PF is unity. However, it requires a higher input voltage at the DC-link of the inverter to effectively suppress the NPV ripple in the non-unity PF. If the input DC voltage does not increase, the NPV ripple is not suppressed due to overmodulation. Note that the PV inverter should be able to properly deliver power at the non-unity PF (absorb or inject reactive power) to improve the power quality by avoiding voltage rise or drop [28].

The dipolar CB-PWM methods can employ dipolar variable injection to balance the NPV offset and suppress the NPV ripple, whether the PF is unity or not [23]–[25]. In [24], the value of dipolar variables is selected based on the neutral point charging potential (integral of the NPC). This method can eliminate the NPV ripple and guarantee the NPV offset remains almost balanced while the PF can be changed from unity to zero. The work in [25] simplifies the selection of dipolar variable values and selects them based on the average NPC. This method modifies the connection duration of the phases to the neutral point to reach the average NPC to zero. As a result, it eliminates the NPV ripple. However, the proposed dipolar method in [24] and [25] degrades the separated MPPT capability that is the outstanding advantage of centralized topology with the three-level inverter. In other words, these methods can only balance the NPV offset, which causes the separated MPPT to cancel. Accordingly, a hybrid method is proposed in [29] to simultaneously provide the NPV ripple elimination and the NPV offset control (asymmetric control of DC-link capacitors) capabilities. Noteworthy that the present paper is the complete and detailed version of [29] while the MPPT control and its process to interact with proposed method, the limitation of the proposed method, simulation study, comprehensive experimental validation, and experimental results analysis are also included.

Considering the hybrid proposed method, the following can be counted as the contributions of this paper.

1) The DC-link capacitors of the 3LT^2 inverter, which commonly consist of electrolyte type, can be constructed by small film capacitors since the proposed method can effectively suppress the NPC ripple. Consequently, the 3LT^2 inverter lifetime and reliability increased, and the PV system's failure rate is decreased.
2) The energy harness and overall efficiency of the PV system are increased since the proposed method provides the separated MPPT capability for PV arrays by controlling the DC-link capacitors' voltage asymmetrically.
3) The voltage regulation at the point of common coupling (PCC) can be effectively accomplished by absorbing or injecting reactive power through the PV system since the proposed method effectively maintains its capabilities at non-unity PF conditions.
4) The proposed method provides NPV ripple elimination and NPV offset control capabilities without any topology modification or adding electrical components. Therefore, it can be easily implemented as an alternative method in the existing PV system based on the centralized topology with any three-level neutral-point-clamped inverter.
5) The proposed method is easy to understand since it is introduced based on the well-known dipolar injection and ZSV injection concepts. Furthermore, the proposed method is based on the CB-PWM technique that simplifies practical implementation and shortens execution time.

The rest of this paper is organized as follows. In section II, NPV and NPC are analyzed and modeled based on 3LT^2 inverter topology. In section III, the hybrid proposed method is introduced. In section IV, the simulation and experimental results are presented and compared with conventional methods. Finally, the paper is concluded in Section V.

II. NPV AND NPC ANALYSIS BASED ON 3LT^2 INVERTER

Fig.2 shows a PV system structured based on the centralized topology with the 3LT^2 inverter. In the 3LT^2 inverter, the [P], [O], and [N] states refer to an on-off state of switches that respectively connects the phase output to positive (P), neutral (O), negative (N) points of DC-link. Given all three phases of the inverter, 27 switching states can be counted for the 3LT^2 inverter. If the output voltage is transformed from the abc-frame to the $\alpha\beta$-frame, these 27 switching states forming voltage vectors which can be categorized into the zero, small, medium, and large types. Note that the type of voltage vectors affects the current flowing into or out of the neutral point, which causes the NPV to change. Table.1 lists all types of voltage vectors and their respective switching state, amplitudes, and NPC.

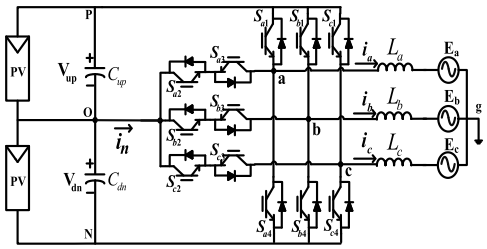

FIGURE 2. PV system based on centralized topology with the 3LT^2 inverter.

TABLE 1. Voltage vectors, switching states, and their NPC.

Vector	Magnitude	Switching states				NPC	
Zero vector	0	[PPP] [OOO] [NNN]				-	
Small vector	$\frac{1}{3}V_{dc}$	1	POO	ONN		i_b+i_c	i_a
		2	PPO	OON		i_c	i_a+i_b
		3	OPO	NON		i_a+i_c	i_b
		4	OPP	NOO		i_a	i_b+i_c
		5	OOP	NNO		i_a+i_b	i_c
		6	POP	ONO		i_b	i_a+i_c
Medium vector	$\frac{\sqrt{3}}{3}V_{dc}$	7	PON	8	OPN	i_b	i_a
		9	NPO	10	NOP	i_c	i_b
		11	ONP	12	PNO	i_a	i_c
Large vector	$\frac{2}{3}V_{dc}$	13	PNN	14	PPN	-	
		15	NPN	16	NPP		
		17	NNP	18	PNP		

Fig.3 graphically shows the NPC condition for all types of voltage vectors. Accordingly, the effect of voltage vectors on the NPV can be analyzed as follows. The switching states of zero and large voltage vectors are affectless on the NPV since they cause the path of NPC flow to open. The switching

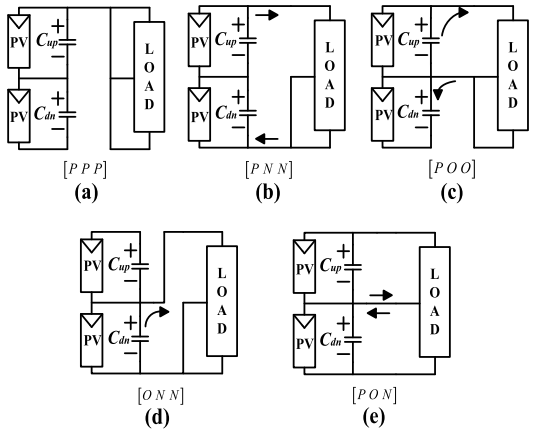

FIGURE 3. Effect of switching states on NPV (a) Zero vector (b) Large vector (c) P-type small vector (d) N-type small vector (e) Medium vector.

states of P-type and N-type small vectors cause the NPV to increase and decrease since they lead the current to flow into and out of the neutral point, respectively. The switching states of the medium voltage vectors make the equivalent circuit symmetrical when the AC grid is three-phase balanced. As a result, they do not affect the NPV since there is no current flow in the path connected to the neutral point.

A. MODELING OF THE NPC AND NPV

In Fig.4, the horizontal and vertical axes represent the normalized voltage of the phases ($d_{(a,b,c)}$) and the clamping time ratio of the phases at the neutral point (1- $d_{(a,b,c)}$), respectively [30]. The phase voltages are normalized by dividing them into half of the DC-link voltage. It can be seen, when normalized voltage is −0.8, the clamping time ratio of that at the neutral point is 0.2. This condition indicates that the phase has been clamped to the neutral point for 0.2 of the carrier period. Moreover, it implies that the phase has been clamped to the N point of the inverter's DC-link for 0.8 of the carrier period. According to the line currents and the clamping time ratio of the phases at the neutral point, the average NPC in a carrier cycle (i'_n) can be derived.

$$i'_n = \sum_x (1 - |d_x|)\, i_x \quad x = a, b, c \tag{1}$$

where d_x is the normalized phase voltage, and i_x is the phase current of the 3LT^2 inverter.

Fig.5 graphically shows the relationship between the NPC and the up and down capacitors' voltage. The NPC (i'_n) flows through the up and down capacitors of the inverter DC-link and results in the NPV change.

III. PROPOSED HYBRID METHOD

This section proposes a hybrid method by simultaneously utilizing the dipolar variable and ZSV concepts for the PV system based on centralized topology with the 3LT^2 inverter. The conventional dipolar CB-PWM benefits the NPV ripple elimination for the full PF range. Nevertheless, it cannot

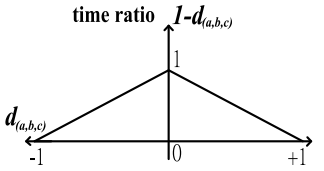

FIGURE 4. Normalized voltage and clamping time ratio at the neutral point of the 3LT^2 inverter.

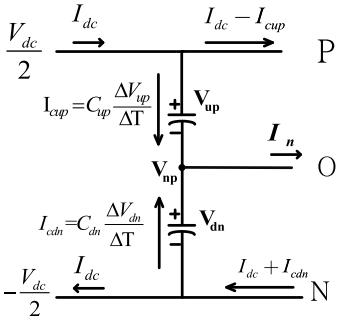

FIGURE 5. NPC effect on the DC-link capacitors' voltage.

control the NPV offset to keep the split capacitors' voltage of the 3LT^2 inverter at separated MPP voltage. Moreover, conventional dipolar CB-PWM causes the line voltages to unbalance and the output currents to distort in the case of NPV offset unbalancing. Therefore, the proposed hybrid method is introduced to not only eliminate the NPV ripple but also control the NPV offset for achieving the separated MPPT. Fig.6 shows the block diagram of the proposed hybrid method. In what follows, the MPPT process, the offset control and ripple elimination for the NPV, the principle of modulation signal generation, analysis of the ZSV injection role, and proposed method limitations are described.

A. MPPT PROCESS

The MPPT approach is considered to maximize the power extraction from the PV arrays. PV arrays' generated power depends on environmental factors (e.g., sunlight and temperature) and load characteristic. Since the environmental factors are uncontrollable parameters, the load characteristics are typically controlled to achieve the maximum power of the PV system. In this regard, the proposed method continuously adapts the DC-link capacitor voltages to the MPP voltage commanded by the MPPT algorithm. With this, the load characteristic of PV arrays is modified, and the PV arrays' operation point is maintained at the MPP. The followings describe the MPPT process considering Fig.6.

1) The actual voltage (V_{up}, V_{dn}) and current (I_{up}, I_{dn}) of the PV arrays are used in the up and down array MPPT algorithm blocks to calculate their MPP voltage (V^*_{up} and V^*_{dn}). Note that the proposed method focuses on implementing MPPT algorithm commands, and the MPPT algorithm is beyond the current paper scope. The proper MPPT algorithms can be selected among conventional algorithms classified in [31] and [32].

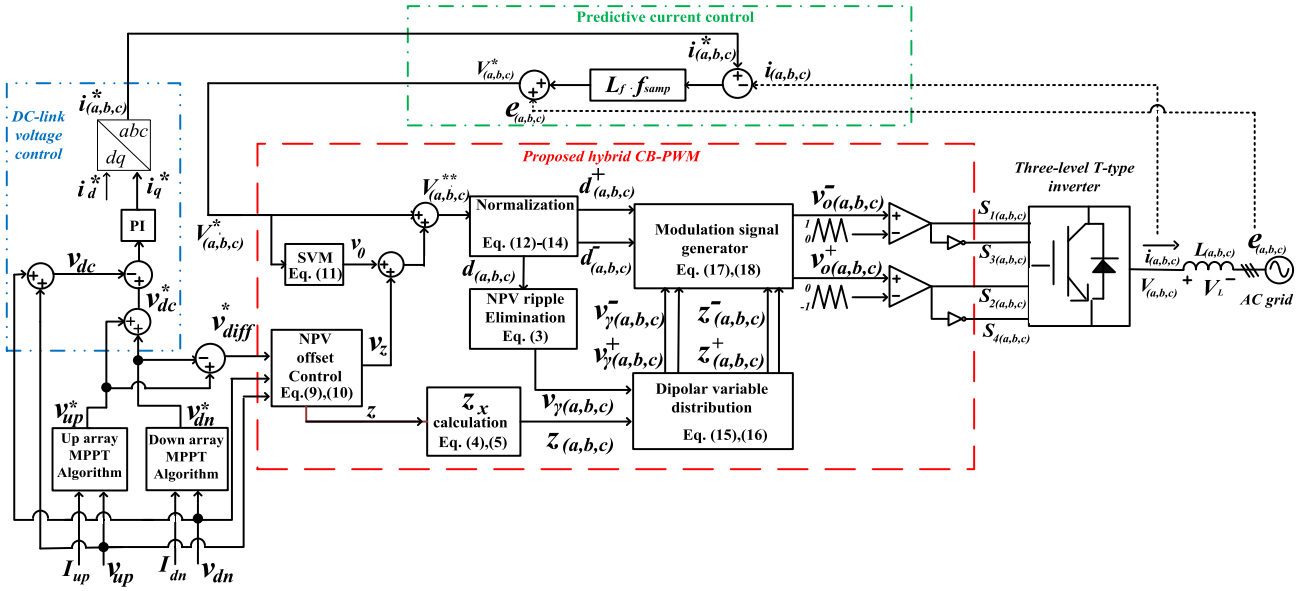

FIGURE 6. The block diagram of the proposed hybrid method.

2) The subtraction of the calculated MPP voltages (V^*_{diff}) is fed into NPV offset control block to modify the NPV offset. The NPV offset control approach is described in the next part.

3) The summation of the calculated MPP voltages generates the command value for DC-link voltage control (V^*_{dc}). The V^*_{dc} is subtracted from its actual value (V_{dc}), and the produced error is fed to a proportional-integral (PI) controller to achieve the q-axis command value of the current (i^*_q). Meanwhile, the d-axis command value of the current (i^*_d) is determined based on the required reactive power. Finally, predictive control is employed to generate the command output voltage ($v^*_{(a,b,c)}$), which is fed to the proposed CB-PWM. Note that the predictive controller's proportional gain (P gain) equals the output filter inductance (L_f) multiplied by the digital signal processor (DSP) sampling frequency (f_{samp}).

B. THE OFFSET CONTROL AND RIPPLE ELIMINATION FOR THE NPV

The proposed method employs the concept of dipolar variable injection to suppress the NPV ripple and control the NPV offset. It injects a primary dipolar variable value ($v_{\gamma x}$) into modulation signals to eliminate the NPV ripple. The primary dipolar variable injection reduces the neutral point clamping ratio of the 3LT^2 inverter phases to the shortest. Moreover, it equally distributes the reduced times to the P and N points' clamping ratio. The value of the primary dipolar variable value is expressed as follows.

$$\mathrm{v}_{\gamma \mathrm{x}} = |d|_{\max} - |d_x| \quad x = a, b, c \tag{2}$$

where $|d|\,max$ equals the maximum value between $|d_a|$, $|d_b|$ and $|d_c|$ ($|d|\,max = \max(|d_a|, |d_b|, |d_c|)$) and the $v_{\gamma x}$ is the primary dipolar variable value.

On the other hand, the proposed method employs a secondary dipolar variable injection to generate positive or negative NPC that, in turn, can decrease or increase the NPV, respectively. The secondary dipolar variable (z_x), contrary to the characteristic of the primary dipolar variable ($v_{\gamma x}$), specifically increases the clamping time ratio to the neutral point for 3LT^2 inverter phases in carrier cycles. According to the desired NPV offset, the following relationships are employed in the z_x calculation block owned by the proposed method block diagram.

1) When the increase of the NPV offset (the decrease of the up capacitor voltage and increase of the down capacitor voltage) is desired, the z_x dipolar variable is considered as follows to negativize the NPC.

$$z_x = \begin{cases} 0 & v^{**}_x \geq 0 \\ \mathrm{z} & v^{**}_x < 0 \end{cases} \qquad x = a, b, c \tag{3}$$

where the v^{**}_x (v^*_x with the addition of ZSVs) is command voltage. z_x is the secondary dipolar variable, and Z is its absolute value. Accordingly, the NPC is negative (flows from the 3LT^2 inverter legs side to the neutral point) since the z_x dipolar value causes the connection between the inverter phases and the neutral point to only establish when the current of the phases is negative.

2) When the decrease of the NPV offset is desired, the z_x dipolar variable is considered as follows to positivize the NPC.

$$z_x = \begin{cases} -\mathrm{z} & v^{**}_x \geq 0 \\ 0 & v^{**}_x < 0 \end{cases} \qquad x = a, b, c \tag{4}$$

As a result, the NPC is positive since the z_x dipolar variable injection causes the connection between the inverter's phases

and the neutral point to only occur when the current of the phases is positive.

Considering the primary and secondary dipolar variables, equation (1) for the NPC can be updated.

$$i_n = \sum_x (1 - |d_x| - \gamma_x + z_x) i_x \quad x = a, b, c \tag{5}$$

The NPC relationship is simplified by substituting equation (2) in (5).

$$i_n = \sum_x (1 - |d_{\max}|)\ i_x + \sum_x (z_x)\, i_x \quad x = a, b, c \tag{6}$$

The first summation of the (6) equals zero since the summation of the line currents is zero in a three-phase balanced system. In this way, the proposed method removes the NPC inherently caused by the $3LT^2$ inverter topology through the primary dipolar variable injection. Moreover, the NPC only depends on the secondary dipolar variable.

$$i_n = \sum_x (z_x)\, i_x \quad x = a, b, c \tag{7}$$

Noteworthy that the total dipolar variable injection ($v_{\gamma x} + z_x$) should be less than the clamping time ratio of the phases at the neutral point to avoid the short-circuit of the DC-link. Besides, it should be greater than or equal to zero to not change the average output voltage of the inverter considering the volt-second balance theory. Accordingly, $0 \le v_{\gamma x} + z_x \le 1 - d_x$ is considered as the allowable range of total dipolar variable injection.

To satisfy the allowable range for total dipolar variable injection, the ZSV injection is utilized and adapts the primary and secondary dipolar variable trends. Precisely, the ZSV injection adjusts the primary dipolar variable trend to make the secondary dipolar variable injectable. Moreover, it determines the absolute value of the secondary dipolar variable (Z) used in (3) and (4).

Fig.7, the internal block diagram owned by the NPV offset control block, indicates the ZSV injection role in the proposed method. In this block, the first ZSV injection (v_{z1}) is generated to change the initial $v_{\gamma x}$ trend to a standard trend (almost identical to the $v_{\gamma x}$ trend when the NPV is balanced). The $v_{\gamma x}$ trend standardizing makes the $v_{\gamma x}$ adjustment process the same and simple for all possible up and down capacitor voltage conditions.

$$v_{z1} = \frac{(V_{up} - V_{dn}) * v_{peak}}{V_{dc}} \tag{8}$$

where V_{peak} is the peak value of command voltage, and the V_{dc} is the actual total DC-link voltage. After standardizing the $v_{\gamma x}$, the second ZSV injection (v_{z2}) changes the standard $v_{\gamma x}$ trend to a trend in which z_x becomes injectable. The second ZSV injection (v_{z2}) is calculated by a proportional-integral (PI) controller (see Fig.7), and the absolute value of z_x is derived as

$$z = \frac{V_{dc}}{V_{up} * V_{dn}} * v_{z2} \tag{9}$$

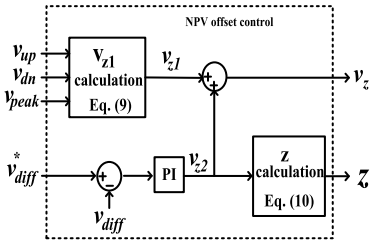

FIGURE 7. Internal block diagram owned by the NPV offset control block.

where v_{z2} is the second ZSV injection. Accordingly, the z_x injection can control the NPV offset while the total dipolar variable injection is limited in the allowable range. Note that the third ZSV (V_0) is applied to increase the linear modulation index range since it reduces the peak value of the command voltage wave to 0.866 of the actual value. With this, the DC-link utilization is maximized.

$$V_0 = \frac{-1}{2}(\max(v_a^*, v_b^*, v_c^*) + \min(v_a^*, v_b^*, v_c^*)) \tag{10}$$

C. COMMAND VOLTAGE NORMALIZATION, DIPOLAR VARIABLE DISTRIBUTION, AND MODULATION SIGNAL GENERATION

The dipolar CB-PWM generates switching signals using two modulation signals and two level-shifted in-phase carrier waves [27]. In conventional dipolar CB-PWM, the decoupled command voltages are normalized by dividing into half of the DC-link voltage. Besides, the dipolar variable values are divided in half and injected into decoupled command voltages to generate modulation signals. The conventional modulation signal generation principle causes the line voltage unbalancing and output current distortion in case of NPV offset unbalancing caused by separated MMPT.

In the proposed method, the generation of modulation signals (v_{ox}^+ and v_{ox}^-) is performed based on up and down capacitors' voltage to avoid drawbacks caused by NPV offset unbalancing. In this regard, the command voltage (v_x^{**}) is firstly decoupled into positive and negative command voltages.

$$v_x^{**+} = \begin{cases} v_x^{**} & if\ v_x^{**} \ge 0 \\ 0 & if\ v_x^{**} < 0 \end{cases} \quad x = a, b, c \tag{11}$$

$$v_x^{**-} = \begin{cases} 0 & if\ v_x^{**} \ge 0 \\ v_x^{**} & if\ v_x^{**} < 0 \end{cases} \quad x = a, b, c \tag{12}$$

where v_x^{**+} and v_x^{**-} respectively are the positive and negative command voltages. Second, the v_x^{**+} and v_x^{**-} are normalized considering the up and down capacitors' voltage, respectively.

$$d_x = d_x^+ + d_x^- \tag{13}$$

where

$$\begin{cases} d_x^+ = \dfrac{v_x^{**+}}{V_{up}} \\ d_x^- = \dfrac{v_x^{**-}}{V_{dn}} \end{cases} \quad x = a, b, c$$

where d_x^+ and d_x^- respectively are normalized positive and negative command voltages. Afterward, the primary ($v_{\gamma x}$) and secondary (z_x) dipolar variable values are also distributed considering up and down capacitors' voltage.

$$\begin{cases} v_{\gamma x}^+ = v_{\gamma x} * \dfrac{V_{dn}}{V_{dc}} & \text{for injection into } (v_o^+) \\ v_{\gamma x}^- = v_{\gamma x} * \dfrac{V_{up}}{V_{dc}} & \text{for injection into } (v_o^-) \end{cases} \quad x = a, b, c \tag{14}$$

$$\begin{cases} z_x^+ = z_x * \dfrac{V_{dn}}{V_{dc}} & \text{for injection into } (v_o^+) \\ z_x^- = z_x * \dfrac{V_{up}}{V_{dc}} & \text{for injection into } (v_o^-) \end{cases} \quad x = a, b, c \tag{15}$$

where $v_{\gamma x}^+$ and $v_{\gamma x}^-$ are the positive and negative values of the primary dipolar variable, respectively. Likewise, z_x^+ and z_x^- respectively are the distributed values of the secondary dipolar variable. Fig.8 graphically shows the effect of considering asymmetric DC-link capacitors' voltage on dipolar variable distribution. To make the figure clearer, the second dipolar variable value is considered zero. Tri^+ and Tri^- are level-shifted carrier waves.

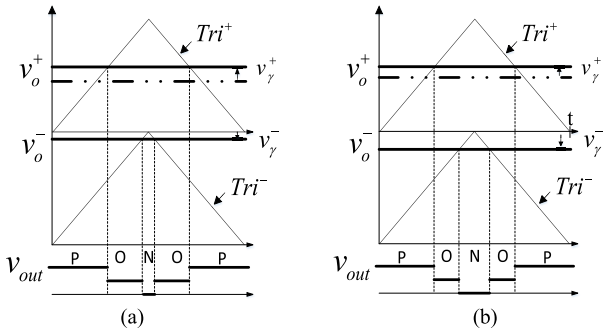

FIGURE 8. Distribution process diagram for the dipolar variable. (a) $V_{up} < V_{dn}$. (b) $V_{up} > V_{dn}$.

Finally, the proposed method uses the distributed primary and secondary dipolar variables to generate the positive and negative modulation signals (v_{ox}^+ and v_{ox}^-). When the NPV is commanded to increase, the positive and negative modulation signals are organized as

$$\begin{cases} v_{ox}^+ = \begin{cases} d_x^+ + v_{\gamma x}^+ & if\ v_x^{**} \geq 0 \\ v_{\gamma x}^+ - z_x^+ & if\ v_x^{**} < 0 \end{cases} \\ v_{ox}^- = \begin{cases} -v_{\gamma x}^- & if\ v_x^{**} \geq 0 \\ d_x^- - v_{\gamma x}^- + z_x^- & if\ v_x^{**} < 0 \end{cases} \end{cases} \quad if\ z \geq 0 \tag{16}$$

When the NPV is commanded to decrease, the positive and negative modulation signals are organized as follows.

$$\begin{cases} v_{ox}^+ = \begin{cases} d_x^+ + v_{\gamma x}^+ - z_x^+ & if\ v_x^{**} \geq 0 \\ v_{\gamma x}^+ & if\ v_x^{**} < 0 \end{cases} \\ v_{ox}^- = \begin{cases} -v_{\gamma x}^- + z_x^- & if\ v_x^{**} \geq 0 \\ d_x^- - v_{\gamma x}^- & if\ v_x^{**} < 0 \end{cases} \end{cases} \quad if\ z < 0 \tag{17}$$

where v_{ox}^+ and v_{ox}^- are the positive and negative modulation signals, respectively.

D. ANALYSIS OF ZSV INJECTION ROLES FOR THE PROPOSED METHOD

To be more illustrative, Fig.9, Fig.10, Fig.11 and Fig.12 are presented to show d_a, $|d_a|$, $|d|\,max$, and $v_{\gamma a}$ and the effect of ZSV injection on them.

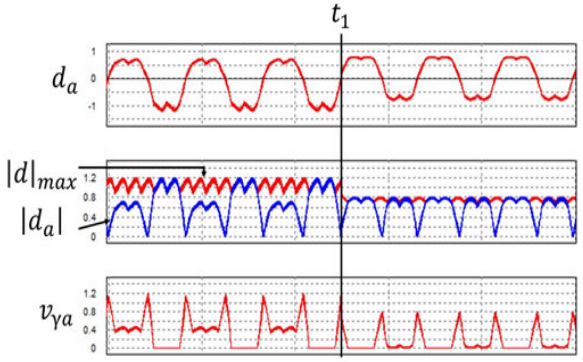

FIGURE 9. The trend standardization of the first dipolar variable when $V_{up} > V_{dn}$.

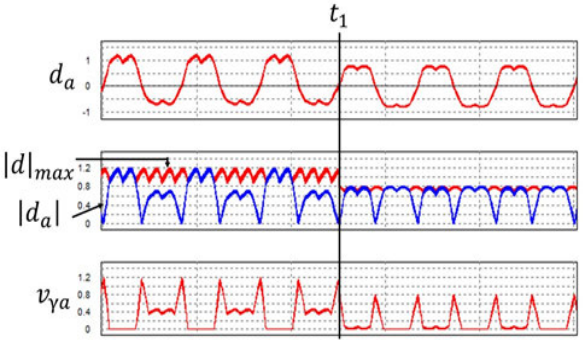

FIGURE 10. The trend standardization of the first dipolar variable when $V_{up} < V_{dn}$.

Fig.9 indicates the $v_{\gamma a}$ standardizing by first ZSV injection (v_{z1}) while initially $V_{up} > V_{dn}$. When d_a is close to the negative peak values, the $|d_a|$ equals $|d|\,max$, and the $v_{\gamma a}$ experience a zero value. When the $v_{\gamma a}$ is zero, the z_a cannot be injected since it causes the total dipolar variable to be less than zero (exceed the allowable range). When d_a is close to the positive peak values, the $|d_a|$ is less than $|d|\,max$, and

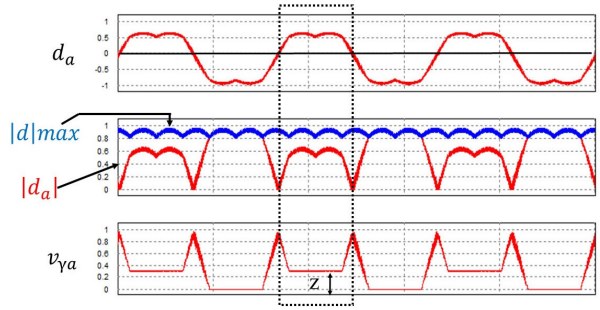

FIGURE 11. The trend adjusting of the first dipolar variable when the increase of NPV offset is commanded.

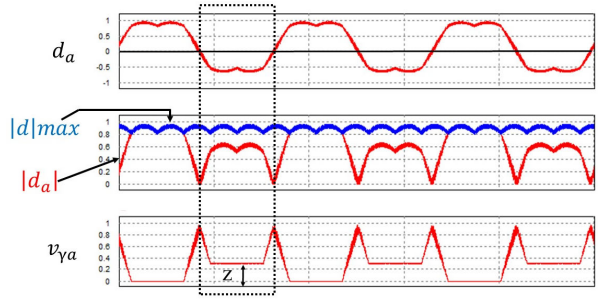

FIGURE 12. The trend adjusting of the first dipolar variable when the decrease of NPV offset is commanded.

the $v_{\gamma a}$ experience positive values before t1 s. Although the z_a can be injected when the $v_{\gamma a}$ is positive, the injectable value of the z_a is not controllable and may not meet the required value (Z) to control the NPV offset. After t1 s, the v_{z1} is injected, resulting in the $v_{\gamma a}$ trend changing to the standard trend. Likewise, Fig.10 shows the $v_{\gamma a}$ standardization process by v_{z1} injection at t1 s when the up capacitor voltage initially is less than the down one ($V_{up} < V_{dn}$).

Fig.11 and Fig.12 show the adjusted $v_{\gamma a}$ trend by second ZSV injection (v_{z2}) when the MPPT algorithm commands the NPV offset to increase and decrease, respectively. The v_{z2} injection changes the $v_{\gamma x}$ trend from the standard to the trends in which the secondary dipolar variable is injectable as much as the Z value.

E. THE PROPOSED METHOD LIMITATIONS

The limitations of the proposed hybrid method can be investigated considering the propitious PF for NPV offset control, maximum asymmetry of DC-link capacitor voltages, and the power losses of the 3LT^2 inverter.

1) Propitious PF for NPV offset control: The NPV offset control approach has been introduced, assuming that the 3LT^2 inverter delivered the generated power at the high PF (more than -0.8 or 0.8). This assumption is valid considering the cost-effective operating condition of the PV systems. Besides, it provides enough PF freedom to accomplish voltage regulation at PCC. Nevertheless, the transient operating conditions with deficient PF, such as voltage sag, have not been considered in proposing the NPV offset control. The deficient PF causes the effect of small vectors on the NPV offset to change compared to the high PF condition [33]. Therefore, the control capability of the NPV offset is transiently disturbed during the PF deficiency.

2) Maximum asymmetry of DC-link capacitor voltages: The sum of ZSV injections should be limited to the amount that avoids overmodulation. The absolute value of v_{z2} generated by PI control in the NPV offset control block (see Fig.7) should be less than $V_{dc}/2 - V_{peak}$ to avoid overmodulation during the asymmetry control of capacitor voltages. It is recommended to limit the output of PI control to $V_{dc}/4 - V_{peak}/2$ to simultaneously avoid overmodulation and obtain an acceptable system response with tolerable overshoots. Note that, according to (8), the higher the capacitor voltage's asymmetry, the more the absolute value of v_{z1}. Consequently, the maximum manageable asymmetry of capacitor voltages by the proposed method can be determined considering v_{z1}, recommended limit for v_{z2}, and the normalization process of command voltage. When the $V_{up} < V_{dn}$, the positive normalized command voltage, which is normalized by dividing to smaller capacitor voltage (V_{up}), may cause over modulation. Since overmodulation typically occurs when the command voltage is at peak value, the following inequality can be expressed

$$\frac{V_{peak} - \left(V_{diff} * V_{peak}/V_{dc}\right) + \left(V_{dc}/4 - V_{peak}/2\right)}{\left(V_{dc} - V_{diff}\right)/2} \leq 1 \tag{18}$$

where $V_{diff} = \left|V_{up} - V_{dn}\right|$, and $(V_{dc} - V_{diff})/2$ equals smaller capacitor voltage. The inequality is satisfied when $V_{diff} < V_{dc}/2$. Therefore, the maximum asymmetry of capacitor voltages equals $V_{dc}/2$. The same result is derived when the maximum asymmetry for capacitor voltages is calculated considering the negative normalized command voltage for $V_{up} > V_{dn}$.

3) Power losses: The 3LT^2 inverter power losses originate from losses in the three-level bridge and output filter [17]. The bridge losses depend on the switching losses and conduction losses. The proposed method composes the command voltage using [P], [O], and [N] switching states in carrier periods due to the dipolar variable injection. Therefore, it increases switching commutations number, which causes the switching losses to increase. In [25], the detailed losses analysis of the switching devices has been accomplished for dipolar CB-PWM methods. The losses analysis implies that the dipolar variable injection in the proposed method increases the switching losses by almost 50%, although it causes almost the same conduction losses.

On the other hand, the higher the output current THD is, the greater the eddy current losses of the filter are. The dipolar CB-PWM methods increase the THD compared to the conventional method based on the unipolar CB-PWM [27]. Considering the losses increase in bridge and output filter, the proposed method decreases the conversion efficiency of the 3LT^2 inverter. However, bridge and output filter losses are

small compared to the power generation increase provided by separated MPPT [18].

IV. SIMULATION STUDY AND EXPERIMENTAL VALIDATION

In this section, the simulation and experimental results of the proposed method are investigated. Moreover, the experimental results are analyzed to clarify and summarize specific aspects of the proposed methods.

A. TEST SYSTEM

The prototype of the experimental setup is shown in Fig.13. To be more illustrative, Fig. 14 demonstrates the hardware configuration diagram of the experimental setup and the measurement points of experiments. The DC power supplies of the Chroma 62024P 600-8 type were paralleled to the DC-link capacitors to operate in constant current mode as the equivalent model of the PV arrays. The bipolar IGBT switches of the K40T1202 model were used in the $3LT^2$ inverter circuit. The power quality analyzer of the HIOKI 3196 model performed the Fourier analysis on the output currents. Moreover, the TEKTRONIX chip model DPO3PWR analyzed the low-frequency oscillation of the capacitors' voltage and the NPC. The digital signal processor (DSP) of the TMS320F28335 model performed the switching signal calculation in the switch driver circuit.

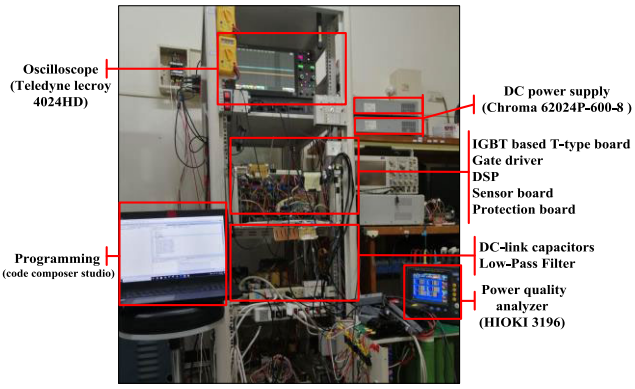

FIGURE 13. The prototype of the test system.

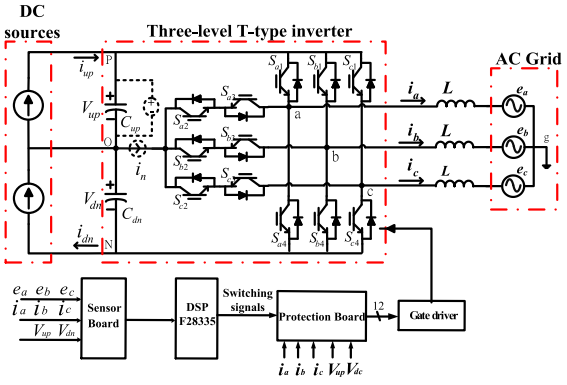

FIGURE 14. The hardware configuration diagram of the experimental set-up.

To clarify the functionality of the switch driver circuit, the sequence of the signal processing can be explained as follows. First, the sensor board measures the actual values of the output voltage, output current, and DC-link capacitors' voltage. Second, in the sensor board, the actual values are scaled to the acceptable range for analog to digital converter (ADC) of the DSP. Afterward, the DSP receives the scaled analog signals from the sensor board and converts them to digital signals to generate modulation signals. Finally, the modulation signals are fed into the enhanced pulse width modulator (ePWM) module of the DSP to generate switching signals.

Table.2 lists the $3LT^2$ inverter and AC grid parameters. The following can be expressed about the selection criteria of the output filter and DC-link capacitors of the $3LT^2$ inverter. The output filter comprises series inductors to provide a low-pass filter. According to the IEEE standard, the output filter should limit the THD of the output current to less than 5% and cause a voltage drop of less than 3% of the AC grid voltage [35]. Consequently, a 5 mH inductor was employed as the filter inductance. Note that although the rated power of the prototype is 1KW, the $3LT^2$ inverter is practically applied for the application of tens of KW. The output filter size can effectively be reduced in realistic applications with higher rated power since the THD is inversely proportional to the fundamental harmonic amplitude of the output current.

TABLE 2. The parameters of $3LT^2$ inverter, AC grid for experiments and simulation study.

Parameters	Description	Value
e_{abc}	3 Φ line to line voltage (RMS)	220 V
f_{fun}	fundamental frequency	60 Hz
f_{sw}	Switching frequency	10 kHz
C_{up},C_{dn}	DC-link capacitors	100 µF
L_{abc}	Output filter inductor	5 mH
P_{out}	The inverter power rating	1 kW

The DC-link capacitors of the $3LT^2$ provide a low impedance path for high-frequency currents and stiffen the DC-link. The DC-link capacitors are sized based on the RMS value of the capacitor current ripple, maximum input DC voltage, and acceptable capacitor voltage ripple [36]. Typically, the capacitor current's RMS value is the main specification and determines which capacitor should be selected. The worst-case for the capacitors' current ripple occurs while the $3LT^2$ inverter delivers the power to the AC grid at 0.612 modulation index and unity PF [37]. However, the proposed method effectively suppresses the capacitors' current ripple regardless of the operation conditions. Consequently, the $50\mu F$ / 250V film capacitors, which benefit from a higher lifetime and lower internal power losses, were used parallel to construct DC-link capacitors. Hereby, the lifetime of the $3LT^2$ inverter is effectively extended since the electrolytic capacitors, which cause 60% of failure in the PV inverter [20], have been replaced with film capacitors with longer lifetimes.

B. SIMULATION RESULTS

In this part, the simulation study is investigated to specifically evaluate the performance of the proposed method in terms of asymmetric control of DC-link capacitors. The simulation is run in PSIM software, and Table.3 shows the command voltage of DC-link capacitors voltage during the simulation study. According to Table.3, the MPP voltage and current of both PV arrays are firstly equal during the T1 period. After T1, the generated current by the up and down PV arrays is changed due to partial shading conditions in T2 and T3 periods. Subsequently, the MPPT algorithm commands for modifying the voltage value of the DC-link capacitors to maximize the generated power by PV arrays. After the partial shading conditions, the commanded voltage values are again equaled for PV arrays in the T4 period.

TABLE 3. PVs' MPP voltage during the simulation study.

Times (s)	T1 (t<0.25)	T2 (0.25<t<0.35)	T3 (0.35<t<0.45)	T4 (t>0.45)
PV current (A)	$I_{up} = 2.5$ $I_{dn} = 2.5$	$I_{up} = 2.8$ $I_{dn} = 2$	$I_{up} = 2.2$ $I_{dn} = 3$	$I_{up} = 2.5$ $I_{dn} = 2.5$
MPP voltages(V)	$v^*_{up} = 220$ $v^*_{dn} = 220$	$v^*_{up} = 190$ $v^*_{dn} = 250$	$v^*_{up} = 235$ $v^*_{dn} = 205$	$v^*_{up} = 220$ $v^*_{dn} = 220$

Fig.15 shows the capacitor's voltage, the NPC, the line voltage (V_{ab}), and the line current for periods T1 to T4 while the 3LT^2 inverter operates at +0.9 PF. The proposed method caused a balanced line voltage to generate even under the unbalanced NPV offset. Moreover, an insignificant harmonic distortion was observed in line current (i_a). The THD was less than 4% during the simulation study. The NPC waveform indicates that the proposed method negativizes the NPC when the up and down capacitors' voltage is commanded to decrease and increase, respectively (consider T2 period). Furthermore, it positivizes the NPC when the reverse condition is commanded for up and down capacitors' voltage (consider T3 period). The maximum modulation index amount was about 0.7 during T1, and it changed to almost 0.85 and 0.8 amount in T2 and T3 periods, respectively.

Fig.16 shows the up capacitor voltage, NPC, and their fast Fourier transform (FFT) for the conditions in which the capacitors' voltage difference equal zero (i.e., $0 < t < 0.25$s), 60V (i.e., $0.28 < t < 0.35$), and 30 V (i.e., $0.38 < t < 0.45$). It can be seen the low frequency oscillation of the NPC and up capacitor voltage are almost zero, whether the NPV is balanced or not. Consequently, the proposed method not only interacts with the MPPT process but also effectively maintains the NPV ripple elimination capability of dipolar CB-PWM methods.

C. EXPERIMENTAL RESULTS

In this part, the proposed method is experimentally investigated considering two scenarios based on the unity and non-unity PF conditions. In the first scenario, the NPV ripple elimination and NPV offset control capabilities are proved under the unity PF condition. The second scenario confirms

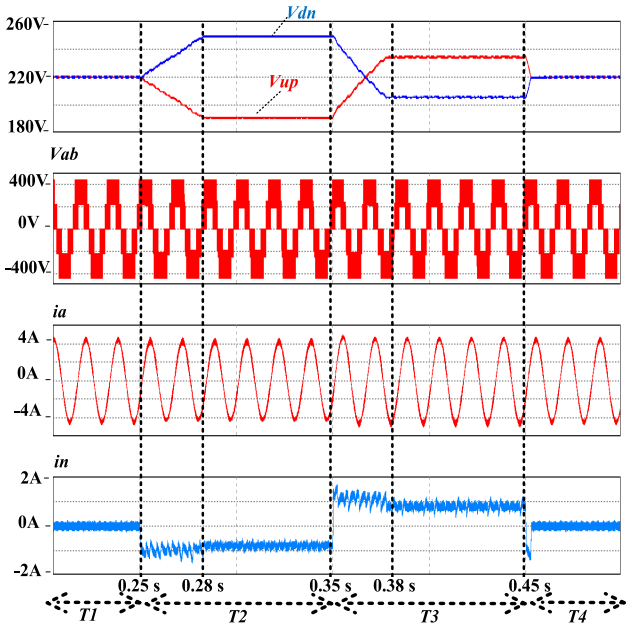

FIGURE 15. NPV offset control performance of the proposed method.

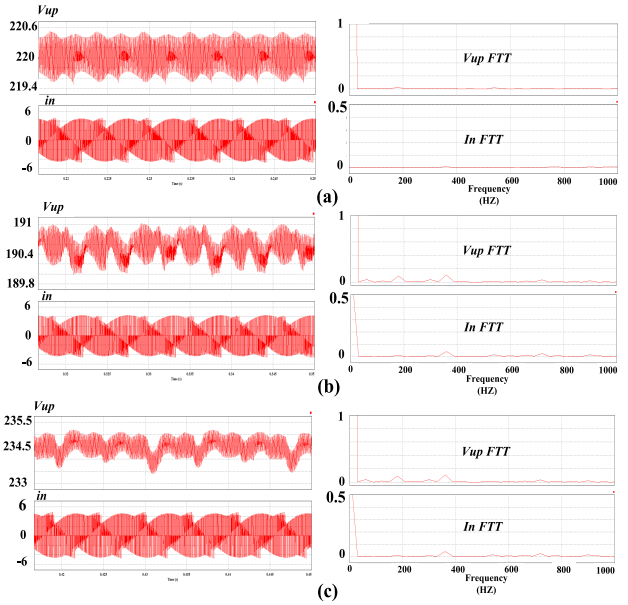

FIGURE 16. The V_{up} and NPC and their FFT analysis. (a) $V_{up} = V_{dn} = 220$ (b) $V_{up} = 190$ and $V_{dn} = 250$ (c) $V_{up} = 235$, $V_{dn} = 205$.

that the proposed method capabilities are maintained under non-unity PF conditions. Note that the experimental results are compared with the results of the well-known space vector PWM (SVPWM [34]) method to validate the proposed method's capability.

1) UNITY POWER FACTOR

Fig.17 shows the phase voltages (V_{ao}, V_{bo}, and V_{co}) and line current (i_a) waveforms for the conventional (SVPWM) and proposed methods. Fig.17 (b) indicates that the proposed

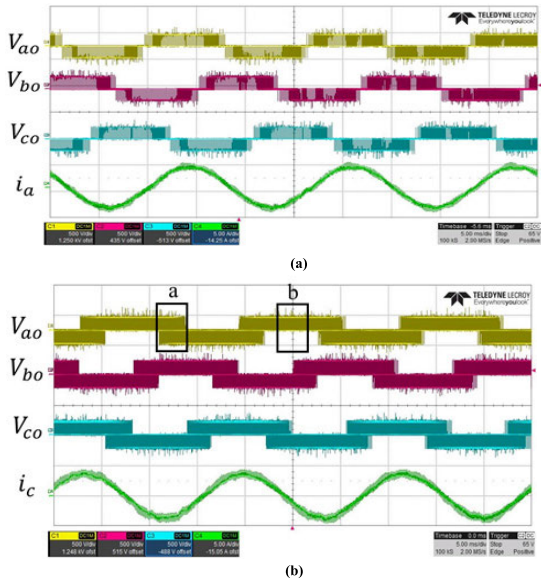

FIGURE 17. Phase voltages and line current waveforms for unity PF. (a) Conventional method. (b) Proposed method.

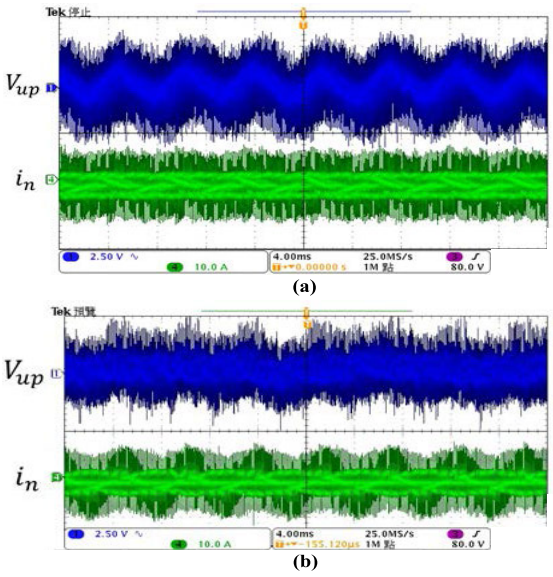

FIGURE 18. The ripple of the V_{up} and NPC for unity PF. (a) Conventional method (b) Proposed method.

method may have caused each phase voltage to chop into discrete parts with positive, neutral, and negative levels in some intervals. For example, the V_{ao} experienced parts with 220V, zero, and −220V levels within the "a" interval and 220V and zero within the "b" interval distinguished in Fig.17(b). However, the average output voltage for the proposed and conventional methods was equal since the proposed method considers the volt-second balance theory for dipolar variable injections. The Fourier analysis of the line currents indicated that the THD was 2.39% for the conventional method, and the proposed method mitigated the THD to 1.86%.

Fig.18 shows the up capacitor voltage and NPC when the conventional and proposed methods were implemented at unity PF. Table.4 and Table.5 respectively lists the AC component characteristics (amplitude and RMS values) of the up capacitor voltage and NPC. When the conventional method was applied, the RMS value of the AC component with triple the fundamental frequency equaled 0.751V and 0.61A for the up capacitor voltage and NPC, respectively. The proposed method respectively suppressed the RMS values of them to 0.088V and 0.053A. The up capacitor voltage and NPC included almost no low-frequency oscillation when the proposed method was implemented. Their insignificant oscillation was generated due to experiment instruments.

Fig.19 shows the proposed method's performance for unity PF when the asymmetric control of the DC-link capacitor voltages is required. Initially, the command voltages of the DC-link capacitors were equal to 220V. At t1, the MPPT algorithm changed the command voltages for the up and down capacitors to 190V and 250V, respectively. The command voltage tracking process took about 40ms, and the required MPP voltage for PV arrays was reached at t2.

Table.6 lists the output current harmonics for the following conditions. First, the balanced condition of DC-link

TABLE 4. The AC components of the V_{up} for unity PF.

NPV ripple order	Frequency (HZ)	Conventional method		Proposed method	
		Amp (%)	RMS (V)	Amp (%)	RMS (V)
1	60.0	100	61.4 m	100	143 m
2	120.0	28.4	17.5 m	23.9	34.3 m
3	180.0	1.22 k	751 m	62.1	88.9 m
4	240.0	28.2	17.3 m	4.60	6.59 m
5	300.0	24.1	14.8 m	10.9	15.6 m
6	360.0	105	64.7 m	7.36	10.5 m
7	420.0	20.1	12.4 m	19.8	28.4 m
8	480.0	14.5	8.93 m	1.28	1.84 m
9	540.0	71.4	43.9 m	47.9	68.7 m

TABLE 5. The AC components of the NPC for unity PF.

NPC ripple order	Frequency (HZ)	Conventional method		Proposed method	
		Amp (%)	RMS (A)	Amp (%)	RMS (A)
1	60.00	100	16.4m	100	30.3m
2	120.0	161	26.5m	85.1	25.8m
3	180.0	3.72 k	610m	177	53.6m
4	240.0	104	17.0m	29.8	9.03m
5	300.0	226	37.1m	118	35.8m
6	360.0	518	85.0m	65.8	19.9m
7	420.0	103	16.9m	122	37.1m
8	480.0	103	17.0m	22.4	6.80m
9	540.0	415	68.1m	335	102m

capacitors in which the up and down capacitor voltages are equal to 220V (before t1 in Fig.19). Second, the unbalanced condition in which the up and down capacitor voltages, respectively, equal to 190V and 250V (after t2 in Fig.19). Typically, the greater the voltage difference of the inverter's DC-link capacitors, the higher amplitude the even-order harmonics. However, the proposed method avoids the even-order

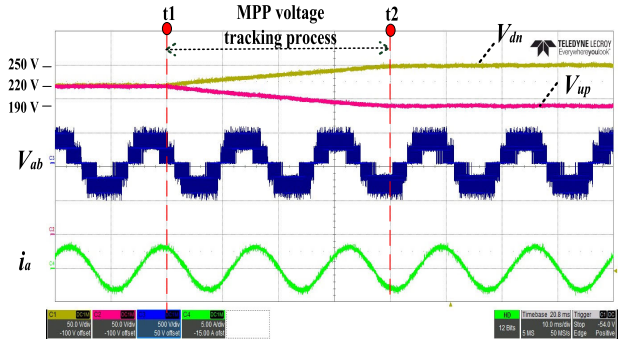

FIGURE 19. Asymmetric control of the DC-link capacitors' voltage for unity PF.

TABLE 6. Low frequency harmonics of output current.

Harmonics of the line current							
With balanced NPV offset				With 60 V unbalancing of NPV offset			
order	Amp (%)	order	Amp (%)	order	Amp (%)	order	Amp (%)
1	100	11	0.49	1	100	11	0.34
2	0.31	12	0.48	2	0.99	12	0.38
3	0.14	13	0.54	3	0.24	13	0.58
4	0.62	14	0.42	4	0.58	14	0.60
5	0.47	15	0.32	5	0.76	15	0.29
6	0.13	16	0.33	6	0.19	16	0.48
7	0.28	17	0.28	7	0.69	17	0.12
8	0.39	18	0.25	8	0.88	18	0.40
9	0.36	19	0.28	9	0.27	19	0.10
10	0.83	20	0.19	10	1.18	20	0.17
THD =1.86				THD=2.52			

harmonics to rise since its command voltage normalization process maintains the line voltage balanced even in NPV unbalancing. The insignificant rise of the even-order harmonics originated from the circuit imperfections, the switches' dead time, and sensing error.

2) NON-UNITY POWER FACTOR

Fig.20 shows the phase voltage and line current for conventional and proposed methods when the $3LT^2$ inverter delivers the power to the AC grid at +0.8 PF. The THD of the line currents was %1.85 for the conventional method, and it was reduced to %1.49 by applying the proposed method.

Fig.21 shows the up capacitor voltage and NPC for implementing conventional and proposed methods when the PF equals +0.8. The AC components with triple the fundamental frequency obviously existed when the conventional method was applied. Conversely, the proposed method suppressed the AC component oscillating with the triple fundamental frequency, although the PF is non-unity. Table.7 and Table.8 list the characteristics of AC components of the up capacitor voltage and NPC, respectively. When the conventional method was applied, the RMS value of the AC component with triple the fundamental frequency was 2.26V and 1.89A for the up capacitor voltage and NPC,

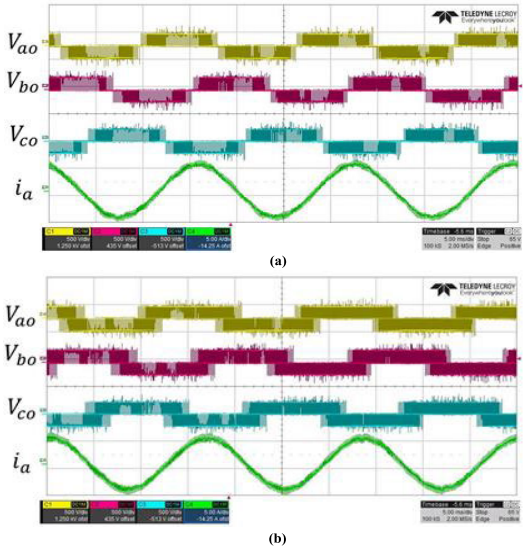

FIGURE 20. Phase voltages and line current waveforms for PF = +0.8 (a) Conventional method (b) Proposed method.

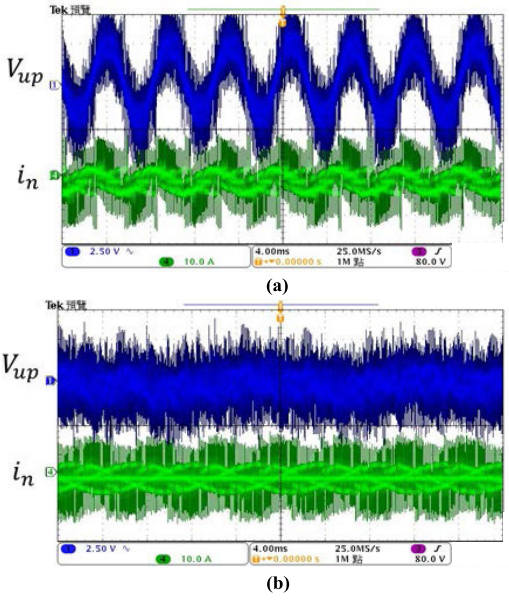

FIGURE 21. The ripple of the V_{up} and NPC for PF = +0.8 (a) Conventional method (b) Proposed method.

respectively. The RMS values of them respectively reduced to 0.116V and 0.105A by implementing the proposed method.

Fig.22 exhibits the proposed method performance at +0.8 PF in terms of MPP voltage tracking. After t1, the command MPP voltage changed to 190 V and 250 V for up and down capacitors' voltage, respectively. The command voltage tracking process took about 42ms. Note that the line voltage remains balanced, although the NPV is unbalanced after t2.

D. RESULTS ANALYSIS AND DISCUSSION

Generally speaking, a desirable method to control the $3LT^2$ inverter operation should provide the capabilities of

TABLE 7. The AC components of the V_{up} for PF = +0.8.

NPV ripple order	Frequency (HZ)	Conventional method		Proposed method	
		Amp (%)	RMS (V)	Amp (%)	RMS (V)
1	60.00	100	59.5m	100	232m
2	120.0	145	86.2m	34.3	79.4m
3	180.0	3.80k	2.26	49.9	116m
4	240.0	55.3	32.9m	17.6	40.6m
5	300.0	36.0	21.4m	9.14	21.2m
6	360.0	136	80.6m	2.12	4.92m
7	420.0	11.4	6.80m	5.70	13.2m
8	480.0	11.9	7.10m	3.25	7.52m
9	540.0	152	90.1m	36.8	85.2m

TABLE 8. The AC components of the NPC for PF = +0.8.

NPC ripple order	Frequency (HZ)	Conventional method		Proposed method	
		Amp (%)	RMS (A)	Amp (%)	RMS (A)
1	60.00	100	39.5m	100	54.1m
2	120.0	112	44.3m	49.3	26.6m
3	180.0	4.79 k	1.89	195	105m
4	240.0	83.5	32.9m	77.6	41.9m
5	300.0	97.6	38.5m	7.30	3.95m
6	360.0	157	61.8m	6.63	3.59m
7	420.0	18.3	7.24m	41.5	22.4m
8	480.0	36.1	14.2m	24.2	13.1m
9	540.0	445	176m	218	118m

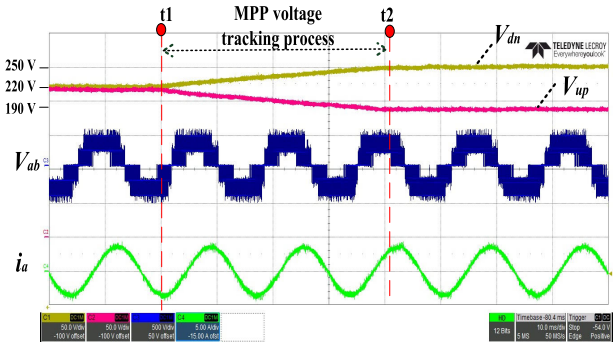

FIGURE 22. Asymmetric control of the DC-link capacitors' voltage for PF = +0.8.

NPV ripple mitigation, proper NPV offset control and THD reduction. This part analyzes the experimental results to clarify the proposed hybrid method's performance according to the desired capabilities.

1) NPV RIPPLE ANALYSIS

Fig.23 shows the comparative bar graphs of the conventional and proposed methods regarding the main AC component of the NPC and up capacitor voltage. The proposed method, respectively, decreased the main AC component of the NPC and up capacitor voltage by at least 90% and 88% compared to the conventional method. Consequently, the experimental results imply the sufficiency of the proposed method for

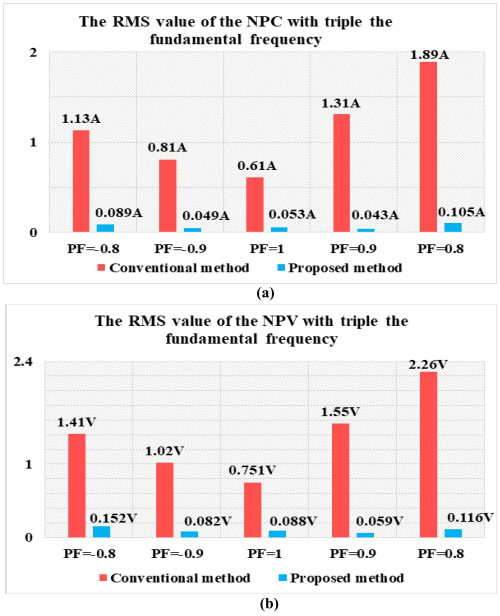

FIGURE 23. Comparative bar graphs for conventional and proposed methods (a) NPC ripple (b) NPV ripple (V_{up} ripple).

ripple mitigation of NPV and NPC, whether the PF is unity or not. Note that the NPC ripple mitigation causes the small film capacitors can be chosen in the designing process of the $3LT^2$ inverter to improve the $3LT^2$ inverter lifetime and reliability.

2) NPV OFFSET CONTROLLABILITY ANALYSIS

It can be seen in Fig.19 and Fig.22 the proposed method can effectively control the up and down capacitor voltages to track the commanded MPP voltage. Meanwhile, it maintains the line voltage balanced and suppresses the even-order harmonics, whether the NPV is balanced or not. Noteworthy that the proposed method not only provides the separated MPPT but also leads the MPPT dynamic response to improve since it causes the smaller capacitors to structure the DC-link of the $3LT^2$ inverter.

3) THD ANALYSIS

Fig.24 shows the comparative bar graph for conventional and proposed methods considering the THD amount. The HIOKI3196 power quality analyzer took into account up to the 40th order of harmonics for THD calculation in the

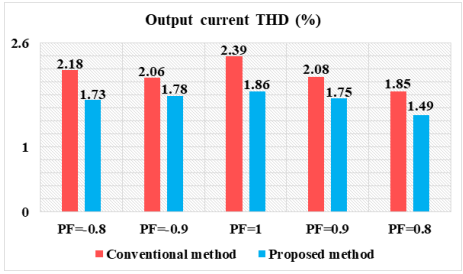

FIGURE 24. THD comparative bar graph for conventional and proposed methods.

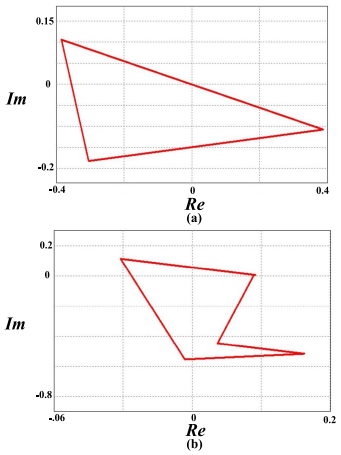

FIGURE 25. Switching frequency harmonic flux trajectory. (a) Conventional method (b) Proposed method.

experimental results. According to the THD comparative bar graph, the proposed method can improve the low-frequency harmonics behavior of the $3LT^2$ inverter. However, the switching frequency harmonics also affect the actual amount of the output current THD. The harmonic flux trajectories analysis can investigate the switching frequency harmonics caused by a modulation technique [38]. The harmonic flux is the time integral of the error between the command voltage and the voltage vectors which compose the command voltage.

Fig.25 shows switching frequency harmonic flux trajectories for proposed and conventional methods while generating the same command voltage. The conventional method applied the voltage vectors based on the 6-18-12-6 sequence within the half carrier cycle to compose the command voltage. On the other hand, the proposed method composes the command voltage according to the 6-18-12-6-1 voltage vector sequence. The proposed method employs an extra voltage vector for composing the command voltage within the half carrier cycle since it uses the dipolar variable injection concept. This extra voltage vector slides the flux trajectories' center of gravity away from the origin—the farther the distance to the origin, the greater harmonic flux. Consequently, the proposed method leads to greater switching frequency harmonics than the conventional method. Noteworthy that the simulation results indicate that the proposed method causes the actual THD of output current (calculated THD based on both low-frequency and switching-frequency harmonics) to increase compared to the conventional method. The actual THD amount was about 2% for the conventional method, and the proposed method increases the THD to 4%.

V. CONCLUSION

In this paper, a hybrid method is proposed to simultaneously eliminate the NPV ripple and control the DC offset of the NPV, whether the PF is unity or non-unity. In this regard, this method employs the dipolar variable injection and ZSV injection concepts in a hybrid manner. By implementing the proposed method in the PV system structured based on the centralized topology with a $3LT^2$ inverter, the split capacitor of the DC-link can be asymmetrically controlled to provide separated MPPTs. The proposed method increases bridge and output filter power losses in the $3LT^2$ inverter; however, these losses are small compared to the power generation increase provided by separated MPPT capability. Consequently, the overall efficiency of the PV generation system is improved by the proposed method. The proposed method reduces the ripple voltage on the split capacitors by 88%, which causes the lifetime of the capacitors to increase. Therefore, the $3LT^2$ inverter reliability is increased, and the PV system's failure rate is decreased.

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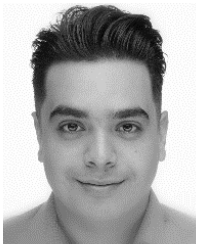

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