Integrated Framework for Development, Emulation, and Testing of High-Level Converter Control Functions for Distributed Generation Sources

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ABSTRACT With the increase in power installed from distributed generation sources (DGS), many problems have appeared following the utilisation of novel topologies and structures. Higher-level controllers for the safe operation of power grids with a high penetration of DGS must be developed. This task becomes difficult as the size and complexity of modern power systems have increased. The development and testing of these systems under strict human supervision controlling each step of the testing procedure is no longer viable. This paper presents a comprehensive integrated platform based on an HIL emulator for the development and testing of electric power systems rich in DGS. Essentially, DGS is considered a controllable black-box system. A detailed calculation of the power references for an arbitrary DGS is shown. The paper also describes the utilisation of enhanced Python scripting which was designed to load all network-related data, start the emulation, collect the data, and generate reports. Furthermore, fully developed controller built-in oscilloscope functionality is introduced. The incorporated oscilloscope facilitates non-intrusive DGS controller data acquisition and analysis, reducing the need for external measurements. The proposed framework was verified by a case study in which a grid topology consisting of 26 nodes was emulated on parallel CHIL infrastructure. Four active and twenty-two passive nodes were instantiated and their reaction to a distribution network grid faults was examined. DGS converter control was executed in external controllers outside of the dedicated HIL environment. All DGSs were governed by different control strategies, regarding maximisation of active/reactive power production, minimisation of the active/reactive power oscillations, adjustable positive/negative components ratio, or without any limitations under voltage disturbances. Real-time experiments confirmed the usefulness and flexibility of the proposed framework concept.

INDEX TERMS Distributed power generation, emulation, hardware-in-the-loop simulation, power control.

NOMENCLATURE

API	Application programming interface.
CHIL	Controller hardware-in-the-loop.
CI/CD	Continuous integration and delivery.
DAA	Data acquisition and analysis.
DG	Distributed generation.
DGS	Distributed generation source.
DGC	Local controller for distributed generation.
DSP	Digital signal processor.
DR	Desired data rate.
Dy	Triangle-star windings connection.

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EPS	Electric power systems.
GCC	Grid-connected converter.
I2C	Inter-integrated circuit.
IDE	Integrated development environment.
HIL	Hardware-in-the-loop.
HLC	High-level control.
JTAG	Joint test action group.
PIL	Processor-in-the-loop.
PLL	Phase-locked loop.
PR	Proportional-resonant.
PV	Photovoltaic.
SIL	Software-in-the-loop.
SPI	Serial peripheral interface.
ST	Scripting tools.
UART	Universal asynchr. receiver-transmitter.
USB	Universal serial bus.
$\Delta P, \Delta Q$	Active and reactive power oscillation amplitude.
f_{PWM}	PWM frequency.
I_{aamp}-I_{camp}	Amplitude of phase currents.
I_{lim}	Limit of phase current amplitude.
i_{dp}^r, i_{qp}^r	Positive current component references in rotating *dq* coordinate system.
i_{dn}^r, i_{qn}^r	Negative current component references in rotating *dq* coordinate system.
i_{dq}^p, i_{dq}^n	Positive/negative current component in rotating *dq* coordinate system.
K, D_1-D_6	Multiplication coefficients in equations.
kbps	Kilobits per second.
k_p, k_q	Adjustable ratio between positive and negative power components.
Mbps	Megabits per second.
S^r, P^r, Q^r	Apparent, active and reactive reference power.
u_{dq}^p, u_{dq}^n	Positive/negative voltage component in rotating *dq* coordinate system.
u_{dp}, u_{qp}	Positive voltage component in rotating *dq* coordinate system.
u_{dn}, u_{qn}	Negative voltage component in rotating *dq* coordinate system.
var_{num}	Number of variables.
var_{length}	Length of variables [Bytes].

I. INTRODUCTION

Electric power systems (EPSs) are experiencing significant transformation imposed by the increase and diversification of power consumption and by the necessity of modernisation of power generation facilities. Following the changes in demand and supply subsystems, the transmission and distribution networks must be augmented with new technologies that enable efficient and safe power transfer. Power electronic devices play a central role in this process.

The development of EPS containing power electronic devices has traditionally been a challenging process. It will become even more complicated in the future owing to the

necessity for the fast and reliable development of new power devices and control concepts. The strong competition in the electrical energy market and ecological urgency has put designers of EPS under pressure, as they have to develop reliable and flexible power systems for different applications. Design, prototyping, and validation of the applications over a wide range of operating conditions and power ratings are time-consuming processes. EPS are very complex to manage, and their complexity is growing owing to the presence of distributed generation sources (DGS). Therefore, a framework that facilitates the rapid development and testing of DGS and its interaction with EPS is necessary.

The goal of this research is to propose solutions to these problems. An integrated platform for the emulation and effective testing of control algorithms for modern DGS and their interaction with the grid is described in this paper.

The proposed testing framework consists of the following integral components:

- higher-level DGS control structures providing black-box functionality,
- management system for extensive testing of various scenarios,
- software for data acquisition and evaluation,
- integrated development environment for complex EPS containing not only passive but also DGS nodes.

The proposed framework is designed by the expansion, generalisation and integration of current state-of-the-art solutions which are summarised in Section 2. The contributions of this study can be outlined as follows.

1) A control scheme for a grid-connected converter (GCC) that secures the safe production of truly arbitrary power/current profiles in accordance with the converter's ratings during nominal conditions and conditions with grid faults. This control scheme enables the GCC to be addressed and utilised as a controllable black box system. It is beneficial for the development of higher-level control structures, and enables the handling of the GCC only by its references. Thus, no insight into GCC operation from grid operator side is needed. The control scheme is suitable for non-islanded operation modes, where GCC is a grid-following unit. The black-box functionality is a unique and original contribution of this study.

2) Guidelines for the development and testing of higher-level control structures are prepared together with a set of fully developed novel tools for data acquisition and analysis.

3) The EPSs rich in DGS can be analysed using emulators. The scope of applicability of emulators within the proposed framework is demonstrated in a case study by the emulation of a network with 26 nodes. The 4 nodes were active and 22 nodes were passive. This serves as a proof of the proposed framework concept.

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II. RELATED WORKS

A. INTEGRATED DEVELOPMENT ENVIRONMENTS

Various integrated development environments or frameworks are available for the development of modern DGS control structures. Their performances, advantages, and disadvantages are discussed briefly in this subsection.

Simulation tools such as MATLAB/Simulink, PSPICE, and PSIM are suitable for the development of control algorithms in power electronics and for transient analysis, but they are not optimised for the simulation of systems consisting of a large number of passive power system nodes (e.g. EPS rich in DGS) or for highly nonlinear power electronic devices. Although, DigSILENT, PSS, NEPLAN, and ETAP can be used for the modelling of large EPS, they lack the bottom-up approach, that is, they do not include models of power electronic devices with sufficient precision [1]. If the number of power electronic components is very high, these tools are of limited use. Simulations save space and funds compared to physical laboratories, but do not offer a real development environment. To make the control design and test closer to real laboratory conditions, a simulation platform called software-in-the-loop (SIL) is utilised [2]. This approach proves to be of low fidelity even though a controller and a plant are simulated in a single device and the integrity of input/output signals is not critical. The same conclusion can be drawn for the processor-in-the-loop (PIL) testing procedure, used to verify the actual control software implemented in a dedicated processor controlling a virtual plant prototype [3].

Scaled-down hardware setups are widely accepted alternatives to traditional simulation tools [4], [5]. Their main advantages are operating conditions that are often almost identical to the conditions under which the application will operate once it is installed. However, this approach has several disadvantages. The time necessary for setting up the environment is quite long. The environment is not flexible if a parameter changes are required. The safety of the testing personnel is often compromised. Most notably, the scalability of these setups is limited.

HIL systems eliminate the disadvantages of scaled-down platforms through their scalability, operability, and safety [6], [7]. The HIL system emulates the power stage in real time with extremely high fidelity [8]. It enables the testing of faults that are dangerous for the equipment and humans if they are induced in full-size or scaled-down setups. The repeatability and reconfigurability of the tests with the HIL are easy. If the system contains nonlinear elements such as power electronics devices, the emulation time step must be below $1 \mu s$. Typical 2-and 3-level PE topologies can be emulated even at $0.5 \mu s$, thus qualifying this technology as a powerful development environment for EPS systems [1], [9], [10].

B. CONTROL STRUCTURES

In most cases, an advanced control structure is applied with the HIL simulation. A brief overview of the control structures for GCC is presented in this subsection. Phase-locked loops (PLLs) and their derivatives are necessary to ensure an accurate estimation of the grid voltage data under nominal and subnominal grid conditions.

A comprehensive overview of different synchronisation solutions for grid connected converters was proposed in [11]. PLLs with improved transient stability during grid faults are given in [12], [13], while PLLs based on enhanced second-order generalised integrators are given in [14], [15].

In addition, many different current control loop solutions have been developed, most of which are based on symmetrical component extraction [11], [16], discussing tuning of parameters [17], as well as dynamic and tracking performance to directly control the injected current [18]. Furthermore, active and reactive power production and utilisation have been extensively analysed in recent years. Microgrid inverters strong coupling together with accompanying nonlinearities is discussed in [19]. The analysis of simultaneous inverter currents quality enhancement together with power oscillations minimisation during unbalanced grid faults is shown in [20], [21]. Different prioritization strategies for active and reactive power generation desired by grid operators are given in [22]. The control scheme presented in Section 4 builds on the ideas proposed in these contributions.

The main goal is to enable the production of arbitrary power/current profiles under various working conditions which in turn would render the GCC a controllable black box unit. The arbitrary power/current references can be forwarded to a GCC unit, which would produce them up to the maximum ratings of the converter values. This feature is of fundamental importance for the establishment of a flexible and safe environment for testing high-level control functions.

C. MANAGEMENT OF TESTING PROCEDURES

EPSs have been developed and tested under strict human supervision. Each step of the corresponding procedure is initiated by a direct command given by the user. The necessity of extensive test reiteration and the increase in complexity have led to the employment of software tools for semi-automated or automated text execution and environmental manipulation. Consequently, the development of application programming interface (API) libraries is necessary [23]. API libraries offer user-friendly functions that interact with the system under development. They enable modifications in both the power stage and the control structure. Software routines are used to manage testing procedures. The commands from users, expressed through the API functions, can be bundled together within scripts. Scripting, previously used almost exclusively for pure software development, has recently been used in the development of EPS. The Python programming language has been recognised as a highly useful tool for script development employed to manage testing procedures [24]. It can be used in the form of plug-in modules, drastically decreasing the development time for scripts and testing itself [25]. Python scripting has become almost synonymous with extensive, semi-automated, and repeatable testing of large and complex

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systems. An example of a Python script proposed in this paper which illustrates the DGS control testing scenario, is shown in Fig. 1.
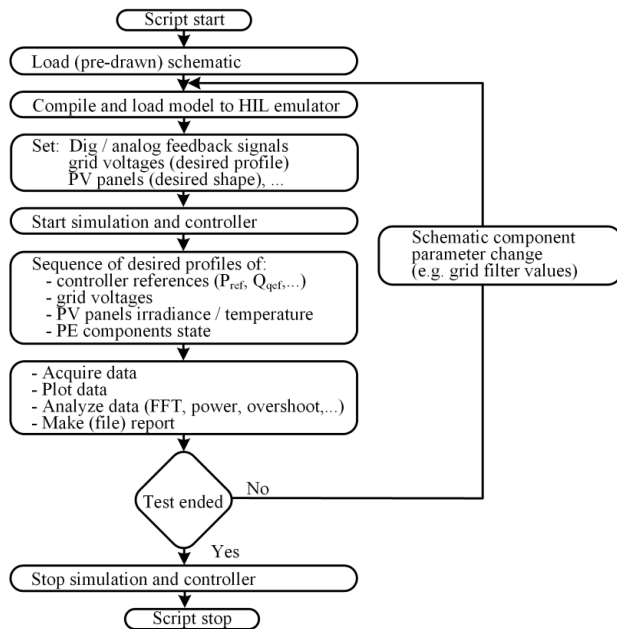

FIGURE 1. Proposed GCC control testing script.

D. DATA ACQUISITION AND ANALYSIS

Data acquisition and analysis are integral parts of the proposed integrated framework. A large amount of data must be collected in real time with high sampling rates from both the power stage and control platform. Hence, data acquisition routines must be effective, and their impact on the standard operation of the controller should be minimised. The analysis of the collected data must be straightforward and comprehensive. Although there are several open-source routines which can be used for the design of software for data acquisition and analysis [26], surprisingly, only a few solutions are commercially available [27]. In addition, guidelines on how to make efficient custom solutions are seldom found in the literature.

III. CONFIGURATION OF THE PROPOSED FRAMEWORK

All the tools and methods presented in the previous section must necessarily be integrated for the successful application of any effective testing framework. The outline of the proposed framework for the development and testing of modern power systems and their control is shown in Fig. 2.

Distributed generators (DG) are connected to a distribution network with an arbitrary topology. In this study, the DG is emulated together with the primary energy sources (PV, wind turbine, etc.). They are connected via three-phase inverters to the AC distribution network. Each DG is controlled by a local controller for distributed generation (DGC), which measures analogue variables and generates control signals for the power stage. The entire power stage was implemented inside
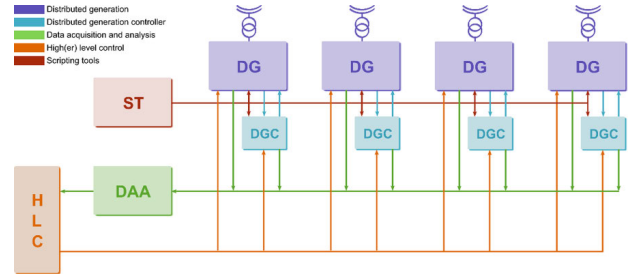

FIGURE 2. General outline of framework: DG - distributed generation, DGC - local controller for distributed generation, DAA - data acquisition and analysis, ST - scripting tools, HLC - high level control.

the HIL emulators [28]. For the experiments in this study, the control code was generated by MATLAB/Simulink and executed on a dedicated digital signal processor (DSP) [29] that was connected to the HIL system.

Data from the emulator and DGC were logged and analysed using data acquisition and analysis (DAA) tools, which will be explained in Section VI.

This framework structure enables the comprehensive development and testing of high-level control (HLC) functions. The HLC receives the necessary data from the power stage and the local controllers. Moreover, HLC generates control actions to be executed either by operations in the power stage of the DG or by DGC. HLC can initiate network reconfiguration and define new power references (e.g. new operation points of the DG). Finally, scripting tools (ST) are implemented in the proposed framework. ST enables automatic system manipulation and testing, which significantly accelerates the development process. The details of the ST are provided in Section V.

The control algorithms implemented in the DGC must provide a black box functionality for all operation modes of the DG. This functionality is described in the following section.

IV. HIGH-LEVEL CONTROL AND BLACK BOX FUNCTIONALITY
A. TOPOLOGY AND CONTROL STRUCTURE

The general hardware structure with the recommended control strategy for a single DG unit is shown in Fig. 3. Black box functionality serves primarily for the human EPS operator. The EPS operator handles DG only by using the references of the DG without any particular knowledge of its detailed operation.

It should be emphasised that the grid-following operation of the GCC unit under non-islanded grid conditions is assumed. Hence, the GCC takes the power/current references generated internally, set by the grid operator or generated by higher-level control functions and executes them in accordance with the converter's ratings and current grid voltage conditions. Control structures suitable for operation in islanded microgrids are a subject of further research.

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The energy from the primary source (a PV string, wind generator, or energy storage system) is supplied to the grid via a three-phase inverter. The power stage contains DC/AC filters and a transformer with a *Dy* windings connection to prevent the propagation of zero-voltage components to the grid. The u_{abc} voltages are supplied into a PLL unit with an extractor to obtain the positive and negative grid voltage components u_{dq}^{pn}, as well as the estimated grid voltage frequency ω and angle θ. The PLL unit is based on a dual second-order generalised integrator [14]. It is capable of rejecting or mitigating the effects of frequency disturbances such as phase jumps or voltage harmonics. The proposed algorithm is very important for comprehensive DG control, as it possesses a wide range of ride-through capabilities. This means that the structure in Fig. 3 is capable of handling different grid disturbances in a satisfactory manner, and at the same time, it will not be disconnected from the grid. Both the active power reference P^r and reactive power reference Q^r are defined by the HLC. Under standard operating conditions, P^r is obtained as the output of the DC-link voltage control loop, and Q^r can be defined by different mechanisms, for example by the grid codes or by the local reactive power requirements. The current references $i_{\alpha\beta}^r$ are calculated using the estimated grid voltage vector characteristics u_{dq}^{pn} and with the required P^r and Q^r. The current references and their measured values were then fed into proportional-resonant (PR) controllers. Different current controllers can be applied here but PR controllers have been applied as they have an excellent performance-to-complexity ratio [30].
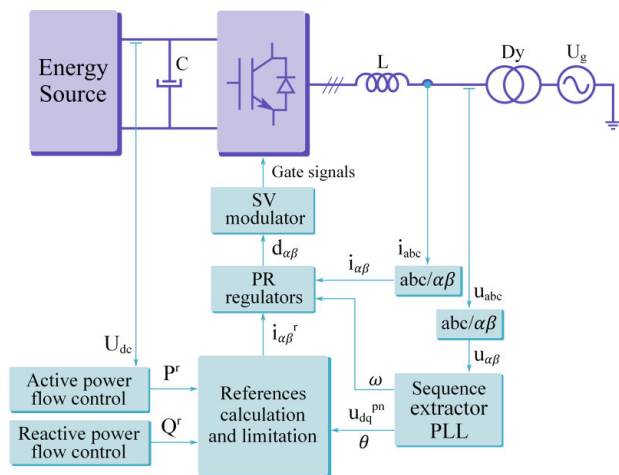

FIGURE 3. The structure of advanced controller for distributed generation.

B. CALCULATION OF POWER REFERENCES

If the current controllers provide the desired tracking performance for the current references, the DG unit can achieve a wide range of functionalities and operation modes. Fundamentally, the management of reference values must be implemented in the control structure. It secures safe power/current production and handles instantaneous voltage excursions.

Moreover, disturbance mitigation features must be implemented for the DG unit for active disturbance cancellation. By expanding the apparent power $\hat{S}$ formula given by (1), the expressions in Tables 1 and 2 can be derived [31].

$$\hat{S}^r = P^r + iQ^r$$
$$= (e^{i\omega t} u_{dq}^p + e^{-i\omega t} u_{dq}^n)(e^{-i\omega t} i_{dq}^{pr*} + e^{i\omega t} i_{dq}^{nr*}). \quad (1)$$

Tables 1 and 2 (all tables are given in Appendix) show the current references calculated from the given power references P^r and Q^r and instantaneous grid voltage components u_{dq}^{pn}.

The references listed in Table 1 enable the mitigation of oscillations. This is important for systems in which the DC-link capacitor size is the fundamental hardware design feature. The smaller and thus the cheaper the capacitor, the higher the oscillations in the DC-link voltage caused by the oscillating power component. As oscillations in reactive power do not degrade the operation of the DG unit, they can remain uncontrolled. For some voltage profiles, the mitigation of reactive power oscillations results in lower current amplitudes when compared with the regime in which only reactive power oscillations are controlled. For these voltage profiles it is advantageous to control the reactive power oscillations while the active power oscillations remain uncontrolled [22].

Table 2 gives expressions for the production of power with an adjustable ratio between the positive and negative power components. In this case, the power oscillations are not controlled but on the other hand, a flexible AC voltage control can be implemented. It is important for microgrids and for low- and medium-voltage grids. Therefore, the expressions listed in Table 2 are of great practical importance.

Neither the references in Table 1 nor the references in Table 2 can secure limited phase currents under disturbance. To meet the converter's current ratings, these references must be recalculated taking into account the limit values. These references are initially calculated using either Table 1 or Table 2, but if the inverter's control estimates that the phase currents are above the limit value I_{lim}, overcurrent protection is triggered and the DC unit is disconnected from the grid.

Table 3 (see Appendix) is equivalent to Table 1 and contains recalculated power references that would result in the phase current being exactly at its defined limit I_{lim}. Different formulas can be used depending on the phase current to be limited or the power oscillations to be mitigated. Table 4 is equivalent to Table 2 and contains recalculated references which can be used to secure safe power and current production with a set ratio between positive and negative power components. Details of the equations given in Table 3 and 4 can be found in [22].

Any power and current profile of practical importance for arbitrary grid conditions can be safely implemented using the expressions in Table 3 and 4. The DG unit governed by the control scheme in Fig. 2, based on references from the tables in this section, can ride through any random distur-

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bance. Furthermore, the DG unit has the ability to implement auxiliary services that mitigate the effects of disturbances and help to restore the nominal operating conditions of the grid. DG unit with this kind of control acts as a black box system for superior human EPS operators. It should be emphasized that the proposed environment does not offer solutions for grid energy management, load-balancing, and similar problems but rather enables the development of those solutions.

V. SCRIPTING TOOLS

The HIL technology provides comprehensive automated testing under all possible operating conditions. Unlike conventional DGS hardware, the HIL platform offers API functions that directly interact with the emulator and can also interact with the controller being tested. The generic scenario of testing using a scripting approach is shown in Fig. 1. Implementation details of scripting technology are provided in this section.

The functions of the API library enable the model to be loaded into the HIL emulator with the desired adjustment of digital and analog pins. The operation of all emulated power sources can be set up online, such as their parameters, phase angles, and higher harmonics. Furthermore, the current state of power electronic devices or contactors can be controlled during runtime. The user is able to capture signals in the emulated model to a very long buffer as powerful FPGA technology is usually used with the emulator. Any desired data analysis or report can be performed during testing or at the end of the test.

An illustration of the script-testing tool is presented in Fig. 4. The upper part of the script editor panel is the text editor responsible for the manual writing and editing of the Python scripts. The console panel in the bottom part displays the output from the user's script. The example in Fig. 4 shows the grid voltage frequency sweep. The desirable flag, pass or fail can be delivered after the test, and particular details are generated in a separate log file. In this manner, a powerful script testing tool is obtained that simplifies and automates the entire testing procedure.

In software engineering, continuous integration and delivery (CI/CD) is the practice of merging all developers' working copies into a shared mainline several times a day, as well as performing software releases in short cycles [32]. The described environment is an excellent candidate that naturally supports the CI/CD development approach.

The solution presented so far is highly flexible, but it can be used by only one user at time. However, the possibility of sharing expensive HIL equipment has been recognised for a long time. Remote Internet access can be adopted in a conventional laboratory [33], [34] but this is a rigid and inflexible solution. The proposed HIL system, together with scripting tools, can overcome these disadvantages by implementing an embedded scope tool that enables convenient web-based development. The software tool is presented in the next section.

FIGURE 4. Developed script editor tool: an example of grid voltage frequency sweep.

VI. REAL-TIME DATA ACQUISITION

The development of a control algorithm for a frequency converter requires comprehensive data acquisition and visualization. In the case of HIL simulators, this is usually provided by powerful FPGA circuits with high computational resources. However, data acquisition in this paper was not implemented within the emulator, but rather in the DSP. The oscilloscope embedded functionality is implemented into the DSP [29] used at the same time for control and data acquisition. The following subsections discuss the implementation details of the embedded oscilloscope for the target DSP and host PC applications.

A. BUILT-IN OSCILLOSCOPE HARDWARE

The built-in oscilloscope should consume as few hardware resources as possible, considering the processing time, available controller memory and the number of occupied pins used to communicate with the host PC [35]. The universal serial bus (USB) is a standard connection from the host PC. From the target DSP, there are several possibilities for communication: parallel interface, JTAG, SPI, I2C and universal asynchronous receive-transmit (UART). Even at low-cost DSP uses UART as the communication interface. Therefore, UART was chosen as the final solution together with an off-the-shelf USB/UART converter chip. It provides independent full-duplex communication between nodes, which suits the needs of the built-in oscilloscope. UART low data-flow speed is significantly diminished nowadays, since the data is first

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packed in a converter placed near the DSP (i.e. at a short distance which is noise resistant) and afterwards, the data is transmitted to the host side.

B. BUILT-IN OSCILLOSCOPE SOFTWARE

The calculation of the data flow is shown in the following example: For eight simultaneously observed DSP variables var_{num} and PWM frequency of converter $f_{PWM} = 20$ kHz, the desired data rate DR in bits/s can be calculated as:

$$DR = f_{PWM} \cdot var_{num} \cdot var_{length}$$
$$= 20000 \cdot 8 \cdot (4 \cdot 8) = 5, 12 \; Mbps. \quad (2)$$

This is valid only for pure data values without communication overhead bytes. The real dataflow is slightly higher. The USB protocol specification defines high data rates, but the system bottleneck is the maximum achievable speed of the UART. Therefore, the data are buffered in the DSP and transmitted in packets. For the maximum UART speed (921.6kbps), DSP buffered data (8kwords of internal RAM) are sent to the host, finally resulting in 8 channels with 500 points per screen, 32 bit/channel, and a refresh rate of 4 screens per second. In general, the number of screen points depends heavily on the allocated buffer size (i.e. DSP RAM size). For the DSP [29] used in this study, the size of the scope buffer represents 25% of the total available RAM memory what provides enough space for additional user code and data.

To avoid extensive memory usage, data are acquired in a single DSP buffer and transmitted immediately when it is received. Two possible modes are illustrated in Fig. 5. The fast mode, where data is collected with a small decimation value (e.g. in each PWM time instant) and then new data buffering is started only after all the data have been transmitted. In the slow oscilloscope mode (high decimation value), data are acquired, transmitted, and received on the host side continuously.
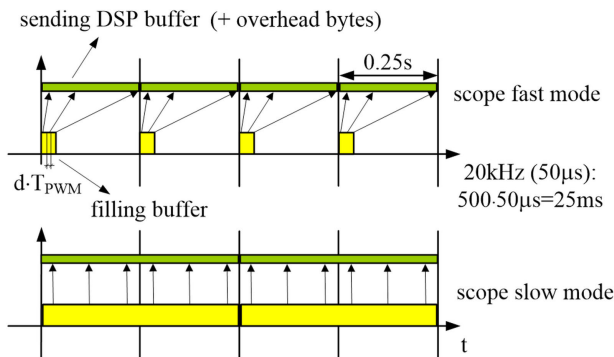

FIGURE 5. Time schedule of DSP buffer filling and sending [29].

The built-in oscilloscope has two modes: AUTO and NORMAL. The AUTO mode implies that samples are acquired and transmitted to the host continuously and there is no special event that triggers data acquisition. In the NORMAL
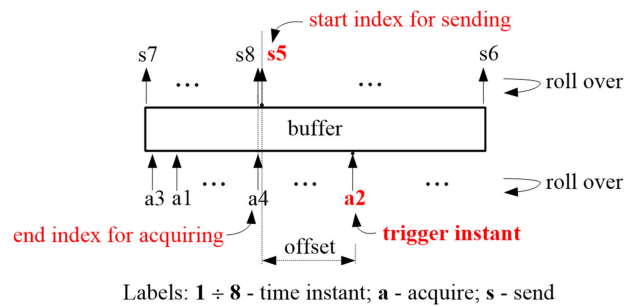

FIGURE 6. Principle of NORMAL triggering mode.

mode, data acquisition starts only when the selected variable value equals its threshold value on the rising or falling edge. This scope mode is useful if a step response (e.g. grid currents) must be evaluated.

A detailed explanation of the NORMAL mode is provided in Fig. 6. In the time period $a_1 - a_2$ before the trigger the samples are acquired, but not sent to the host. At the trigger time instant a_2, the DSP calculates the end-index value a_4 up to which the buffer will be filled (depending on the user-chosen time). If the buffer is full at a_4, the DSP starts transmitting the data to the host PC at s_5. During periods $s_5 - s_8$, no new trigger is allowed. Therefore, this situation differs from AUTO mode. The start index values in the AUTO mode are zero, but in the NORMAL mode, the start index values are adjustable.

Buffered data are sent to the host PC in packet frames. The encoding technique must be applied so that host can extract the values of the variables from the received packet. There are two possible options: an ASCII character-encoding scheme and a pure binary data format. The latter format was chosen because of the large amount of data to be transmitted.

To achieve the easily implementable built-in oscilloscope functionality with the generic DSP intended for power converter control, an algorithm structure was proposed, as shown in Fig. 7. In the function *ScopeHandlerInit()*, the UART pins, the main data, and auxiliary buffers with accompanying
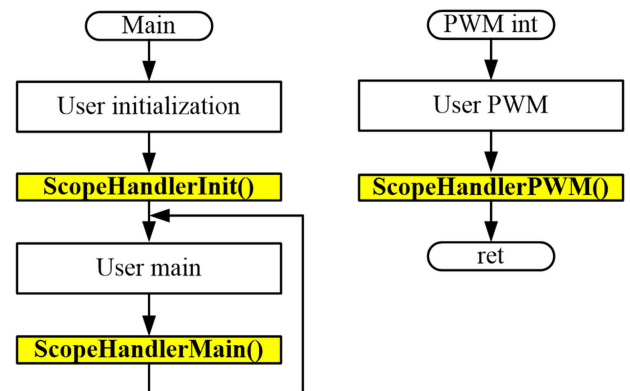

FIGURE 7. Proposed algorithm: the location of the built-in oscilloscope functions in the main function.

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pointers are initialised. The *ScopeHandlerMain()* function checks if there is host data to be received, then parses it, and performs suitable action as the start of the scope, variable write, etc. If the scope function is active, it fills the sending buffer with the data. The *ScopeHandlerPWM()* function is placed at the end of the user's PWM interrupt routine. Depending on the chosen variable names, decimation, and trigger mode, it fills the main buffer with the data. It can be seen that the scope frequency range is directly related to the PWM frequency. All described functions were optimised with respect to the processing time of the DSP. This is based on the fact that the main role of the DSP is to control the power converter in real time. The proposed built-in oscilloscope consumes less than 5% of the total calculation time resources of a specific DSP.

The selection of the built-in oscilloscope variables is performed via a drop-down list in the user application window, as shown in Fig. 8. Based on the names of the variables, the host application extracts addresses from the mapped variable file (.map). Consequently, these addresses are sent to the DSP which reads the data from the corresponding memory locations. In this manner, the user does not have to specify the variable names and addresses, because they are dynamically changed as soon as the new project is generated. This is a novel solution that considerably facilitates the development procedure.
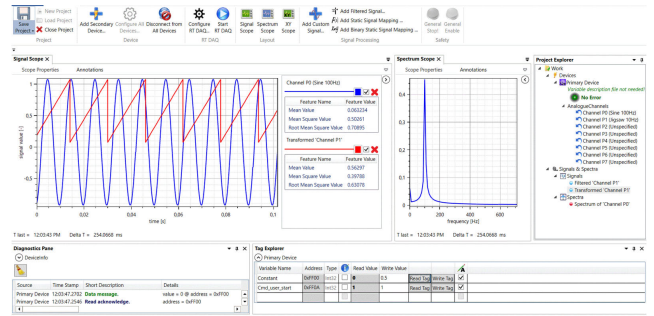

FIGURE 8. Oscilloscope decimation and variable selection.

The variables received from the DSP can be visualised on the panel in real time as shown in Fig. 9. The developed software tool provides filtering, mathematical operations, and harmonic analysis of the signals on the host PC side, what alleviates the DPS processing time. Furthermore, any selected

FIGURE 9. Final software tool: The panel of built-in oscilloscope.

DSP variable can be modified even when the scope is running. Further details can be found in [36]. The built-in oscilloscope proposed here does not require an expensive debugger via JTAG and can be used not only during the development phase but also for on-site maintenance of the DGS.

VII. THE CASE STUDY: EMULATION OF A GRID WITH 26 NODES

The design of the novel testing framework and all of its subsystems were verified by addressing the typical problem in distribution networks with several DGS. The results are presented in the following section. A distribution network consisting of 4 active and 22 passive nodes was emulated and its reaction to a grid fault was tested. The model was instantiated with the data obtained from the real distribution network. The real-world results were compared with the results obtained during the emulation, and they coincided with errors of less than 3% for all voltages and currents in the network. The active nodes (DGS) were initially turned off. The complete grid network was emulated by the connection of Typhoon HIL602 devices in parallel.

The experimental setup is shown in Fig. 10. The emulator units for the emulation of the grid in real time are indicated as '1'. Four Texas Instruments F28335 DSP units were connected to the emulators, corresponding to four active nodes in the network. These DSPs are indicated as '2'. The
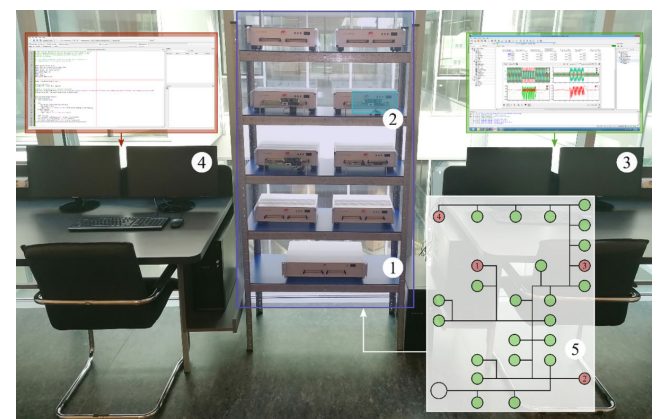

FIGURE 10. Experimental setup for verification of testing framework.

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FIGURE 11. Experimental test results for DGS 1 and DGS 2. DG1 column: Q_{MAX} and ΔP_{MIN}, DG2 column: P_{MAX} and ΔQ_{MIN}, DG3 column: Q_{MAX} and adjustable pos/neg ratio, DG4 column: no current/power limitation.

host PC for data acquisition and analysis is indicated as '3'. Another PC, indicated as '4', was used for the execution of user commands. The distribution of active and passive

nodes and the network outline is shown in '5'. The green circles represent passive nodes, and the red circles represent active DGS. The active DGSs were initially turned off. Then,

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FIGURE 12. Experimental test results for DGS 3 and DGS 4. DG1 column: Q_{MAX} and ΔP_{MIN}, DG2 column: $P_{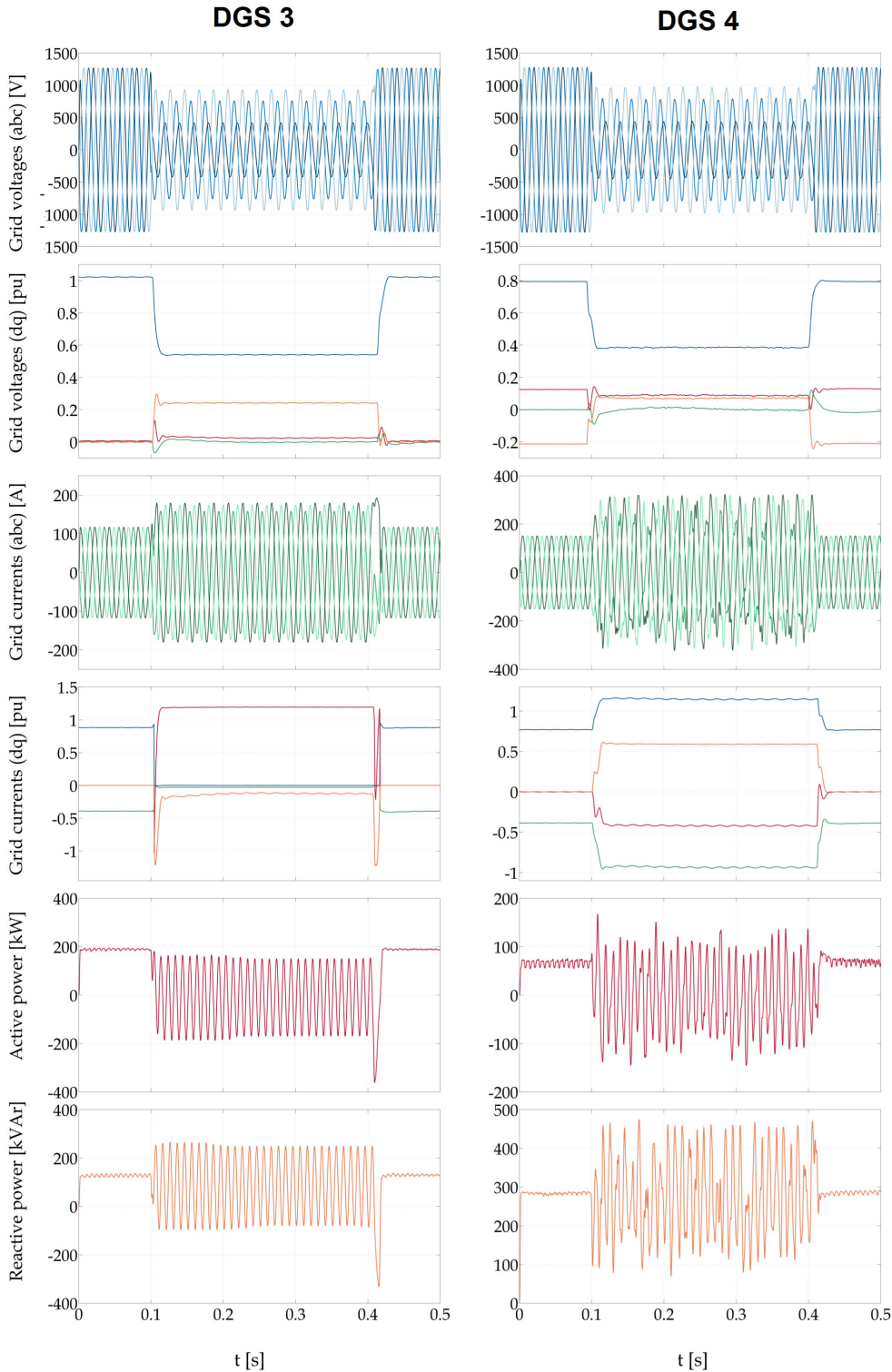MAX}$ and ΔQ_{MIN}, DG3 column: Q_{MAX} and adjustable pos/neg ratio, DG4 column: no current/power limitation.

they were activated, their basic functionalities were enabled, and the standard operation of the distribution network was established. All active DGSs were governed by the control strategy introduced in Section IV.

The goal was to test the performance of different control structures under short-circuit faults. Therefore, Python scripts were used to automate the testing procedure. The scripts were designed to load all network-related data, start the

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TABLE 1. Current references - power oscillations addressed.

	$\Delta P = 0$	$\Delta Q = 0$
i_{dp}^r	$\dfrac{P^r u_{dp}}{u_p^2 - u_n^2} + \dfrac{Q^r u_{qp}}{u_p^2 + u_n^2}$	$\dfrac{P^r u_{dp}}{u_p^2 + u_n^2} + \dfrac{Q^r u_{qp}}{u_p^2 - u_n^2}$
i_{qp}^r	$\dfrac{P^r u_{qp}}{u_p^2 - u_n^2} - \dfrac{Q^r u_{dp}}{u_p^2 + u_n^2}$	$\dfrac{P^r u_{qp}}{u_p^2 + u_n^2} - \dfrac{Q^r u_{dp}}{u_p^2 - u_n^2}$
i_{dn}^r	$-\dfrac{P^r u_{dn}}{u_p^2 - u_n^2} + \dfrac{Q^r u_{qn}}{u_p^2 + u_n^2}$	$\dfrac{P^r u_{dn}}{u_p^2 + u_n^2} - \dfrac{Q^r u_{qn}}{u_p^2 - u_n^2}$
i_{qn}^r	$-\dfrac{P^r u_{qn}}{u_p^2 - u_n^2} - \dfrac{Q^r u_{dn}}{u_p^2 + u_n^2}$	$\dfrac{P^r u_{qn}}{u_p^2 + u_n^2} + \dfrac{Q^r u_{dn}}{u_p^2 - u_n^2}$

$$u_p^2 = u_{dp}^2 + u_{qp}^2, \quad u_n^2 = u_{dn}^2 + u_{qn}^2$$

TABLE 2. Current references - power oscillations are not addressed.

	ΔP and ΔQ uncontrolled
i_{dp}^r	$\dfrac{P^r u_{dp} k_p}{u_p^2} + \dfrac{Q^r u_{qp} k_q}{u_p^2}$
i_{qp}^r	$\dfrac{P^r u_{qp} k_p}{u_p^2} - \dfrac{Q^r u_{dp} k_q}{u_p^2}$
i_{dn}^r	$\dfrac{P^r u_{dn}(1 - k_p)}{u_n^2} + \dfrac{Q^r u_{qn}(1 - k_q)}{u_n^2}$
i_{qn}^r	$\dfrac{P^r u_{qn}(1 - k_p)}{u_n^2} - \dfrac{Q^r u_{dn}(1 - k_q)}{u_n^2}$

$$u_p^2 = u_{dp}^2 + u_{qp}^2, \quad u_n^2 = u_{dn}^2 + u_{qn}^2$$

TABLE 3. New power references - oscillations are addressed.

	$\Delta P = 0$: $\quad P_{new}^r$
$I_{aamp} \geq I_{lim}$	$K \dfrac{u_p^2 - u_n^2}{u_{dp} - u_{dn}}$
$I_{bamp} \geq I_{lim}$	$K \dfrac{u_p^2 - u_n^2}{2u_{dp} + u_{dn} + \sqrt{3}u_{qn}}$
$I_{camp} \geq I_{lim}$	$K \dfrac{u_p^2 - u_n^2}{2u_{dp} + u_{dn} + \sqrt{3}u_{qn}}$

	$\Delta P = 0$: $\quad Q_{new}^r$
$I_{aamp} \geq I_{lim}$	$K \dfrac{u_p^2 + u_n^2}{u_{dp} - u_{dn}}$
$I_{bamp} \geq I_{lim}$	$K \dfrac{u_p^2 + u_n^2}{2u_{dp} + u_{dn} + \sqrt{3}u_{qn}}$
$I_{camp} \geq I_{lim}$	$K \dfrac{u_p^2 + u_n^2}{2u_{dp} + u_{dn} + \sqrt{3}u_{qn}}$

	$\Delta Q = 0$: $\quad P_{new}^r$
$I_{aamp} \geq I_{lim}$	$K \dfrac{u_p^2 + u_n^2}{u_{dp} + u_{dn}}$
$I_{bamp} \geq I_{lim}$	$K \dfrac{u_p^2 + u_n^2}{2u_{dp} - u_{dn} - \sqrt{3}u_{qn}}$
$I_{camp} \geq I_{lim}$	$K \dfrac{u_p^2 + u_n^2}{2u_{dp} - u_{dn} + \sqrt{3}u_{qn}}$

	$\Delta Q = 0$: $\quad Q_{new}^r$
$I_{aamp} \geq I_{lim}$	$K \dfrac{u_p^2 - u_n^2}{u_{dp} + u_{dn}}$
$I_{bamp} \geq I_{lim}$	$K \dfrac{u_p^2 - u_n^2}{2u_{dp} - u_{dn} - \sqrt{3}u_{qn}}$
$I_{camp} \geq I_{lim}$	$K \dfrac{u_p^2 - u_n^2}{2u_{dp} - u_{dn} + \sqrt{3}u_{qn}}$

$$u_p^2 = u_{dp}^2 + u_{qp}^2, \quad u_n^2 = u_{dn}^2 + u_{qn}^2, \quad K = \sqrt{\frac{3}{2}} I_{lim}$$

emulation, collect the data, and generate simple reports. The scripting tool initiated the faults by closing the contactors, which resulted in phase-to-ground or phase-to-phase faults. After 300ms, the contactors were opened, and the nominal conditions were recovered. Several consecutive faults were initiated at different locations in the network.

Owing to the length considerations, only one set of experimental results is shown in Fig. 11. The high-level control functions implemented define the amount of active and reactive power produced in each DGS. The 1st DGS unit was set to produce 150 kW and 125 kVAr while maximising the reactive power production and minimising the reactive power oscillations under voltage disturbances. The 2nd unit was set to produce 75 kW and 150 kVAr while maximising the active power production and minimising the reactive power oscillations under voltage disturbances. The 3rd unit was set to produce 200 kW and 150 kVAr while maximising the reactive power production and producing powers with adjustable positive/negative power ratios. The 4th unit was set to produce 100 kW and 300 kVAr while executing no current/power limitation in the case of active voltage disturbance. As shown in Fig. 11, all units had the expected responses as currents were limited and the power oscillations were controlled in accordance with the control strategy used.

The report generated by the scripting tool contains the following information: the first three units successfully ride through the disturbance, while the 4th one is disconnected in the real-life scenario because of overcurrent protection triggering. The following conclusions can be drawn: The control algorithm secures safe fault ride-through. It has been tested only against short-circuit faults; however, these disturbances are the most severe and the hardest to ride-through, therefore, it can be expected that the DGS would also be able to handle the other types of disturbances.

It is important to note that real grid data were used to model the emulated network. Thus, by experimenting on this model, it can be observed that the real network and real DGS would behave under nominal and sub-nominal conditions with a high degree of certainty.

VIII. ORIGINALITY AND DISCUSSION

The modelling of power electronic devices is a challenging task because of the heavy computations required to be

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TABLE 4. New power references - oscillations are not addressed.

	P_{new}^r	Q_{new}^r
$I_{aamp} \geq I_{lim}$	$K\dfrac{u_p^2 u_n^2}{D_1}$	$K\dfrac{u_p^2 u_n^2}{D_4}$
$I_{bamp} \geq I_{lim}$	$K\dfrac{2u_p^2 u_n^2}{D_2}$	$K\dfrac{2u_p^2 u_n^2}{D_5}$
$I_{camp} \geq I_{lim}$	$K\dfrac{2u_p^2 u_n^2}{D_3}$	$K\dfrac{2u_p^2 u_n^2}{D_6}$

executed during short time steps. The computational performance is also influenced by the number of grid nodes. Even for medium-scale grids in which the transient phenomena must be addressed, HIL computational overburden is highly possible. Consequently, in the case where several PE devices together with a couple of nodes are involved, it is not clear when the computational limits are exceeded. Various HIL setups possess different performance levels, and it is very difficult to provide a detailed comparison of different HIL, considering their complexity as well. Therefore, the comparison is often simplified to compare a reachable time step. The state-of-art for different HIL simulators, containing a comprehensive list provided in the tabular review, given in [37], concludes that only a few of them are capable of simulating large systems.

In this study, highly flexible DGS converter control, in a distribution network environment consisting of 26 nodes, was successfully established on a parallel HIL infrastructure with $0.5\mu s$ time step, which outperforms most of the applications presented in [37] and [38]. Compared to other HIL setups, the setup presented in this paper is unique as it integrates enhanced Python scripting. Although Python was already used in [39] to establish high-level control over real hardware, it was not used as a comprehensive environment. In our solution, Python was utilised for enhanced system development and testing. It provides a dynamic system change achievable in each parameter, starting from the grid side attributes and ending with the controller side parameters. The utilisation of Python enables continuous integration, delivery, and deployment, contributing to a fully rapid

development and testing framework. In addition, the original aspect of our solution is the embedded oscilloscope tool. This tool was built from the ground up regarding the software architecture along with implementation aspects both on the controller and operator sides. It provides powerful controller data acquisition and analysis. Finally, the last original aspect is the DGS black-bock functionality which, to the best authors' knowledge, has not been reported yet.

IX. CONCLUSION

In this paper, a comprehensive framework for the development and testing of DGS control algorithms is presented. HIL systems can simply and effectively test the behaviour of EPS systems rich in DGS. Modern power systems' DGS are considered to be flexible black box units governed by high-level controllers. The proposed framework has four inherent parts: an HIL simulator for the emulation of complex EPS systems, a high-level controller executed in DSP, an embedded oscilloscope tool for data acquisition and Python scripting. The embedded oscilloscope tool, developed completely from the ground up, does not impose an additional burden on the controllers and does not disrupt the proper control of the DGS. Furthermore, the embedded oscilloscope tool reduces the need for external measurements, thus reducing the complexity and the cost of the system. Utilizing the embedded oscilloscope tool with the DGS converter's current and voltage sensors enhances the overall system insight. Employing proposed flexible and generalized oscilloscope architecture, both measured or any internal controller data can be selected synchronously with the PWM frequency of the converter. No additional embedded hardware components are needed, due to optimized usage of already existing controller's memory and common periphery. This functionality is favorable not only for the producers of DGS during the development process but also for grid operators during the exploitation phase. Python scripting is a valuable tool for the automation of tests and generation of reports. The scripts can initiate tests, record results, analyse them, and generate reports without the user's presence. A library with a collection of diverse scripts created can be exchanged and maintained on a global level, expanding platform scalability usage additionally. Unique and clear design principles, team awareness and transparency,

TABLE 5. The constants from Table 4.

$$D_1 = \left(u_p^2(1-k_p)u_{qn} - u_n^2 k_p u_{qp}\right)\sin\theta_{pa} + \left(u_p^2(1-k_p)u_{dn} + u_n^2 k_p u_{dp}\right)\cos\theta_{pa}.$$

$$D_2 = \left(u_p^2(1-k_p)(-\sqrt{3}u_{dn} - u_{qn}) + u_n^2 k_p(\sqrt{3}u_{dp} + u_{qp})\right)\sin\theta_{pb} + \left(u_p^2(1-k_p)(-u_{dn} - \sqrt{3}u_{qn}) + u_n^2 k_p(-u_{dp} + \sqrt{3}u_{qp})\right)\cos\theta_{pb}.$$

$$D_3 = \left(u_p^2(1-k_p)(\sqrt{3}u_{dn} - u_{qn}) + u_n^2 k_p(-\sqrt{3}u_{dp} + u_{qp})\right)\sin\theta_{pc} + \left(u_p^2(1-k_p)(-u_{dn} - \sqrt{3}u_{qn}) + u_n^2 k_p(-u_{dp} - \sqrt{3}u_{qp})\right)\cos\theta_{pc}.$$

$$D_4 = \left(-u_p^2(1-k_q)u_{dn} + u_n^2 k_q u_{dp}\right)\sin\theta_{qa} + \left(u_p^2(1-k_q)u_{qn} + u_n^2 k_q u_{qp}\right)\cos\theta_{qa}.$$

$$D_5 = \left(u_p^2(1-k_q)(u_{dn} - u_{qn}\sqrt{3}) + u_n^2 k_q(u_{qp}\sqrt{3} - u_{dp})\right)\sin\theta_{qb} + \left(u_p^2(1-k_q)(-u_{qn} - u_{dn}\sqrt{3}) + u_n^2 k_q(-u_{dp}\sqrt{3} - u_{qp})\right)\cos\theta_{qb}.$$

$$D_6 = \left(u_p^2(1-k_q)(u_{qn}\sqrt{3} + u_{dn}) + u_n^2 k_q(-u_{dp} - u_{qp}\sqrt{3})\right)\sin\theta_{qc} + \left(u_p^2(1-k_q)(u_{dn}\sqrt{3} - u_{qn}) + u_n^2 k_q(u_{dp}\sqrt{3} - u_{qp})\right)\cos\theta_{qc}.$$

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along with rapid strengthening of highly skilled teams are promising with the proposed infrastructure. The quality of the data gathered both on HIL and controller side in this paper was high and the data can be used for further analysis. In addition, the data can be forwarded to other control layers. The combination of these rapid prototyping tools leads to a significant reduction in the time and effort needed for the development and verification of DGS complex control functions in modern power systems. Moreover, thanks to the unrestricted converter's power range, as well as power grid topology compared to the even small (down-powered) real-hardware setups, the proposed system reduces overall costs to a minimum.

Future development scenarios could deal with automated scripting of real-time grid communication using various protocols to expand system fidelity. Furthermore, the environment will be enhanced so it can be examined on islanded microgrid systems. Finally, certain high-level functionalities will be implemented and tested using the proposed approach.

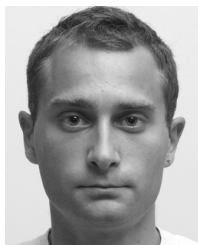## APPENDIX
Table 1 to Table 5.

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