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Gate Driver for Wide-Bandgap Power Semiconductors With Small Negative Spike and Switching Ringing in Zero-Voltage Switching Circuit

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ABSTRACT Because SiC MOSFET-based zero-voltage switching (ZVS) power converter circuits provide high-speed switching, high power density and high efficiency can be achieved. However, an undesired negative spike is formed at the gate-source voltage owing to the crosstalk phenomenon in leg structures, such as half-bridge switch configurations, during high-speed switching. Additionally, ringing voltage occurs owing to resonance between the snubber capacitor and the common source inductance of the SiC MOSFET. Because SiC MOSFETs have a lower gate voltage rating than conventional Si devices, it is essential to reduce the negative spike and ringing voltages to ensure reliability. In this paper, the gate driver circuit is proposed for reducing the negative spike and ringing voltages of the gate-source in ZVS circuits. Because the proposed gate driver circuit provides an effective impedance path for each section through an active switch, a stable driving voltage range of the gate-source can be achieved. To verify the proposed gate driver circuit, an accurate simulation model of the 3-pin SiC MOSFET package is proposed, and the validity of the proposed model is verified through comparison of the simulated waveforms with experimental waveforms. The performance of the proposed gate driver circuit is verified through PSpice simulation.

INDEX TERMS Crosstalk, gate driver, negative spike, SiC MOSFET, snubber capacitor, ZVS.

I. INTRODUCTION

Power converters are key components in various industrial applications, such as renewable energy, electric transportation, and aerospace systems. Accordingly, high-speed switching techniques for switching devices are being implemented to achieve miniaturization, high efficiency, and weight reduction of power converters. Examples include widely applied soft-switching techniques, which use the resonance of a capacitor and an inductor. Soft switching technique enable switching devices to achieve high-speed switching and increased efficiency by reducing switching losses through zero-voltage or zero-current transitions during on/off operations [1]–[7]. Additionally, high-speed switching can be realized by replacing the conventional silicon (Si)-based switching devices with wide-bandgap (WBG) devices. WBG devices have superior physical properties to Si-based devices and offer the advantages of fast switching speed and low conduction resistance [6]–[11]. Therefore, high power density and high efficiency can be achieved by concurrently using a WBG device and applying a soft-switching technique.

However, during high-speed switching, undesirable crosstalk occurs in leg structures, such as half-bridge switch configurations [12]–[23]. Crosstalk is a phenomenon in which positive and negative spikes appear in the gate-source voltage owing to the current flowing into the Miller capacitor in the *dv/dt* section of the drain-source during turn-on and

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TABLE 1. Parameters of switch devices [24]–[26].

Parameter	SiC MOSFET	Si MOSFET	Si IGBT
Part number	SCTW90N65G2V	STY139N65M5	STGW80H65FB
Gate threshold voltage	1.9 V ~ 5 V	3 V ~ 5 V	5 V ~ 7 V
Gate-source voltage	+22 V ~ −10 V	+25 V ~ −25 V	+20 V ~ −20 V
Recommended gate-source voltage	+18 V ~ −5 V	+25 V ~ −25 V	+20 V ~ −20 V

turn-off. As shown in Table 1, because SiC MOSFETs have a lower threshold voltage than Si devices, unwanted turn-on may occur because of positive spikes. Therefore, this may result in an increase in switching loss and, in the worst case, switch burnout [14], [15]. Additionally, because SiC MOSFETs have low gate-source negative voltage rating, the rating may be exceeded owing to a negative spike by crosstalk, which results in switch burnout [22], [23].

In [15]–[17], negative offset voltage was applied during turn-off to reduce the effect of the positive spike voltage. If negative offset voltage is applied during turn-off, the threshold voltage margin for a positive spike can be obtained. In [17]–[21], the positive spike voltage was reduced by adding an active Miller clamp to the gate-source. Because the active Miller clamp technique is operated in the dead time period after turn-off, it does not affect the switching performance. Additionally, it provides a low-impedance path, and the positive spike voltage formed at the gate-source can be reduced. However, conventional methods for reducing the positive spike caused by crosstalk cannot decrease the negative spike voltage but can worsen it instead. In [22] and [23], the positive and negative spike voltages caused by crosstalk were reduced by adding an auxiliary circuit to the gate-source. However, the ringing voltage due to inductances such as common source inductance (CSI) included in the gate loop was not fully considered.

Meanwhile, isolation converters, such as series-resonant, parallel-resonant, phase-shift full-bridge, dual-active-bridge, and LLC converters, can achieve zero-voltage switching (ZVS) over the designed frequency range [1]–[7]. However, turn-off loss still exists because hard switching occurs at turn-off [1], [6]. To solve this problem, the turn-off loss can be reduced by adding additional snubber capacitors at both sides of the switches [2], [27]–[29]. However, a ZVS with a snubber capacitor suffers from a resonance problem between the CSI and snubber capacitor [30]–[32]. For 3-pin package SiC MOSFET devices particularly, because CSI is unavoidably included in gate-source loops, ringing voltage occurs at the gate-source owing to the resonance [33], [34]. Because SiC MOSFETs have low gate-source threshold voltage and low negative voltage rating, as shown in Table 1, the negative spike and ringing voltages must be reduced to ensure the reliability of the gate driver circuit.

In this paper, we propose a new gate driver circuit for a SiC MOSFET-based ZVS circuit. It can reduce both the negative spike voltage caused by crosstalk and the ringing voltage caused by the resonance of the snubber capacitor and CSI. Before proposing the gate driver circuit, a detailed mode analysis of the dead time period is performed, and the gate loop is analyzed. For accurately analyzing the proposed gate driver circuit, a simulation model that reflects the dynamic characteristics of a 3-pin SiC MOSFET is proposed. Additionally, the proposed simulation model is validated through comparison with actual experimental results. The performance of the proposed gate driver circuit is verified through PSpice simulation.

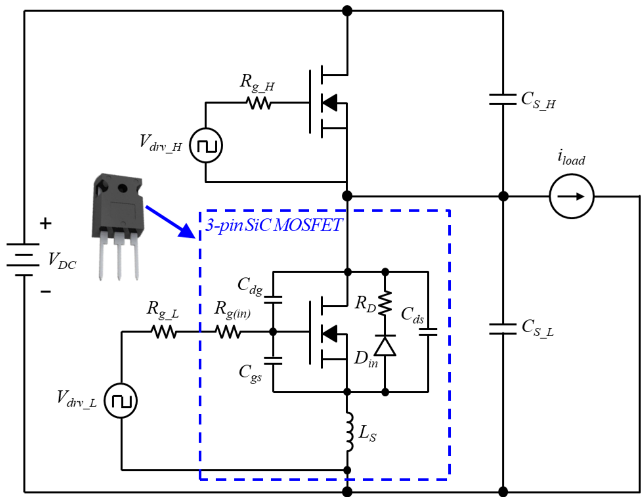


FIGURE 1. Equivalent ZVS circuit with a 3-pin SiC MOSFET.

II. GATE-SOURCE MODE ANALYSIS FOR ZVS CIRCUIT

In this section, a detailed mode analysis is conducted to analyze the causes of the negative spike and ringing voltages of the gate-source. Figure 1 shows the equivalent ZVS circuit, in which the parasitic components of the 3-pin package SiC MOSFET are included. Here, V_{DC} represents the input voltage of the ZVS circuit; C_{S_H} and C_{S_L} denote the snubber capacitors connected in parallel with high and low switches; C_{ds}, C_{dg}, and C_{gs} represent parasitic capacitors of the switch; and L_s denotes the CSI by the inner bonding wire and source terminal of the package. D_{in} denotes the body diode of the switch, R_d is the equivalent resistance of the body diode, and $R_{g(in)}$ is the internal gate resistance. R_{g_H} and R_{g_L} represent the external gate resistances, V_{drv_H} and V_{drv_L} are the input voltages of the gate driver, and i_{load} is the load current.

A. ANALYZING THE NEGATIVE SPIKE VOLTAGE OF GATE-SOURCE

Figure 2 shows the operation waveform during the dead time period from the turn-off of the high switch to the section in which the body diode of the low-switch conducts. Figure 3 shows the operation mode for each section from t_0 to t_4. Here, i_{sw_H} represents the current of the high switch and i_D is the current of the body diode. i_{Cds}, i_{Cdg}, and i_{Cgs} denote the

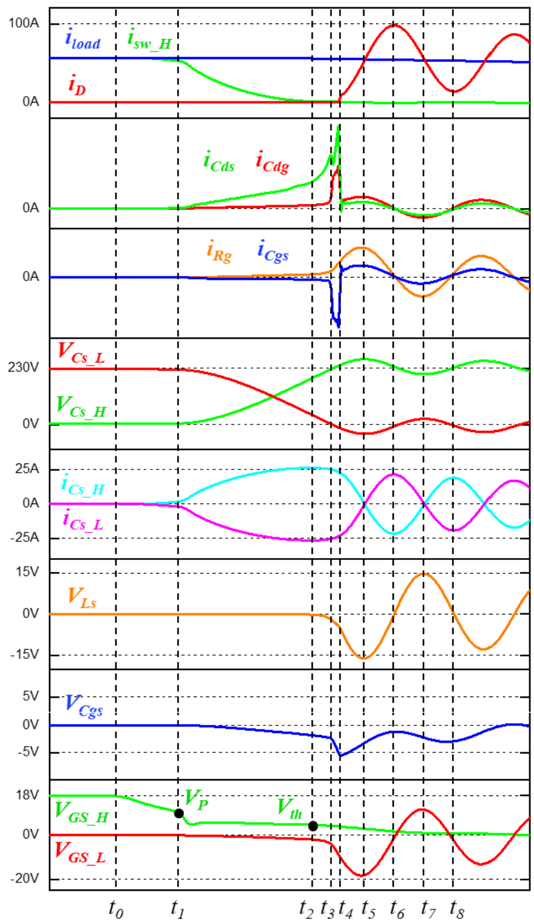


FIGURE 2. **Operation waveform of the ZVS circuit during dead time.**

currents flowing through each parasitic capacitor, and i_{Rg} is the current flowing through the gate resistor. V_{Cs_H} and i_{Cs_H}, and V_{Cs_L} and i_{Cs_L} represent the voltages and currents of the high-and low-side snubber capacitors, respectively, and V_{Ls} denotes the voltage formed across the CSI. V_{Cgs} represents the voltage across the input capacitor C_{gs}, and V_{GS_H} and V_{GS_L} denote the gate-source voltages of the high- and low-side switches, respectively. V_P represents the Miller plateau voltage of the switch, and V_{th} denotes the threshold voltage of the switch.

Before t_0, V_{GS_H} is 18 V and V_{GS_L} is 0 V; thus, the high switch is turned on, and the low switch is turned off. Therefore, in this section, power is transmitted to the load through the high switch.

1) STAGE 1 (t_0–t_1)

At t_0, V_{GS_H} decreases to V_P by the turn-off signal of the high-side gate driver, and the operation region of the high switch moves from the linear region to saturation region. Therefore, although V_{GS_H} decreases, the channel of the high switch is maintained because the operating region of the switch is located in the saturation region, and i_{sw_H} is equal to i_{load}.

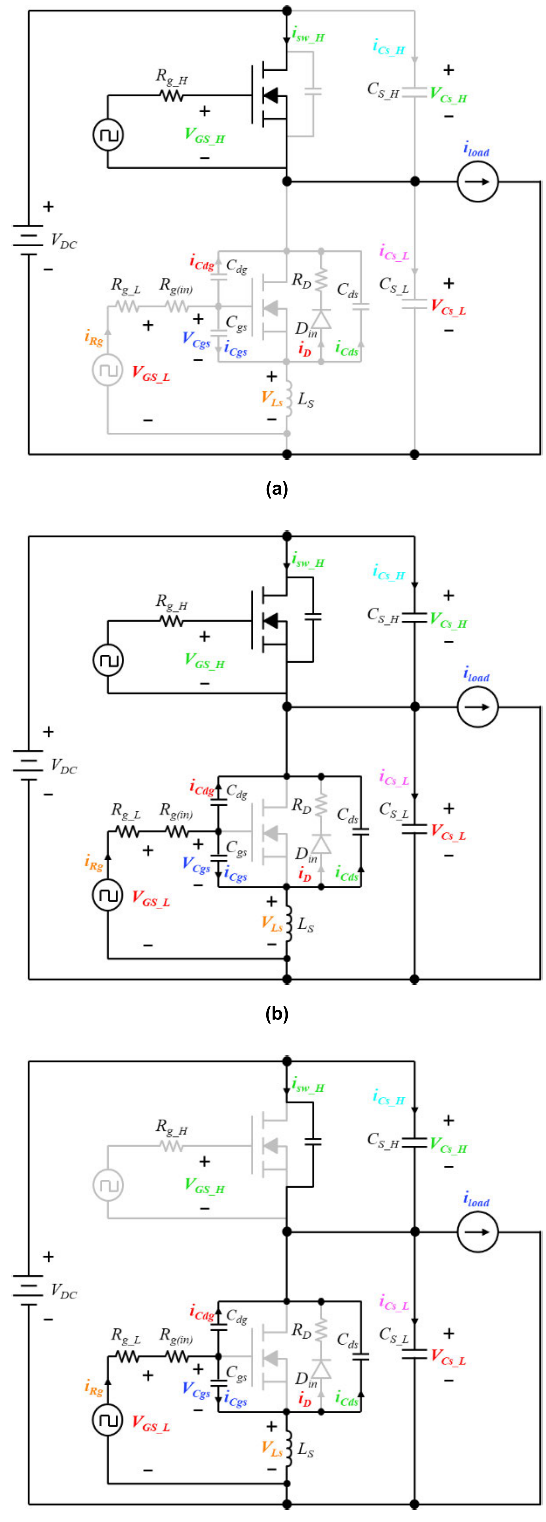


FIGURE 3. **Operation mode of the ZVS circuit. (a) Stage 1 (t_0–t_1), (b) Stage 2 (t_1–t_2), and (c) Stage 3 (t_2–t_4).**

2) STAGE 2 (t_1–t_2)

In the section from V_p to V_{th} of V_{GS_H}, i_{sw_H} starts to decrease at t_1 and the high swich completely turns off at t_2. Therefore, the output capacitors of the high and low switches are charged

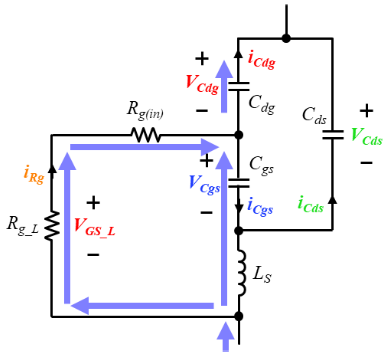


FIGURE 4. Equivalent circuit of the gate loop at t_1–t_4.

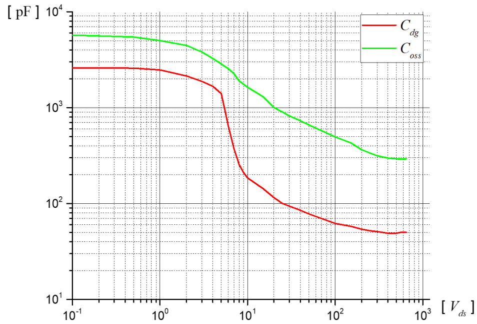


FIGURE 5. Capacitance of the SCTW90N65G2V device according to drain-source voltage.

and discharged by i_{load} as i_{sw_H} decreases. Additionally, at t_1, V_{Cs_H} and V_{Cs_L} start to rise and fall, and because the current and voltage of the switch intersect in the corresponding section, turn-off loss occurs in the high switch.

Figure 4 shows the current path formed in the gate loop of the low switch from t_1 to t_4. At t_1, V_{Cds} drops to –*dv/dt* by the discharge of C_{ds} and C_{S_L} of the low switch, and the discharge current i_{Cds} gradually increases. Simultaneously, according to the relationship among V_{Cds}, V_{Cdg}, and V_{Cgs}, as shown in (1), V_{Cdg} and V_{Cgs} decrease in proportion to V_{Cds}. Therefore, the current paths of i_{Cdg} and i_{Cgs} are formed in the discharge direction, as shown in Figure 4, and i_{Cdg} is equal to the sum of i_{Rg} and i_{Cgs}, as shown in (2).

$$V_{Cds} = V_{Cdg} + V_{Cgs} \tag{1}$$

$$i_{Cdg} = i_{Rg} + \left|i_{Cgs}\right| \tag{2}$$

Therefore, because of the current flowing through the gate loop, a negative spike starts to form in V_{GS_L} and V_{Cgs}, in proportion to the voltage drops of R_{g_L} and $R_{g(in)}$, as shown in the following equations:

$$V_{GS\_L} = -R_{g\_L} \times \Delta i_{Rg} \tag{3}$$

$$V_{Cgs} \approx -\left(R_{g\_L} + R_{g(in)}\right) \times \Delta i_{Rg} \tag{4}$$

3) STAGE 3 (t_2–t_3)

At t_2, the high switch is turned off, and most of the load current flows through C_{S_H} and C_{S_L}. Because the charging and discharging of the snubber capacitors are not completed in this section, C_{S_H} and C_{S_L} are continuously charged and discharged from the load current in the same way as in Stage 2.

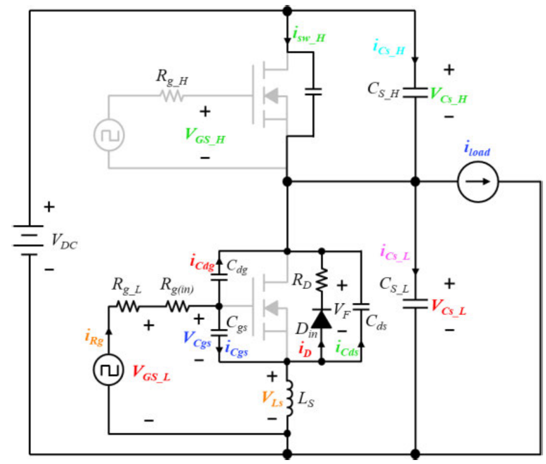


FIGURE 6. Operation mode of the ZVS circuit at Stages 5–8 (t_4–t_8).

4) STAGE 4 (t_3–t_4)

At t_3, V_{ds} of the low switch is sufficiently discharged to be 10 V or less. The device used in this study is the same as the SiC MOSFET in Table 1 (SCTW90N65G2V), and Figure 5 shows the capacitance of the device according to drain-source voltage. As shown in the figure, when the drain-source voltage is less than 10 V, C_{ds} and C_{dg} increase rapidly, and the impedance decreases. Therefore, the slopes of i_{Cds} and i_{Cdg} increase rapidly in this section, and i_{Rg} and i_{Cgs} increase in proportion to i_{Cdg}, as shown in (2). Accordingly, a negative spike with a sharp slope is formed in V_{GS_L} and V_{Cgs}.

B. ANALYZING THE RINGING VOLTAGE OF THE GATE-SOURCE

Figure 6 shows the operation mode from t_4 to t_8. At t_4, V_{Cds} is formed as $-V_F$, and thus D_{in} conducts. Based on these characteristics, ZVS is achieved during turn-on.

1) STAGE 5 (t_4–t_5)

Because most of the load current flows through D_{in} after t_4, i_D increases to i_{load}. Owing to the increase in i_D, a negative voltage is formed in L_S by $-di/dt$. Accordingly, V_{Cs_L} decreases by $-V_{Ls}$ and reaches a minimum voltage, and V_{Cs_H} increases by V_{Ls} and reaches a maximum voltage. Therefore, overshoot and undershoot occur in V_{Cs_H} and V_{Cs_L} at t_5, and *dv/dt* equals 0; hence, i_{Cs_H} and i_{Cs_L} become 0 A.

2) STAGE 6 (t_5–t_6)

From t_5 to t_6, V_{Cs_L} rises to $-V_F$, and V_{Cs_H} falls to $V_{DC}+ V_F$, returning to the same voltage as that at t_4. Simultaneously, the current direction of the snubber capacitor is reversed by *dv/dt* of V_{Cs_H} and V_{Cs_L}. Therefore, as shown in (5), i_D increases by the current of the snubber capacitor and reaches a maximum value at t_6. Accordingly, *di/dt* of i_D

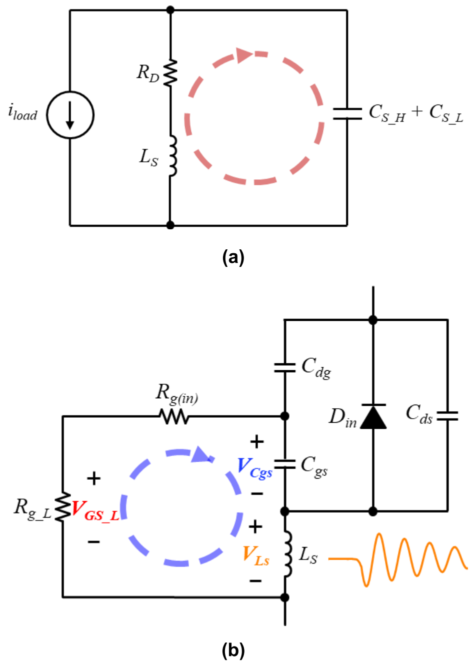


FIGURE 7. **Equivalent circuit at t_4–t_8. (a) Power loop. (b) Gate loop.**

becomes 0 at t_6, and thus V_{Ls} rises to 0 V:

$$i_D \cong i_{load} + \left|i_{Cs\_H}\right| + \left|i_{Cs\_L}\right| \tag{5}$$

3) STAGE 7 (t_6–t_7)

At t_6, i_D is formed to a maximum value because of the current of the snubber capacitor, and at t_7, i_D returns to i_{load}. Simultaneously, V_{Ls} increases by $+di/dt$ owing to the decrease in i_D. Accordingly, V_{Cs_L} increases and V_{Cs_H} decreases by V_{Ls}. Therefore, at t_7, dv/dt of V_{Cs_H} and V_{Cs_L} become 0; thus, i_{Cs_H} and i_{Cs_L} become 0 A.

4) STAGE 8 (t_7–t_8)

At t_7, V_{Cs_L} is equal to $-V_F$, and V_{Cs_H} is equal to $V_{DC}+V_F$. The current direction of the snubber capacitor is reversed after t_7 by dv/dt of V_{Cs_H} and V_{Cs_L}. Therefore, as shown in (6), i_D decreases by the snubber capacitor current and reaches a minimum value at t_8. Accordingly, di/dt of i_D becomes 0 at t_8; thus, V_{Ls} drops to 0 V.

$$i_D \cong i_{load} - \left|i_{Cs_H}\right| - \left|i_{Cs\_L}\right| \tag{6}$$

Through mode analysis from Stages 5 to 8, the power loop can be simplified, as shown in Figure 7(a). A resonance is induced between the snubber capacitors and L_S after the body diode conducts. Consequently, the ringing voltage with a resonance frequency occurs in V_{Ls}, i_{Cs_H}, and i_{Cs_L}, as follows:

$$f = 1/2\pi\sqrt{L_S \cdot \left(C_{S\_H} + C_{S\_L}\right)} \tag{7}$$

The gate loop can be equalized as shown in Figure 7(b), and ringing occurs at V_{GS_L} as a result of V_{Ls}, as follows:

$$V_{GS\_L} = \frac{R_{g\_L}}{R_{g\_L} + R_{g(in)}} \cdot \left(V_{Cgs} + V_{Ls}\right) \tag{8}$$

III. GATE LOOP ANALYSIS FOR RELIABILITY

In this section, a detailed gate loop analysis is performed to analyze the physical relationship between the characteristics of a 3-pin SiC MOSFET and passive elements of the gate driver. Figure 8 shows the operation waveform according to the gate resistance under the same load conditions. Between t_1 and t_4, negative spike voltages are formed in V_{GS_L} and V_{Cgs} by the current formed in the negative direction of the gate loop. Because the negative spike voltage is generated by the voltage drop of the gate resistance, as shown in (3) and (4), the smaller the gate resistance, the lower the negative spike voltage. Between t_4 and t_8, the ringing voltage occurs in V_{GS_L} because of the resonance between the snubber capacitors and L_s. The ringing voltage formed in V_{GS_L} is dominantly affected by the ringing voltage of V_{Ls}, as shown in (8). However, V_{Cgs} varies according to the magnitude of the gate resistance, as shown in Figure 8. A detailed analysis of these relationships is provided in the following.

A. DETAILED ANALYSIS OF GATE LOOP BETWEEN t_4 AND t_8

1) STAGE A (t_4–t_6)

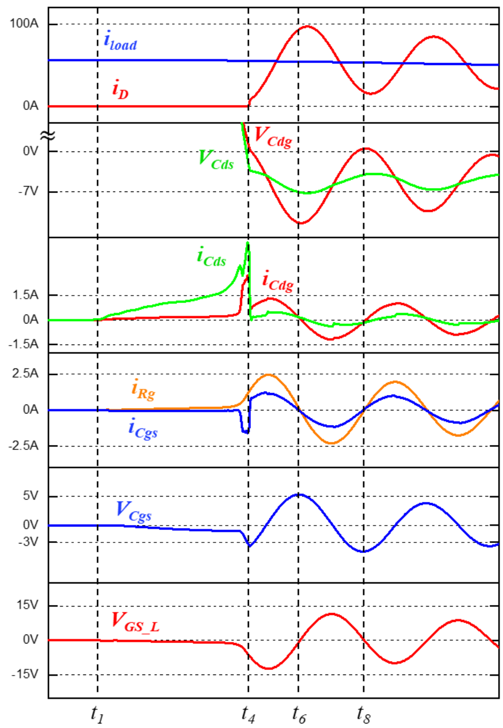
As i_D increases, i_{Cds} and i_{Cdg} flow along the path shown in Figure 9(a). Therefore, the resulting V_{Cds} and V_{Cdg} are negative, and V_{Cgs} is determined accordingly. Here, V_{Cds} changes depending on the load current. When the load condition is equal, V_{Cgs} is more affected by the change in V_{Cdg}. Notably, V_{Cdg} is formed by the i_{Rg} flowing through the gate resistor, and the magnitude of i_{Rg} increases when the gate resistance is small, as shown in Figure 8. Therefore, when R_{g_L} is small, as shown in Figure 8(a), V_{Cdg} increases to a negative value smaller than V_{Cds}, and, consequently, V_{Cgs} increases to a positive value. However, if R_{g_L} is large, as shown in Figure 8(b), V_{Cgs} is formed as a negative value because V_{Cdg} is higher than V_{Cds}.

2) STAGE B (t_6–t_8)

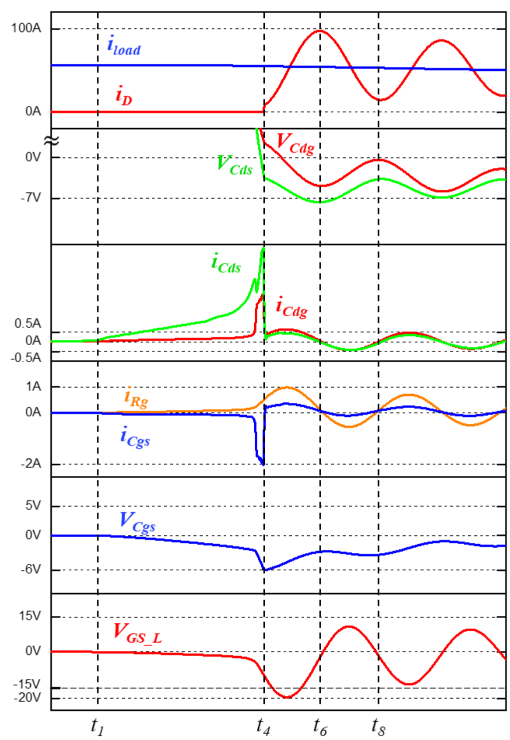
In contrast with Stage A, i_D decreases; thus, i_{Cds} and i_{Cdg} flow in the path shown in Figure 9 (b). Therefore, V_{Cds} and V_{Cdg} are charged in the positive direction. In this section, V_{Cdg} increases more than V_{Cds} regardless of the gate resistance, and the variation in V_{Cdg} is high when R_{g_L} is small, as shown in Figure 8. Thus, V_{Cgs} drops to a negative value in both cases. Consequently, the smaller the gate resistance, the greater the variation in V_{Cgs}.

B. RELATIONSHIP BETWEEN V_{GS_L} AND V_{Cgs}

Figure 10 shows the simulation results according to the gate resistance under the 2 kW load condition. The gate threshold voltage of the SiC MOSFET used is 3.2 V, and the maximum negative rating of the gate voltage is –10 V. As shown in the figure, the negative spike voltage of V_{GS_L} increases with the gate resistance. However, the ringing voltage and negative voltage of V_{Cgs} increase as the gate resistance decreases.

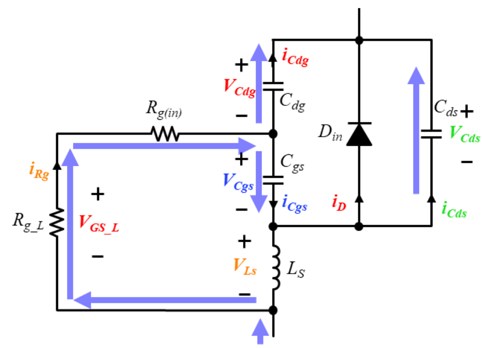


(a)

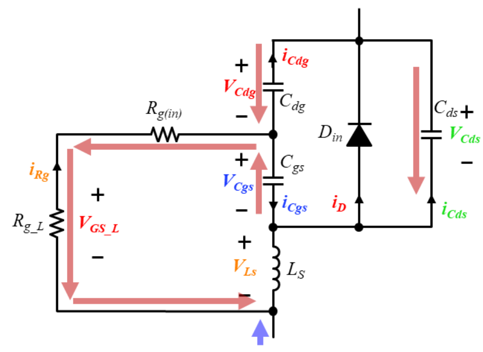


(b)

FIGURE 8. Operation waveform according to gate resistance. (a) For low gate resistance; $R_{g\_L} = 5\ \Omega$. (b) For high gate resistance; $R_{g\_L} = 20\ \Omega$.

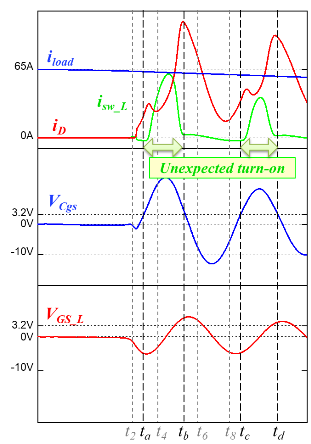


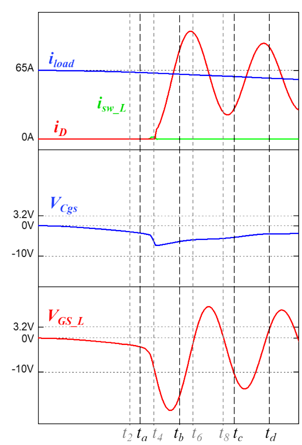
(a)



(b)

FIGURE 9. Gate loop equivalent circuit. (a) Stage A (t_4–t_6). (b) Stage B (t_6–t_8).





(a) (b)

FIGURE 10. Operation waveform at a 2 kW load condition. (a) Considerably low gate resistance; $R_{g\_L} = 1\ \Omega$. (b) Considerably high gate resistance; $R_{g\_L} = 30\ \Omega$.

Generally, the reliability of the gate-source voltage can be estimated through V_{GS_L}, which is the shortest measurable point externally. However, although V_{GS_L} exceeds the gate threshold voltage, the channel current of the low switch (i_{sw_L}) does not flow, as shown in Figure 10(b). The reason behind this phenomenon is that V_{Cgs} does not exceed the threshold voltage. Meanwhile, a large ringing voltage is generated in V_{Cgs} owing to the small gate resistance, as shown in Figure 10(a). This results in an unexpected turn-on because the ring voltage of V_{Cgs} exceeds the threshold voltage. Therefore, the reliability of gate-source voltages cannot be determined by externally measurable points (V_{GS_L}), and it is important to secure V_{Cgs} in a safe range.

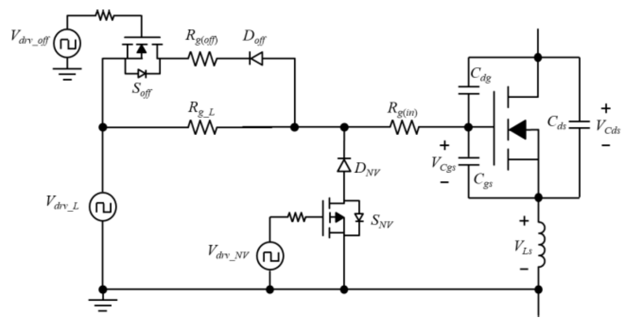


FIGURE 11. Proposed gate driver circuit.

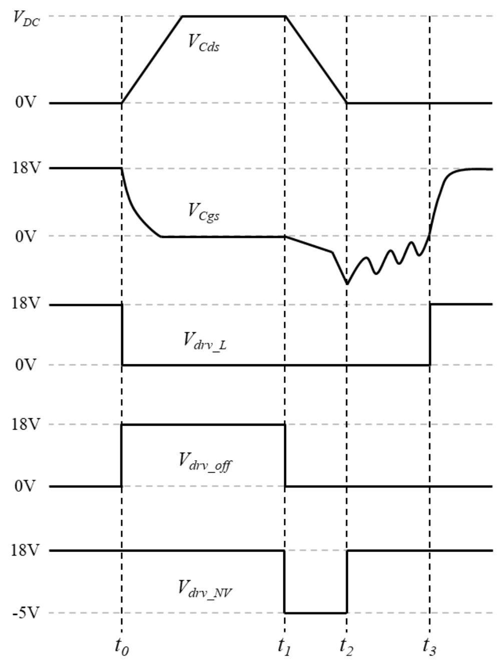


FIGURE 12. Operation waveform of the proposed gate driver circuit.

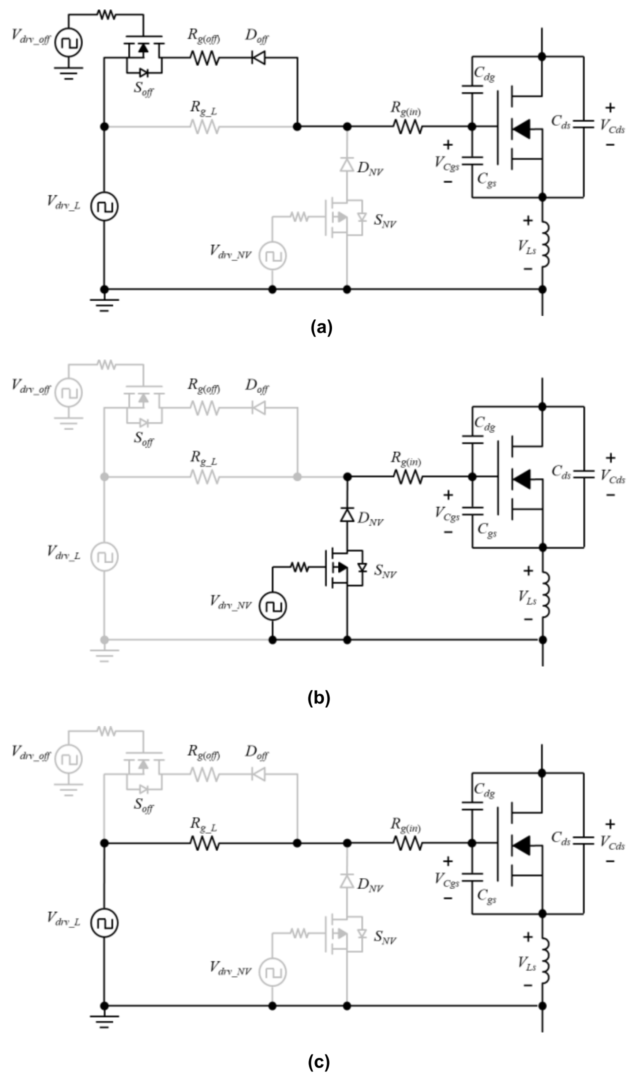


FIGURE 13. Operation modes of the proposed gate driver circuit. (a) Mode 1 (t_0–t_1). (b) Mode 2 (t_1–t_2). (c) Mode 3 (t_2–t_3).

IV. PROPOSED GATE DRIVER CIRCUIT FOR IMPROVING RELIABILITY

As analyzed in Section 3, a conventional gate driver circuit with a single-gate resistor has unavoidable performance limitations owing to the trade-off relationship between the negative spike voltage and ringing voltage. Therefore, we propose a gate driver circuit in this section to reduce the negative spike and ringing voltages simultaneously and detail the operation of the proposed circuit.

A. CONCEPT OF THE PROPOSED GATE DRIVER CIRCUIT

Figure 11 shows the proposed gate driver circuit. D_{off}, $R_{g(off)}$, and S_{off} represent a diode, resistor, and N-channel MOSFET, respectively, for the turn-off path. D_{NV} and S_{NV} denote a diode and P-channel MOSFET for reducing the negative spike voltage, respectively. V_{drv_off} and V_{drv_NV} represent the gate driving voltages for the S_{off} and S_{NV} switches, respectively. The proposed circuit maintains small and large gate resistance when negative spike voltage and ringing voltage occur, respectively. This can be realized by providing an effective impedance path for each section through the active switch (S_{off}, S_{NV}). Through this operation, the negative spike and ringing of V_{Cgs} can be simultaneously reduced.

B. OPERATIONAL PRINCIPLE OF THE PROPOSED GATE DRIVER CIRCUIT

Figure 12 shows the operation waveform of the proposed gate driver circuit, which consists of three operation modes, as shown in Figure 13. Before t_0, the low switch is turned on, and S_{off} and S_{NV} are turned off. Each operation mode is described as follows.

1) MODE 1 (t_0–t_1)

The equivalent circuit of Mode 1 is shown in Figure 13(a). As V_{drv_L} changes to 0 V at t_0, V_{Cgs} is discharged. Here, turn-off loss occurs in the low switch, as described in Stage 2 of Section 2. To reduce the switching loss, it is better to have a small gate resistance for fast turn-off. After t_0, S_{off} is turned on, and the discharge path of V_{Cgs} is blocked by D_{NV}.

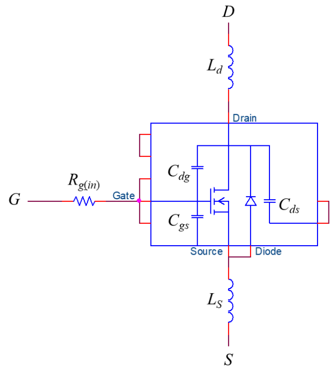


FIGURE 14. **PSpice switch model of a 3-pin SiC MOSFET.**

Therefore, V_{Cgs} is discharged through R_{g_L} or through a path leading to D_{off}, $R_{g(off)}$, and S_{off}. Simultaneously, because R_{off} is smaller than R_{g_L}, V_{Cgs} is mostly discharged through $R_{g(off)}$ and S_{off}.

2) MODE 2 (t_1–t_2)

At t_1 and t_2, a negative spike voltage is formed by the current flowing through the gate loop. Because a small impedance can lower the negative spike voltage, S_{NV} and D_{NV} should be selected as having a small impedance. As shown in Figure 13(b), S_{off} is turned off, and S_{NV} is turned on. Additionally, the current path is blocked by D_{off}. Therefore, the gate-loop current flows through the R_{g_L} path or S_{NV} path. Simultaneously, because the impedance of the path from S_{NV} to D_{NV} is relatively small, most of the current flows through this path.

3) MODE 3 (t_2–t_3)

In this section, the ringing voltage is formed after the body diode conducts. The ringing voltage is generated by V_{Ls} and can be reduced through a large gate resistance. As shown in Figure 13(c), S_{off} and S_{NV} are turned off, and the bidirectional current due to ringing is blocked by the body-diodes of S_{off} and S_{NV} and diodes D_{off} and D_{NV}. Therefore, the ringing current only flows through R_{g_L}. To reduce the ringing voltage, a high resistance should be selected for R_{g_L}. Because the switching time between Modes 2 and 3 is short, D_{NV} must have a fast reverse recovery time.

Using the proposed gate driver circuit, fast turn-off to reduce switching loss is realized in Mode 1, and the negative spike voltage is reduced through a small impedance path in Mode 2. Additionally, the ringing voltage is reduced by the large gate resistance in Mode 3.

V. VERIFICATION OF THE PROPOSED GATE DRIVER CIRCUIT

To verify the effectiveness of the proposed gate driver circuit, a PSpice simulation was performed. First, to apply the characteristics of CSI and the internal capacitances of the device, a simulation model for 3-pin SiC MOSFET was proposed. The proposed gate driver circuit was validated by comparing its performance with that of a conventional circuit.

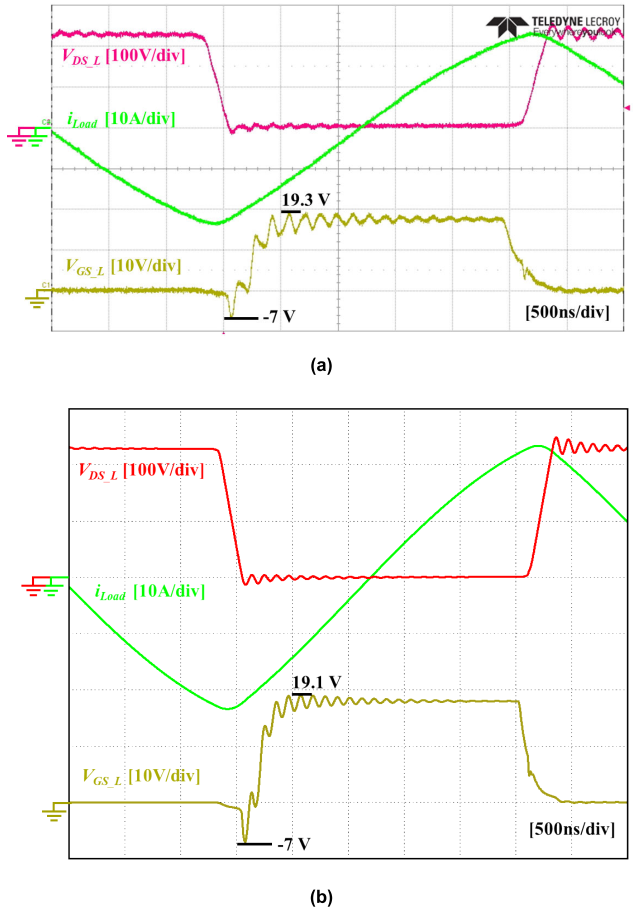


FIGURE 15. **Switch model verification. (a) Experimental waveform. (b) Simulation waveform.**

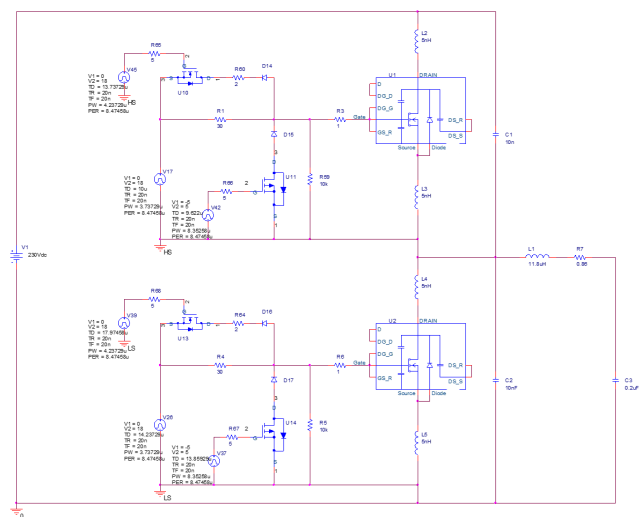


FIGURE 16. **Simulation model with the proposed gate driver circuit.**

A. SIMULATION MODEL OF A 3-PIN SiC MOSFET

Typically, the switch model applies the spice model provided by the manufacturer. However, in the conventional spice model, the voltage of the parasitic components cannot be measured because its properties are already mathematically considered in the spice model. Therefore, we built and applied

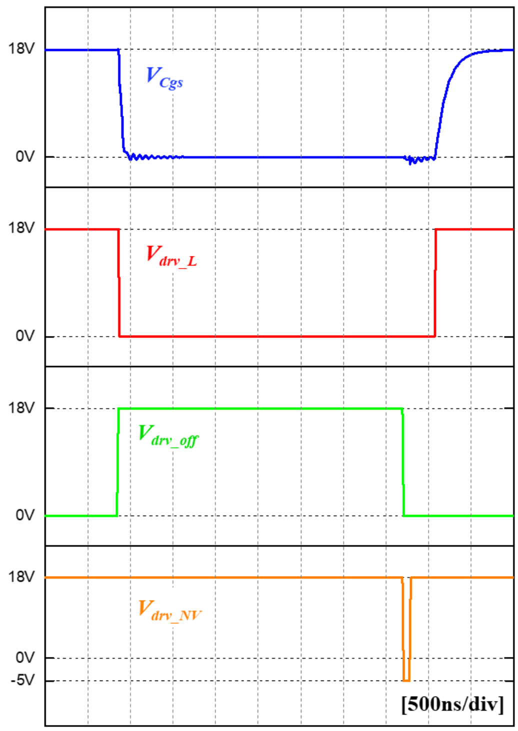


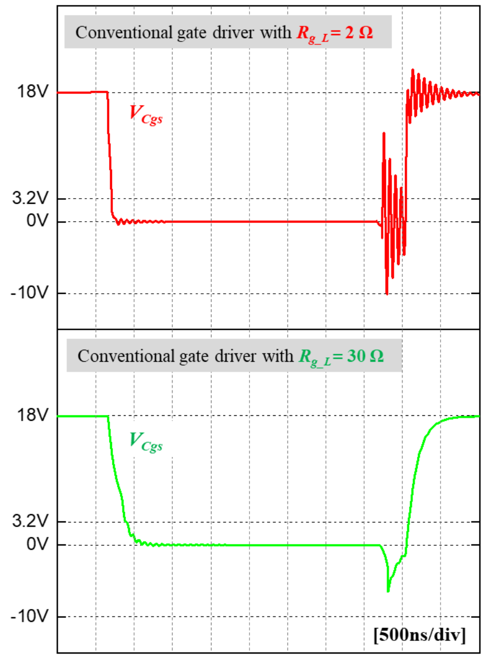
FIGURE 17. Simulation results of the proposed gate driver circuit.

TABLE 2. System parameters.

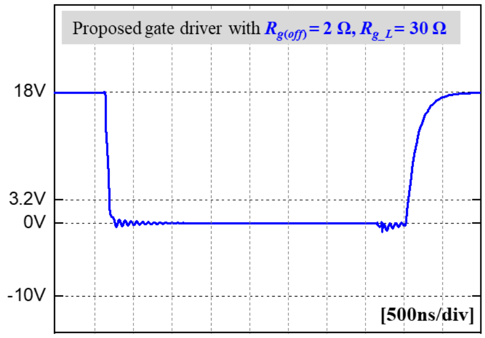
Parameter	Symbol	Value (or Part No.)
Input voltage	V_{DC}	230 V
Snubber capacitance	C_{S_H}, C_{S_L}	10 nF
Switching frequency	f_{sw}	118 kHz
Dead time	t_{dead}	500 ns
Output power	P_{out}	2 kW
Gate resistance	R_{g_L}	30 Ω
Turn-off gate resistance	$R_{g(off)}$	2 Ω
Schottky diode	D_{off}, D_{NV}	RBR3L30BDD
N-channel MOSFET	S_{off}	Si2318CDS
P-channel MOSFET	S_{NV}	Si2319CDS
Common source inductance	L_S	5 nH
Gate driver voltage	V_{drv_L}	18 V / 0 V
Gate voltage of S_{off}	V_{drv_off}	18 V / 0 V
Gate voltage of S_{NV}	V_{drv_NV}	18 V / -5 V

a switch model that can measure the voltage of the parasitic components externally, as shown in Figure 14.

Figure 15 shows the experimental and simulation waveforms of the ZVS circuit. The negative spike voltage of the simulation waveform is −7 V, which is the same as that of the experimental waveform. Additionally, the maximum voltage is 19.1 V, which has only a 1% error compared with the experimental result. Based on this result, the validity of the switch model is verified, and it confirms that the analysis resultant with simulation will be equal to the experiment.



(a)



(b)

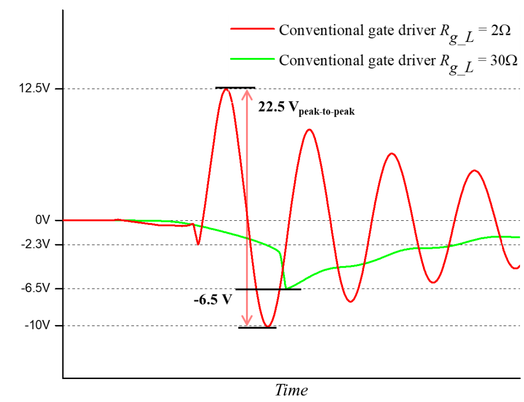
FIGURE 18. Simulation waveform of V_{Cgs} for: (a) conventional gate driver and (b) proposed gate driver.

Figure 16 shows the simulation configuration of the 2 kW half-bridge ZVS circuit to which the proposed gate driver is applied. The detailed system parameters are presented in Table 2. Schottky diodes with fast reverse recovery time are applied at D_{off} and D_{NV}, and switch devices with small $R_{ds(on)}$ are applied to the N-channel MOSFET (S_{off}) and P-channel MOSFET (S_{NV}).

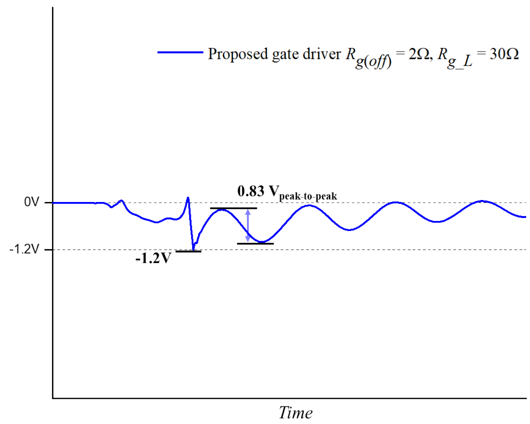
B. SIMULATION RESULTS

The operation waveform from turn-off to turn-on of the proposed gate driver circuit is shown in Figure 17. In the proposed circuit, a designed effective impedance path is provided for each section by V_{drv_off} and V_{drv_NV}.

Figure 18(a) shows the results of the conventional gate driver composed of a single resistor. If the gate resistance is low, the negative spike voltage is reduced, but a considerably high ringing voltage appears. However, if the gate resistance



(a)



(b)

FIGURE 19. Performance verification. (a) Conventional gate driver. (b) Proposed gate driver.

TABLE 3. Performance comparison of gate driver circuits.

Parameter	Conventional with R_{g_L} = 2 Ω	Conventional with R_{g_L} = 30 Ω	Proposed
Negative voltage [V]	−2.3	−6.5	−1.2
Ringing voltage [V_{pp}]	22.5	0.66	0.83

is high, the ringing voltage is reduced, but the negative spike voltage increases. Figure 18(b) shows the result of the proposed gate driver circuit; a small negative spike and ringing voltages are evident. Therefore, it is possible to secure a stable driving voltage range using the proposed circuit.

Figure 19 shows a magnified waveform of the negative spike and ringing voltages in Figure 18. In Figure 19(a), when the gate resistance is low, the negative spike voltage is −2.3 V, and the peak-to-peak of the ringing voltage is 22.5 V. When the gate resistance is high, the negative spike voltage is −6.5 V, and the peak-to-peak of the ringing voltage is 0.66 V. However, in the proposed circuit, the negative spike voltage is −1.2 V, and the peak-to-peak of the ringing voltage is 0.83 V, as shown in Figure 19(b). The performance comparison results are arranged in the Table 3. Consequently, the negative spike voltage is reduced by more than 81%, and the peak-to-peak of the ringing voltage decreases by more than 96% compared with the conventional circuit.

VI. CONCLUSION

In this paper, we proposed a gate driver circuit for reducing the negative spike and ringing voltages of the gate-source in a SiC MOSFET based ZVS circuit. By analyzing the detailed operating principles of the dead-time interval, the relationship between the parasitic components of a 3-pin SiC MOSFET and ZVS circuit parameters was determined.

To realize and analyze the precise operational characteristics of the 3-pin SiC MOSFET, we fabricated a switch model and demonstrated the validity of the model by comparing the simulation and experimental waveforms. The proposed gate driver circuit provided an effective impedance path for the gate loop through two additional active switches, and a stable driving range of the gate-source voltage could be secured. The performance of the proposed circuit was verified through PSpice simulation, and the negative spike voltage reduced by 81% and the ringing voltage by more than 96% compared with the conventional gate driver composed of a single gate resistor.

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