An Ultra-Low-Power 2.4 GHz All-Digital Phase-Locked Loop With Injection-Locked Frequency Multiplier and Continuous Frequency Tracking

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ABSTRACT This paper presents a 0.46 mW and 2.4 GHz; All-Digital Phase-Locked Loop (ADPLL) through an Injection-Locked Frequency Multiplier (ILFM) and Continuous Frequency Tracking Loop (CFTL) circuitry for low power Internet-of-Thing (IoT) applications. In the proposed ADPLL architecture to save power, the need for Time-to-Digital Converter (TDC) is eliminated through providing the CFTL circuitry. This feature makes the design compact, low power, and suitable for IoT applications. The proposed design is based on a synthesizable pulse injection and frequency-locked loop along with an ultra-low-power LC Digitally-Controlled Oscillator (LC-DCO). The presented CFTL circuit adjusts the frequency of the DCO continuously and prevents the frequency drift after the reference injection. Inside the designed LC-DCO core, the power consumption is minimized by optimizing the g_m/I_D and adjusting the power supply to 0.5 V. The proposed ILFM based ADPLL is fabricated in 55 nm CMOS technology and covers the operational frequency range of 2.402 GHz to 2.480 GHz with a reference frequency of 32 MHz. The measured phase noise performance of the ADPLL is -111.15 dBc/Hz at 1 MHz offset frequency from the carrier frequency of 2.4 GHz. It consumes only 0.46 mW power with an active area of 0.129 mm^2.

INDEX TERMS ADPLL, injection locked frequency multiplier, low power, small area, Internet of Things, digitally-controlled oscillator.

I. INTRODUCTION

Nowadays, a frequency synthesizer is a key building block of a Radio Frequency (RF) transceiver, which provides the Local Oscillator (LO) signal to convert up or down the signal to the desired frequency band. With the advancement in

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Complementary-Metal-Oxide-Semiconductor (CMOS) technology, the design of a frequency multiplier based PLL is shifting from analog to digital, for low power and low area target applications [1]. The digital design provides significant advantages in terms of low power and low area [2], [3]. Due to the benefits of the All-Digital Phase-Locked Loop (ADPLL), it becomes an attractive candidate for low power Internet-of-Things (IoT) applications. Traditional ADPLL design utilizes
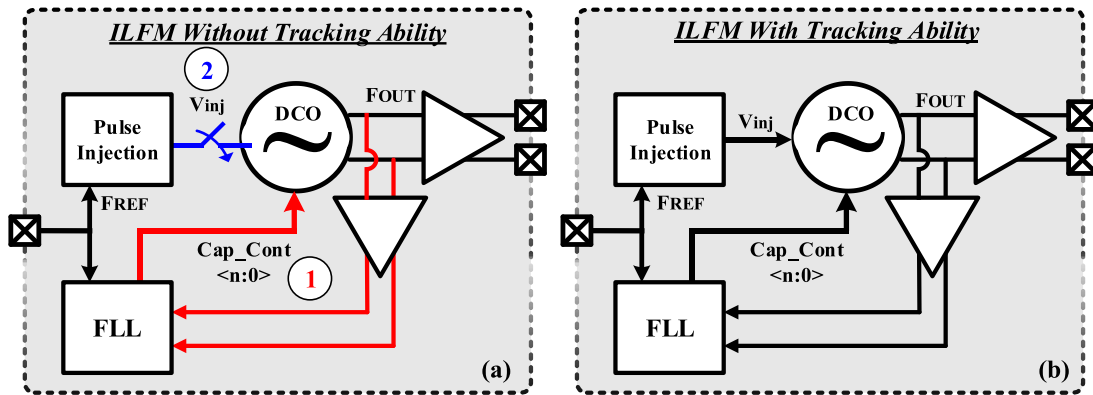
FIGURE 1. Conventional ILFM (a) Injection only (b) injection with frequency tracking.

the Time-to-Digital Converter (TDC) for the phase offset detection [4]–[6]. But due to the high power consumption and complexity of the TDC, it is not suitable for low power design. Recently the Injection-Locked Frequency Multipliers (ILFM) become attractive options for the design of digital PLLs for a low phase noise performance with low power consumption [7]–[9]. As compared to analog sampling PLL, injection locked ADPLL offers less complexity, low cost and less area utilization. Through this technique, a very low jitter integer-N sclock multiplier can be implemented by using a ring oscillator (RO) or an LC Digitally Controlled Oscillator (DCO). The RO offers a wider tuning range with a small area but exhibits poor jitter performance [10]. On the other hand, the LC-oscillator based ILFM offers better phase noise performance and outstanding power efficiency [11]. In [17], [18] an injection locked rotary traveling- wave oscillator (IL-RTWO) is presented which offers low skew clock generation. We can get multiple phases and its provides similar phase noise performance as LC-VCO.

By taking the benefit of the LC-DCO, a low phase noise and power LC-DCO based ILFM is proposed in this paper. It offers low power consumption and better jitter and phase noise performance as compared to the RO based ADPLL or ILFM design.

The error between the oscillator target frequency and the free-running frequency degrades the performance of the ILFM. On the other hand, the work proposed in [12] does only foreground frequency adjustment. After the injection by the reference clock, the frequency of the oscillator drifts due to PVT variations. This frequency drift would not be detected by the frequency-locked loop, and the structure can suffer from large reference spurs. Besides, without continuous frequency tracking ability the ILFM does not offer excellent jitter performance. To keep the oscillator at the target frequency, a frequency tracking loop is required. To overcome this problem the works [4]–[16] propose different techniques to keep the frequency error as low as possible. Although it gives better jitter performance but at the cost of high power consumption and design complexity. Figure 1 demonstrates the two approaches, with and without frequency tracking in

the implementation of the ILFM. In Fig. 1(a), a frequency lock loop (FLL) is used to bring the oscillator frequency near to the target frequency. After that, the FLL is disabled and reference frequency (F_{REF}) is injected directly to the oscillator. In Fig. 1 (b), an FLL is running continuously in the background to keep the DCO at the target frequency against PVT variations.

When the frequency tuning of the DCO through the FLL finished, the pulse injection circuit aligns the output phase of the DCO with F_{REF} and resets the phase error between two clocks. The effect of the reference frequency injection on the DCO output F_{OUT} is shown in Fig. 2. The relationship of injection pulse width and phase noise performance is analyzed in [14]. Higher harmonic power at frequency $2N \cdot f_{REF}$ results in improved phase noise performace of injection-locked oscillator. Asume injection pulse has width D and amplitude V_0 then the Fourier series of $2N$th harmonic power at frequency of $2N \cdot f_{REF}$ is given as

$$p(t) = a_0 V_0 + \sum_{n=1}^{\infty} a_n . V_0 . cos(2\pi . f_{REF} . n . t) \qquad (1)$$

where $a_0 = f_{REF} . D$ and $a_n = \frac{2}{n\pi} . sin(2\pi) . f_{REF} . n . \frac{D}{2}$.

Fig. 3 compares the phase noise performance for free running DCO, ILFM with the only injection, and ILFM with injection and frequency tracking ability. In this paper, an ILFM based ADPLL design is proposed, that offers low complexity and low power consumption. The reference injection controller and FLL controller are designed using HDL, which is fully synthesizable. The major contributions of this paper are as follows:

- Design of low power ILFM based ADPLL, which makes it suitable for low power and low-cost IoT applications.
- Design of FLL and injection controller are fully synthesizable which offers low area and design portability.
- Design of low phase noise and low power LC-DCO that makes the whole design low power and suitable for the required specifications.

The rest of the paper is structured as follows: In section 2, the proposed architecture of the ILFM based ADPLL is
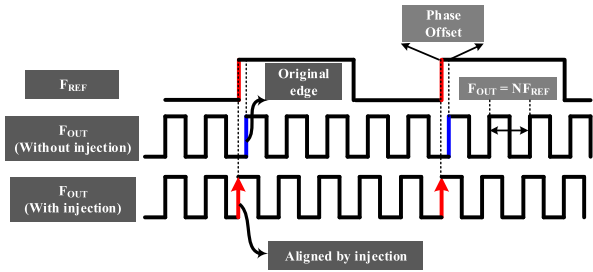
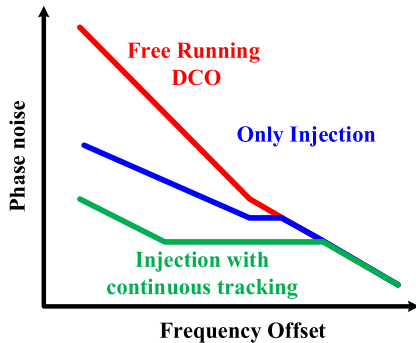**FIGURE 2.** Phase adjustment after injection of the reference frequency.

FIGURE 3. Phase noise trend for RI-based ADPLL when Injection without CFTL and injection with CFTL.
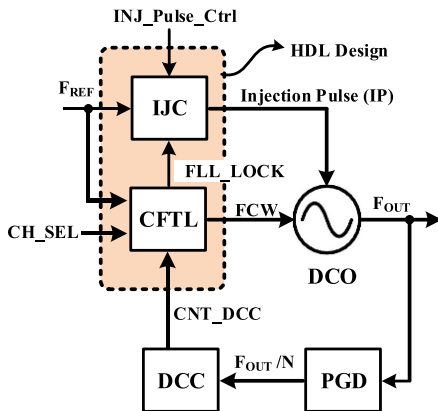

FIGURE 4. Block diagram of the ILFM based ADPLL.

FIGURE 5. Block diagram of the injection controller.

FIGURE 6. Block diagram of CFTL.

discussed. Experimental results are discussed in section 3. Lastly, the paper is concluded in section 4.

II. PROPOSED ILFM BASED ADPLL ARCHITECTURE

The block diagram of the proposed architecture of the ILFM based ADPLL is shown in Fig. 4. It consists of Injection Controller (IJC), Continuous Frequency Tracking Loop (CFTL), DCO, Programmable Divider (PGD), and DCO Clock Counter (DCC). The task of the CFTL is to bring the DCO output frequency F_{OUT} to the target center frequency which can be selected by the CH_SEL. The CFTL is operating at the reference frequency of F_{REF}. The Frequency Control Word (FCW) is provided to the DCO by the CFTL to increase or decrease the frequency of the DCO output (F_{OUT}).
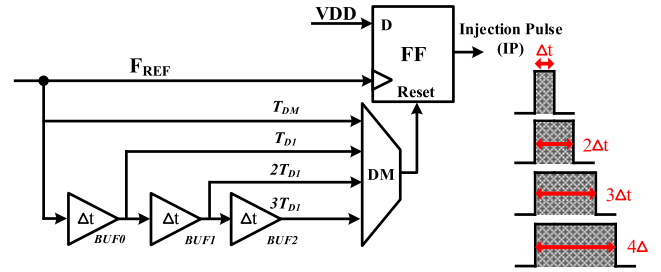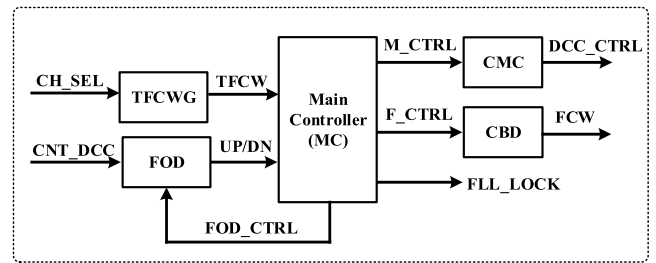
The F_{OUT} is divided by the PGD and the output of the PGD is fed to the DCC. The output of the DCC is used by the CFTL and it is compared with the target value depending on the channel frequency. The CFTL increase or decrease the output frequency of DCO by adjusting the FCW. Once the CFTL brings the DCO frequency to the target frequency, it sets the FLL_LOCK signal to high and enables the IJC. The IJC adjusts the phase of the DCO by periodically injecting the reference frequency pulse to the DCO. The pulse width of the injection pulse is controlled by the INJ_Pulse_Ctrl, and different injection pulse widths would be made through this block. Narrow pulse width for the injection process is essential for reduction in distortion caused by pulse injection. However lock failure can occur due to excessively narrow pulse width or strong distortion can occur due to wide pulse width. Fig. 5 shows the block diagram of the IJC. It mainly consists of the Flip-Flop (FF), Delay Multiplexer (DM), and buffer delay line. It is designed through HDL to make it fully synthesizable. The data input of the FF is set to high, and it is clocked by F_{REF}. The F_{REF} propagates through the delay line.

The output of each delay cell is connected to the DM input. By controlling the INJ_Pulse_Ctrl, we can get the delayed version of F_{REF} at the output of the DM. The output of DM is used to reset the FF to control the injection pulse width. The timing diagram of the operation of the IJC is shown in Fig. 5. The purpose of the CFTL is to bring the free-running DCO output frequency to the target channel frequency. It uses a binary searching algorithm to bring the DCO frequency to the target frequency. Let's suppose we have 40 channels which can be specified through k where k = 0, 1, 2 ... 39. To select a channel among 40 channels, the FLL generates the frequency
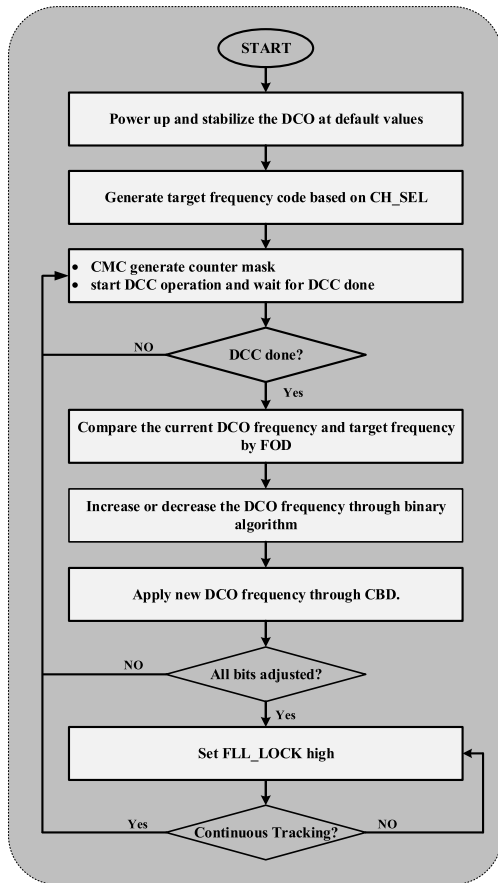
FIGURE 7. Flow diagram of CFTL.

FIGURE 8. Simplified architecture of DCO.

control word (FCW) for the DCO by the following equation.

$$N_{FCW}(k) = k + N_{CH0}(\frac{M}{D} \times 10^{-6}) \qquad (2)$$

where the $N_{FCW}(k)$ is the required FCW as a function of k, N_{CH0} is the base frequency of the channel 0, M is the frequency multiplier for the DCO and DCO frequency division factor is given by D.

The block diagram of the CFTL is shown in the Fig. 6. The main blocks of the CFTL consist of the Main Controller (MC), Counter Mask Control (CMC), Target Frequency Control Word Generator (TFCWG), Frequency Offset Detector (FOD), and Capacitor Bank Decoder (CBD). The CFTL is fully synthesizable and designed by HDL coding. The MC is controlling the overall operation of the CFTL.

The DCC will count the DCO clock cycles within the counter mask duration generated by CMC. The TFCWG generates the target frequency control word (TFCW) which is provided to the MC. The FOD compares the current DCO frequency with the target DCO frequency. It generates the control signals for the MC to increase or decrease the DCO frequency. To achieve the target frequency, the CBD controls the capacitor banks in the DCO and increases or decreases the DCO frequency. The CBD generates a corresponding thermometer code to control the capacitor's bank in the DCO.
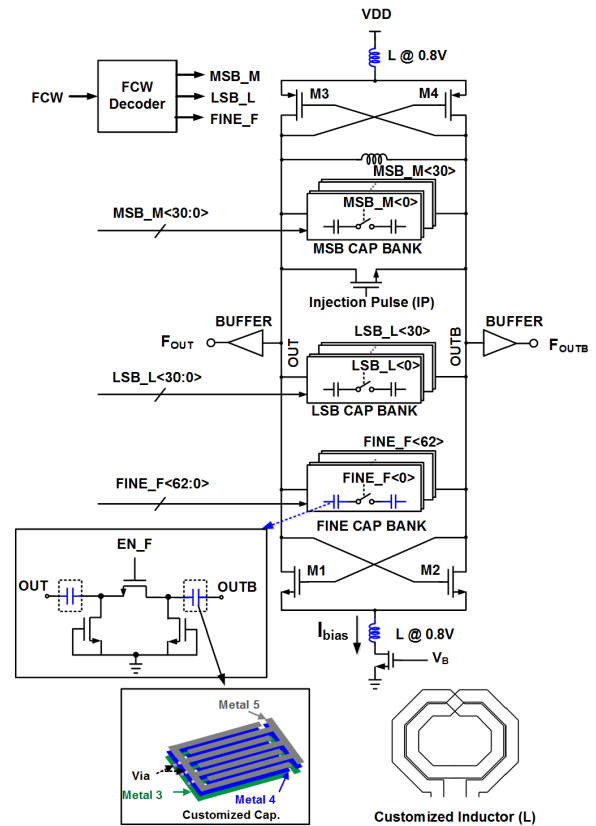
The flow diagram indicating the operation of the CFTL is shown in Fig. 7. When the CFTL is powered up, then it is initialized with the default setting of the DCO and waits till DCO output frequency is stable. Then the TFCW generates the Target_F code based on the CH_SEL. The MC provides mask control (M_CTRL) signal to the CMC to generate the counter mask. The DCC starts counting the number of cycles based on the counter mask provided by DCC_CTRL. The MC waits till DCC complete its operation. After the completion, the MC activates the FOD to compare the DCO current frequency (CNT_DCC) and the target frequency.

The FOD generates the UP/DN control signals accordingly to increase or decrease the F_{OUT}. The MN adjust the DCO frequency through a binary algorithm. The binary algorithm adjusts bits of the capacitor banks from MSB to LSB to achieve target DCO frequency. After adjusting all control bits of DCO, the MN generates the FLL LOCK signal and the DCO output frequency is set at the target frequency. In the case of continuous tracking, the CFTL again calculates the DCO current frequency and compensates any PVT variations. Reference frequency is used as 32 MHz with 50% duty cycle. Duty cycle of reference frequency significantly affects the operation of the ADPLL. It can result in incorrect calculation of output frequency of ADPLL and cause strong distortion at the output of ADPLL.
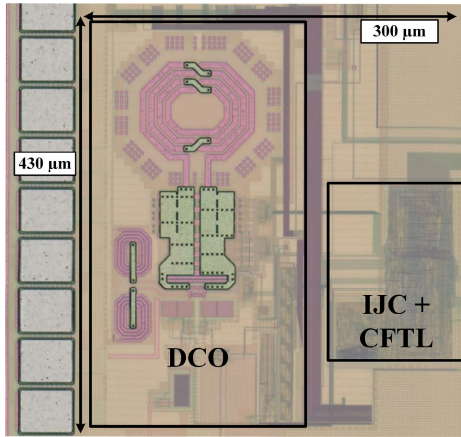
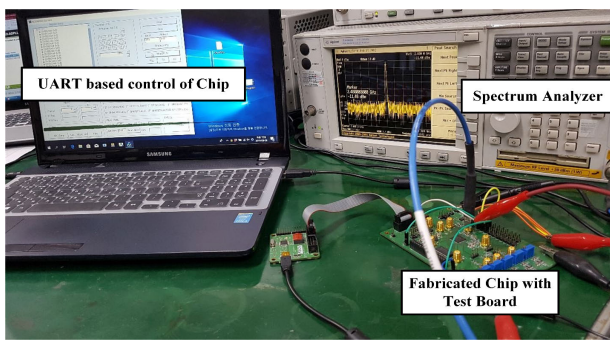**FIGURE 9.** Chip photograph of the proposed ILFM based ADPLL.

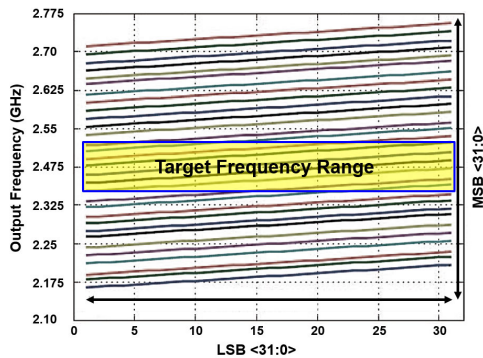**FIGURE 10.** Chip measurement setup.

FIGURE 11. Tuning curve of DCO versus tuning codes to cap banks MSB and LSB.

The DCO is designed by focusing on the ultra-low power consumption for IoT applications. The target frequency range of the DCO is from 2.402 GHz to 2.480 GHz. The DCO is designed by MOSFET switches and their sizes are adjusted to provide almost ideal characteristics. During the design, considering the Process, Voltage, and Temperature (PVT) variations, the frequency range of the DCO is optimized to use the maximum inductance value for the resonance. Besides, it offers high swing characteristics and omits the need for increasing current to achieve sufficient swing.

The proposed DCO operates in the sub-threshold region and satisfies the oscillation condition of equation (3) as represented in [13].

$$g_m \geq 1/R_p \tag{3}$$

where g_m and R_p are the transconductance of the cross-coupled pair and equivalent parallel resistance of the tank, respectively. The high-frequency resolution is achieved through the fine-tuning bank. The small capacitance is achieved through customized lateral MOM capacitors. This provides low capacitance values of 16.22 aF. An ultra-wide Aluminum (Al) metal layer is used as a superconductor to eliminate routing metal parasitic inductance. The simplified DCO schematic is shown in Fig. 8. Three capacitor banks configurations (MSB CAP BANK, LSB CAP BANK, and FINE CAP BANK) are shown which are controlled by the decoding FCW. A low supply voltage (VDD) of 0.5 V is used for the DCO, which reduces the total power consumption of the DCO circuit efficiently. Each MSB CAP Bank and LSB CAP bank consists of 32 capacitors units. While the FINE CAP bank consists of 64 unit capacitors. The 1-bit resolution of the MSB CAP BANK, LSB CAP BANK, and FINE CAP BANK is 18.7 MHz, 72 kHz, and 4.8 kHz, respectively

III. EXPERIMENTAL RESULTS
The chip is fabricated using 55 nm CMOS technology. Fig. 9 shows the microphotograph of the proposed chip. The active area of the proposed ILFM is 0.129 mm^2. The active size of DCO is 0.1175 mm^2 which mainly because of the inductor. The area of IJC and CFTL is significantly smaller than the DCO. The measurement environment of the proposed ILFM is shown in Fig. 10. It consists of a fabricated chip with the test board, spectrum analyzer, power supply, and UART based control of chip The tuning curves for the DCO versus tuning codes to capacitor banks MSB and LSB are shown in Fig. 11. As we increase the tuning codes for the MSB capacitor bank, the output frequency of DCO is changing with a large frequency offset which is around 18 MHz. Due to PVT variation, the step size for the output frequency of DCO is not equal to the lower tuning range but in target frequency range the output frequency of DCO shows linear step size. The change in LSB tuning codes for the DCO shows almost linear behaviors and it has fewer effects of PVT variation at the DCO output frequency. Phase noise is measured by using divider output which divides the DCO output frequency by a factor of 4. The phase noise performance of the ILFM based ADPLL is about -111.15 dBc/Hz at 1 MHz offset from the carrier frequency of 2.4 GHz. The operation of the FLL is shown in Fig. 12. The DCC generates a counter mask for counting the number of cycles of DCO output. At the start, the difference in the target frequency and DCO output frequency is large so a small counter mask is generated. When the output frequency of DCO is getting closer to the target frequency, CMC adaptively increases the duration of mask for the better accuracy of the target frequency. When the target frequency is achieved at the DCO output, the FLL_LOCK signal is set high. When the
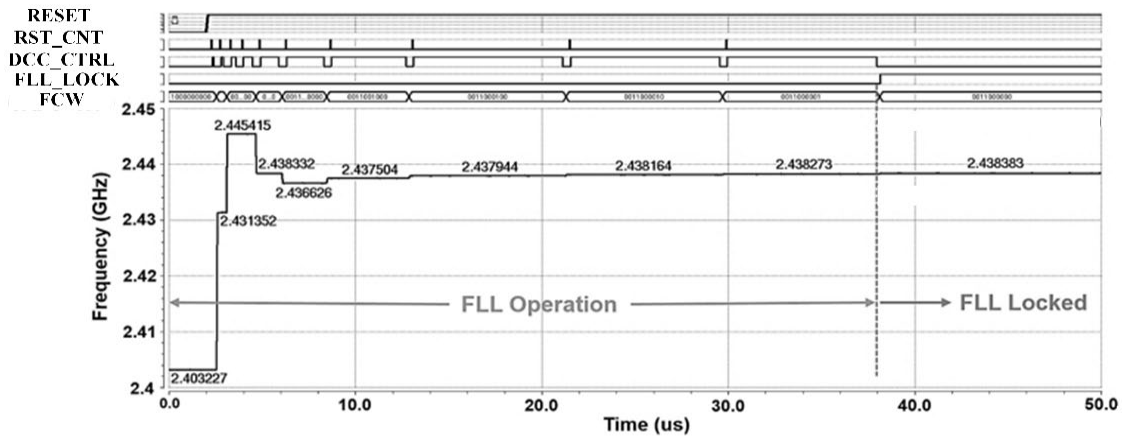
FIGURE 12. The frequency-locked loop operation.

TABLE 1. Performance comparison.

	[14]	[15]	[16]	[10]	[7]	This work
Technology (nm)	40	55	65	65	65	55
Architecture	PLL	PLL	PLL	PLL	PLL	PLL
Output Frequency Range (GHz)	0.4-1.6	0.216	0.52-1.15	2.5-5.75	2.5-5.63	2.402-2.480
Reference Frequency (MHz)	50	27	150	125	156.25	32
Integrated RMS jitter (ps)	2.29	2.4	0.42	0.34	0.168	1.652
Phase noise dBc @1MHz	-106	-122	-119	-115	-105	-110.78
Spur Level dBc	-44	-70	NA	-45	-42	-51.2
Power (mW)	1.49	6.9	3.8	5.3	15.4	0.46
Area (mm^2)	0.14	0.03	0.028	0.09	0.06	0.129
FOM	-231.1	-224	-241.3	-242.1	-243.6	-245.3
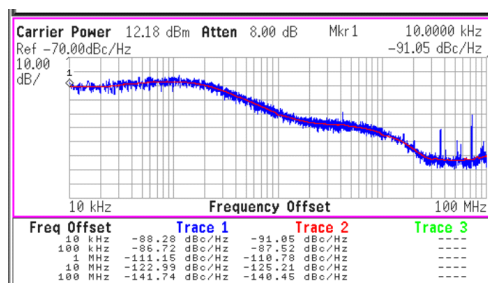
FIGURE 13. Phase noise plot of ILFM based ADPLL at 2.4 GHz.
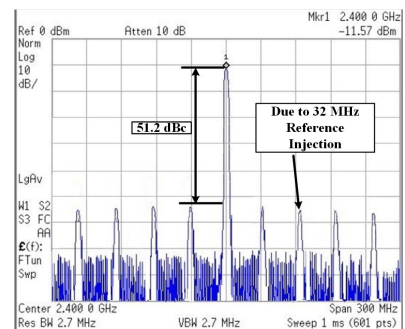
FIGURE 14. The Spectrum of the output of ILFM based ADPLL after injection of 32 MHz reference.

counter mask is generated through DCC_CTRL, the counter is reset through the RST_CNT signal. The phase noise of ILFM based ADPLL is shown in Fig. 13. The output frequency is 2.4 GHz for the measurement of DCO phase noise. The phase noise at offset of 10 kHz, 100 kHz, 1 MHz,

10 MHz and 100 MHz are −88.28 dBc/Hz, −86.72 dBc/Hz, −111.15 dBc/Hz, −122.99 dBc/Hz, and −141.74 dBc/Hz respectively. The Spectrum of the output of ILFM based

ADPLL after injection of 32 MHz reference are shown in Fig. 14. Table 1 shows the comparison of the proposed design with the previous architectures. The integrated rms jitter of proposed design is 1.652ps. Other works such as [16], [10] and [7] shows better integrated rms jitter performance but at the cost of additional hardware which results in design complexity and higher power consumption.

The figure of merit (FoM) to evaluate the performance of the design based on the measured integrated jitter and the power consumption is given by equation (4).

$$FOM = 10log_{10}\left[\left(\frac{\sigma_t}{1s}\right)\left(\frac{P_{DC}}{1mW}\right)\right] \quad (4)$$

where σt is integrated jitter, P_{DC} is the power consumption of the design, and 1s indicates the one second time reference. Table 1 indicates that FOM of proposed design shows better performance than previous works. It is mainly due to less power consumption as compared to previous designs.

IV. CONCLUSION

An ILFM based ADPLL was proposed for low power IoT sensor applications. The ILFM based ADPLL eliminates the requirement of TDC which makes the design simple and reduces the power consumption. The operating frequency range of the ILFM based ADPLL is from 2.402 to 2.480 GHz. The power consumption of the whole architecture is minimized using all-digital implementation and design of an ultra low power LC-DCO. It consumes only 0.46 mW with an area of 0.129 mm^2. The phase noise is -111.15 dBc/Hz at 1 MHz offset from the carrier frequency of 2.4 GHz.

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