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# A Bidirectional Isolated Integrated AC–DC Converter Based on an Interleaved 3-Level T-Type Power Converters

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**ABSTRACT** This paper presents an integrated single-phase bidirectional ac–dc converter based on a dual-active-bridge (DAB) topology. The primary side is based on a multi-state switching cell (MSSC) with a T-type (TNPC) cell, which is composed of two three-level interleaved legs and coupled inductor, while the secondary side is a single-phase full-bridge (FB). Moreover, a comparative analysis between an isolated ac–dc converter with a neutral point clamped (NPC) converter on the primary side is presented. The basic converter operating principles and experimental results of a 850 W prototype are presented in order to validate the theoretical analysis. The control strategy is implemented on the TMS320F28379D DSP. The proposed topology achieves a maximum efficiency of 91.40% at 300 W output power, and 89.40% at rated power. From the experimental results, it can be stated that the converter based on the T-type topology is more efficient than the structure based on the NPC.

**INDEX TERMS** Coupled inductor, high-frequency isolation, multilevel converter, phase-shift control, single-stage converter.

## I. INTRODUCTION

In the last decades, the concern over the emission of greenhouse gases has prompted the automotive industry to look for alternatives to replace fossil fuel-powered engines for the ones powered by alternative energy sources [1], [2]. Thereby, as found in the literature, bidirectional, single-phase, and isolated topologies for battery chargers applied in electric vehicles have gained prominence. Then, a categorization of such converters should be adopted in order to organize their characteristics. For this study, it is adopted the categorization by the number of energy conversion stages, resulting in two families: dual-stage and single-stage [3].

For instance, Fig. 1 shows the generalized structure for a single-stage converter. This kind of converters are attractive due to their bidirectional power flow and power factor correction (PFC), besides a higher power density can be archived when compared to the dual-stage ones, as well the possibility of higher efficiency due to the fewer number of active semiconductors and soft-switching regions operation, [4]–[6]. For these last ones, a resonant filter is usually inserted into the high-frequency isolation link, [7], [8]. Moreover, soft-switching operation also allows an increment of switching frequency, resulting in weight and volume reduction of magnetic elements, however leading to losses increment on semiconductors. Then, an optimal configuration among soft-switching operation, switching frequency, and power density should be considered for those topologies.

There is another kind of categorization, originally discussed in [9], known as integrated-stage structures, and can also be addressed with single-stage topologies. These structures employ interleaved multilevel converters with coupled inductor on the primary side, and also contain a dc-link that is not used as an intermediate energy store for power

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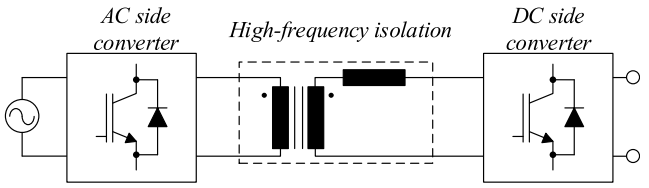


**FIGURE 1. Single-stage single-phase bidirectional isolated ac–dc converter typical configuration.**

transfer [10], [11], as usually happens on dual-stage converters. Thus, multilevel converters have been an alternative quite interesting to high power and medium voltage industrial applications in the last decades [12].

Moreover, the use of the interleaving technique with coupled inductor provides good distribution of semiconductor losses, since its current is half of the input current, and can also reduces weight, and volume of magnetic components when compared to the configuration with interleaved legs and uncoupled inductor [13].

In particular, the three-level multilevel neutral point clamped (NPC) inverter has received more attention in power electronics field due to its advantages. When compared to the two-level inverter, three-level NPC one has some advantages, such as lower total harmonic distortion (THD) of the output voltage, reduction of the blocking voltage on semiconductors, reduced losses on switches, and higher efficiency [14].

The three well-known types of neutral point clamped are: conventional NPC [15], [16], active NPC (ANPC) [17] and NPC T-type (TNPC) [18]. The TNPC shows improvements over the NPC and ANPC, such as reduced conduction losses, fewer switches, volume reduction, and simpler operation. Indeed, recent works have shown interest in the study of the five-level TNPC single-phase inverter [19], [20], due to the aforementioned characteristics.

In this sense, since the T-type presented high performance [21], [22], and also assuming that it behaves better than NPC [23], a power converter using the T-type configuration providing bidirectional power flow in an ac–dc integrated stage is proposed, experimentally investigated, and compared with the structure based on the NPC configuration [24].

Thus, this paper mainly focuses on presenting the proof of concept of the proposed converter through the following organization: operation principle, design considerations and losses analysis are presented in Section II, while the mathematical model and control scheme are described in Section III and IV, respectively. Experimental results are shown in order to validate the proposed structure, as the comparative power analysis of both topologies (T-type based and NPC one based) are presented in section V. Finally, the conclusion is presented in Section VI.

## II. TOPOLOGY AND OPERATION PRINCIPLE

### A. CONVERTER STRUCTURE

The proposed structure is shown in Fig. 2a, consisting in a T-type converter associated with coupled inductor (CI) on the primary side (ac side) and a full-bridge on the secondary side (dc side), with a high-frequency transformer providing galvanic isolation. In this figure, $L_f$ is the input filter inductor, $L_a$ and $L_b$ are the self-inductances of CI, $L_s$ is the power transfer inductor, and $\phi$ is the phase-shift angle responsible for the power flow operation modes. The proposed topology is called I2TDF1: I (interleaved), 2 (dual), T (T-type), D (dual-active-bridge), F (full-bridge), 1 (single-phase), whereas the topology based on the NPC converter, proposed in [24], is called I2NDF1, where 'N' stands for NPC in the adopted acronym, and is presented in Fig. 2b.

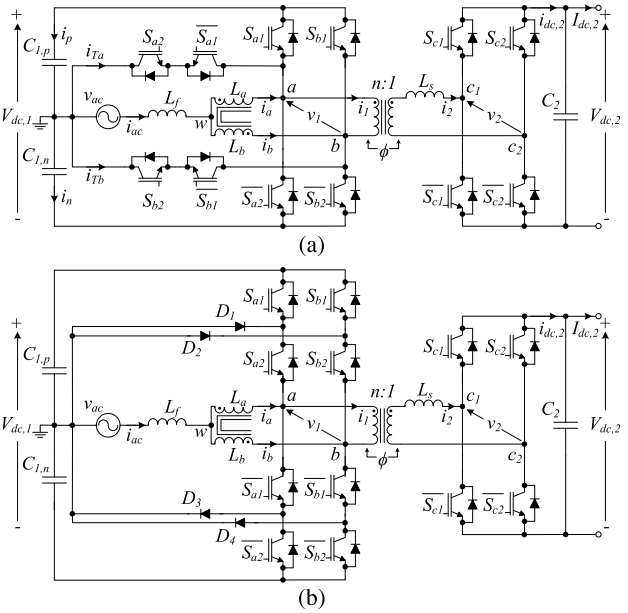


**FIGURE 2. Integrated stage single-phase bidirectional isolated ac–dc converter. (a) I2TDF1. (b) I2NDF1.**

It can immediately be observed that the advantage of the T-type converter over the NPC one is the suppression of the diodes D1 to D4, should implies a reduction of conduction losses, and simpler implementation.

Furthermore, the modulation, the model, and the control requirement are the same for both converters, as evidenced in the following sections.

### B. OPERATION PRINCIPLE

Both converters use level-shifted pulse width modulation (LSPWM) with carriers in-phase disposition (IPD) on the primary side, as indicated in Fig. 3. Carriers $cr_{a1}$ and $cr_{a2}$ are level displaced, but are in phase, while carriers $cr_{b1}$ and $cr_{b2}$ are shifted by 180 degrees from carriers $cr_{a1}$ and $cr_{a2}$, respectively. It is adopted the phase-shifted pulse width modulation (PSPWM) on the secondary side, where the carriers $cr_{c1}$ and $cr_{c2}$ are shifted by 180 degrees among each other. Thus, the behavior of complementary switches ($S_{xy}$, $\overline{S}_{xy}$) is determined by comparing the modulating signal $v_{mz}$ with carrier $cr_{xy}$, so the switching function $s_{xy}$

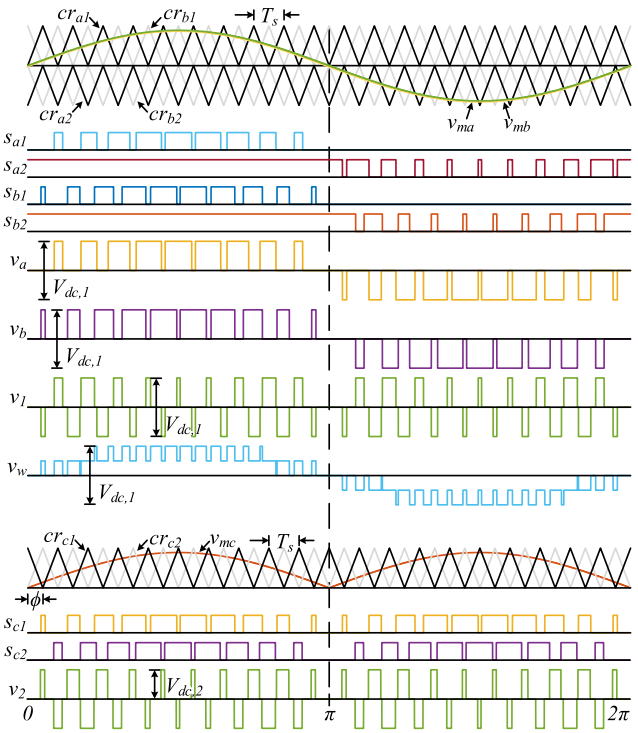


**FIGURE 3.** Waveforms of the proposed converter.

can assume two possible states:

$$s_{xy} = \begin{cases} 1 & \text{if } v_{mx} \geq cr_{xy} \\ 0 & \text{if } v_{mx} < cr_{xy} \end{cases} \tag{1}$$

where $x \in \{(a, b)$ legs on ac side, $(c)$ full-bridge on dc side$\}$, and $y \in \{1, 2\}$. For the applied modulation, there are seven possible combinations of switching states on the primary side, and four ones on the secondary side, as listed in Tables 1 and 2, respectively.

**TABLE 1.** Switching state and voltage level on the ac side.

| Switching State | | | | Voltage Level | | | |
|---|---|---|---|---|---|---|---|
| $S_{a1}$ | $S_{b1}$ | $S_{a2}$ | $S_{b2}$ | $v_a$ | $v_b$ | $v_w$ | $v_1$ |
| 1 | 1 | 1 | 1 | $V_{dc,1}/2$ | $V_{dc,1}/2$ | $V_{dc,1}/2$ | 0 |
| 1 | 0 | 1 | 1 | $V_{dc,1}/2$ | 0 | $V_{dc,1}/4$ | $V_{dc,1}/2$ |
| 0 | 1 | 1 | 1 | 0 | $V_{dc,1}/2$ | $V_{dc,1}/4$ | $-V_{dc,1}/2$ |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | $-V_{dc,1}/2$ | $-V_{dc,1}/4$ | $V_{dc,1}/2$ |
| 0 | 0 | 0 | 1 | $-V_{dc,1}/2$ | 0 | $-V_{dc,1}/4$ | $-V_{dc,1}/2$ |
| 0 | 0 | 0 | 0 | $-V_{dc,1}/2$ | $-V_{dc,1}/2$ | $-V_{dc,1}/2$ | 0 |

For ideal conditions, the voltages across capacitors $C_{1,p}$, and $C_{1,n}$ is $V_{dc,1}/2$. Thus, the multilevel and transformer primary voltage can be expressed, respectively, as follows:

$$v_w = \frac{V_{dc,1}}{4}(s_{a1} + s_{a2} + s_{b1} + s_{b2} - 2) \tag{2}$$

$$v_1 = \frac{V_{dc,1}}{2}(s_{a1} + s_{a2} - s_{b1} - s_{b2}) \tag{3}$$

**TABLE 2.** Switching state and voltage level on the dc side.

| Switching State | | Voltage Level | | |
|---|---|---|---|---|
| $S_{c1}$ | $S_{c2}$ | $v_{c1}$ | $v_{c2}$ | $v_2$ |
| 1 | 1 | $V_{dc,2}$ | $V_{dc,2}$ | 0 |
| 1 | 0 | $V_{dc,2}$ | 0 | $V_{dc,2}$ |
| 0 | 1 | 0 | $V_{dc,2}$ | $-V_{dc,2}$ |
| 0 | 0 | 0 | 0 | 0 |

The voltage on the primary side of the transformer can also be expressed as:

$$v_1 = v_a - v_b \tag{4}$$

where:

$$v_a = \frac{V_{dc,1}}{2}(s_{a1} + s_{a2} - 1) \tag{5}$$

$$v_b = \frac{V_{dc,1}}{2}(s_{b1} + s_{b2} - 1) \tag{6}$$

If $v_{ma} \leq 1$ and $v_{mb} \leq 1$, the amplitudes of the fundamental frequency voltages $v_a$ and $v_b$ are linearly proportional to $v_{ma}$ and $v_{mb}$, respectively. Then:

$$v_a = v_{ma}\frac{V_{dc,1}}{2} = (m + m_o)\frac{V_{dc,1}}{2} \tag{7}$$

$$v_b = v_{mb}\frac{V_{dc,1}}{2} = (m - m_o)\frac{V_{dc,1}}{2} \tag{8}$$

where $m$ is the ac fundamental modulation signal, and $m_o$ is the offset to maintain the dc bias current [25], which in this work is supposed to be null.

Similarly, on the dc side, the voltage across capacitor $C_2$ is $V_{dc,2}$, also under ideal conditions. Thus the transformer secondary voltage is expressed as:

$$v_2 = V_{dc,2}(s_{c1} - s_{c2}) = v_{mc}V_{dc,2} \tag{9}$$

where $v_{mc}$ is the absolute value of $m$.

The input current is obtained by summing the currents flowing through the inductances of windings $L_a$ and $L_b$, which is given by:

$$i_{ac} = i_a + i_b \tag{10}$$

Therefore, the frequency of the filter inductor current $f_{ap}$ is double of the switching frequency $f_s$.

The circulating current is defined as:

$$i_{cir} = i_a - i_b \tag{11}$$

Its average value per frequency cycle has to be zero and its variation has to be low to avoid magnetic saturation and size and volume reduction of the CI [26].

Then, after established the basic equations for the proposed converter, it is possible to address its theoretical model, as presented in the following section.

### C. DESIGN CONSIDERATIONS

#### 1) INPUT FILTER INDUCTOR

According to [26], the input filter inductance is given by:

$$L_f \geq \frac{V_{dc,1}}{32 f_s \Delta I_{L_f}} \tag{12}$$

where $\Delta I_{L_f}$ is the current ripple through the inductor $L_f$.

#### 2) POWER TRANSFER INDUCTOR

Fig. 4 presents the effective duty ratio of the high-frequency link primary side voltage $v_1$, whose analytical description is given by:

$$\delta(t) = \begin{cases} \pi\,|d(t)| & \text{if } |d(t)| \leq 0.5 \\ \pi(1 - |d(t)|) & \text{if } |d(t)| > 0.5 \end{cases} \tag{13}$$

where $d(t) = m_a \sin(\omega_o t)$, $\omega_o$ is the grid angular frequency, and $m_a$ is it the modulation index.

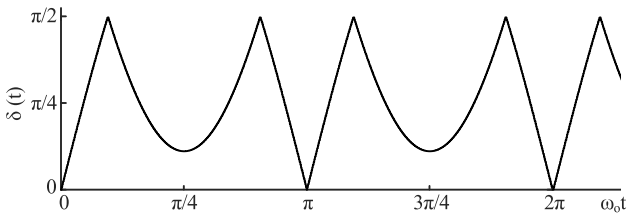


**FIGURE 4.** Effective duty ratio associated to voltage $v_1$.

The power transfer inductor, obtained by the active power fundamental model at switching frequency, can be calculated as:

$$L_s \cong \frac{V_{dc,1} V_{dc,2} \sin(\phi)}{n\pi^4 f_s P_o} \int_0^{2\pi} \sin^2(\delta(\omega_o t))\, d(\omega_o t) \tag{14}$$

where $n$ is the transformer turns ratio, and $P_o$ is the rated power [27]. Note that there is no closed-form solution for $L_s$, and a numerical method is required.

#### 3) COUPLED INDUCTOR AND TRANSFORMER

The coupled inductor and the high-frequency transformer are obtained taking into account the maximum voltage, the rms current, and the switching frequency on these elements, using the criteria established in [28].

#### 4) FILTER CAPACITORS

The capacitance design is performed considering their accumulated energy [29]. The capacitances of the primary and secondary buses are determined, respectively, as:

$$C_{1,p} = C_{1,n} \geq \frac{P_o}{2 f_o V_{dc,1} \Delta V_{dc,1}} \tag{15}$$

$$C_2 \geq \frac{P_o}{8 f_o V_{dc,2} \Delta V_{dc,2}} \tag{16}$$

#### 5) DESIGN PROCEDURES

The design specifications of the I2TDF1 are listed in Table 3, and using the presented considerations, the components used in the implementation of the experimental prototype are listed in Table 4.

**TABLE 3.** System parameters and specifications.

| Description | Label | Value |
|---|---|---|
| Rated power | $P_o$ | 850 W |
| Input voltage (rms) | $V_{ac}$ | 127 V |
| Input current ripple | $\Delta I_{L_f}$ | 0.5 A |
| Grid frequency | $f_o$ | 60 Hz |
| Switching frequency | $f_s$ | 21 kHz |
| Primary bus voltage | $V_{dc,1}$ | 404 V |
| Primary bus voltage ripple | $\Delta V_{dc,1}$ | 12 V |
| Secondary bus voltage (output) | $V_{dc,2}$ | 220 V |
| Output voltage ripple | $\Delta V_{dc,2}$ | 6 V |
| Phase-shift | $\phi$ | 30° |

**TABLE 4.** Power stage elements.

| Description | Specification |
|---|---|
| Load Resistance (output) | $R_o = 56.94\ \Omega$ |
| DC bus capacitance | $C_{1,p}, C_{1,n}, C_2 =$ 3 x 470 $\mu$F/ 450 V (EPCOS) in parallel |
| Filter inductor | Core MMT034T7725 (Magmattec)<br>$N = 160$ turns / Wire: 9 x 22AWG<br>$L_f = 1.1$ mH |
| Coupled inductor | Core MMT140T5020 (Magmattec)<br>$N_p = N_s = 72$ turns / Wire: 4 x 22AWG<br>Self-inductance $L(L_a, L_b)$ = 30.006 mH<br>Leakage-inductance $L_k$ = 6 $\mu$H<br>Mutual-inductance $M$ = 30 mH |
| Transformer | Core MMT140T5020 (Magmattec)<br>$N_p = 49$ turns / Wire: 9 x 22AWG<br>$N_s = 54$ turns / Wire: 8 x 22AWG<br>Transformer turns ratio $n$ = 49/54 |
| Power transfer inductor | Core MMT002T7713 (Magmattec)<br>$N = 89$ turns / Wire: 8 x 22AWG<br>$L_s = 85\ \mu$H |

### D. LOSSES ANALYSIS

The calculated losses of the I2TDF1 and I2NDF1 converters with rated power are shown in Fig. 5. The analysis of the semiconductors losses was estimated using the methodology described in [30]–[32]. The IGBT conduction power losses during one switching period $T_s$ are given by:

$$P_{cond} = \frac{1}{T_s} \int_0^{T_s} v_{CE}(t) i_{CE}(t)\, dt \tag{17}$$

where $v_{CE}$ is the collector-emitter voltage, and $i_{CE}$ is the collector current.

The conduction losses of the anti-parallel diodes (body diode) or the I2NDF1 converter diodes are given by:

$$P_{Dloss} = \frac{1}{T_s}\int_0^{T_s} v_F(t) i_F(t)\, dt \tag{18}$$

where $v_F$ is the diode forward voltage, and $i_F$ is the diode forward current.

The IGBT switching losses can be estimated from equation below:

$$P_{Sloss} = (E_{on} + E_{off}) f_s \tag{19}$$

where $E_{on}$ and $E_{off}$ are, respectively, the turn-on and turn-off switching energy losses.

Moreover, the losses of magnetic components were calculated using the procedure presented in [28], as the copper losses are defined as:

$$P_{copper} = I_{s,rms}^2 R_s \tag{20}$$

where $I_{s,rms}$ is the rms current flowing through the conductor, and $R_s$ is the conductor resistance.

The core losses are given by Steinmetz's Equation:

$$P_{core} = k f^{\alpha} B^{\beta} \tag{21}$$

where $k$, $\alpha$ and $\beta$ are parameters related to the properties of the core (empirical values), while $f$ is the magnetic field frequency, and $B$ is the magnetic flux density [13].

Therefore, taking into account the parameters listed in Tables 3 and 4, and considering the values presented in datasheet of the IGBT IRGP50B60PD and the diode SCS230AE2, a MATLAB routine was used to perform the calculations of (17) to (21), during the entire grid electrical period.

Considering the rectifier operation mode, Fig. 5a presents the overall losses of the I2TDF1 and I2NDF1 converters, which is equal to 75.43 W and 82.22 W, respectively. Whereas, considering the inverter operation mode, the overall losses of the I2TDF1 and I2NDF1 converters are equal to 84.14 W and 94.79 W, respectively, as shown in Fig. 5b. In both situations, the I2TDF1 has presented lower losses than the I2NDF1 converter. Furthermore, through Fig.5, it can be seen that the major losses are due to the semiconductors on the primary side.

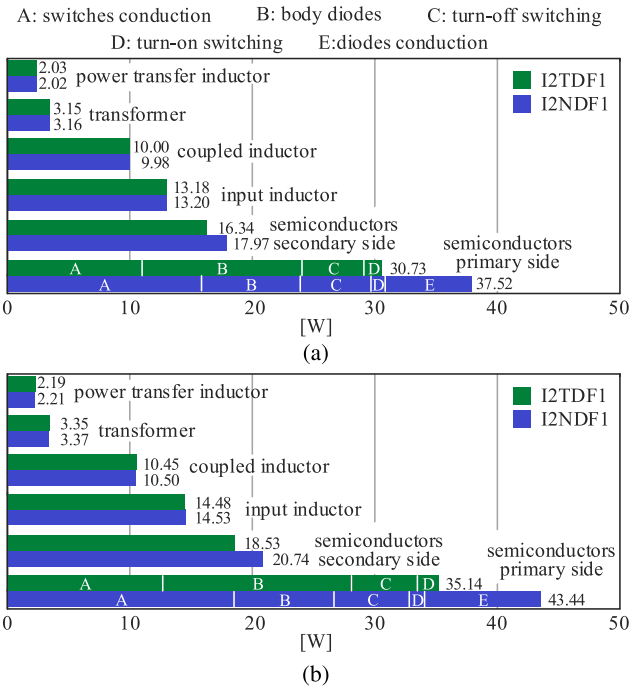


**FIGURE 5.** Losses distribution at the rated load condition: (a) rectifier mode; (b) inverter mode.

## III. CONVERTER MODEL

This section presents the model of the proposed converter, divided into two parts: one related to the modeling of the converter on the primary side, a T-type converter, and the other one in relation to the secondary side, a full-bridge converter.

### A. PRIMARY SIDE CONVERTER MODEL

The model of the inversely coupled inductor is used to obtain an uncoupled relation between the circulation current and the input current. In order to model the differential and primary bus voltage, it is considered the current flow through capacitors $C_{1,p}$ and $C_{1,n}$.

#### 1) DIFFERENTIAL-/COMMON-MODE CURRENT

Fig. 6a shows the CI equivalent circuit, containing the following variables: individual windings resistance $R_w$; dispersion inductance $L_k$; mutual inductance $M$; voltages and current of each converter arm, respectively ($v_a$ and $v_b$) and ($i_a$ and $i_b$); and input voltage ($v_{ac}$) and current ($i_{ac}$).

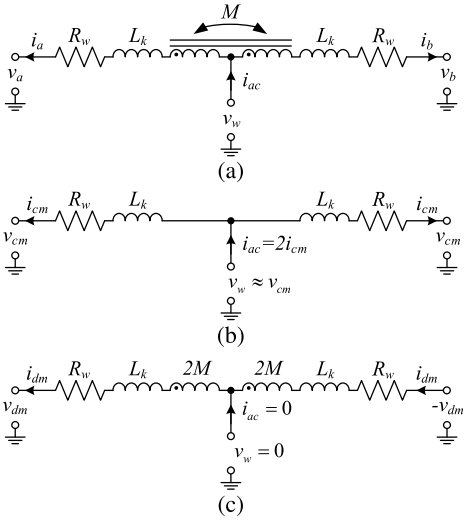


**FIGURE 6.** Equivalent circuits for (a) coupled inductor, (b) common-mode current, and (c) differential-mode current.

These voltages and currents can be defined in terms of common-mode and differential-mode, as follows:

$$v_a = v_{cm} + v_{dm} \quad i_a = i_{cm} + i_{dm} \tag{22}$$

$$v_b = v_{cm} - v_{dm} \quad i_b = i_{cm} - i_{dm} \tag{23}$$

$$v_{cm} = \frac{v_a + v_b}{2} \quad i_{cm} = \frac{i_a + i_b}{2} \tag{24}$$

$$v_{dm} = \frac{v_a - v_b}{2} \quad i_{dm} = \frac{i_a - i_b}{2} \tag{25}$$

Thus, the input and circulating currents are defined as:

$$i_{ac} = 2\,i_{cm} \tag{26}$$

$$i_{cir} = 2\,i_{dm} \tag{27}$$

From Fig. 6a, it can be inferred the following equations:

$$v_w = v_a + R_w i_a + L\frac{di_a}{dt} - M\frac{di_b}{dt} \tag{28}$$

$$v_w = v_b + R_w i_b + L\frac{di_b}{dt} - M\frac{di_a}{dt} \tag{29}$$

where $L$ ($L_a = L_b$) represents the self-inductance and is given by the sum of the leakage inductance $L_k$ and the mutual inductance $M$.

Combining (22) and (23) with (28) and (29):

$$v_w = v_{cm} + v_{dm} + R_w(i_{cm} + i_{dm}) + L_k\frac{di_{cm}}{dt} + (2M + L_k)\frac{di_{dm}}{dt} \tag{30}$$

$$v_w = v_{cm} - v_{dm} + R_w(i_{cm} - i_{dm}) + L_k\frac{di_{cm}}{dt} - (2M + L_k)\frac{di_{dm}}{dt} \tag{31}$$

Summing and subtracting (30) and (31), it can be obtained the common-mode and differential-mode voltages, respectively. Moreover such relations are represented in Fig. 6b and Fig. 6c, and analytically expressed as:

$$v_{cm} = v_w - R_w i_{cm} - L_k\frac{di_{cm}}{dt} \tag{32}$$

$$v_{dm} = -R_w i_{dm} - (2M + L_k)\frac{di_{dm}}{dt} \tag{33}$$

As it can be seen from Fig.2a, the voltage across the filter inductor $L_f$ is:

$$v_{Lf} = v_{ac} - v_w = R_{Lf} i_{ac} + L_f\frac{di_{ac}}{dt} \tag{34}$$

Replacing (26) in (34):

$$v_w = v_{ac} - 2R_{Lf} i_{cm} - 2L_f\frac{di_{cm}}{dt} \tag{35}$$

Combining (35) and (32):

$$v_{cm} = v_{ac} - (2R_{Lf} + R_w)i_{cm} - (2L_f + L_k)\frac{di_{cm}}{dt} \tag{36}$$

Performing the Laplace transform of (33) and (36), assuming zero initial conditions, the transfer functions of the differential-mode and common-mode currents can be obtained and are defined, respectively, as:

$$G_P^{dm}(s) = -\frac{1}{R_w}\left[\frac{1}{1 + s\tau_P^{dm}}\right]$$

$$\tau_P^{dm} = \frac{2M + L_k}{R_w} \tag{37}$$

$$G_P^{cm}(s) = -\frac{1}{2R_{Lf} + R_w}\left[\frac{1}{1 + s\tau_P^{cm}}\right]$$

$$\tau_P^{cm} = \frac{2L_f + L_k}{2R_{Lf} + R_w} \tag{38}$$

Last, considering (7) and (8), the voltages $V_{dm}(s)$ and $V_{cm}(s)$ are given by:

$$V_{dm}(s) = M_{dm}(s)\frac{V_{dc,1}}{2} \quad M_{dm}(s) = m - m_o \tag{39}$$

$$V_{cm}(s) = M_{cm}(s)\frac{V_{dc,1}}{2} \quad M_{cm}(s) = m + m_o \tag{40}$$

### 2) DIFFERENTIAL AND PRIMARY BUS VOLTAGE

As can be seen from Fig. 7, the currents flowing through capacitors $C_{1,p}$ and $C_{1,n}$, as well as the currents exiting in the neutral point node, can be expressed as:

$$i_p - i_n = i_{ac} + i_{Ta} + i_{Tb} \tag{41}$$

where $i_{Ta}$ and $i_{Tb}$ are related to the legs of the three-level T-type converter, and $i_{ac}$ is the input current.

Considering that capacitors $C_{1,p}$ and $C_{1,n}$ have the same capacitance $C_1$, and the currents $i_{Ta}$ and $i_{Tb}$ are internal disturbances of the system, the differential equation for the differential voltage is given by:

$$\frac{dv_{dif}}{dt} = \frac{1}{C_1} i_{ac} \tag{42}$$

where $v_{dif} = v_{C1,p} - v_{C1,n}$ represents the differential voltage.

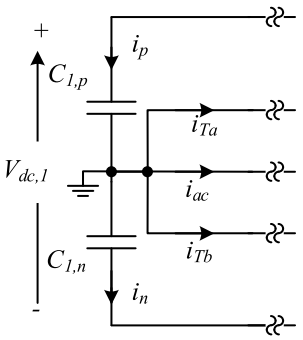


**FIGURE 7.** Current flow through the primary bus for I2TDF1.

Taking the Laplace transform of (42), with zero initial conditions, it can be written the following equation:

$$G_P^{vdif}(s) = \frac{V_{dif}(s)}{I_{ac}(s)} = \frac{1}{sC_1} \tag{43}$$

Following a similar approach to the one developed for the differential voltage loop, the transfer function between the primary bus voltage and the input current can be expressed as:

$$G_P^{vdc1}(s) = \frac{V_{dc1}(s)}{I_{ac}(s)} = \frac{1}{sC_1} \tag{44}$$

### B. SECONDARY SIDE CONVERTER MODEL

#### 1) VOLTAGE LOOP

The representation of the converter from the point of view of the output is shown in Fig. 8, where it can be noted that the converter behaves as a voltage source controlled by a phase-shift, and thus this must be the variable to be adjusted.

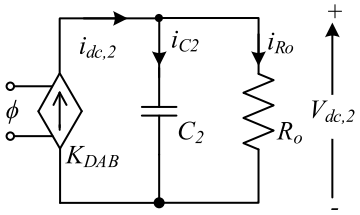


**FIGURE 8.** Secondary side equivalent circuit.

The linearization process to determine the gain $K_{DAB}$ consists on calculating the angular coefficient of the line equation from the two phase-shift conditions near to the operating point (i.e., rated phase-shift $\phi$). Then, for small variations of $\phi$, it can be obtained:

$$K_{DAB} = \frac{I_{dc,2}}{\phi} \tag{45}$$

where $I_{dc,2}$ is the rated load current.

According to Fig. 8, the differential equation that models the $K_{DAB}$ behavior is obtained as follows:

$$i_{dc,2} = C_2 \frac{dv_{dc,2}}{dt} + \frac{v_{dc,2}}{R_o} \tag{46}$$

So the transfer function that relates the secondary bus voltage with the phase-shift angle is given by:

$$G_P^{vdc2}(s) = K_{DAB} \frac{R_o}{\tau_{DAB} s + 1} \tag{47}$$

$$\tau_{DAB} = R_o C_2 \tag{48}$$

## IV. CONTROL METHOD

This section presents the control strategy used in the proposed converter. The proposal is also divided into parts for the sake of clarity: the first one is for primary side control, while the other one is for the secondary side [24], as indicated in Fig. 9. Also, three distinct control loops can be identified: two loops related to the primary side, and one to the secondary one.

### A. PRIMARY SIDE CONTROL STRATEGY

The block diagram with the controllers responsible for regulating the voltages and currents on the primary side of the converter is shown in Fig. 9. The controllers (I) and (II) are responsible, respectively, for the control of the circulating ($i_{cir}$) and input ($i_{ac}$) currents, the strategy used is adapted from [25], [33]. On the other hand, the controllers (III) and (IV) are responsible, respectively, for the bus voltage control $V_{dc1}$ and the capacitors voltages balancing $v_{C1,p}$ and $v_{C1,n}$, as adaptation of the strategy presented in [34].

#### 1) CURRENT LOOP

It is presented in [33] an optimization method of proportional-integrative (PI) controllers that enables the increase of proportional gain $k_P$ and decreases the integral time constant $\tau_I$, thus increasing the integrative gain $k_I$, while taking into account the effects of transport and sampling delays $T_D = 3/(4f_s)$, by given a desirable phase margin $\phi_M$. This strategy is used in the current control of a multilevel converter with coupled inductor, because it presents, as an advantage, the possibility of controlling, through two distinct processes, the common- and differential-mode currents, since these currents are uncoupled [25]. In the proposed converter, only PI controllers are used, due to the simplicity of equation and digital implementation.

The PI controller for the differential-mode current presented in the loop (I) is defined as:

$$G_C^{dm}(s) = k_P^{dm} \left[ 1 + \frac{1}{s\tau_I^{dm}} \right] \tag{49}$$

The open-loop transfer function of the differential-mode current with compensator $OLTF_{wc}^{idm}(s)$ is given by:

$$G_C^{dm}(s) e^{-sT_D} K_{conv} G_P^{dm}(s) = \frac{k_P^{dm} K_{conv}}{R_w \tau_I^{dm}} \frac{\left(1 + s\tau_I^{dm}\right) e^{-sT_D}}{s\left(1 + s\tau_P^{dm}\right)} \tag{50}$$

where $K_{conv}$ is the converter gain and is equal to $V_{dc,1}/2$.

The phase angle of $OLTF_{wc}^{idm}(s)$ at the crossover frequency $\omega_C$, in radians, is given by:

$$\begin{aligned} &\angle \left\{ G_C^{dm}(j\omega_C) e^{-j\omega_C T_D} K_{conv} G_P^{dm}(j\omega_C) \right\} \\ &= \angle \left\{ -\frac{k_P^{dm} K_{conv}}{R_w \tau_I^{dm}} \frac{\left(1 + j\omega_C \tau_I^{dm}\right) e^{-j\omega_C T_D}}{j\omega_C \left(1 + j\omega_C \tau_P^{dm}\right)} \right\} \\ &= -\pi + \phi_M \\ &= \tan^{-1}\left(\omega_C \tau_I^{dm}\right) - \pi/2 - \omega_C T_D - \tan^{-1}\left(\omega_C \tau_P^{dm}\right) \end{aligned} \tag{51}$$

Typically, $\omega_C \tau_P^{dm} \approx \pi/2$, thus, from (51), the integral time constant can be defined as:

$$\tau_I^{dm} = \frac{\tan(\phi_M + \tan^{-1}(\omega_C T_D))}{\omega_C} \tag{52}$$

And since the gain of $OLTF_{wc}^{dm}(s)$ is equal to 1, at the crossover frequency, the proportional gain is given by:

$$k_P^{dm} = -\frac{R_w \tau_I^{dm}}{K_{conv}} \omega_C \sqrt{\frac{1 + \omega_C^2 \left(\tau_P^{dm}\right)^2}{1 + \omega_C^2 \left(\tau_I^{dm}\right)^2}} \tag{53}$$

Typically, $\omega_C \tau_P^{dm} \gg 1$, and $\omega_C \tau_I^{dm} \gg 1$ so the proportional gain is reduced to:

$$k_P^{dm} \approx -\frac{\omega_C (2M + L_k)}{K_{conv}} \cong -\frac{2\omega_C L}{K_{conv}} \tag{54}$$

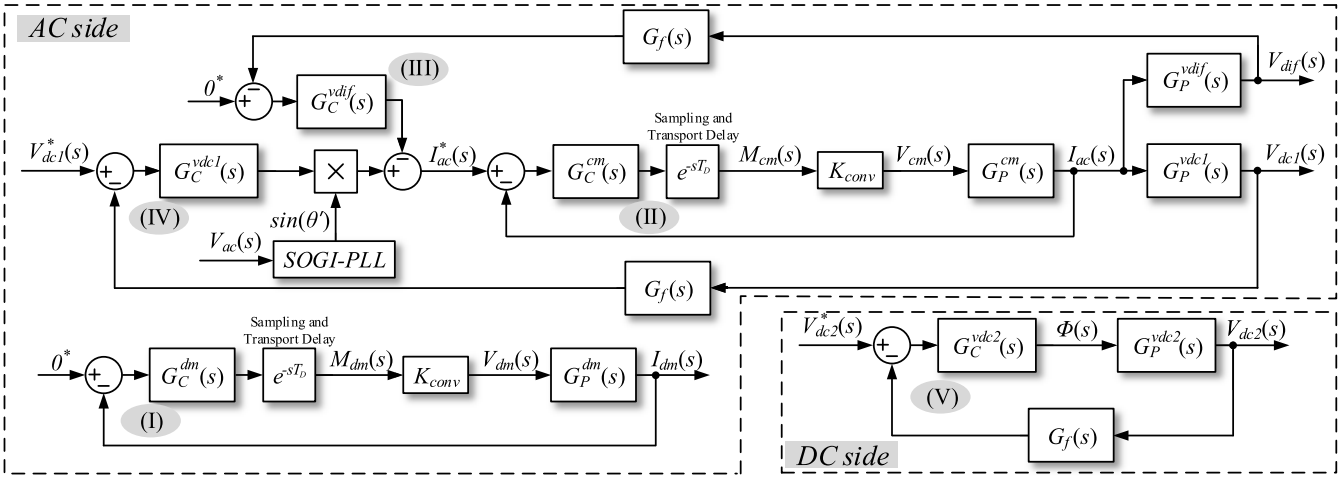


**FIGURE 9.** Simplified block diagram of the closed-loop control system.

On the other hand, regarding the loop (II), the PI controller for the common-mode current is defined as:

$$G_C^{cm}(s) = k_P^{cm}\left[1 + \frac{1}{s\tau_I^{cm}}\right] \tag{55}$$

The open-loop transfer function of the common-mode current with compensator $OLTF_{wc}^{icm}(s)$ is given by:

$$G_C^{cm}(s)e^{-sT_D}K_{conv}G_P^{cm}(s) = \frac{k_P^{cm}K_{conv}}{(2R_{Lf}+R_w)\tau_I^{cm}}\frac{\left(1+s\tau_I^{cm}\right)e^{-sT_D}}{s\left(1+s\tau_P^{cm}\right)} \tag{56}$$

Comparing $OLTF_{wc}^{icm}(s)$ and $OLTF_{wc}^{idm}(s)$, the differences relays on the plant transfer function. In this way, the methodology to find the proportional gain, as well as the integral time constant for $G_C^{cm}$, is similar to the one developed for the differential-mode controller. Thus:

$$k_P^{cm} \approx -\frac{\omega_C(2L_f+L_k)}{K_{conv}} \cong -\frac{2\omega_C L_f}{K_{conv}} \tag{57}$$

$$\tau_I^{cm} = \tau_I^{dm} \tag{58}$$

### 2) VOLTAGE LOOP

For the cascade control system presented in Fig. 9, it is important to notice that the current closed-loop system is considered by the voltage loop simply as a constant, defined as the inverse of the current sensor gain, which assumed as unitary, simplifies the system, as similarly investigated by [35].

The open-loop transfer function of the differential voltage with compensator $OLTF_{wc}^{vdif}(s)$ is defined as:

$$G_C^{vdif}(s)G_P^{vdif}(s)G_f(s) = \frac{k_P^{vdif}}{C_1\tau_I^{vdif}}\frac{\left(1+s\tau_I^{vdif}\right)}{s^2\left(1+s\tau_f\right)} \tag{59}$$

where $G_f(s)$ is the transfer function of the first order low-pass filter, and $\tau_f$ is the filter time constant equal to $1/(2\pi f_o)$.

The phase angle of $OLTF_{wc}^{vdif}(s)$ at the crossover frequency $\omega_C$, in radians, is given by:

$$\begin{aligned}
&\angle\left\{G_C^{vdif}(j\omega_C)G_P^{vdif}(j\omega_C)G_f(j\omega_C)\right\} \\
&= \angle\left\{\frac{k_P^{vdif}}{C_1\tau_I^{vdif}}\frac{\left(1+j\omega_C\tau_I^{vdif}\right)}{(j\omega_C)^2\left(1+j\omega_C\tau_f\right)}\right\} \\
&= -\pi + \phi_M \\
&= \tan^{-1}\left(\omega_C\tau_I^{vdif}\right) - \pi - \tan^{-1}\left(\omega_C\tau_f\right)
\end{aligned} \tag{60}$$

So, by rearranging (60), the integral time constant is given by:

$$\tau_I^{vdif} = \frac{\tan(\phi_M + \tan^{-1}(\omega_C\tau_f))}{\omega_C} \tag{61}$$

And since the gain of $OLTF_{wc}^{vdif}(s)$ is equal to 1, at the crossover frequency, the proportional gain is:

$$k_P^{vdif} = C_1\tau_I^{vdif}\omega_C^2\sqrt{\frac{1+\omega_C^2\tau_f^2}{1+\omega_C^2\left(\tau_I^{vdif}\right)^2}} \tag{62}$$

Similar to the development of the differential voltage loop, the integral time constant and the proportional gain for the primary bus voltage loop are given, respectively, by:

$$\tau_I^{vdc1} = \frac{\tan(\phi_M + \tan^{-1}(\omega_C\tau_f))}{\omega_C} \tag{63}$$

$$k_P^{vdc1} = C_1\tau_I^{vdc1}\omega_C^2\sqrt{\frac{1+\omega_C^2\tau_f^2}{1+\omega_C^2\left(\tau_I^{vdc1}\right)^2}} \tag{64}$$

## B. SECONDARY SIDE CONTROL STRATEGY

The block diagram with the controller responsible for regulating the voltage of the secondary side (dc side) of the converter is also shown in Fig. 9.

The open-loop transfer function of the secondary bus voltage $OLTF_{wc}^{vdc2}(s)$, the loop (V), is given by:

$$G_C^{vdc2}(s)G_P^{vdc2}(s)G_f(s) = \frac{k_P^{vdc2}K_{DAB}R_o}{\tau_I^{vdc2}} \frac{\left(1+s\tau_I^{vdc2}\right)}{s\left(1+s\tau_{DAB}\right)\left(1+s\tau_f\right)} \quad (65)$$

Similar to the development of the voltage loops at primary side, choosing the phase margin and the crossover frequency, the integral time constant and the proportional gain are given, respectively, by:

$$\tau_I^{vdc2} = \frac{\tan(\phi_M - \pi/2 + \tan^{-1}(\omega_C\tau_{DAB}) + \tan^{-1}(\omega_C\tau_f))}{\omega_C} \quad (66)$$

$$k_P^{vdc2} = \frac{\tau_I^{vdc2}}{K_{DAB}R_o}\omega_C \sqrt{\frac{(1+\omega_C^2\tau_{DAB}^2)(1+\omega_C^2\tau_f^2)}{1+\omega_C^2\left(\tau_I^{vdc2}\right)^2}} \quad (67)$$

### C. TUNING CONTROLLERS

The phase margins and crossover frequencies were chosen with the commitment between system speed response and the possibility of embedded implementation, considering the assumptions found in the literature, similarly to the ones found in [35].

The differential-/common-mode current controllers gains have been chosen in order to keep the phase margin as $f_s/10$, and the crossover frequency as 50°, as shown in Fig. 10. The crossover frequency for the primary and secondary bus voltage loops have been chosen as $f_o/4 = 15$ Hz, while the phase margin is 75°, as presented in Fig. 11 and Fig. 12, respectively. Moreover, the crossover frequency for the differential voltage has been chosen as $f_{cvdif} = f_o/10 = 5$ Hz and the phase margin is 75°, as presented in Fig. 11. Using the values listed in Tables 3 and 4, and considering the aforementioned specifications, the controllers gains are presented in Table 5.

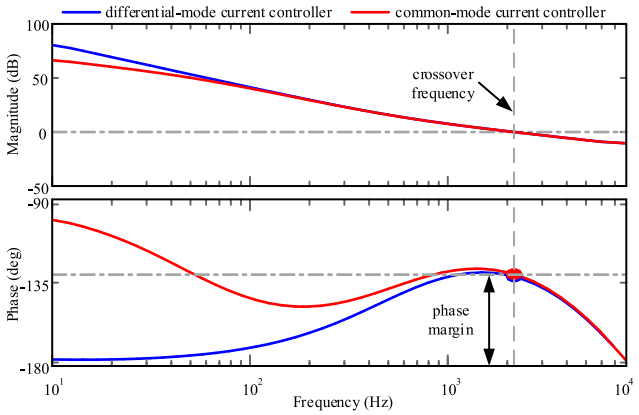


**FIGURE 10.** Differential- and common-mode current controllers: magnitude and phase Bode diagrams.

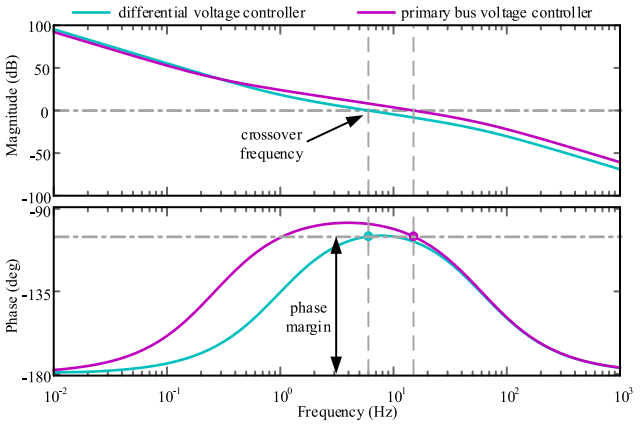


**FIGURE 11.** Differential and primary bus voltage controllers: magnitude and phase Bode diagrams.

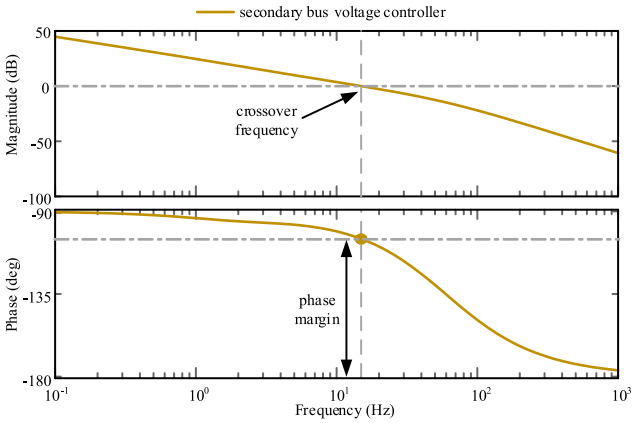


**FIGURE 12.** Secondary bus voltage controller: magnitude and phase Bode diagrams.

**TABLE 5.** Controllers gains.

| Description | Label | Value |
|---|---|---|
| Input current controller | | |
| Proportional gain | $k_P^{cm}$ | −0.1437 |
| Integral time constant | $\tau_I^{cm}$ | 2.8749e−04 s |
| Differential-mode current controller | | |
| Proportional gain | $k_P^{dm}$ | −3.9200 |
| Integral time constant | $\tau_I^{dm}$ | 2.8749e−04 s |
| Primary bus voltage controller | | |
| Proportional gain | $k_P^{vdc1}$ | 0.1370 |
| Integral time constant | $\tau_I^{vdc1}$ | 0.6307 s |
| Differential voltage controller | | |
| Proportional gain | $k_P^{vdif}$ | 0.0527 |
| Integral time constant | $\tau_I^{vdif}$ | 0.1622 s |
| Voltage output controller | | |
| Proportional gain | $k_P^{vdc2}$ | 0.0185 |
| Integral time constant | $\tau_I^{vdc2}$ | 0.0711 s |

## V. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed converter, a prototype has been built and tested according to the specifications listed in Tables 3 and 4, as presented in Fig. 13. The control platform is a TMS320F28379D DSP from Texas Instruments. The currents and voltages signals acquisitions are obtained through

sensors HO 25-NP/SP33 and LV 20-P, respectively, both from the manufacturer LEM. The switches on the primary and secondary sides are IGBT IRGP50B60PD from SEMIKRON SKHI61R driver, while diodes SCS230AE2 are used on the primary side of the NPC.

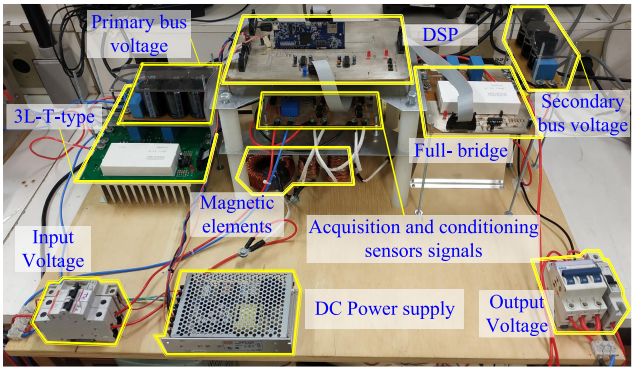


**FIGURE 13.** Built prototype for experimental evaluation.

### A. PRIMARY BUS PRELOAD

The initial configuration consists on loading the primary bus voltage before initiating the secondary bus control. This process aims to reduce undesirable voltage derivatives, and consequently, current peaks on the magnetic elements, and thus preventing the IGBTs from being damaged or the converter protections to act early.

Initially, in order to avoid that, the switches are all turned-off, and the voltage across capacitors $C_{1,p}$, and $C_{1,n}$ are equal to the peak ac side voltage. Then to preload the capacitors, the control is enabled to obtain the rated voltage on the primary bus. Thus, when the steady state occurs, there is balance situation at the neutral point, as the voltages, $C_{1,p}$, and $C_{1,n}$, present the same average value of $V_{dc,1}/2$. Once this process is finished, the secondary bus control is activated.

### B. DYNAMICS TESTS

#### 1) STEP-LOAD AT RECTIFIER OPERATION MODE (ROM)

To verify the control loops stability, it was performed a load step from 50% to 100% of the rated load, as presented in Fig. 14a. It is important to notice the DC voltages undershoots: $V_{C,2}$ stabilizes at, approximately, 40 ms, while $V_{C1,p}$ and $V_{C1,n}$ voltages at, approximately, 160 ms.

Fig. 14b indicates the load step from 100% to 50%, where bus voltage $V_{C,2}$ stabilizes around 40 ms, while $V_{C1,p}$ and $V_{C1,n}$ stabilize at, approximately, 120 ms. It can observed from both steps that the control loops worked as expected.

#### 2) STEP-LOAD AT INVERTER OPERATION MODE (IOM)

As observed during the load steps at the ROM, the control loops were also able to stabilize the variables in their reference values at the IOM, according to Figs. 14c and 14d. As can be noted, the main difference is a greater voltage and current oscillations on the primary side while the process return to their rated voltages.

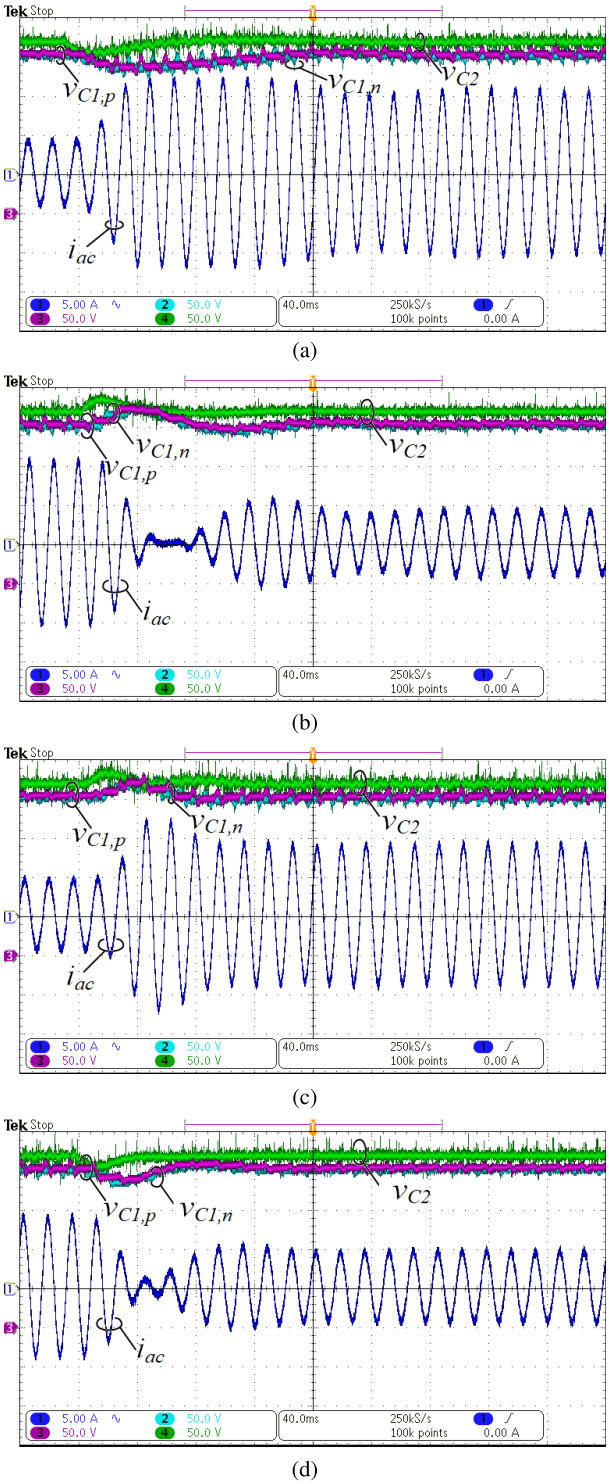


**FIGURE 14.** Input current $i_{ac}$, channel 1 (5 A/div); voltage across the capacitor $C_{1,p}$, $v_{C1,p}$; channel 2 (50 V/div); voltage across the capacitor $C_{1,n}$, $v_{C1,n}$; channel 3 (50 V/div); voltage across the capacitor $C_2$, $v_{C2}$, channel 4 (50 V/div). (a) ROM load step-up. (b) ROM load step-down. (c) IOM load step-up. (d) IOM load step-down.

### C. BIDIRECTIONAL TESTS

Initially, the converter is working at ROM, until the power flow is reversed, at 40 ms, as shown in Fig. 15a. It can be noted that bus voltages are stabilized, which proves the voltage

control loop good performance. The power flow inversion is noted at 60 ms, when the current is phase shifted from the reference voltage waveform at 180° (curve in light gray). On the other hand, Fig. 15b shows a similar process to the previously one, but, the converter is in IOM, initially. The inversion occurs around 20 ms after the beginning of the process. It can also be noted that the voltage loops regulate the DC buses.

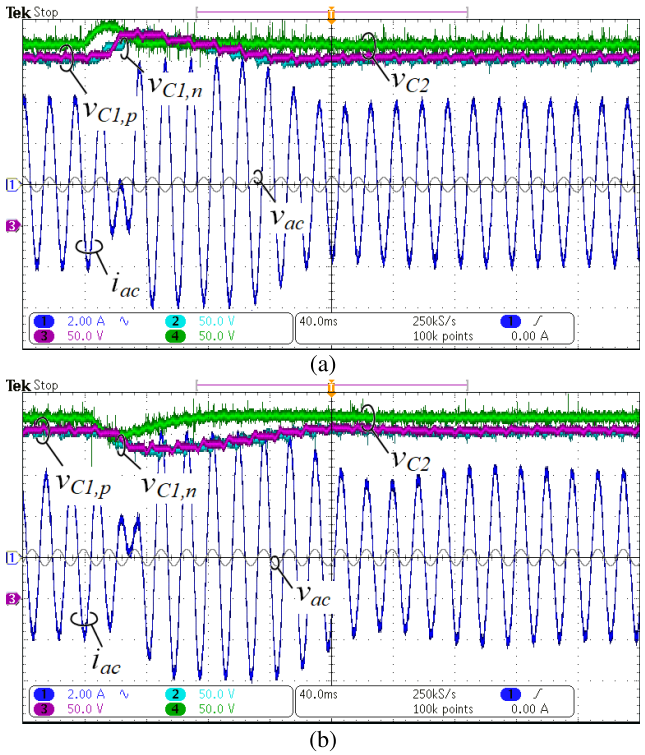


**FIGURE 15.** Power flow inversion: input current $i_{ac}$, channel 1 (2 A/div); voltage across the capacitor $C_{1,p}$, $v_{C1,p}$; channel 2 (50 V/div); voltage across the capacitor $C_{1,n}$, $v_{C1,n}$; channel 3 (50 V/div); voltage across the capacitor $C_2$, $v_{C2}$, channel 4 (50 V/div). (a) ROM to IOM. (b) IOM to ROM.

### D. POWER ANALYSIS

Power analysis takes into account the following aspects: power factor, efficiency, total current harmonic distortion (THD*i*) and current harmonic content measurement for both modes of operation (ROM and IOM) considering the international standard IEC 61000-3-2 for class A equipment. The tests were performed considering an initial output power of 200 W, with increments of 100 W, until reaching the rated power at 850 W, for both I2NDF1 and I2TDF1 converters.

Two power analyzers (YOKOGAWA WT310) were connected to the input and output from both converters. The power factor reaches almost 0.996 in both modes, as can be seen in Fig. 16. At ROM, the power factor increases and reaches its maximum value at 300 W, and decreases down to 0.993 at the rated power of 850 W. On the other hand, at IOM, it reaches its maximum at 400 W and then decreases to 0.994, again at the rated power. Both converters present a high power factor and similar trend regarding to the variation of theirs operation power levels.

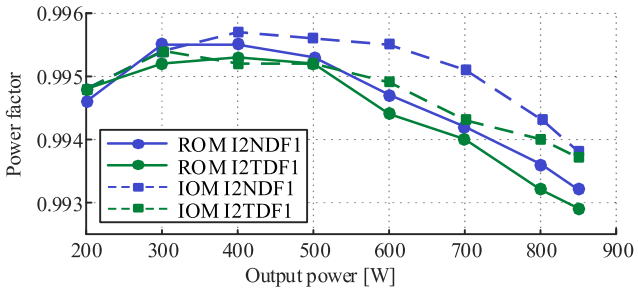


**FIGURE 16.** Measured power factor for load variations.

Fig. 17 shows the efficiency curves for the rectifier and inverter modes for both converters. It can be seen that the I2TDF1 topology performed slightly better than the I2NDF1 one for the entire operating power range, presenting a better result at the nominal output power of around 1%. More particularly, the I2TDF1 converter presented its maximum efficiency around 300 W, being 91.398% and 90.602% in the rectifier and inverter modes, respectively. As for the rated power, the efficiencies are 89.397% and 87.515%, respectively, and on average, was 1.23% less than the estimated efficiency, as detailed in Fig 5. It is worth to mention that the efficiency can be further improved with the use of modern materials for magnetic elements and semiconductor devices.

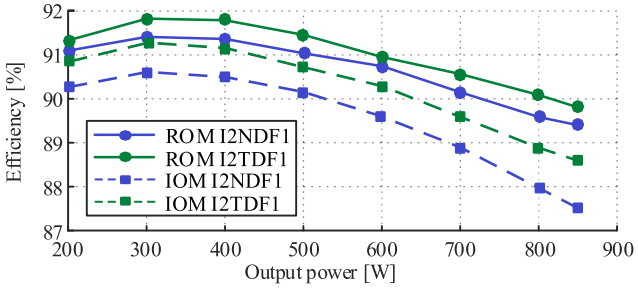


**FIGURE 17.** Measured efficiency curves for different load conditions.

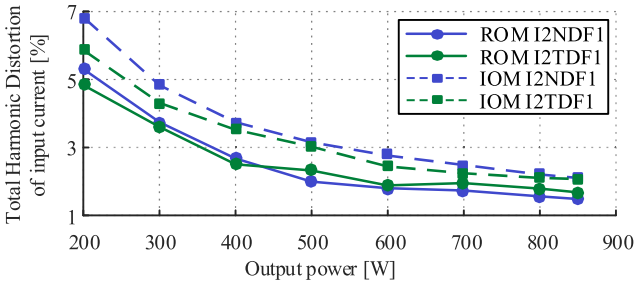


**FIGURE 18.** Measured THD*i* curves for load variations.

For the harmonic analysis results, in the rectifier mode, the THD*i* is less than 5% for almost the entire operating

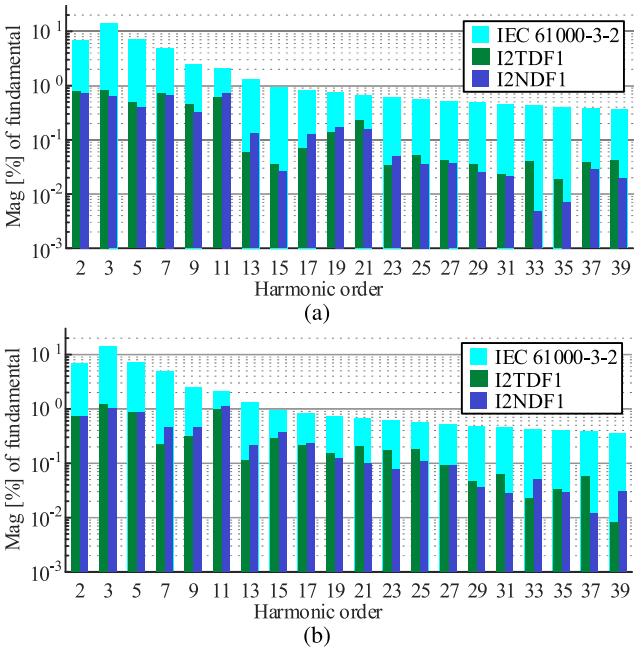


**FIGURE 19.** Harmonic spectrum of the input current at the rated load condition: (a) rectifier mode; (b) inverter mode.

range, as can be observed in Fig. 18. Moreover, this value is still kept low while the operation is around to 200 W. Above 300 W, both converters present THD*i* less than 5% for both operation modes. It was also verified that, when load power is reduced, the 11th harmonica is greater than the one predicted in the standard IEC 61000-3-2. More clearly, in the ROM, such behavior is verified until 350 W, while at IOM, until 400 W. From Figs. 19a and 19b, it is possible to verify that both converters are in accordance with the international standard IEC 61000-3-2 for both rated power operating modes.

## VI. CONCLUSION

This paper presented a bidirectional isolated ac–dc converter based on the multi-state switching cell (MSSC) with a T-type (TNPC) cell on primary side. Converter modeling is a fundamental point for its correct functioning and understood, as the model found is also used for both converters. Furthermore, a great advantage of these type of converters are the possibility of employing a relatively simple control method, as uses classic control techniques on its structure.

The experimental results with rated conditions showed a high power factor on the AC grid, of approximately 0.993, and a low THD*i*, less than 3%, for both rectifier and inverter operation modes. Dynamic and bidirectional tests have been performed in order to validate the proposed structure and compared with the NPC converter. It was noted that the I2TDF1 topology achieved a better performance than I2NDF1, being more efficient as it employs only active switches and no additional diodes. Indeed, it was observed that the efficiencies were, on average, less than 1.23% of the estimated values obtained from elaborated losses analysis.

Therefore, the proposed converter must be seen as an attractive solution to replace the NPC-based power converter topologies in applications such as Solid State Transformers in MV Traction, and in battery charging, where a bidirectional power flow, as well as power factor correction are mandatory.

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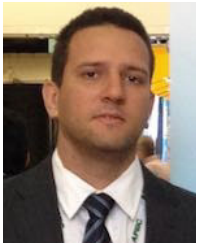

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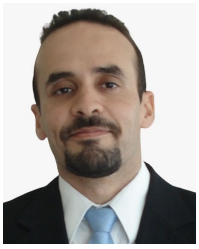

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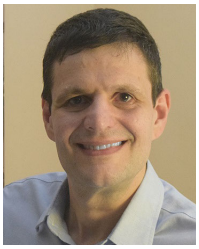

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