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PZT Ferroelectric Synapse TFT With Multi-Level of Conductance State for Neuromorphic Applications

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ABSTRACT To fundamentally solve the bottleneck of Von Neumann's computing architecture, a neuromorphic thin-film transistor (NTFT) employing Pb(Zr, Ti)O_3 (PZT) was investigated. The indium gallium zinc oxide (IGZO) channel back gate TFT structure was chosen to solve the diffusion of atoms that form a channel layer during the annealing process for crystallization of PZT. A post-deposition process with IGZO after annealing PZT and using an oxide-based material as a channel structure can minimize the diffusion phenomenon of junction materials and oxygen together, which leads to a high and reliable performance of the NTFT. The basic operations of synapses short-term memory (STM) and long-term memory (LTM) were also analyzed to confirm the application of a neuromorphic device. The high dielectric constant and polarization properties of Pb(Zr, Ti)O_3 (PZT) allow the power consumption of spike signals used in spike dependent plasticity change to be reduced to 10 pJ. Moreover, a wide dynamic range of $G_{max}/G_{min} \cong 1000$ was obtained, and the channel conductance was maintained over 40000 seconds. The optimized pulse achieved multi-level states (>32), which made the learning process efficient. This study verified that the PZT-TFT structure has a high potential and merits for neuromorphic devices.

INDEX TERMS Ferroelectric, synapse, neuromorphic, multi-level, transistor.

I. INTRODUCTION

Despite advances in semiconductor devices, when processing big data, the limitation of the bus unit between the memory device and the processing device creates a bottleneck in the Von-Neumann computing architecture. This problem is mainly caused by processing data serially between memory and a processing device, and therefore a structure that processes data in parallel can be a solution. Inspired by this, researchers are studying imitation of the brain nervous system, one of the representative parallel processing structures. The important parameters of this neuron-type biologically based synaptic device are its low power consumption, massively parallel computation, and non-volatile properties [1]. Initially, 8-T SRAM was used to realize a synapse structure and the biological functions [2]. However, this method has some disadvantages in that it requires a lot of area and energy to express a single synapse. To solve this problem, two-terminal single synaptic mechanisms were suggested: resistance change [3], phase change [4], spintronics [5], and ferroelectric [6]. The two-terminal design has some merits, namely high integration density and easy fabrication. However, this structure has difficulty in maintaining reliable operation and uniformity at a large scale. Moreover, it requires additional devices such as a selector or a transistor to improve the controllability of the memory state and the accessibility of a specific cell and to minimize leakage current and malfunction of the device in the matrix design. On the other hand, a three-terminal structure or a transistor in which learning and working are performed at the same time is close to the operation of the brain and has the advantage that it does not require an additional device mentioned previously [7].

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The reliability of short-term memory and long-term memory is an important point in realizing the biological function of the human brain. Considering long-term memory and uniformity among cells, ferroelectric material has been suggested as a promising candidate for a synaptic mechanism due to its stable permanent dipole moment. With the principle of polarization characteristics, the degree of polarization can be controlled precisely so that multiple levels of states can be created easily. Various ferroelectric materials, including strontium bismuth tantalate (SBT) and polyvinylidene fluoride (PVDF), require optimized polarization values and coercive field values to operate at low power for multiple memory applications [8], [9]. To solve this problem, hafnium-based ferroelectric materials have recently been studied. However, because such materials have relatively low polarizability, they require a very thin film layer to get enough capacitance, which induces a very severe fabrication process margin and a leakage current pathway by a tunneling mechanism. On the other hand, $Pb(Zr,Ti)O_3$ (PZT) can be a suitable choice for low-power operation and non-volatile memory function due to its high residual permittivity and coercive field value [10]. In addition, it is simple to fabricate a large-scale parallel structure for devices using a sputtering system or chemical vapor deposition (CVD). However, in the case of a ferroelectric field-effect transistor (Fe-FET) based on Si, it is difficult to use a ferroelectric film as gate oxide due to the diffusion of Si atoms to the ferroelectric layer during a high-temperature annealing process [11]. Additionally, oxygen diffusion from the ferroelectric oxide to the Si junction layer induces oxygen vacancies which result in a high leakage current with low reliability. Therefore, a thin oxide diffusion barrier is necessary, and it induces a parasitic capacitance by which the high dielectric property of the ferroelectric material deteriorates.

Here, we studied the characteristics and the design of PZT film for a Fe-FET structure to achieve a high-performance neuromorphic device. To solve the interfacial reaction problem of PZT and the channel material, we chosen a thin film transistor (TFT) with a back gate structure instead of adding a diffusion barrier of thin oxide film as in previous studies. Indium gallium zinc oxide (IGZO) was selected as the channel material since it is an oxide base material with high mobility and high carrier density so that it can solve oxygen defect issues and can guarantee high performance. High-performance transistor devices can be obtained by using PZT to mimic biological brain functions. In neuromorphic engineering, it is necessary to implement large-scale parallel processing by implementing spike dependent plasticity leveling, short-term memory (STM), and long-term memory (LTM) with low power due to material and structural features. Therefore, we studied and improved these points in the TFT structure by employing PZT and IGZO. With the optimized process conditions of the PZT-IGZO TFT structure, it was possible to learn and process the program efficiently by implementing multiple levels based on a wide weight range.

II. EXPERIMENTAL

A. FABRICATION OF THE SYNAPSE DEVICE BASED ON PZT

The fabrication process of the PZT-based synapse device was as follows. Glass was used as the substrate of the device. The bottom electrode consisted of indium-tin-oxide (ITO). To get stable ITO film during annealing process, we formed the film in the conditions the partial pressure of Ar: O_2 = 50: 3, 100 watts (W) radio frequency (RF) power sputtering, and the annealing process for 1 hour at 300 °C were optimized. The ITO electrode was deposited on the entire glass surface. The thickness was about 200 nm, and the sheet resistivity was 8∼10 ohm/square. The patterning on a substrate by photolithography and a wet-etching process was performed to define the ITO bottom gate. To achieve a high dielectric constant and low leakage, a PZT target in the morphotropic phase composition (MPC) region at a ratio of Zr: Ti = 48: 52 was deposited at 200 nm in a 40: 5 = Ar: O_2 environment using a radio frequency (RF) magnetron sputtering system. To obtain the perovskite phase, the device was annealed in a tube furnace at 550 °C for 30 minutes, and then it was naturally cooled. The IGZO film used as the channel material was deposited at 40 nm through RF-sputtering in a 50: 5 = Ar: O_2 environment to minimize the oxygen starvation interference with the PZT layer. IGZO was annealed for 60 minutes after reaching 350 °C at a rate of 5 °C/min in a tube furnace. For the top electrode, 70 nm thick Al was deposited using thermal evaporation for ohmic contact with IGZO.

B. MEASUREMENT SETUP FOR THE MATERIAL CHARACTERISTICS OF THE DEVICE

An X-ray diffraction analyzer was used to confirm the perovskite phase with ferroelectric properties (Panalytical/Empyrean). An atomic force microscope was used to examine the surface characteristics according to the annealing temperature (AFM, Park-systems/XE-150). Field emission transmission electron microscopy (FE-TEM, Hitachi, HF-3300) and X-ray photoelectron spectrometer (XPS, Thermo Scientific/ESCALAB 250Xi) were used to determine the stability and interfacial reaction of PZT and IGZO oxides.

C. MEASUREMENT SETUP FOR THE ELECTRICAL CHARACTERISTICS OF THE DEVICE

To examine the electrical characteristics of PZT, the capacitance-voltage, leakage, and current-voltage were measured through a semiconductor characteristic analyzer (Keithley, 4200-SCS). A ferroelectric tester (radiant, RT66C) was used to confirm the ferroelectric properties of Ferroelectric.

D. MEASUREMENT SETUP FOR SYNAPSE CHARACTERISTICS

To check the synapse operation of the optimized ferroelectric-based TFT, pulse measurement was performed in a three-terminal measurement structure environment through a series precision source/measurement device (Keysight, B2902A).

Various types of pulses were created through the internal software (Easy EXPERT). The input signal duration was 300 ms as the minimum implementation condition of the measuring equipment.

E. NEURAL NETWORK SIMULATION FOR PATTERN RECOGNITION ACCURACY

We implemented a neural network in a MATLAB environment to determine the pattern recognition accuracy, which changed according to the performance of the synaptic device. Each of the three layers (input, hidden, and output layer) consisted of 400,200,10 neurons. The performance was verified by learning a modified National Institute of Standards and Technology database (MNIST), a hand-written digit dataset. A more detailed description of the nonlinear MLP simulation process can be found in Supplementary Material S3 with the flow chart and source code. We observed the pattern recognition accuracy by changing the number of level states that each neuron can represent.

III. RESULTS AND DISCUSSION

Figs. 1 (a) and (b) show the crystalline phase of various conditions of PZT on ITO coated glass, which was analyzed by grazing-angle incidence X-ray diffraction (GA-XRD) and atomic force microscopy (AFM). There were no crystallization phase peaks of PZT in the as-deposited state by a sputtering system. After an annealing process at 500 °C, 550 °C, and 600 °C, the pyrochlore and perovskite phase were identified [12]. It showed that higher temperature conditions in the PZT annealing process induced a more vigorous intensity of the perovskite phase while the noise peaks are increased as well. As a result of the AFM surface morphology, the degree of roughness increased with an increasing annealing temperature. The roughness increased rapidly above 600 °C. Because the channel mobility of a TFT is related to its roughness, it should be considered a trade-off between the roughness and polarization characteristics at high annealing temperatures. Considering the process margin in the complementary metal-oxide-semiconductor (CMOS) process, a process temperature below 600 °C was suitable for the polarization annealing process. For these reasons, we selected a PZT annealing temperature of 550 °C to optimize the characteristics of the device.

Indium-gallium-zinc-oxide (IGZO) was used as an oxide channel material. The inset presenting the depth profile of the X-ray photoelectron spectroscopy (XPS) in Fig. 1(c), the lead (Pb, red line) and the oxygen (O, blue line) elements did not diffuse to other layers, and each layer maintained the ratio with optimal properties. The composition ratio of the PZT layer acting as the gate oxide of the device was confirmed around Zr: Ti = 52: 48 by energy dispersion spectroscopy (EDS), as shown in Fig. 1(d). This ratio is a morphotropic phase boundary that has high ferroelectric properties in terms of structural and electrical properties, and various crystal structures are mixed to optimize the device properties and stability [13], [14]. From the gate electrode to the channel

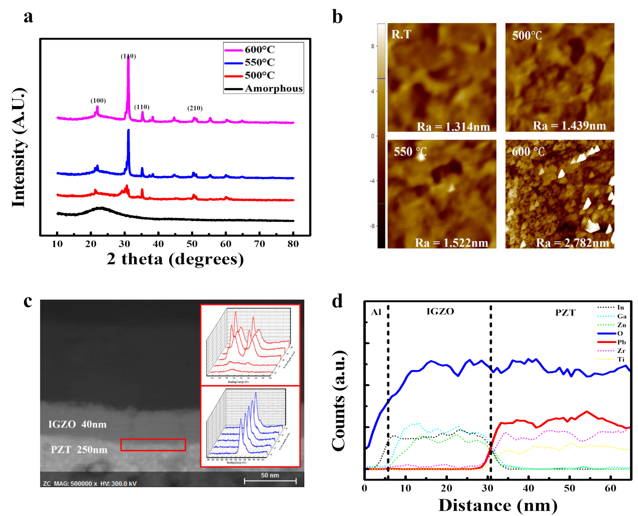

FIGURE 1. (a) XRD spectrum RT, 500 °C, 550 °C, 600 °C annealing, (b) AFM surface morphology, (c) FE-TEM image of the Al/IGZO/PZT stack with XPS depth profile. The blue and red lines show the spectra of O and Pb, respectively. (d) EDS line profiles of the Al/IGZO/PZT stack.

material, all the film layers are oxide material, ITO, PZT, and IGZO. Therefore, the TFT structure is free from Si diffusion, which is a severe problem in the Si transistor employing PZT, and oxygen deficiency in the PZT film, which is due to oxygen diffusion to other adjacent layers and one of the significant reasons for leakage current of PZT can be minimized.

The ferroelectric characteristics of PZT were verified as shown in Figs. 2 (a)-(c). The traditional butterfly shape of the capacitance-voltage (C-V) characteristic for ferroelectric material was apparent in the post-annealed PZT film. This figure confirmed that the higher the annealing temperature, the better the polarizability of the PZT film. Leakage current, mainly related to the effects such as defects, grain boundaries, and domain walls, is also an important parameter for transistor application. In Fig. 2 (b), the case of 500 °C annealing has many defects, but the 550 °C annealing case has a lower defect concentration due to the sporadic grain. However, as the temperature increases further, the leakage current increases again, exacerbated by charge trapping as the domain walls and grain boundaries [15], [16]. Based on the above results, we concluded that 550 °C is the most optimized condition for having a perovskite phase that can have polarization characteristics with an allowable low leakage current. In addition, it is possible to have a stable process flow by avoiding the glass transition temperature around 600°C, which can give more diversity to choose the process substrate.

Fig. 2 (c) confirms the high residual polarization value ($P_r = 10\ \mu C/cm^2$) and the high coercive field value. These properties allow the PZT film to enable low-power operation in multiple oxide layers.

As shown in Fig. 2 (d), the current-voltage sweep of the memory window of PZT-TFT was verified well by the result of the hysteresis curve. A window in the counterclockwise direction is created due to the n-type channel material IGZO.

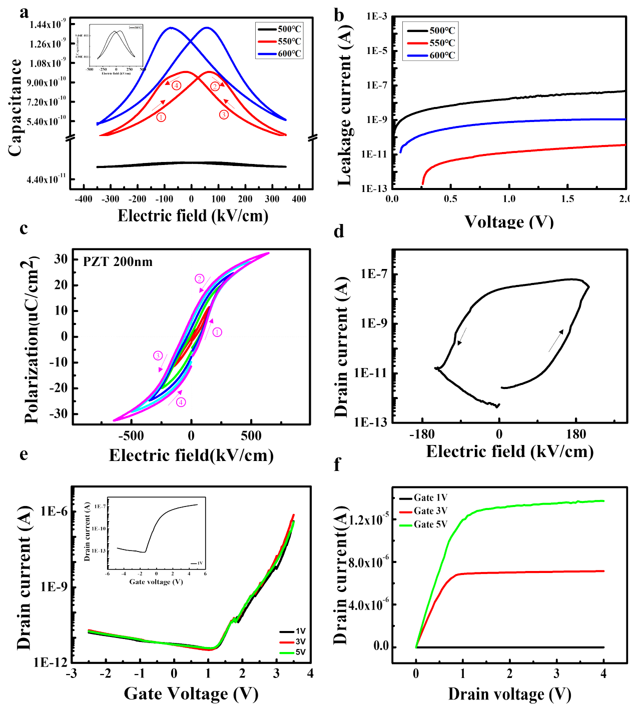

FIGURE 2. (a) Capacitance-Electric filed (C-E) characteristics of ferroelectric PZT at various temperatures with a frequency of 100 kHz. The inset is the 500 °C C-E characteristics. (b) Leakage current-voltage characteristics of ferroelectric PZT at various temperatures. (c) Polarization hysteresis measurements (1 kHz) of the Al/PZT/ITO stack reveal a characteristic sub-loop behavior when the bias sweep is increased. (d) Memory window hysteresis in the threshold slope measurement of Fe-FET. (e) IV characteristics of the Fe-FET (I_{DS} versus V_G) with SiO_2-TFT at V_{DS} = 1V. The inset is the SiO_2 dielectric FET IV characteristics. (f) Output characteristics of the Fe-FET (I_{DS} versus V_{DS}).

The transmission (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) characteristics show that the FE-TFT acts as a typical transistor (Figures 2 (e) and (f)). Fig. 2(e), when comparing SiO_2 base and PZT base, unlike SiO_2 based PZT base reaches on/off saturation value even in a narrow voltage range because saturation depends on the polarization characteristics of PZT. Additionally, differences in electrical properties including mobility, threshold voltage, and gate-leakage curves can be found in supplementary material S1,S2. Due to these characteristics, the I-V characteristics reveal that the gate voltage is more dominant than the drain voltage as in Figs. 2 (c) and (f). These low leakage currents and narrow voltage sweep range characteristics allow the device to be driven with low power.

The artificial ferroelectric synapse system was implemented to mimic synaptic-like biological behavior and may also be useful in psychology for implementing a model of human memory in the brain. It is believed that human memory is created by the dynamic change of neural circuits based on the synaptic connections, and it is accepted that some architecture for human memory exists in the brain, although its mechanism has not yet been fully elucidated. In 1968, Atkinson and Shiffrin proposed 'the multistore model' of human memory, which is still the most accepted model in psychology. In this model, new information from the external environment is stored for a very short time in the sensory register as a sensory memory (SM), and then selected information is transferred from temporary short-term memory (STM) in the short-term store to a permanent long-term memory (LTM) in the long-term store, as illustrated in Fig. 3 (a). Importantly, Atkinson and Shiffrin assumed that STM can become LTM through a process of rehearsal and that the probability of transfer to LTM increases with rehearsal repetition [17].

According to the psychological model of human memory proposed by Atkinson and Shiffrin, short-term memory and long-term memory functions are very important in mimicking biological human brain function in Fig. 3 (b). Ferroelectric materials can mimic brain function due to their coercivity and multi-domain polarization properties [18].

Fig. 3 (c) shows the excitatory postsynaptic current (EPSC) response model, which is similar to the operation of a transistor. This shows how conductance returns to its original state over time when a single pulse is applied to the device. This phenomenon is very similar to the weight change due to the synapse spike in biological brain function [19], [20]. A presynaptic spike applied to the gate electrode triggers an excitatory postsynaptic current in the IGZO channel. The increase in current can be interpreted as a change in channel conductance. The responses to a change in conductance are monitored at a small V_{DS} of 0.5 V in Fig. 3(d). The conductance shows a rapid increase after a presynaptic pulse is applied, and it reaches a peak value of $\Delta G \approx 60$. Then, it decays gradually to reach a resting conductance value, about $\Delta G \approx 4$ in 10 sec. Similarly, decayed excitatory postsynaptic conductance curves can be interpreted by the following equation:

$$G_{EPSC} = (G_{EPSC\cdot peak} - G_{EPSC\cdot\infty}) \exp\left[-(\frac{t-t_0}{\tau})^{\beta}\right] + G_{EPSC\cdot\infty} \quad (1)$$

where τ, t_0, $G_{EPSC-\infty}$, and β are the retention time, the time taken for the spike to be finished, the resting conductance state, and the stretch index ranging between 0 and 1, respectively [21].

The energy consumption is calculated as about 10 pJ with the expression $E_C = I_{peak} \times t_d \times V_{SD}$, where I_{peak}, t_d, and V_{SD} represents the peak value of the EPSC, the duration of the pulse voltage, and the source-drain voltage, respectively. Since the gate oxide of the three-terminal structure consists of ferroelectric material, the device can operate with very low power consumption. The energy consumption is lower than that of devices using other mechanisms [2], [22]–[24]. This device has the potential to reduce the power consumption exponentially when mimicking the synaptic density of a real brain.

Fig. 3 (e) shows a typical EPSC response of this synaptic transistor triggered by a series of presynaptic spikes (2 V, 300 ms). Due to the lower duration, the conductance value was changed to approximately $\Delta G \approx 10$ with the

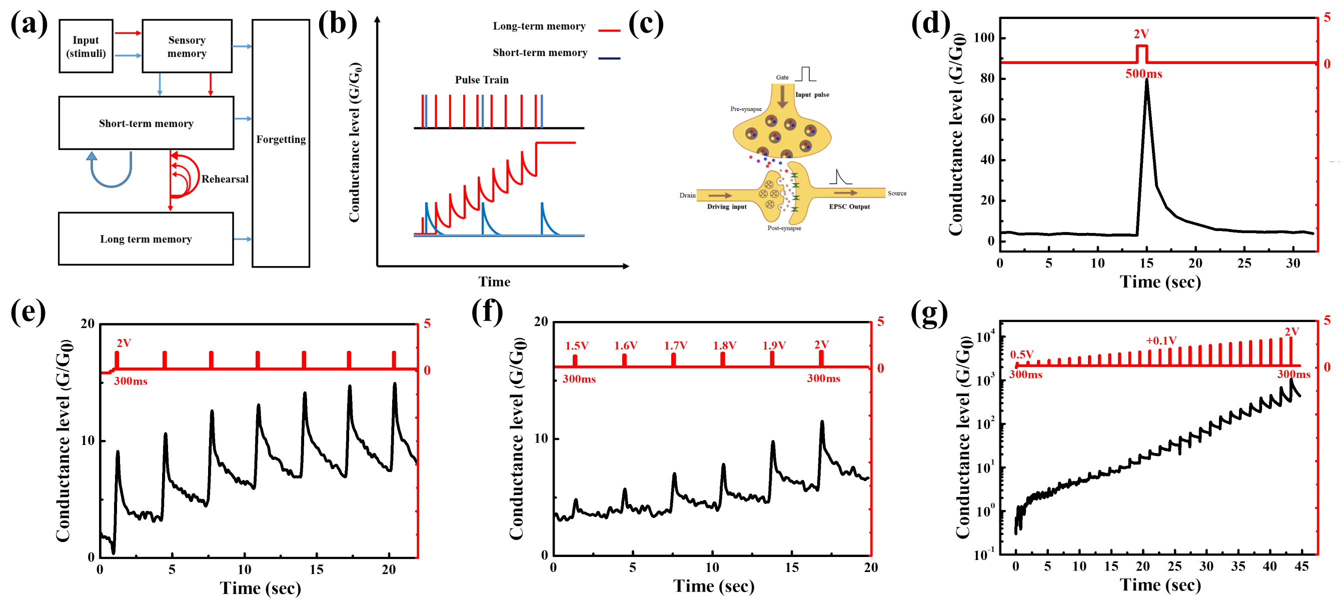

FIGURE 3. (a) The psychological model of human memory proposed by Atkinson and Shiffrin. (b) Simplified memorization model in the inorganic synapse, which was inspired by the multistore model. (c) Excitatory postsynaptic current (EPSC) response model of the schematics of three-terminal transistors. (d) EPSC triggered by a presynaptic spike (V_G = 2 V, t_d = 500 ms, V_{SD} = 0.5 V). (e) EPSC was triggered by a series of presynaptic pulses with the same duration (300 ms) and amplitudes (2 V). (f) EPSC was triggered by a series of presynaptic pulses with the same duration time (300 ms) and different amplitudes (1.5 V to 2 V) in the form of voltage increments of 0.1 V. (g) EPSC was triggered by a series of presynaptic pulses with the same duration (300 ms) and different amplitudes (0.5 V to 3.5 V) in the form of voltage increments of 0.1 V.

first pulse. Then, when the same pulse was applied continuously every 3 sec, it increased by approximately $\Delta G \approx 2$. However, when pulses were continuously applied with the same voltage, the conductance value became saturated. This is because the PZT dipoles aligned with the electric field generated by repeated pulses with constant amplitude became saturated.

Contrary to the previous result, in Fig. 3. (f), the conductance value continuously increased when the increment of the gate voltage was applied. In other words, to effectively control the polarization characteristics of ferroelectric PZT, an optimized pulse pattern should be used rather than a constant amplitude pulse. If a specific bias is first applied to a unidirectionally polarized ferroelectric film (in a random orientation state) at $t = 0$, then the converted polarization P(t) can be expressed using the following equation:

$$P(t) = P_s \left\{ 1 - 2\exp\left[-\frac{t}{t_s} \exp(-\frac{E_d}{V/d_{FE}})^n \right] \right\} \tag{2}$$

Here, P_r is the spontaneous polarization, E_a is the activation electric field, d_{FE} is the ferroelectric film thickness, n is a constant used to describe the nucleation mechanism, and t_S is the switching time for $V = d_{FE} \gg E_a$. According to Eq. (2), the polarization switching can be controlled continuously, e.g., by application of a voltage pulse with changing its amplitude. The partially switched state can be realized by applying a pulse gate voltage with a suitable duration and amplitude [25]–[27]. Therefore, to control STM conductance fully, frequency, as well as the voltage of the pulse, is important. In the case of Fig. 3 (g), when a series of the voltage increasing from 0.5 to 2 V is applied, it showed various levels of a conductance change rate. Through this, it is possible to create a more efficient neural network environment using various levels of STM values [28]. In addition, the level and operation of synapses can be optimized through pulse train engineering.

The memory retention of the PZT-based synapses corresponds with the commonly used forgetting curve $y = b \times t^{-m}$, where y, t, b, and m represent memory retention, time, the fitting constant for scaling, and the power function rate, respectively. Here, the power function rate "m" is a value relative to the retention time, where a lower decay rate represents a larger retention time. The retention time increases with the increasing duration or voltage amplitude of the spike [29]. Fig. 4(a) shows the degree of change of conductance according to voltage amplitude. After the Off state, the conductance level decreased slightly with time, but saturation occurs at a certain level. In other words, the saturation value in the Off state is determined according to the gate amplitude value. This satisfies the minimum condition (>5 multi-levels) of a neuromorphic device by having various conductance level values required for long-term memory by controlling the magnitude of the voltage if the pulse time is sufficient in the ferroelectric-based synaptic device. Fig.4 shows that the drain current levels were maintained to about 40000 s by up and down pulses. As shown in Figures, 4 (a) and (b), the LTM function can implement various levels according to the gate input voltage of the PZT based three-terminal device. With this characteristic, it is possible to imitate the behavior of the

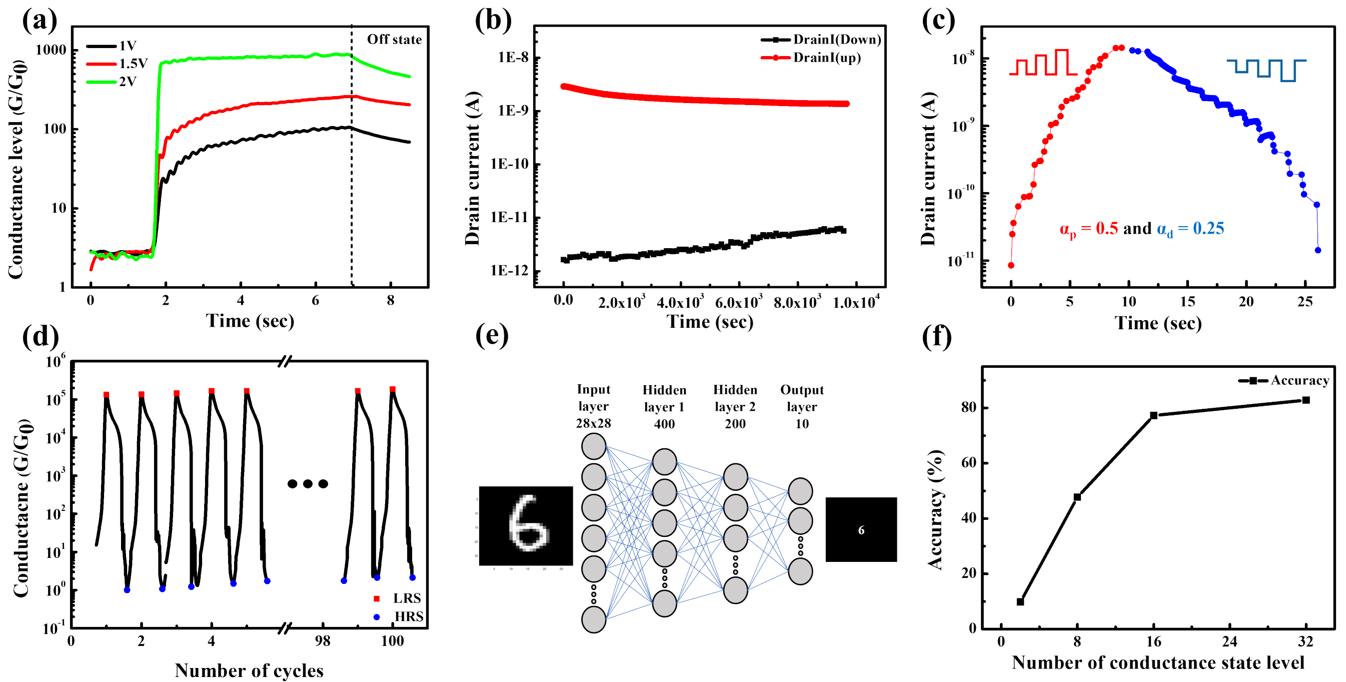

FIGURE 4. (a) LTM conductance level at various voltage pulses (1 V, 1.5 V, 2 V). (b) Retention test for 40000 s of the pulse with 3 V of magnitude and 300 ms of duration. (c) 32-level potentiation and depression in drain current curve at reading voltage V_{DS} = 0.5 V. (d) The endurance test through range (2.5 V to −2.5 V) direct voltage sweeps. (e) Schematic diagram of the three-layer neural network simulation. (f) The pattern recognition accuracy of the three-layer neural network simulation with multi-level capability.

brain with the difference in delay between the gate and source input signals [25]. Figure 4 (c) shows the current response to a series of 32 positive voltage pulses (0.5∼3.5 V, 300 ms, "P process") followed sequentially by 64 negative pulses (−0.5∼−2.5V, 300 ms, "N process"). Although the conductivity also increased (decreased) under the stimulation of consecutive positive (negative) pulses, a gap was observed between the final state of the "P process" and the initial state of the "N process". This gap is caused by the difference in interfacial properties due to the asymmetric structure and interfacial properties of IGZO/PZT/Al.

$$G = \begin{cases} ((G_{LRS}^{\alpha} - G_{HRS}^{\alpha}) \times w + G_{HRS}^{\alpha})^{1/\alpha}, & if\ \alpha \neq 0, \\ G_{HRS}^{\alpha} \times \left(\dfrac{G_{LRS}}{G_{HRS}}\right)^{w}, & if\ \alpha \neq 0. \end{cases} \quad (3)$$

where G_{LRS} and G_{HRS} are the low resistance state (LRS) and the high resistance state (HRS) conductance, respectively. α is a parameter that controls potentiation (α_p) or depression (α_d) characteristics and ω is an internal variable that ranges from 0 to 1. During learning, ω increases or decreases as potentiating (depressing) pulses are applied to the synaptic device. The potentiation and depression characteristics of the resistive-memory-based synaptic device model are concave-down if $\alpha > 1$ and concave-up if $\alpha < 1$. The closer the values of α_p and α_d are to 1, the more linear the devices are, which means the status of a synapse can be easily controlled with linear characteristics devices. Although $\alpha_p = 0.5$ and $\alpha_d = 0.25$, this device has great potential as a synaptic device because it can be sufficiently close to 1 through pulse engineering [30]. Figures 4 (d) confirmed that HRS and LRS states were maintained through repeated voltage sweeps. This result suggests that this device has the potential to perform well reading and writing operations in memory function.

To estimate the effect of the synaptic characteristics on the pattern recognition accuracy, as shown in Fig. 4 (e), we performed a simulation of a three-layer (input, hidden, and output layers) perceptron neural network using a hand-written digit dataset (MNIST). In the MNIST data, each image was classified as data by pixelating it 28 × 28. The number of neurons of the input, the 1_{st} hidden, 2_{nd} hidden, and output layer was 528, 400, 200, and 10, respectively. Each neuron was connected to all neurons in the next layer through the synapses, and the input neurons transmit signals to the next neurons through the conductance of the synapses. The back-propagation learning algorithm was used to update the weighting value of the synapse device, reflecting the characteristics of the synapse device, such as the linearity and the number of multi-levels of potentiation and depression. The pattern recognition accuracy increased as the multi-level capabilities increased, and the recognition accuracy was about 82.83% for the 32 levels mentioned in this letter.

IV. CONCLUSION

To achieve a high polarization value of Fe-FET with reliable performance, the PZT-IGZO TFT structure was

studied and optimized. Our study demonstrated that the incremental voltage scheme allowed for a gradual transition of more ferroelectric polarization domain regions, ensuring a wide range of residual polarization states. The manufactured Fe-FET synaptic device exhibited more than 32 analog states and modulated (potentiation and depression) conductance values using a variable amplitude pulse method with 300ms pulse width over a wide dynamic range of $G_{max}/G_{min} = 1000$. A neural network simulation based on conductance-change characteristics measured experimentally was also performed. The accuracy of MNIST handwritten number recognition was estimated at 82.83%. This study confirmed that ferroelectric-based devices have potential in the neuromorphic field. We demonstrated a ferroelectric-field-effect transistor for mimicking the human brain system and low power operation. High dielectric constant and polarization characteristics of $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) allowed a high remnant polarization value ($P_r = 10\ \mu C/cm^2$), which resulted in very low power consumption for excitatory post-synaptic potential (EPSC). Compared with a two-terminal structure, the PZT transistor performed neural network learning and signal processing simultaneously due to its unique three-terminal structure. The spike signal used in spike dependent plasticity change was about 10 pJ, which enabled low power in a large-scale parallel structure. The basic operations of synapses, short-term memory (STM), and long-term memory (LTM) were confirmed, as well. Moreover, a wide dynamic range of $G_{max}/G_{min} \cong 1000$ was obtained, and the channel conductance was maintained over 40000 seconds. The optimized pulse achieved multi-level states (>32), which led the learning process efficiently. The increase in reliability of cognitive ability due to the multiple levels of the device was proved by the simulation process. The above results show that this device has potential in neuromorphic engineering.

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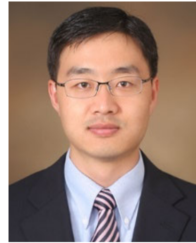

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