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Reliability Study of Miniaturized Surface Acoustic Wave RF-Filters With Copper Pillar Bump Interconnections

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ABSTRACT Microacoustic radio frequency filters are essential electronic components for all devices using wireless communication. For miniaturization and cost reduction it is necessary to further reduce the area for the electrical contacts on the chip. CPB (copper pillar bump) interconnections on radio frequency filters can release valuable chip design area of up to 26 % compared to standard SB (solder bump) interconnections on a Qualcomm TFAP (Thin Film Acoustic Package). We developed a process to deposit CPB interconnections on microacoustic radio frequency filters. A 1.20 mm × 1.60 mm SAW (surface acoustic wave) LTE (Long Term Evolution) band 26 duplexer with a height of 0.20 mm including the CPB interconnections was investigated. Unbiased highly accelerated stress test, damp heat steady state, dry heat, and temperature cycling reliability tests have shown that the new interconnection technology fulfills the reliability requirements of the smart device industry. Two failure modes caused by extended temperature cycling were identified via scanning acoustic microscopy and scanning electron microscopy analyses on cross sections.

INDEX TERMS Cu pillars, electronics packaging, component reliability, mobile communication, SAW, Qualcomm TFAP.

I. INTRODUCTION

In our globally connected world, the volume of mobile network data transfer increased around 46 % from Q1 2020 to Q1 2021 according to the Ericsson Mobility Report [1]. Thus, the demand for electronic components in devices like smartphones, which use mobile data communication as one of their main features, steadily increases. The key elements for transmission and reception of mobile data in defined frequency bands are RF-filters (radio frequency filters) like SAW (surface acoustic wave) filters and BAW (bulk acoustic wave) filters along with other electronic components. These RF-filters use a piezoelectric material to generate mechanical waves from an electrical signal. Only a specific frequency band is converted back into an electrical signal with low attenuation, which can be determined by the filter design. All smartphones can communicate in multiple frequency bands to achieve high data transfer rates, long transmission distances and international usability, which requires dozens of filters in such a device [2].

The demand for today's consumer devices is increasing and so do the number and complexity of built-in RF-filters. To satisfy customer demands, the industry is striving for further miniaturization of microelectronic components, including RF-filters. In the last two decades, packages for SAW- and BAW-filter components have been miniaturized by 99 % in volume [3], [4].

Besides space savings, miniaturization can reduce manufacturing costs. RF-filters are processed on wafer level; thus, miniaturization leads to more filters per wafer. This can reduce the manufacturing costs for a single RF-filter, but only if yield loss and additional process costs generated by miniaturization do not use up the benefit. Therefore, the industry's goal is to implement innovations for miniaturization in mass production, while fulfilling the requirements for electrical device performance and reliability.

Like most micromechanical and microelectronic structures RF-filter structures also need a package as protection against

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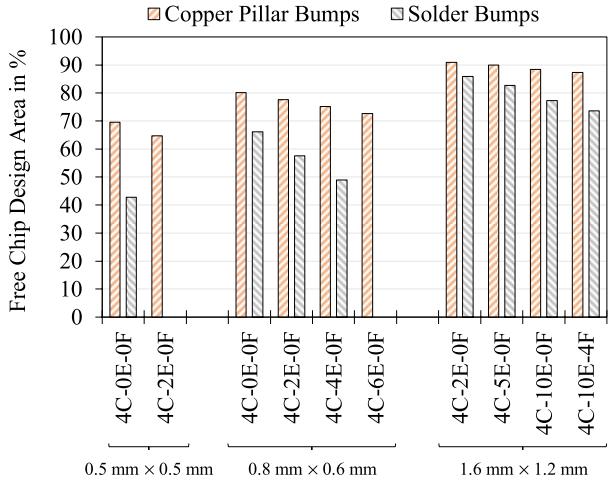

FIGURE 1. Chip area saving potential of CPBs: The percentage of free chip design area on SAW RF-filters with a TFAP is shown as a comparison between CPB and SB interconnections. The configuration is defined by chip size and the interconnection position, where C = corner position, E = edge position, and F = middle position on a SAW RF-filter chip. The preceding digit equals the number of interconnections at the corresponding position. A missing column indicates that the chip design is not possible at all.

environmental impacts. As a special feature, microacoustic RF-filter packages must provide a cavity above the filter structures. The cavity ensures undisturbed formation and propagation of surface or bulk acoustic waves. TFAP (Thin Film Acoustic Package) technology provides this cavity and is moreover one of the thinnest commercially available package solutions for BAW and SAW RF-filters. Standard TFAP technology uses SBs (solder bumps) as electrical interconnection to the PCB (printed circuit board) after flip chip assembly. The RF-filter structures and the SBs are on the same chip side; hence interconnections consume valuable chip space. Unfortunately, further SB miniaturization on TFAP is limited by the required gap between RF-filter and PCB for molded underfill after flip chip assembly. That is because SBs are spherical, and a further miniaturization would no longer result in a sufficient gap height for molded underfill.

One solution for further device miniaturization was shown in [5] and [6] by using CPBs as interconnection for RF-filter devices. CPBs consist of a Cu column and a spherical Sn-Ag solder cap on top. A thin Ni diffusion barrier layer between Cu and Sn-Ag is optional. Compared to SBs the CPB interconnections have a smaller footprint on the chip, which saves valuable chip area. Furthermore, CPBs allow smaller pitches between interconnections, which gives more freedom for RF-filter design. The gap height for molded underfill between the RF-filter and the module substrate can easily be adjusted by the CPB Cu base height. Better electrical reliability of CPBs compared to SBs was supposed in [7]. The potential of saving chip area by using CPBs instead of SBs on TFAP following present design rules is illustrated in Fig. 1. It shows the remaining chip area in percent useable for package and filter structures depending on chip size, amount, and position of interconnections. CPBs have a high chip area saving potential, particularly for small chip sizes. Furthermore, CPBs facilitate higher connection density on TFAP compared to SBs. This even allows new designs, which are not feasible with SBs.

Structure and material composition of CPBs and SBs are fundamentally different; thus, examining the RF-filter reliability in terms of industry standards is essential. We already published promising reliability results of TFAP technology with CPBs in [8]. However, due to poor soldering and unsuitable sample preparation for failure analysis, it was not possible to make a final statement on the suitability of the CPBs on TFAPs as interconnections.

The results shown in this publication are based on our previously published work in [8]. By improving the assembly process and the failure analysis, a detailed understanding of the reliability of TFAP RF-filters with CPB interconnections was achieved. Additionally, we describe the geometry, manufacturing processes, the material composition of our CPB interconnections, and the corresponding test vehicle. The test vehicles investigated included daisy chain components and functional SAW-filters with design variations at the CPB interconnections. TC (temperature cycling at −40 °C / +125 °C, air, 15 min dwell), uHAST (unbiased highly accelerated stress test at 130 °C, 85 % RH), DHSS (damp heat steady state at 85 °C, 85 % RH) and DH (dry heat at 150 °C) reliability tests were performed. The potential failure mechanisms were identified and are discussed in this study.

II. TEST VEHICLE–PROCESSING AND MATERIALS

Our test vehicles included daisy chain components and SAW RF-filters with TFAP technology and CPB interconnections. The substitution of SBs by CPBs generates a 7 % gain of free chip design area for our particular test vehicle.

Both daisy chain components and functional SAW RF-filters were tested on appropriate PCB boards. The daisy chain components had no RF-filter function but could loop an electrical current through all interconnections. A failure was detected if the electrical circuit was interrupted. This allowed detecting primarily failures in the interconnection rather than in the package or the RF-filter structure. In-situ failure detection during TC reliability testing was performed for daisy chain components by monitoring the electrical resistivity. The investigated functional SAW RF-filters are duplexer systems and support the LTE Band 26 uplink frequency of 814-849 MHz and downlink frequency of 859-894 MHz for frequency division duplexing. The functional RF-filters are built up in a test vehicle environment, which was not optimized in terms of radio frequency characteristics. All chip variations including daisy chain components and functional RF-filters followed the same manufacturing steps due to a multi design wafer layout.

A. RF-FILTERS AND TFAP TECHNOLOGY

The investigated daisy chain and functional components have a size of 1.20 mm × 1.60 mm with a height of 0.20 mm including the CPBs. Fig. 2 a) shows a completely processed

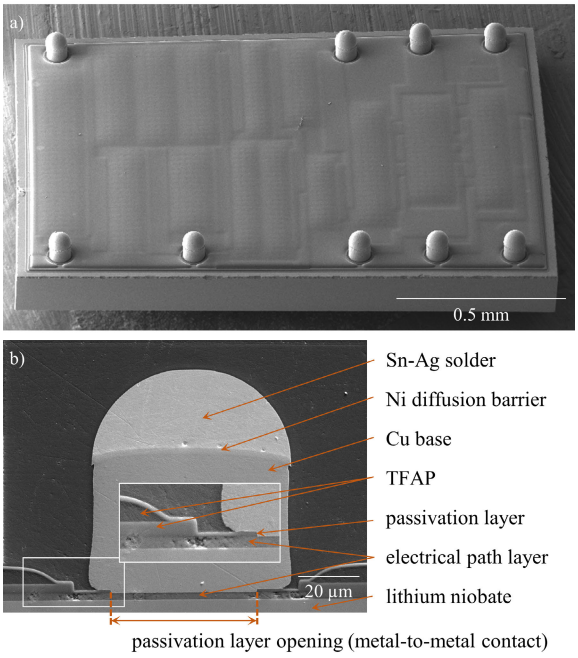

FIGURE 2. In a) SEM image of fully processed SAW RF-filter chip with CPBs and in b) cross sectional SEM image of a CPB. The area of the white frame is magnified in the inset. The peculiarities in the electrical path layer are caused by cross section preparation.

chip with TFAP technology and CPB interconnections. Nine unevenly distributed CPBs on each chip provide the electrical interconnection. The uneven distribution and a potentially larger chip size may be more prone to interconnection failure due to the difference in mechanical load on each CPB induced by reliability testing and it was therefore the preferred layout. The highest mechanical stress can be expected on the stand alone CPB in the upper left chip corner shown in Fig. 2 a) during TC. The CPBs in our test vehicle consist of a material layer stack made of a cylindrical Cu base with a height of approx. 47 μm, a 3 μm thick Ni diffusion barrier and a Sn-Ag solder cap with a height of approx. 25 μm. The CPB diameter is 65 μm. A cross-sectional SEM image of the CPB layer stack and the surrounding TFAP topology is illustrated in Fig. 2 b). The TFAP causes a package induced topology of up to 20 μm. TFAPs are constructed as a 3-layer material stack by using a sacrificial layer and are manufactured at wafer-level. First, the sacrificial layer is deposited on the RF-filter structures. Then the capping layer is applied on the sacrificial layer and the sacrificial layer is subsequently removed through holes in the capping layer. Hereafter a sealing layer followed by a reinforcement passivation layer is deposited. This creates a sealed air cavity over the RF-filter structures, which completes the TFAP. Further details of TFAPs can be found in [4].

For this study, we tested 4 different test vehicle setups including one functional (fc) SAW RF-filter design and three different daisy chain (dc) component designs. The relation between design, functionality and the resulting chip name is illustrated in Fig. 3. A, B and C represent the corresponding designs, which differ by the metal-to-metal contact area of the

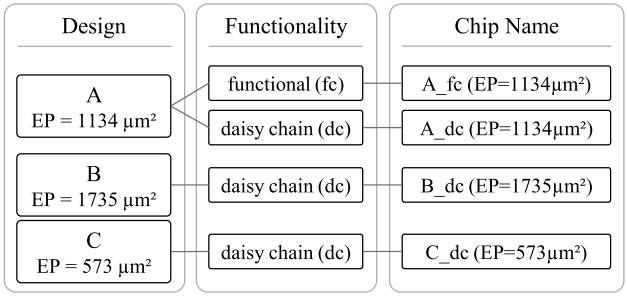

FIGURE 3. Chip design variations and functionalities. EP = electrical path contact area to CPB Cu base. Design B has the largest and Design C the smallest metal-to-metal contact area. EP value of design A is between B and C. B and C are only tested as daisy chain version. Design A is tested as functional SAW RF-filter and daisy chain component. CPB diameter is always 65 μm.

CPB Cu base to the electrical path (EP) layer. The contact area is specified by the opening diameter of the passivation layer, which is on top of the EP layer and is indicated in Fig. 2 b).

B. COPPER PILLAR BUMPS MANUFACTURING

CPBs were processed after TFAP manufacturing at wafer-level, directly on the EP layer openings. The EP layer area is defined by the passivation openings shown in Fig. 2 b) and provides the metal-to-metal connection between the EP layer and the CPB Cu base. The CPB overlaps with the passivation layer to prevent the exposure of the EP layer to the environment. The CPB processing steps are schematically illustrated in Fig. 4. At first surface oxides are removed on the EP layer openings by dry etch, directly followed by the deposition of a 50 nm thick Ti and 200 nm thick Cu seed-layer on the whole wafer. This serves as an electrically conducting layer for the later electroplating metal deposition. Positive tone thick film photolithography is performed to achieve a resist thickness of at least 80 μm above the EP layer openings by a single coat.

The use of positive tone resist prevents resist cross linking in the intended resist openings, because the surrounding TFAP topology is not exposed to UV light during exposure with a mask aligner. In contrast, thick film lithography with negative tone resist shows significant cross linking caused by scattered light from surrounding topology for this TFAP and CPB combination and is therefore not suitable. A commercial TMAH (tetramethylammonium hydroxide) based developer is used. The exact spin coat recipe, the impact of resist bake temperature and duration, and the development process on the resist opening shape and diameter is described in our previous work [9]. This publication also describes the significant impact of the required plasma cleaning after resist development on the adhesion of the electroplated Cu to the underlying Cu seed-layer.

Commercial electroplating bath compositions and a fully automated tool are used for electroplating the CPB metal layer stack of Cu, Ni, and Sn-Ag into the resist openings. The resist is then removed by a wet batch process. Seed-layer etching is also performed with multiple wafers

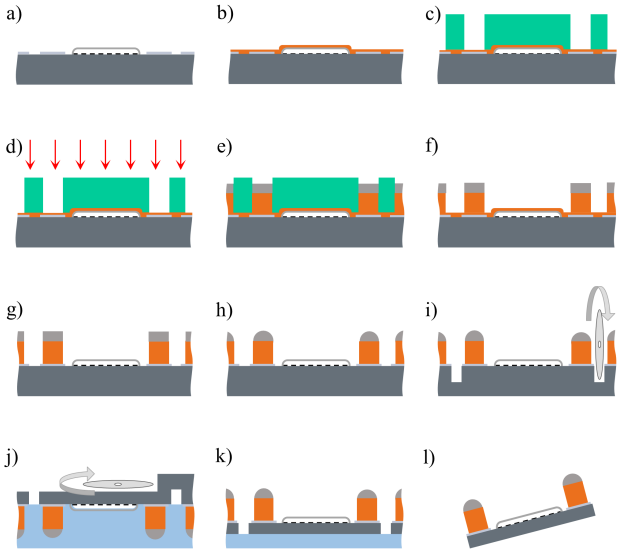

FIGURE 4. Schematic cross section of CPB manufacturing. Dimensions are not to scale. In the graph one exemplary SAW RF-filter cross section area on the wafer and parts of two bordering RF-filters are illustrated. In a) fully processed TFAP with open EP area for CPBs. In b) seed-layer sputtering Ti/Cu. In c) structured thick film photoresist. In d) plasma cleaning. In e) electroplating of Cu/Ni/Sn-Ag metal stack. In f) resist removal. In g) seed-layer etch of Cu/Ti. In h) CPB solder cap reflow. In i) dicing before grinding. In j) backside grinding. In k) singulated dies on frame. In l) dies ready for tape & reel.

simultaneously in a wet batch process. The etch process causes only a minor radius loss of less than 1 μm at the CPB Cu base and a Ti under-etch below 1μm. The spherical Sn-Ag solder cap is created by a wafer reflow under formic acid atmosphere or by applying flux and reflowing in a furnace under nitrogen atmosphere. The lithium niobate wafers are then half cut diced at the front side and transferred face down into a grinding foil before grinding the backside until singularization. The singulated wafer is transferred on a frame and specific chip designs are taped for assembly.

C. PCB, STENCIL PRINTING AND ASSEMBLY

For our test vehicle we used a standard FR4 multilayer PCB. ENIG (electroless Ni, immersion Au) was used as landing pad finish. Solder mask resist openings had a size of 120 μm $\times$ 80 μm but the actual landing pad size on the PCB was only 100 μm $\times$ 80 μm. This was due to the shape of the metal pad, which is a trace with a width of 100 μm. Therefore, 2 sides of the landing pad were solder mask defined and the other 2 sides were defined by the trace width.

There was a specific PCB design for each functionality. For daisy chain components the electrical path was routed alternatingly between PCB and each chip through all CPB interconnections one after the other. A resistivity measurement allowed detecting an interruption of the electrical circuit, which corresponded to a CPB interconnection failure. For functional SAW RF-filters the PCB design facilitated the electrical characterization of each SAW RF-filter by a network analyzer to allow a comparison prior and after reliability testing.

As already mentioned in the introduction, in our former publication [8] poor solderability was discovered to be the root cause for premature failures in TC reliability testing. In this study, we achieved very good solderability and even self-centering behavior of the assembled components by applying solder paste on the PCB via stencil printing prior chip assembly. The solder paste was printed using a 40 μm thick stencil with 100 μm $\times$ 80 μm rectangular openings. The solder paste was a commercial SAC305 (ROL0, type 5 powder) no-clean and halogen-free solder paste.

The components were assembled with laboratory equipment via flip chip placement on the PCB boards after solder paste stencil printing. Directly after assembly the soldering process was performed in a conventional 3-zones reflow furnace with nitrogen flush and a peak temperature of approximately 250 °C. The time above liquidus temperature was 80-90 seconds. Only prior uHAST and DHSS reliability testing a flux cleaning with an automated tool and a commercial flux cleaner was performed.

Usually the SAW RF-filters with a TFAP are mechanically supported by a molded underfill after assembly. In our test vehicles the components were kept open top, i.e. no molded underfill was applied. The missing underfill makes the components more susceptible to failures and permits to identify possible flaws in our design at an earlier stage. Our experience with similar builds shows that the reliability results of molded components compared to open top components are better by several factors especially for TC.

III. RELIABILITY TESTING

We performed standard reliability tests, which are typically required by the industry for SAW RF-filter components. For daisy chain components only a simple resistivity measurement was performed to approve functionality. However, the functional SAW RF-filters were tested for multiple parameters, e.g. insertion loss and frequency shift.

As a precondition all test vehicles were placed in a chamber with 60 °C / 60 % RH for 120 hours followed by 6 additional reflows, corresponding to the JEDEC Standard "moisture sensitivity level 2a" (MSL 2a). Functionality was tested prior and after preconditioning.

The TC reliability test was performed in a dual chamber with moving platform between −40 °C / +125 °C, both in air with a dwell time of 15 minutes each. Therefore, one temperature cycle took 30 minutes. As mentioned in the previous chapter, for the daisy chain components the electrical path was routed alternatingly between PCB and component through all CPB interconnections one after the other. Furthermore, all mounting spaces on the PCB are in series and each one has its own parallel 1 kΩ resistor. In case of a failure of a CPB interconnection the measurement current flows solely through the parallel resistor. As a consequence, the resistance of the whole measurement loop is increased by approximately 1 kΩ. Hence, the overall test vehicle resistance changed by incremental steps of 1 kΩ for each component failed. This facilitated an in-situ failure detection during TC

by a simple electrical resistivity monitoring of the whole PCB. For functional SAW RF-filter duplexers the impedances of the ports were roughly matched to 50 Ω by SMD (surface mounted device) inductors, which were also soldered to the PCB. The functional SAW RF-filters were measured by a network analyzer after a defined number of TCs (temperature cycles) and then placed back into the chamber.

Further reliability tests were uHAST at 130 °C / 85 % RH, DHSS at 85 °C / 85 % RH, and DH at 150 °C. The respective duration times are mentioned in the results chapter. Both daisy chain and functional components were tested after a defined duration time for uHAST, DHSS, and DH, i.e. here no in-situ measurements were performed.

IV. RELIABILITY RESULTS, FAILURE ANALYSIS, AND DISCUSSION

A. ASSEMBLY AND MULTIPLE REFLOWS

The assembly was directly performed after solder paste printing. A standard laboratory pick and place flip chip assembly tool was used. The components were fed to the assembly tool via tape. The laboratory assembly tool did not meet the required high placement accuracy, which arose due to the small size of the landing pad of 100 μm × 80 μm, the PCB manufacturing fluctuations and the 65 μm CPB diameter. However, the solder paste led to self-centering, which moved the assembled components precisely to the correct position on the PCB during reflow. No failures were caused in our test vehicles by MSL 2a preconditioning including 6 additional reflows. Nevertheless, the objective is to increase the PCB manufacturing accuracy and to use pick and place machines with higher placement accuracy.

B. TEMPERATURE CYCLING

TC induces repetitive mechanical stress into the test vehicle due to the mismatch of the coefficients of thermal expansion (CTE) between the different materials. The materials that contribute most to the CTE mismatch are the PCB with a CTE of approx. 16 ppm/K and the chip material which is lithium niobate. Lithium niobate has an anisotropic thermal expansion. The thermal expansions along the x-, y- and z-direction depend on the angle of the cut when separating the wafer from the ingot. For this work chips with an in plane CTE of 12 ppm/K in the direction along the long chip side and 15 ppm/K in the direction along the short chip side were used. In Fig. 5 the failures detected during TC at −40 °C / +125 °C are shown as a Weibull probability plot. The component sample size for each TC test vehicle was 146 for design A_fc(EP = 1134μm^2), 98 for design A_dc(EP1134μm^2) and B_dc(EP = 1735μm^2), and 49 for design C_dc(EP = 573μm^2). The functional test vehicle with components of the design A_fc(EP = 1134μm^2) was measured after 480x, 816x, 1008x, 1488x and 2016x TCs by a network analyzer. For daisy chain test vehicles, the electrical resistivity was monitored during TC and each incremental resistivity change of 1 kΩ was considered as one failed component. Functional test vehicles were subjected to much stricter criteria by comparing the electrical performance after reliability to the initial specified one. For all test vehicles the CPB diameters of 65 μm and the solder volumes were the same within the process fluctuations. It can clearly be seen in Fig. 5 that the metal-to-metal contact area has a significant influence on the TC reliability. C_dc(EP = 573μm^2) had the smallest contact area and resulted in the poorest TC reliability, whereas A_dc(EP = 1134μm^2) and B_dc(EP = 1735μm^2) showed a fairly comparable TC reliability. All three were daisy chain test vehicles and therefore directly comparable. Test vehicle A_fc(EP1134 = μm^2) is equal in the metal-to-metal contact area to A_dc(EP = 1134μm^2), but a functional design and therefore much more sensitive to failure. This explains the parallel shift in the Weibull probability plot.

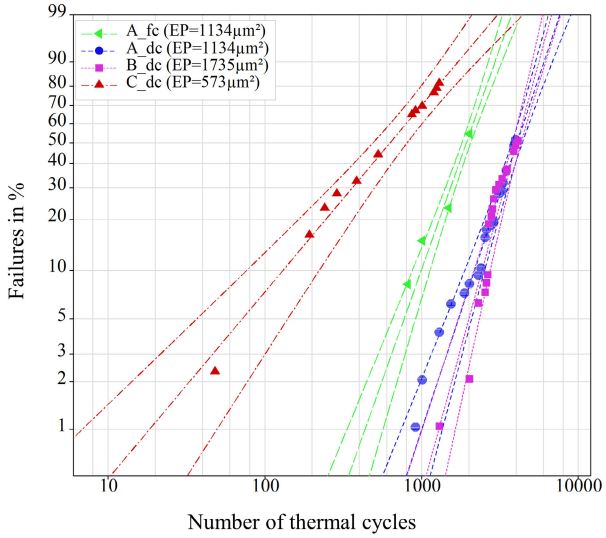

FIGURE 5. Weibull probability plot of temperature cycling at −40 °C / +125 °C in air with 15 min dwell time. Test vehicle was open top, i.e. components are soldered to PCB and no underfiller is applied. 4 different test vehicles were investigated, which differ in the metal-to-metal contact area of CPB Cu base to electrical path (EP) layer and their functionality of either daisy chain (dc) or functional (fc) type. 90 % confidence interval is indicated.

Multiple components were analyzed by optical microscopy inspection of mechanical cross sections and C-SAM (C-mode scanning acoustic microscopy) imaging after TC. Analysis revealed two different failure modes, which were responsible for component fatigue. The first mode was a crack through the bulk Sn-Ag solder as illustrated in Fig. 6 a). The second failure mode was a crack in the EP layer below the CPB Cu base and is shown in Fig. 6 c). C-SAM analysis allowed the detection of cracks or delamination by showing white areas in the image of the horizontal plane of interest. For our test vehicle the C-SAM focus was set at the horizontal plane of the EP layer as shown in Fig. 6 b) and d). C-SAM is not able to detect cracks in the bulk solder.

Beside the crack in the solder or in the EP layer we could not detect any delamination of CPBs at the metal-to-metal contact area or at the substrate interface. This indicates a strong adhesion between the individual layers. However,

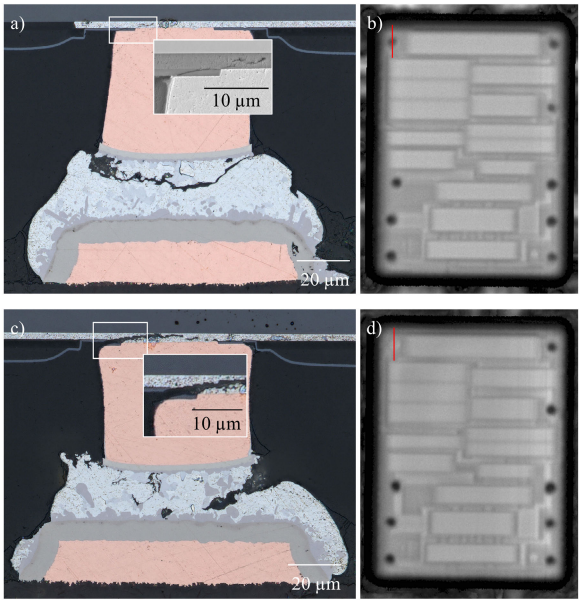

FIGURE 6. Failure modes detected after temperature cycling. In a) cross sectional optical microscope image of crack through the bulk Sn Ag solder as the first failure mode. The SEM image inset illustrates the crack through passivation layer and the beginning of crack formation in the electrical path layer. b) shows the top view C SAM image of the corresponding chip in a) prior cross sectioning. Red line in b) indicates cross section level of a). In c) crack in electrical path layer is shown as second failure mode with magnified area as inset. d) shows the C SAM image of the corresponding chip in c). White bump area indicates crack or delamination in electrical path layer level. Red line in d) indicates cross section level of c).

a crack in the passivation layer as shown in the inset of Fig. 6 a) was often already present in the early stage of TC. The crack in the passivation layer was typically accompanied by a delamination of the passivation layer from the underlying EP layer, indicating poor adhesion between both layers. This delamination can clearly be detected by the C-SAM, as the original shape of the dark round area of the CBP position then appeared with a smaller size or deformed shape. Cross section analysis confirmed the detected delamination of the passivation layer with C-SAM. The delamination probably had no impact on the electrical performance of the SAW RF-filters as the metal-to-metal contact area was not affected in the early stage of TC. However, possible crack formation and propagation into the EP layer always started from the delaminated passivation layer.

To understand which failure mode was the dominant one in each design, a C-SAM analysis was performed after TC at each test vehicle. The dominant failure of the design C_dc(EP $= 573\mu m^2$) was a crack in the EP layer, which affected multiple CPBs on almost every chip after 1500x TCs. 37 % of the components within the design B_dc(EP $= 1134\mu m^2$) were discovered to have a complete EP layer crack after 4000x TCs. In comparison, only 6 % of the components within the design C_dc(EP $= 1735\mu m^2$) had a complete crack through the EP layer after 4000x TCs. These results indicate that a complete crack through the EP layer below the CPBs was more likely, the smaller the metal-to-metal area of the CPB Cu base to EP layer was and the larger the overlap of the

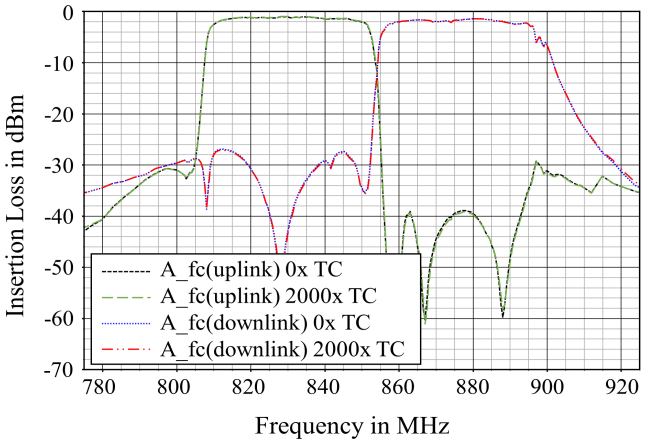

FIGURE 7. Graph shows the insertion loss measured against the frequency of one representative SAW RF-filter LTE band 26 duplexer after assembly and after 2000x temperature cycles (−40 °C / +125 °C, air, 15 min dwell) including MSL 2a preconditioning with 6 additional reflows as a comparison. No significant change could be detected for still functional SAW RF-filters. Only a rough impedance matching of the SAW RF-filter duplexer was performed with SMD inductors.

CPB and the passivation layer. A crack and delamination of the passivation layer probably creates a mechanical lever if the CPB experiences mechanical force sideways during TC, which magnifies the potential stress at the corner of the metal-to-metal interface between CPB and EP layer. This might also promote the crack formation and propagation in the EP layer.

Even measuring in-situ did not allow us to identify a specific failed chip during TC or to detect the reason for the failure. However, to understand, which failure mode occurred first during TC, an additional test series was set up. Therefore, 14 components with the design A_dc(EP $= 1134\mu m^2$) were assembled on each of the 6 individual PCBs followed by MSL 2a preconditioning including 6 additional reflows. Afterwards, the test vehicles were stressed with 432x, 672x, 1008x, 1344x, 1680x, and 2016x TCs, respectively. C-SAM analysis followed and revealed that only 1 component was detected with a complete crack in the electrical path layer at 1344x TCs. However, a significant size and shape change in the C-SAM images could be noticed on some components, indicating an already initiated crack formation. This could already influence the electrical performance. As mentioned earlier, in the same design 37 % of the components were affected by a complete crack in the electrical path layer after 4000x TCs.

Based on the results and analyses described previously, the dominant failure mode for design C_dc(EP $= 573\mu m^2$) was a complete crack in the EP layer. For the designs A_dc(EP $= 1134\mu m^2$) and A_fc(EP $= 1134\mu m^2$), which only differ in functionality, the crack in the bulk Sn-Ag solder and the crack in the EP layer probably overlapped as failure modes. The design B_dc(EP $= 1735\mu m^2$) probably had the crack in the Sn-Ag solder as dominant failure mode but this did not result in a significantly better TC reliability. Fig. 7 shows the insertion loss and frequency plot of one still functional SAW RF-filter duplexer from our test vehicle as a comparison prior and after 2000x TCs.

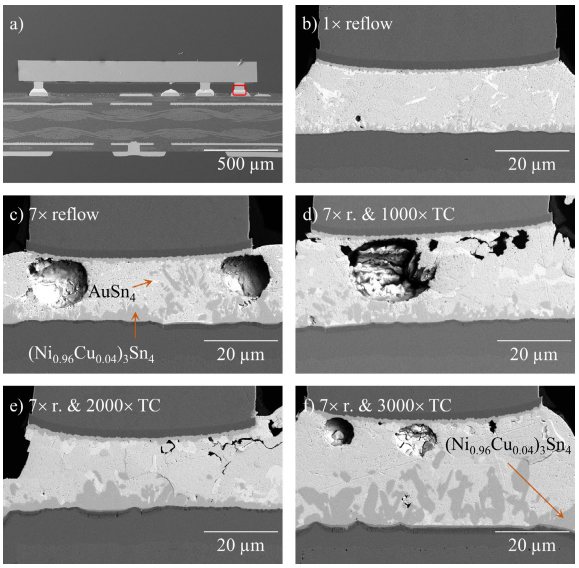

FIGURE 8. Cross sectional SEM images with BSE detector of CPBs soldered to ENIG laminate to evaluate IMC growth during temperature cycling. a) shows exemplary cross section overview. In all cross-section images, the in a) tagged pillar position was examined. b) only with 1 reflow after assembly. c) preconditioned with MSL 2a including 6 additional reflows. d), e) and f) preconditioned and additional temperature cycles. Large voids are due to manufacturing and assembly process. Bright areas in the solder material have a high Au content.

Multiple reflows and TC cause the formation of intermetallic compounds (IMC) between the Sn-Ag solder and the adjacent Ni layers. Fig. 8 shows the growth of the IMC during TC. The IMC thickness increased with the number of TCs. EDX (energy-dispersive X-ray spectroscopy) suggested $(Ni_{0.96}Cu_{0.04})_3Sn_4$ as the main IMC. The result of the IMC EDX analysis in Fig. 8 c) indicates a content of 38.3 at.% Ni, 1.7 at.% Cu, 2.1 at.% Ag, 57.7 at.% Sn, and 0.2 at.% Au. The result of the IMC EDX analysis in Fig. 8 f) indicates a content of 40.4 at.% Ni, 1.7 at.% Cu, and 57,9 at.% Sn. We observed a faster IMC growth rate on the ENIG PCB side compared to the one at the electroplated Ni side of the CPB. Au rich $AuSn_4$ compositions are illustrated as bright areas in the SEM images. However, even after 3000x TCs there are still bulk Sn-Ag solder material and a Ni diffusion barrier left. Significant voiding due to IMC growth was only present in the phosphor enriched electroless Ni layer at the PCB side and is discussed more in detail in the next chapter.

C. uHAST, DHSS, AND DH

The uHAST, DHSS, and DH reliability tests do not exert cyclic mechanical stress on the CPB interconnections like TC. However, they can easily induce aging and corrosion processes at the interconnections and below the package unless hermetically sealed. All test vehicles were tested open top, i.e. no underfilling was performed prior testing. In Table 1 the reliability results are shown for the design variations tested. Each test vehicle was tested with 49 components. No failures were detected during testing in the given test duration for functional and daisy chain components. The column ''1x reflow'' in Table 1 represents the reflow after assembly and

TABLE 1. Reliability test results. Percentage of passed components.

Design & Test	1x Reflow	7x Reflow	144 h	504 h	2016 h
A_fc DH 150 °C	100 %	100 %	100 %	100 %	n.a.
A_dc DH 150 °C	100 %	100 %	100 %	100 %	100 %
B_dc DH 150 °C	100 %	100 %	100 %	100 %	100 %
A_fc uHAST 130 °C 85 % RH	100 %	100 %	100 %	n.a.	n.a.
A_dc uHAST 130 °C 85% RH	100 %	100 %	100 %	100 %	n.a.
B_dc uHAST 130 °C 85 % RH	100 %	100 %	100 %	100 %	n.a.
A_fc DHSS 85 °C 85 % RH	100 %	100 %	100 %	100 %	n.a.
A_dc DHSS 85 °C 85 % RH	100 %	100 %	100 %	100 %	100 %
B_dc DHSS 85 °C 85 % RH	100 %	100 %	100 %	100 %	100 %

the column ''7x reflow'' represents the MSL 2a preconditioning including 6 additional reflows.

The results indicate, that the CPBs and the TFAP were not sensitive to aging or corrosion effects affecting the SAW RF-filter functionality. In Fig. 9 the insertion loss against frequency of one representative SAW RF-filter LTE band 26 duplexer is illustrated prior and after 144 h uHAST reliability testing. No significant change was detected for any of our uHAST, DHSS and DH test vehicles. Multiple reflows and the increased temperature during a DH reliability test cause the formation of IMCs in the interconnection solder region. The IMC formation can be critical for reliability and was therefore assessed for DH testing at 150 °C. Cross sectional SEM analysis was performed after different DH duration times as illustrated in Fig. 10. IMC growth is clearly noticeable and EDX analysis suggested $(Ni_{0.96}Cu_{0.04})_3Sn_4$ as the main IMC after preconditioning as shown in Fig. 10 b). The result of the IMC EDX analysis in Fig. 10 b) indicates a content of 38.3 at.% Ni, 1.7 at.% Cu, 2.1 at.% Ag, 57.7 at.% Sn, and 0.2 at.% Au. As already observed for TC, in DH the IMC growth rate is faster on the electroless Ni at the ENIG substrate pad side. We detected a pronounced laminar-like voiding in the electroless Ni layer. The inset of Fig. 10 b) shows a magnified void area. Phosphor enrichment was detected by EDX and the former $Ni + Ni_3P$ layer transformed into a phosphor enriched Ni_3P layer. A similar behavior of the electroless Ni layer was observed by [10]. However, further EDX analyses revealed a copper rich $(Cu_{0.59}Ni_{0.41})_6Sn_5$ IMC layer after 2016 h DH at 150 °C, which is illustrated in Fig. 10 f). The result of the IMC EDX analysis in Fig. 10 f) indicates a content of 21.2 at.% Ni, 30.8 at.% Cu, 46.8 at.% Sn, and 1.3 at.% Au. Au rich $AuSn_4$ compositions are illustrated as bright areas in the SEM images.

A commercial SAC305 solder paste with only 0.5 wt.% copper content was printed prior assembly, which cannot explain the high copper content combined with the large

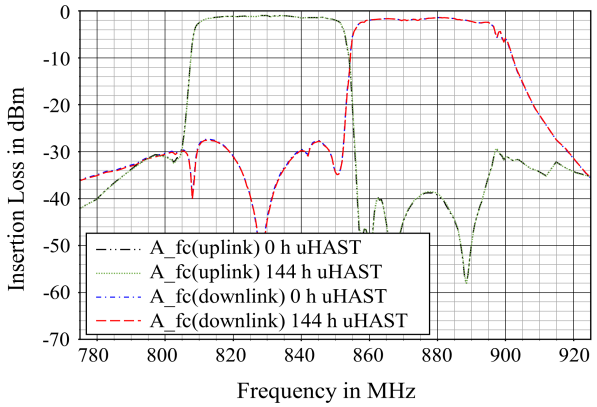

FIGURE 9. Graph shows the insertion loss measured against the frequency of one representative SAW RF filter LTE band 26 duplexer after assembly and after 144 h uHAST (130 °C / 85 % RH) including MSL 2a preconditioning with 6 additional reflows. No significant change could be detected for all SAW RF-filters tested. Only a rough impedance matching of the SAW RF-filter duplexer was performed with SMD inductors.

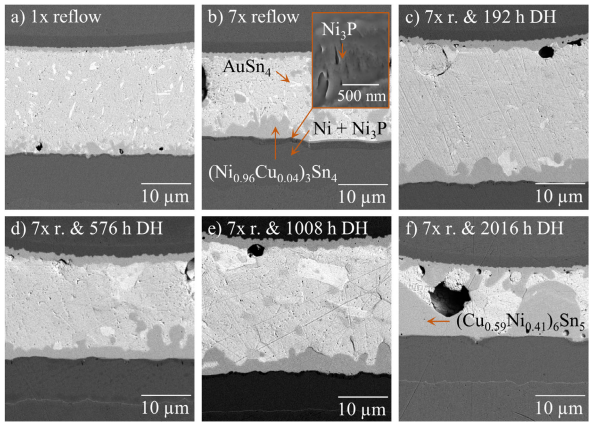

FIGURE 10. Cross sectional SEM images with BSE detector of CPBs soldered to ENIG laminate to evaluate IMC growth during dry heat (DH) testing at 150 °C. a) with only 1 reflow after assembly. b) preconditioned with MSL 2a including 6 additional reflows. c), d), e) and f) preconditioned and additional dry heat storage duration at 150 °C. The IMCs are characterized in b) and f) by EDX. Voiding is present in the upper ENIG (Ni + Ni_3P) layer shown in the inset of b) resulting in a phosphor-rich Ni_3P layer.

IMC volume after 2016 h DH. This poses the question of an additional copper source. A plausible Cu source would be the unprotected sidewalls of the CPB Cu base, provided there was contact with the solder as already described in [11]. This behavior is not visible for the specific cross-sectional plane of Fig. 10 f), but solder might have had contact on a non-visible plane with the Cu base. In fact, in rare cases solder wetting on the sidewall of the CPB Cu base was detected, if strong chip misalignment was present prior assembly reflow. This might explain the high Cu content and the $(Cu_{0.59}Ni_{0.41})_6Sn_5$ IMC layer. However, $(Cu_{0.59}Ni_{0.41})_6Sn_5$ and $(Ni_{0.96}Cu_{0.04})_3Sn_4$ IMC compositions suggested by EDX coincide with other literature. [12] describes the preferred IMC formation of $(Cu, Ni)_6Sn_5$ or $(Ni, Cu)_3Sn_4$ depending on the Cu concentration in the solder. Further, [10] and [11] found similar IMC compositions. No excessive voiding in the IMC layers, except in the electroless phosphor enriched Ni layer, was present. However, this voiding did not induce any crack formation in our test vehicles. A more detailed analysis of IMC formation and composition of our test vehicle will be published elsewhere. The IMC analysis demonstrates that there is still bulk Sn-Ag solder material and sufficient Ni diffusion barrier left even after 2016 h of DH at 150 °C. Thus, the diffusion barrier layer thickness considered in the design retains enough material.

V. LIMITATIONS

There is, however, a limitation to our study in that it does not include a method to quickly assess the effects of further design or material changes on component reliability. Corresponding finite elements simulation would allow a quick assessment. For future simulations our reliability results can serve as a basis to validate the simulation model. Unsuitable material and design combinations could be excluded in advance via the simulation to produce only promising material and design combinations for component reliability tests. This would save resources and still provide an optimized component solution. Additionally, the IMC characterization reveals the question of a possible Cu source explaining the formation of a high Cu content $(Cu_{0.59}Ni_{0.41})_6Sn_5$ IMC layer, which could not be answered with certainty.

VI. OUTLOOK AND CONCLUSION

The extended open top TC reliability tests revealed some potential for design improvements. This includes the avoidance of crack formation and delamination of the passivation layer by e.g. minimizing the overlap between the passivation layer and the CPB Cu base, or by a material change in the passivation and EP layer, respectively.

Further work should be carried out on a more detailed IMC characterization and the development of finite elements simulation to facilitate predicting the influence of design and material changes on component reliability. In addition, the footprint area of the CPB interconnection can be further minimized by design changes, moving the TFAP topology below the CPB. This can further significantly reduce the interconnection area required on SAW RF-filters with TFAPs. However, in this work we demonstrated the high potential of SAW RF-filter miniaturization by replacing the SB interconnection on TFAPs through CPBs. TC, uHAST, DHSS, and DH reliability requirements demanded by industry were achieved with open top SAW RF-filters soldered to a test PCB, i.e. the test vehicles had no molded underfill. This proves that CPB interconnections in combination with TFAPs is a technology that is sufficient for microacoustic SAW RF-filters. Furthermore, an additional significant increase in reliability by several factors can be expected for underfilled SAW RF-filters with CPB interconnections especially for TC.

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