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Effect of Drain Induced Barrier Enhancement on Subthreshold Swing and OFF-State Current of Short Channel MOSFETs: A TCAD Study

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ABSTRACT In this paper, with the help of calibrated 2-D simulations, we report a detailed study on the effect of drain induced barrier enhancement on the subthreshold swing and OFF-state current of a short channel MOSFET. We demonstrate that the presence of gate-on-drain overlap in a short channel MOSFET leads to drain induced barrier enhancement (DIBE). We show that as a result of DIBE, a MOSFET can achieve near ideal subthreshold swing, diminished DIBL, constant threshold voltage and improved I_{ON}/I_{OFF} ratio at room temperature, without being affected by channel length variations.

INDEX TERMS Drain induced barrier enhancement (DIBE), drain induced barrier lowering (DIBL), gate-on-drain overlap, leakage current, MOSFET, scaling, short channel effects (SCE), subthreshold swing, and threshold voltage.

I. INTRODUCTION

When compared to a MOSFET, the TFET exhibits a sub-60 mV/decade subthreshold swing (SS) and lower leakage current. TFETs are also far less susceptible to short channel effects which makes the TFET a promising candidate for future low power integrated circuits [1]–[7]. However, due to the presence of ambipolar current in TFETs, they are not an ideal choice for wide scale implementation [1], [8], [9]. To suppress ambipolar current, a gate-on-drain overlap can be used on a TFET [9]. TFETs also exhibit lower drain current as compared to MOSFETs [1], [3]. While gate overlaps (both on the source and drain side) are common in MOSFETs due to fabrication limitations such as the lateral straggle of implanted dopant atoms, the effect of an intentionally formed gate-on-drain overlap in a MOSFET has not been studied the way it has been for a TFET [9]. To the best of our knowledge, using gate-on-drain overlap, there is no reported work on (i) enhancing the barrier height at the source-channel junction of a MOSFET and (ii) analyzing its impact on Drain Induced Barrier Lowering (DIBL), SS and I_{ON}/I_{OFF} ratio in short channel MOSFETs for channel lengths less than 50 nm. Those papers that have studied the impact of gate-on-drain overlap are related to tunnel field effect transistors. Although there are some papers which deal with the effect of gate overlap on source and drain, they primarily focus on the gate overlap resulting from process conditions. This is the first study on short channel MOSFETs which provides a comprehensive analysis on how optimized gate-on-drain overlap can be used to retain the long channel behavior of the transistor even when the channel length is scaled down.

In this paper, using calibrated two-dimensional simulations, we demonstrate for the first time how the gate-on-drain overlap leads to drain induced barrier enhancement (DIBE) in a MOSFET. We study the effect of DIBE on the DC performance of a short channel MOSFET focusing on the average subthreshold swing, I_{ON}/I_{OFF} ratio and threshold voltage. Our results indicate that the presence of DIBE causes the average subthreshold swing to be near ideal and makes the threshold voltage and I_{ON}/I_{OFF} ratio at room temperature independent of channel length variations.

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Fig. 1 shows the cross-sectional schematic views for (a) the double gate MOSFET (Conventional MOSFET), and (b) the

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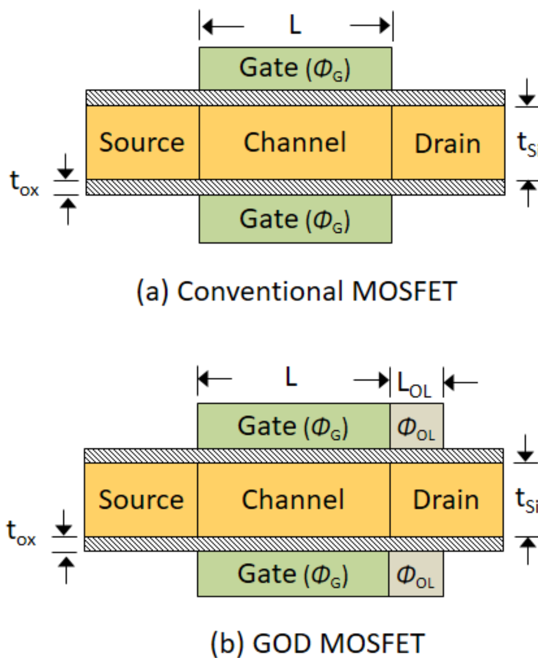


FIGURE 1. Cross-sectional schematic view of (a) the double gate MOSFET (Conventional MOSFET), and (b) the double gate MOSFET with a gate-on-drain overlap (GOD MOSFET).

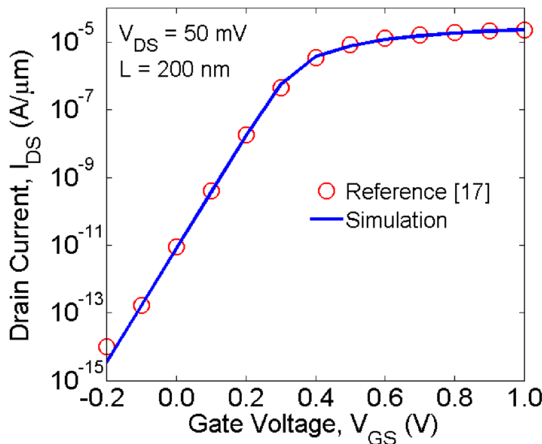


FIGURE 2. Calibration of simulation setup by reproducing the results of [17].

double gate MOSFET with a gate-on-drain overlap (GOD MOSFET). The device parameters used for both the structures in our simulations are as follows: silicon film thickness, t_{Si} = 10 nm, equivalent oxide thickness (EOT) under the gate and gate-on-drain overlap, t_{ox} = 1 nm, gate work function Φ_G = 4.5 eV, gate-on-drain overlap work function Φ_{OL} is varied from 4.5 eV to 5.5 eV, source and drain doping concentrations $N_D = 1 \times 10^{19}$ cm^{-3} and channel doping concentration $N_A = 1 \times 10^{17}$ cm^{-3}. The channel length (L) is scaled from 200 nm to 7 nm. Since quantum mechanical effects need to be included for L < 7 nm, we have limited the scaling of L to 7 nm. The length of the gate-on-drain overlap (L_{OL}) is optimised by varying L_{OL} from 0 nm to 40 nm. The gate-on-drain overlap required in this study can be fabricated using the techniques reported in [10]–[15].

III. SIMULATION APPROACH

All the simulations were done in Silvaco Atlas [16]. The simulation setup was calibrated by reproducing the transfer characteristics of [17] as shown in Fig. 2. The Shirahata carrier mobility model which includes both the lateral and vertical electric field degradation, doping concentration dependent mobility and field dependent mobility for considering velocity saturation are invoked as done in [17]. It may be pointed out that the Shirahata mobility model also takes into account the screening effect in the inversion layer and an improved normal-field dependence for MOSFET's with thin gate oxides. Since the above mobility models are used in [17] against which we have calibrated our results, we have used the same mobility models in our study. Bandgap narrowing model is enabled. The concentration dependent Shockley-Read-Hall model, Auger recombination model and the Fermi Dirac statistics are enabled. We also used a nonlocal band-to-band tunneling (BTBT) model to incorporate tunneling induced leakage current at the abrupt channel-drain p-n junction [18]. All the doping profiles are assumed to be abrupt in these simulations as previously done in [8], [19].

IV. RESULTS AND DISCUSSION

Figs. 3 (a) and (b) show the transfer characteristics and the average subthreshold swing of a MOSFET with L = 10 nm where the length of the gate-on-drain overlap (L_{OL}) is varied from 0 nm to 40 nm and $\Phi_G = \Phi_{OL}$ = 4.5 eV. The average SS is calculated using [20]:

$$Average\ SS = \frac{V_t - V_{SS}}{logI_{Vt} - logI_{SS}} \tag{1}$$

where the threshold voltage (V_t) is the V_{GS} at $I_{DS} = 1 \times 10^{-6}$ A/μm, V_{SS} is the V_{GS} at $I_{DS} = 1 \times 10^{-11}$ A/μm, I_{Vt} is the drain current at V_t and I_{SS} is the drain current at V_{SS}. The threshold voltage is an important parameter in the design and characterization of a MOSFET. The threshold voltage is defined as the gate voltage when the surface potential becomes equal to $2\psi_B$ where ψ_B is the difference between Fermi level and intrinsic Fermi level, and the inversion layer charge is equal to the channel doping. It may be pointed out that the threshold voltage V_t of a MOSFET is conventionally calculated using maximum g_m method [21]. In this case, V_t is determined by extrapolating the point of maximum slope on the transfer characteristics to the V_{GS} axis. However, in modern MOSFETs, the convention is to calculate V_t using the constant current method [20] as this method is widely used in industry because of its simplicity in calculating V_t with only one voltage measurement [21]. Following [20], therefore, in our work we have calculated V_t as the gate voltage (V_{GS}) at which the drain current $I_{DS} = 1 \times 10^{-6}$ A/μm.

It is observed from the transfer characteristics shown in Fig. 3 (a) that as the L_{OL} increases, the subthreshold swing also improves with no significant effect on the

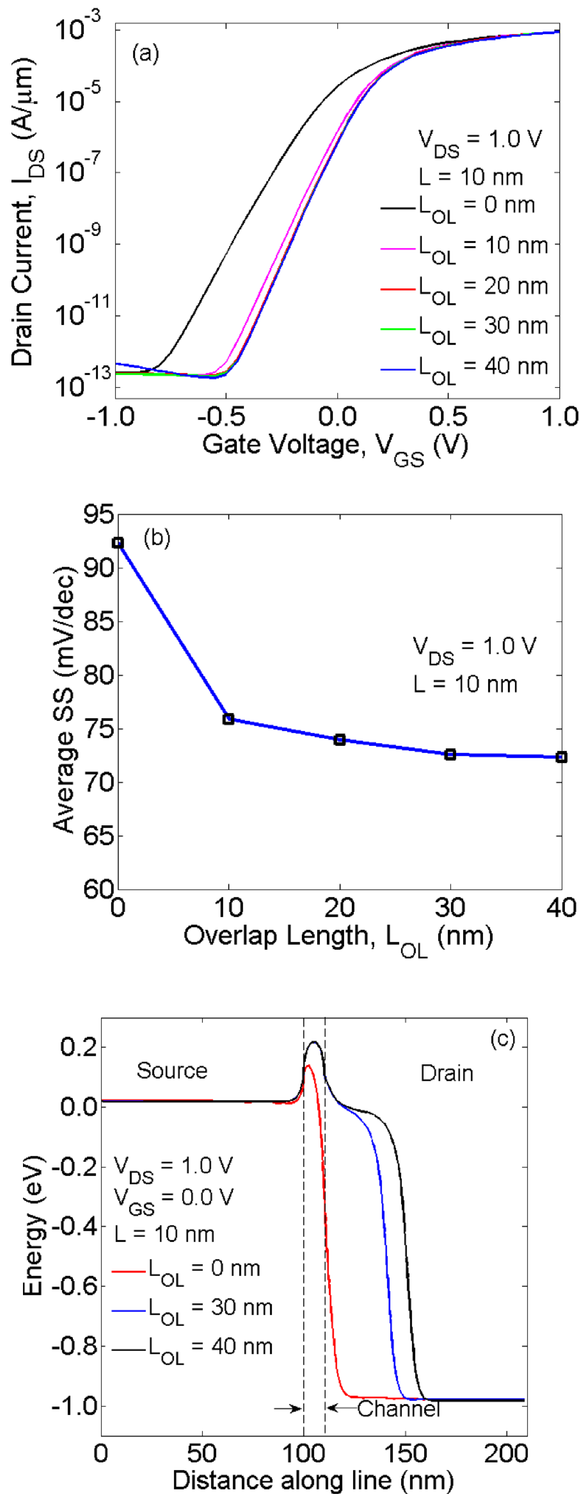


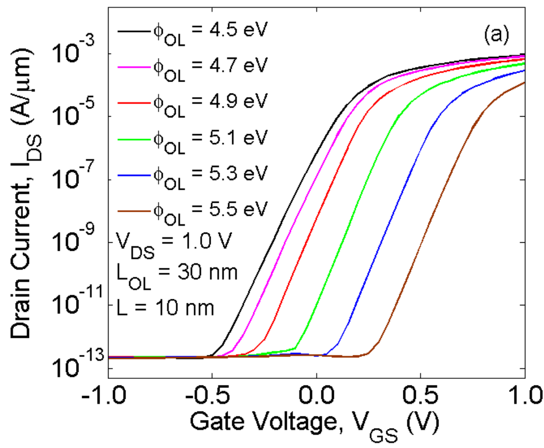
FIGURE 3. **(a) Transfer characteristics, (b) average SS for different lengths of the gate-on-drain overlap (L_{OL}) and (c) the conduction band energy profiles at 1 nm below the Si – SiO_2 interface for the GOD MOSFET with $\Phi_G = \Phi_{OL} = 4.5$ eV at $V_{DS} = 1.0$ V in the OFF-state ($V_{GS} = 0.0$ V).**

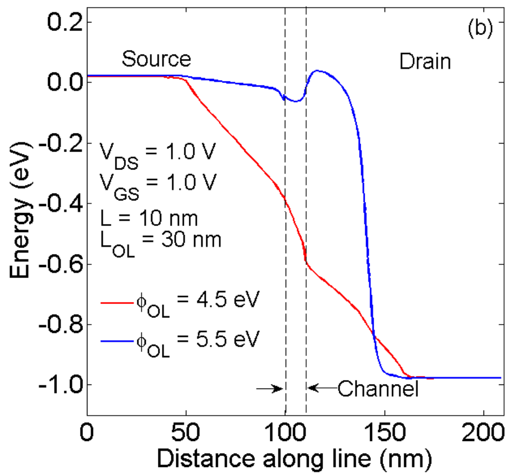
ON-state current (I_{DS} at V_{GS} = 1.0 V). However, from Figs. 3 (a) and (b), we observe that for the GOD MOSFET when $L_{OL} > 30$ nm, there is no observable difference in the transfer characteristics and the average subthreshold swing, respectively. The reason for this can be understood from Fig. 3 (c), which shows the conduction band energy profiles at 1 nm below the Si – SiO_2 interface for the GOD MOSFET for L_{OL} = 0 nm, 30 nm and 40 nm. As we can notice, the drain induced barrier enhancement is clearly visible when L_{OL} is increased from 0 nm to 30 nm. However, the barrier enhancement is nearly the same for $L_{OL} > 30$ nm and this is the reason why we see in Figs. 3 (a) and (b) that there is no significant change in the transfer characteristics and the average subthreshold swing, respectively, for $L_{OL} > 30$ nm. Since there is no further reduction in average subthreshold swing for $L_{OL} > 30$ nm, we have chosen $L_{OL} = 30$ nm as the optimum gate-on-drain overlap length in the rest of our study.

Fig. 4 (a) shows the effect of varying the work function of the gate-on-drain overlap (Φ_{OL}) on the transfer characteristics of the GOD MOSFET with $L_{OL} = 30$ nm. We observe that, as Φ_{OL} is increased above 5.1 eV, the ON-state current decreases significantly. To understand the reason behind the decrease in I_{ON} for larger φ_{OL}, we have shown the conduction band energy profiles at 1 nm below the Si – SiO_2 interface for the GOD MOSFET for $L_{OL} = 30$ nm and for $\varphi_{OL} = 4.5$ eV and 5.5 eV in Fig. 4 (b). It is observed from Fig. 4 (b) that the drain-channel barrier height increases when $\varphi_{OL} = 5.5$ eV as compared to $\varphi_{OL} = 4.5$ eV. When $\varphi_{OL} = 5.5$ eV, to get the same drain current that one would realize for the GOD MOSFET with $\varphi_{OL} = 4.5$ eV, the gate voltage needs to be increased to suppress the barrier height in the GOD MOSFET with $\varphi_{OL} = 5.5$ eV. It is equivalent to an increase in the threshold voltage. This increase in threshold voltage, therefore, decreases I_{ON} as φ_{OL} is increased from 4.5 eV to 5.5 eV.

Fig. 4 (c) shows the effect of varying the work function of the gate-on-drain overlap (Φ_{OL}) on the average SS of the GOD MOSFET with L_{OL} = 30 nm. It is observed from Fig. 4(c) that the average SS is the least when $\Phi_{OL} = 5.1$ eV. Therefore, 30 nm and 5.1 eV are chosen to be the optimum values for L_{OL} and Φ_{OL}, respectively, in the rest of our study for the GOD MOSFET. Nickel can be used as the metal for gate-on-drain overlap since it has a work function of 5.1 eV [22].

Fig. 5 shows the transfer characteristics of the conventional MOSFET and the GOD MOSFET for different channel lengths. From Fig. 5 (a), we observe that as the channel length of the conventional MOSFET is scaled down from L = 200 nm to 7 nm, there is a significant deterioration in the subthreshold swing and an increase in the OFF-state leakage current (I_{DS} at V_{GS} = 0.0 V) making the conventional MOSFET unusable for $L \leq 30$ nm [17]. In the case of GOD MOSFET, the effect of the gate-on-drain overlap can be seen in Fig. 5 (b). It is observed that as the channel length is scaled down, the GOD MOSFET exhibits no increased OFF-state leakage current. The threshold voltage and subthrehsold slope also remain identical with negligible change for all channel lengths from L = 200 nm to 7 nm, clearly indicating the suppression of DIBL. A suppressed DIBL in a MOSFET is





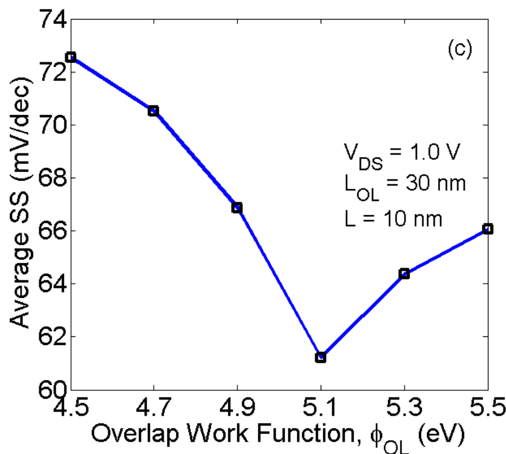
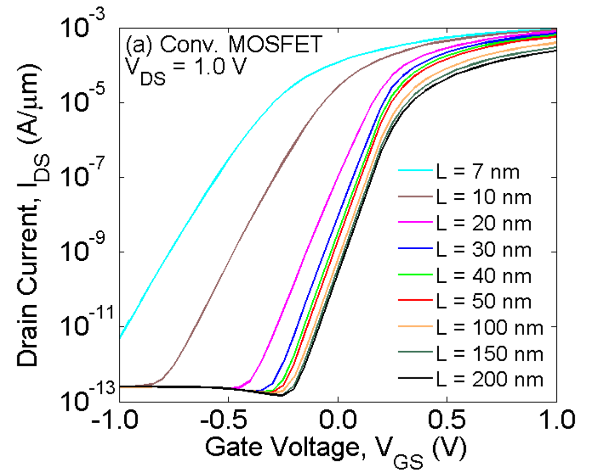


FIGURE 4. (a) Transfer characteristics for different Φ_{OL}, (b) the conduction band energy profiles at 1 nm below the $Si - SiO_2$ interface for the GOD MOSFET with $\Phi_{OL} = 4.5$ eV and 5.5 eV at $V_{DS} = 1.0$ V in the ON-state ($V_{GS} = 1.0$ V) and (c) average SS for different Φ_{OL}.

possible only when the barrier height at the source-channel junction is unaffected by the increased proximity between the drain and the source regions. The reason for this nearly identical MOSFET performance when the channel length is



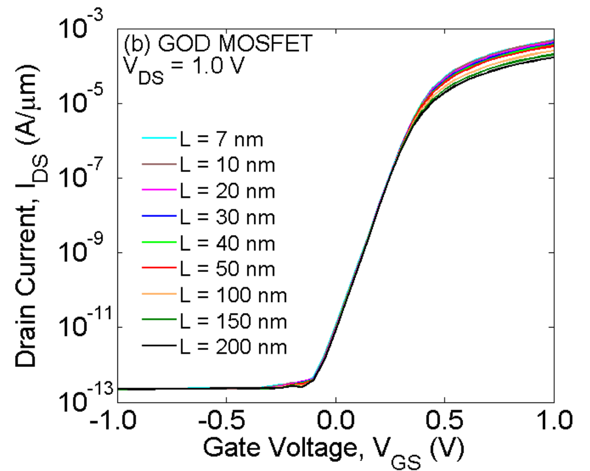


FIGURE 5. Transfer characteristics for (a) Conventional MOSFET and (b) GOD MOSFET as L is scaled from 200 nm to 7 nm.

varied from 200 nm to 7 nm, is due to the presence of drain induced barrier enhancement caused by the gate-on-drain overlap in the GOD MOSFET. The effect of DIBE can be understood by analyzing the conduction band energy profiles shown in Fig. 6.

Figs. 6 (a) and (b) show the conduction band energy profiles in the OFF-state ($V_{GS} = 0.0$ V) for L = 200 nm and 7 nm, respectively. The drain induced barrier enhancement (DIBE) at the channel-drain junction in the GOD MOSFET is due to the gate-on-drain overlap (where $\Phi_{OL} > \Phi_G$). From Fig. 6 (a), for L = 200 nm, we observe that when V_{DS} is increased from 50 mV to 1.0 V, the barrier height at the source-channel junction in both the conventional MOSFET and GOD MOSFET remains unchanged at 0.328 eV. However, from Fig. 6 (b), for L = 7 nm, we observe that even when V_{DS} = 50 mV, the source-channel junction barrier height of the conventional MOSFET decreases significantly from 0.328 eV (for L = 200 nm) to 0.181eV due to the increased proximity between the drain and the source regions. As V_{DS} is increased from 50 mV to 1.0 V for L = 7 nm, we observe that the source-channel junction barrier height further decreases from 0.181eV to 0.080 eV

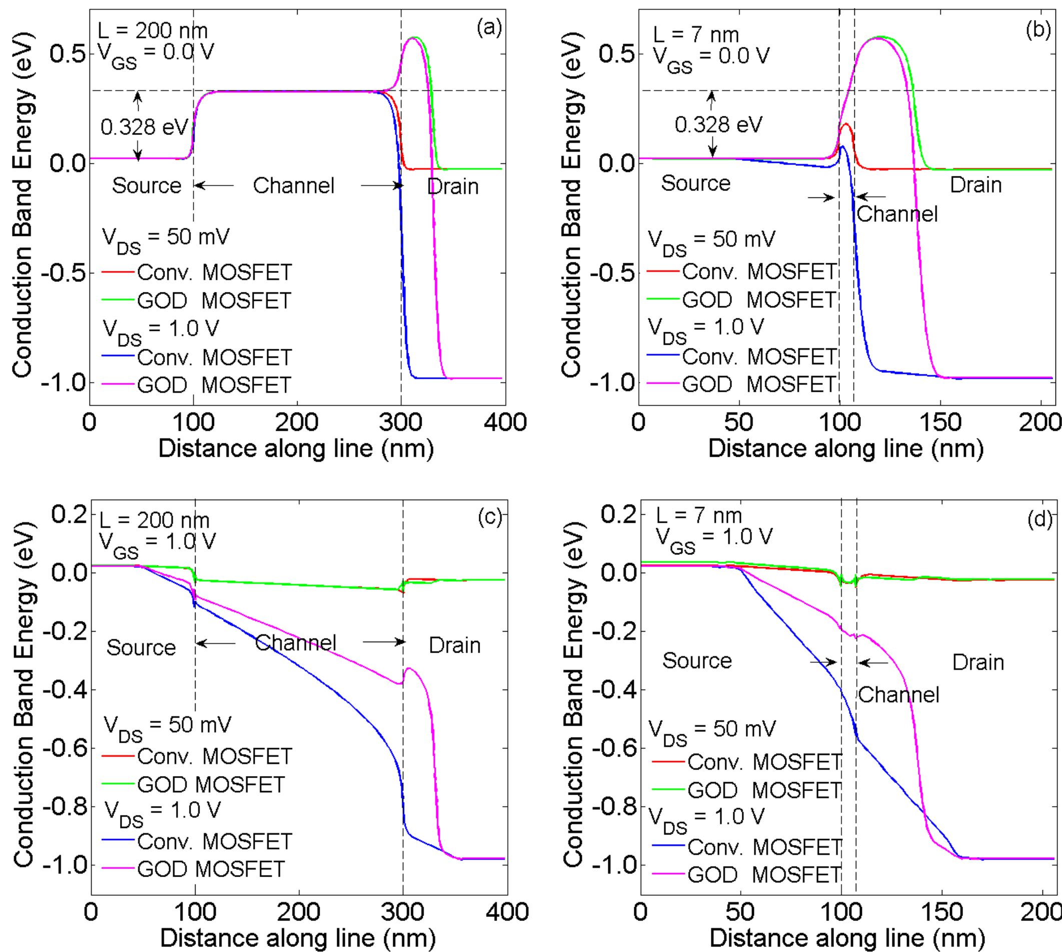


FIGURE 6. **The conduction band energy profiles at 1 nm below the Si – SiO_2 interface for the conventional MOSFET and GOD MOSFET at V_{DS} = 50 mV and 1.0 V in the OFF-state (V_{GS} = 0.0 V) for (a) L = 200 nm and (b) L = 7 nm; in The ON-state (V_{GS} = 1.0 V) for (c) L = 200 nm and (d) L = 7 nm.**

in the conventional MOSFET resulting in an unacceptably large increase in the OFF-state leakage current as shown in Fig. 5 (a). In the case of GOD MOSFET, when L is reduced from 200 nm to 7 nm, the source-channel junction barrier height increases significantly in the OFF-state due to the modulation of the conduction band energy profile by the gate-on-drain overlap. We have referred to this conduction band energy profile modulation as drain induced barrier enhancement (DIBE). As V_{DS} is increased from 50 mV to 1.0 V, we observe that the source-channel junction barrier height remains high and unaffected in the GOD MOSFET leading to no increase in the OFF-state leakage current as shown in Fig. 5 (b). Figs. 6 (c) and (d) show the conduction band energy profiles in the ON- state (V_{GS} = 1.0 V), for L = 200 nm and 7 nm, respectively. It can be observed that the height of the modulated energy band profiles under the gate-on-drain overlap in the GOD MOSFET is significantly reduced and, therefore, has no noticeable effect on the ON-state current. Therefore, due to DIBE in the GOD MOSFET, the transfer characteristics the OFF-state leakage current are unaffected even though the channel length is decreased from L = 200 nm to L = 7 nm.

The impact of drain induced barrier enhancement in the GOD MOSFET on DIBL, V_t, average SS and I_{ON}/I_{OFF} ratio at room temperature is examined below.

The DIBL can be calculated as the difference in the gate voltage required to attain the same drain current (I_{DIBL}), at a low drain voltage (V_{DS} = 50 mV) and at the supply voltage (V_{DS} = 1.0 V). In our work, the DIBL is computed at $I_{DIBL} = 10^{-9}$A/μm using the following equation as done in [8]:

$$DIBL = \frac{V_{GS}(@V_{DS} = 0.05\,V) - V_{GS}(@V_{DS} = 1.0\,V)}{1.0 - 0.05} \quad (2)$$

Fig. 7 (a) shows DIBL versus L. We observe that DIBL of the conventional MOSFET rapidly increases from 7.36 mV/V at L = 200 nm to 291.10 mV/V at L = 7 nm. This severe degradation of DIBL in the conventional MOSFET is due to the reduction in the source-channel junction barrier height as shown in Fig. 6 (b). On the other hand, as L is scaled down,

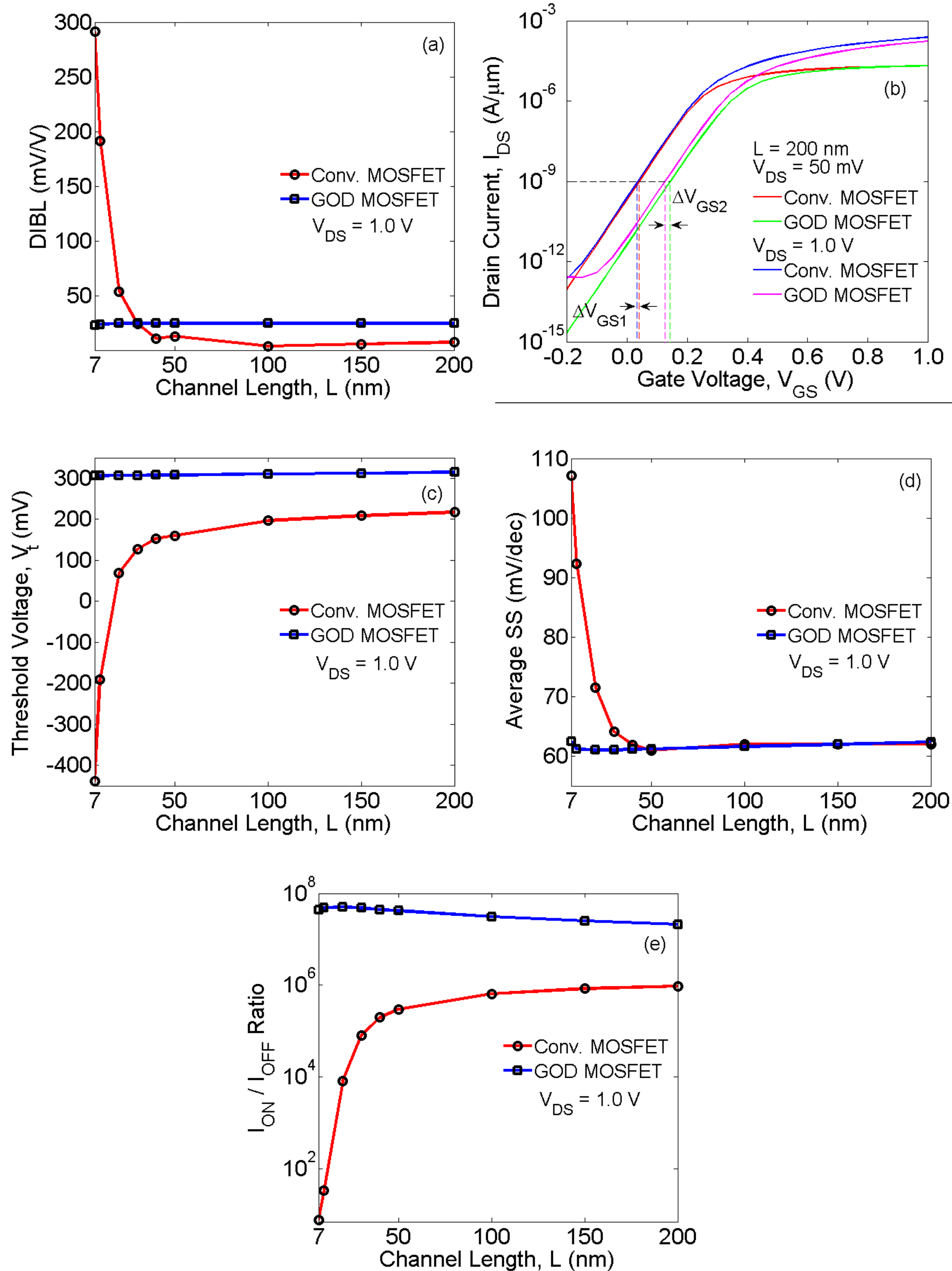


FIGURE 7. (a) DIBL versus L, (b) transfer characteristics of the conventional MOSFET and the GOD MOSFET for L = 200 nm at different drain voltages, (c) V_t versus L, (d) Average SS versus L and (e) I_{ON}/I_{OFF} ratio versus L.

DIBL of the GOD MOSFET remains nearly identical for L = 200 nm (24.56 mV/V) and L = 7 nm (22.98 mV/V) due to the drain induced barrier enhancement at the source-channel junction as shown in Fig. 6 (b).

To understand why the DIBL is larger in the case of GOD MOSFET as compared to the conventional MOSFET for long channel lengths, in Fig. 7 (b), we have shown the transfer characteristics of the conventional MOSFET and the GOD

MOSFET for L = 200 nm at V_{DS} = 50 mV and 1.0 V. In Fig. 7 (b), we notice that for realizing $I_{DIBL} = 10^{-9}$A/μm in a conventional MOSFET, the required V_{GS} is 0.032 V and 0.025 V for V_{DS} = 50 mV and 1.0 V, respectively. However, in the case of GOD MOSFET, for realizing $I_{DIBL} = 10^{-9}$A/μm, the required V_{GS} is 0.138 V and 0.115 V for V_{DS} = 50 mV and 1.0 V, respectively. As a result, in eq.(2), the ΔV_{GS2} in the numerator is greater for GOD MOSFET as compared to the ΔV_{GS1} of the conventional MOSFET as is clearly visible in Fig. 7 (b). This is the reason why at longer channel lengths, the DIBL of GOD MOSFET is larger than that of the conventional MOSFET. However, when the channel length is lower than 50 nm, in the case of GOD MOSFET, drain barrier enhancement takes place due to the gate-on-drain overlap and the DIBL does not worsen. On the other hand, in the case of the conventional MOSFET, drain induced barrier lowering takes place when the channel length is lower than 50 nm resulting in a larger DIBL as compared to the GOD MOSFET.

Fig. 7 (c) shows the threshold voltage (V_{GS} at I_{DS} = 1×10^{-6} A/μm [20]) versus L. The GOD MOSFET has a higher V_t than the conventional MOSFET for all the channel lengths due to the presence of the gate-on-drain overlap in the GOD MOSFET. We further observe that the V_t of the conventional MOSFET rapidly decreases from 217.50 mV at L = 200 nm to −438.38 mV at L = 7 nm exhibiting a significant V_t roll-off. For the conventional MOSFET, for $L < 20$ nm, we note that the threshold voltage becomes negative due to the worsening DIBL and therefore, it causes an increase in the drain current at negative gate voltages as shown in Fig. 5 (a). Although n-channel MOSFETs are required to have a positive V_t, they can exhibit zero or even a negative threshold voltage for shorter channel lengths and it has been studied extensively in literature [23]. On the other hand, the V_t of the GOD MOSFET remains nearly identical for L = 200 nm (314.19 mV) and for L = 7 nm (305.88 mV). This negligible V_t roll-off ($<3\%$) is due to the drain induced barrier enhancement as shown in Fig. 6 (b).

Fig. 7 (d) shows the average subthreshold swing versus L. We observe that the average SS of the conventional MOSFET rapidly deteriorates from 62.02 mV/dec at L = 200 nm to 107.13 mV/dec at L = 7 nm. However, the average SS of the GOD MOSFET at 200 nm (62.39 mV/dec) is approximately the same as the average SS at 7 nm (62.42 mV/dec) clearly indicating that the average SS remains near ideal regardless of the channel length due to the drain induced barrier enhancement.

Fig. 7 (e) shows the ratio of I_{ON} (I_{DS} at V_{GS} = 1.0 V) and I_{OFF} (I_{DS} at V_{GS} = 0.0 V) versus L. Since the drain current of a MOSFET is inversely proportional the channel length, the drain current increases with a reduction in the channel length. In the case of the conventional MOSFET, as the channel length decreases, while the ON-state current increases marginally, the OFF-state current increases by several orders of magnitude due to worsening DIBL as shown in Fig. 5 (a). Therefore, the I_{ON}/I_{OFF} ratio of the conventional MOSFET decreases from 9.45×10^5 for L = 200 nm to 7.65 for L = 7 nm due to the increase in OFF-state current. However, in the case of GOD MOSFET as shown in Fig. 5 (b), while there is a slight increase in the ON-state current, the OFF-state current does not change with a reduction in the channel length due to the drain induced barrier enhancement. As a result, the I_{ON}/I_{OFF} ratio of the GOD MOSFET increases slightly from 2.12×10^7 for L = 200 nm to 4.44×10^7 for L = 7 nm.

From the above discussions, it is evident that due to the presence of drain induced barrier enhancement in the GOD MOSFET, the DC performance of the device is nearly identical as the channel length is varied from 200 nm to 7 nm independent of the channel length variations.

V. CONCLUSION

To conclude, with the help of calibrated 2-D simulations, we reported a detailed study on the effect of drain induced barrier enhancement on the DC performance of a short channel MOSFET. We have demonstrated how the presence of drain induced barrier enhancement due to the gate-on-drain overlap leads to near ideal average SS, nearly identical Vt, diminished DIBL and improved I_{ON}/I_{OFF} ratio at room temperature across different channel lengths in a MOSFET.

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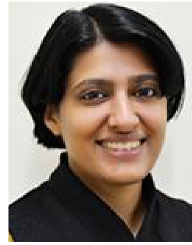

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