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Single-Phase Hybrid Switched-Capacitor Interleaved AC-DC Boost Converter

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ABSTRACT In this paper a single-phase boost PFC multilevel interleaved high-voltage gain based on the hybrid switched-capacitor concept is presented. The proposed converter merges interphase transformers and switched-capacitor cells to obtain current sharing and high voltage gain. These features allow for both the reduction of voltage and current stresses on the semiconductors. Furthermore, the interleaving method allows for obtaining multilevel voltages at AC terminals, thereby reducing the weight and bulk of the input inductor. PFC operation is guaranteed through both input current control and output voltage control. Both steady-state and dynamic analyses were conducted. Experimental results for a 1.25 kW, 127 V to 800 V laboratory prototype are presented and discussed.

INDEX TERMS High voltage gain, interleaving, interphase transformer cells, power factor correction, PWM rectifier, switched-capacitor.

I. INTRODUCTION

In recent years there has been a growing demand for high voltage power supplies. These sources are required in applications such as renewable energy systems [1] and electric vehicle powertrains [2], among others [3], [4].

Hybrid topologies are the prominent technique that allows for high voltage gain. This technique combines a traditional boost topology with switched capacitor (SC) converters. The SCs allow increased voltage gain by means of diode-capacitor cells, that guarantees the voltage division on the semiconductors. It has been developed for numerous applications, such as LED systems [4], pulse generation [5], and high static gain systems [6], [7], among others [8]–[19].

On the contrary, in applications connected to the electrical network, power factor correction is required owing to the regulations. Typically, a PFC boost rectifier is applied to obtain a sinusoidal current at the input and a high power factor. Although it has a voltage-elevating characteristic, the gain of this converter is limited owing to losses and high efforts in semiconductors. One solution to this problem is the use of hybrid topologies. In [20] a family of unidirectional single-phase hybrid switched-capacitor (HSC) AC-DC boost rectifiers is presented, whose converters provide a static gain twice that of the conventional PFC boost rectifier, and can be increased with the addition of cascading multiplier stages. In [21] another family of single-phase and three-phase unidirectional hybrid rectifiers with a high power factor is presented. Through a three-level generic cell, a static gain four times greater than that of the conventional boost converter was obtained. A reduction in the voltage stresses on the switches to one-fourth the output voltage, the PFC operation, and high efficiency. However, the topologies have an operating range limited to some applications owing to the significantly increased current stress at high power.

To overcome the high current stresses the interleaved technique can be employed. The interleaving technology is applied in power applications above 600 W, which also increases the equivalent switching frequency as demonstrated by [22]–[24]. It presents the current share between the connection arms, promotes waveform frequency multiplication of inductive and capacitive elements, and reduces voltage efforts [25], [26]. In addition, it promotes input-current ripple reduction, thereby allowing for filter size reduction, and contributes to a low electromagnetic interference level [27]–[30]. Recent studies have demonstrated that the interleaving technique associated with HSC converters, can be

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used in applications with high static gain and low ripple current, such as [25], [31], [32].

In [33] an interleaved double-input three-level boost converter, which is composed of two boost converters indirectly in series, is proposed. In [34] a nonisolated three-level bidirectional dc-dc boost converter is proposed using the interleaving technique. In [35] an input-parallel-output-series multilevel boost converter integrated with SC cells. These topologies present high-voltage gain and small voltage across all components, owing to the advantages of the interleaving method associated with SC concept. However, these topologies were applied only in DC-DC converters.

From the above, this paper presents a single-phase HSC interleaved AC-DC boost converter with a high power factor and high static gain. The converter has the inherent advantages of interleaved operation with a hybrid topology with an SC. Among the advantages are reduced input current ripple, low AC losses in the inductor, low voltage stresses across all semiconductor devices, and high output voltage.

In the following sections, the basic operation principle of the proposed high step-up converter and mathematical model are described. In addition, the control strategy and the main characteristics are presented. Finally, to validate the proposed converter, experimental results were obtained from a 1.25 kW prototype with 800 V output voltage.

II. PROPOSED CONVERTER

The proposed single-phase HSC interleaved AC-DC boost converter is shown in Fig. 1. It comprises four switches S_n $n \in \{1, .., 4\}$, an input inductor L switching capacitors $C_{j,k}$ $j \in \{1, 2, 3\}$ $k \in \{A, B\}$, and two interphase transformers with inductors. The interphase transformers are represented by self inductances L_s, which are connected to an interleaved arm.

As previously mentioned, the interleaving technique associated with SC converters is advantageous for high static gain applications. Owing to the interleaving technique, the input inductor operates at twice the switching frequency, which reduces its bulk. The inductors of interphase transformers also have a bulk reduction, as they only have high-frequency magnetic flux. These advantages make the proposed topology more interesting when compared with the topologies presented by [21] because it operates in the PFC, as the reference topologies, and makes it possible to obtain other topologies with lower current stresses on semiconductors for high power applications compared to the reference.

A. OPERATIONAL STAGES

As the proposed converter operates symmetrically it is analyzed over a positive half cycle of the grid. However, quantitative and qualitative analyses are also valid for negative grid semi-cycles. It operates in four stages depending on the PWM modulation scheme shown in Fig. 2.

Fig. 2(a) shows the waveform from input voltage v_g, switching voltage v_{ao}, the modulation signals v_{modK} $k \in \{A, B\}$, and the triangular carriers v_{tri_1} and v_{tri_2}. Angles θ_1 and

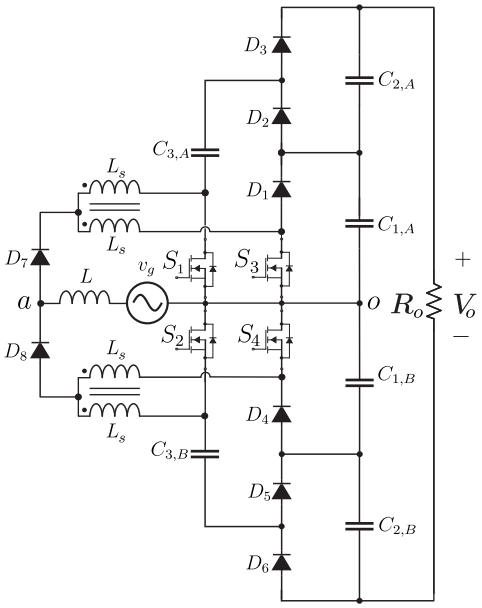

FIGURE 1. Proposed single-phase HSC interleaved AC-DC boost converter.

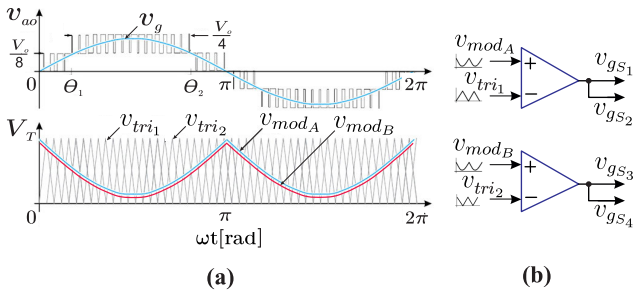

FIGURE 2. (a) Idealized waveforms for high power factor operation valid to modulation index $M > 0.5$, (b) PWM modulation scheme.

θ_2 are the points at which correspond to the voltage level transition boundary. The switching pattern of the switches is generated by means of two comparators, as shown in Fig. 2(b), where the modulation signal v_{mod_A} is compared with the triangular carried v_{tri_1} to generate the command signals v_{gS_1} and v_{gS_2} for switches S_1 and S_2, respectively. The switching pattern for switches S_3 and S_4 is generated by means of a second comparator employing a carrier signal v_{tri_2} shifted 180°. Ideally, for the same switching period, the switches are fed with the same duty cycle. Switches S_1 and S_3 operate for the positive semi-cycle of the grid, while S_2 and S_4 operate for the negative semi-cycle.

As the duty cycle d is variable over a grid period, it can be performed according to the voltage level transition angles θ_1 and θ_2, facilitating analysis. Thereby, the duty cycle is $d > 0.5$ to $\omega t < \theta_1$ and $d < 0.5$ to $\theta_1 < \omega t < \theta_2$.

Fig. 3 shown the command signals v_{gS1} and v_{gS3} for switches S_1 and S_3, respectively. The respective operational stages and their time intervals over a switching period T_s, where d is the duty cycle. Fig. 4 represents the equivalent

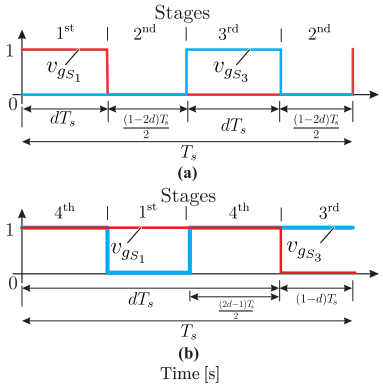

FIGURE 3. Operational stages defined by the command signals v_{gS_1} and v_{gS_3}: (a) valid to duty cycle $d < 0.5$; (b) valid to $d > 0.5$.

circuit to each operational stage, where $r_{C3,A}$ represents the capacitor series resistance.

For operational stages the capacitors are previously charged and their voltages are constant.

1) FIRST STAGE

As shown in Fig. 4(a), the command for driving switch S_1 occurs, while switch S_3 is turned off. During this period, inductor L_1 transfers energy to capacitor $C_{3,A}$, through diodes D_1 and D_2. Capacitor $C_{1,A}$ transfers energy to capacitor $C_{3,A}$ through diode D_2. Capacitor $C_{2,A}$ transfers energy to the load R_o, while inductor L_2 stores the energy supplied by the input inductor L. The input inductor L receives energy from the power source v_g, while diode D_3 remains blocked. Applying Kirchhoff's loop law, the equations describing this stage are presented in equations by (1).

$$\begin{cases} v_g = v_L + v_{L_2} \\ i_{C_{2,A}} = i_{C_{1,A}} + i_{C_{3,A}} - i_{L_1} \\ v_{C_{1,A}} = i_{C_{3,A}} \cdot r_{C_{3,A}} + v_{C_{3,A}} \\ i_{C_{2,A}} = -\dfrac{\left(v_{C_{1,A}} + v_{C_{2,A}}\right)}{R_o} \\ v_g = v_L + v_{L_1} + v_{C_{1,A}} \end{cases} \tag{1}$$

2) SECOND STAGE

As illustrated in Fig. 4(b), switches S_1 and S_3 are turned off. The input inductor L together with inductors L_1 and L_2 transfers energy to all capacitors. The inductor L_2 transfers energy to capacitor $C_{3,A}$. Capacitor $C_{2,A}$ and the load R_o receive energy from capacitor $C_{3,A}$ through diode D_3. The inductor L_1 transfers energy to capacitor $C_{1,A}$ through diode D_1. The diode D_2 remains blocked. The expressions in (2) define this stage.

$$\begin{cases} v_g = v_L + v_{L_1} + v_{C_{1,A}} \\ v_g = v_L + v_{L_2} - v_{C_{3,A}} - i_{C_{3,A}} \cdot r_{C_{3,A}} + v_{C_{1,A}} + v_{C_{2,A}} \\ -v_{C_{1,A}} - v_{C_{2,A}} + i_{C_{3,A}} \cdot r_{C_{3,A}} + v_{C_{3,A}} + v_{L_1} - v_{L_2} = 0 \\ i_{C_{3,A}} + i_{C_{2,A}} + \dfrac{\left(v_{C_{1,A}} + v_{C_{2,A}}\right)}{R_o} = 0 \\ i_{L_1} + i_{C_{2,A}} = i_{C_{1,A}} \\ i_{C_{3,A}} = -i_{L_2} \end{cases} \tag{2}$$

3) THIRD STAGE

As shown in Fig. 4(c), switch S_1 is turned off, while switch S_3 is driving. The inductor L_1 stores the energy supplied by the input inductor L, which in turn receives energy from the power source v_g. The inductor L_2 transfers energy to capacitor $C_{3,A}$. Capacitor $C_{3,A}$ transfers energy to the load R_o, as well as

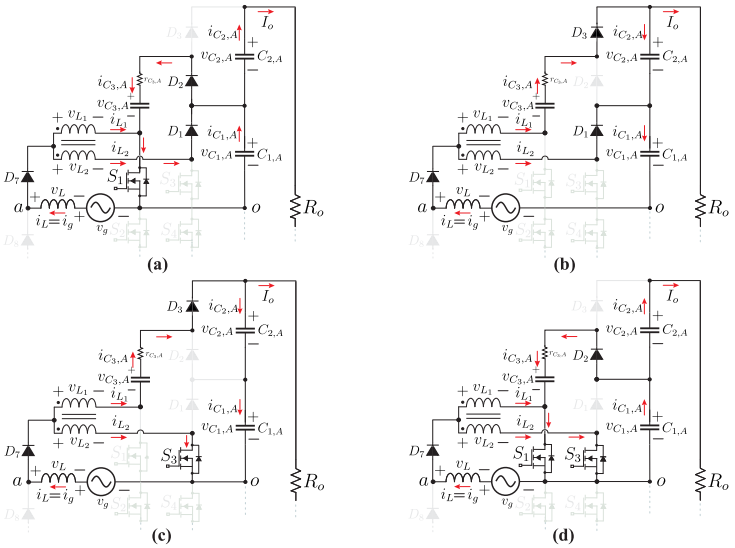

FIGURE 4. Operational stages of the proposed converter valid to positive semi-cycle of the grid: (a) switch S_1 is turned on and S_3 is turned off; (b) S_1 and S_2 are turned off; (c) S_1 is turned off and S_3 is turned on; (d) S_1 and S_3 are turned on.

to the capacitors $C_{2,A}$ and $C_{1,A}$ through diode D_3, showing the switched-capacitor operation. The diodes D_1 and D_2 remain blocked. The equations for this stage are shown in (3).

$$\begin{cases} v_g = v_L + v_{L_1} \\ v_g = v_L + v_L - v_{C_{3,A}} - i_{C_{3,A}} \cdot r_{C_{3,A}} + v_{C_{1,A}} + v_{C_{2,A}} \\ i_{C_{3,A}} = -i_{L_2} \\ i_{C_{3,A}} + i_{C_{2,A}} + \dfrac{\left(v_{C_{1,A}} + v_{C_{2,A}}\right)}{R_o} = 0 \\ i_{C_{1,A}} = i_{C_{2,A}} \end{cases} \tag{3}$$

4) FOURTH STAGE

Fig. 4(d) shows that when the duty cycle is $d > 0.5$. Switches S_1 and S_3 were turned on. The input inductor stores energy from the power supply through switch S_3, as well as from capacitor $C_{3,A}$ through switch S_1. The load R_o receives energy from capacitor $C_{2,A}$.

Fig. 5 shown the basic waveforms from the proposed converter over a switching period T_s including the four operational stages. The command signals for switches v_{gS_1} and v_{gS_3}, levels from switching terminal voltage v_{ao}, voltage v_L and ripple current $\Delta i_{L,pk-pk}$ of the input inductor, where v_g is the input voltage and V_o is the output voltage.

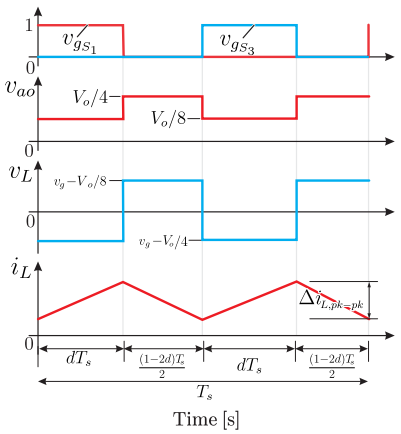

FIGURE 5. Theoretical waveforms from proposed converter, valid to duty cycle $d < 0.5$.

B. STATE-SPACE ANALYSIS

The analysis by the state-space averaged model is presented considering the converter operating in continuous conduction mode. The analysis can be performed in matrix form by equations in (4).

$$\begin{cases} \dot{x} = \mathbf{A} \cdot x + \mathbf{B} \cdot u \\ \mathbf{y} = \mathbf{C} \cdot \mathbf{x} \end{cases} \tag{4}$$

where $\mathbf{A}$, $\mathbf{B}$ e $\mathbf{C}$ are the matrices with the variables states in each operational stage within one switching period T_s. The vector $\dot{x}$ is the derivative vector of x that is the space state vector, u is the input vector, and y is the output vector of the system, those are expressed by the equations in (5).

$$\begin{cases} \dot{x}^{T_s} = \left[\dfrac{d\,i_{L_1}}{dt}, \dfrac{d\,i_{L_2}}{dt}, \dfrac{d\,v_{C_{1,A}}}{dt}, \dfrac{d\,v_{C_{2,A}}}{dt}, \dfrac{d\,v_{C_{3,A}}}{dt}\right] \\ x^{T_s} = \left[i_{L_1}, i_{L_2}, v_{C_{1,A}}, v_{C_{2,A}}, v_{C_{3,A}}\right] \\ u = [v_g] \\ y = [i_g, V_o] \end{cases} \tag{5}$$

Considering the operational stages to $d < 0.5$, shown in Fig. 3(a), the matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$ are determined by the expressions in (6).

$$\begin{cases} A = (A_1 + A_3) \cdot d + A_2 \cdot (1 - 2d) \\ B = (B_1 + B_3) \cdot d + B_2 \cdot (1 - 2d) \\ C = (C_1 + C_3) \cdot d + C_2 \cdot (1 - 2d) \end{cases} \tag{6}$$

where $\mathbf{A_n}$, $\mathbf{B_n}$, $\mathbf{C_n}$, $n \in \{1, 2, 3\}$, are the matrices with state variables from each operational stage.

For the state analysis, the derivative result of the space-state vector is zero ($\dot{x} = 0$) thus, the analytical solution for expressions in (4) is $x = (-\mathbf{A}^{-1} \cdot \mathbf{B}u)$. Solving for it, the state variable expressions are obtained in (7) to vector x as a function of the input voltage v_g, load R_o, and duty cycle d.

$$x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_{1,A}} \\ v_{C_{2,A}} \\ v_{C_{3,A}} \end{bmatrix} = \begin{bmatrix} \dfrac{2 \cdot v_g}{R_o \cdot (d-1)^2} \\ \dfrac{2 \cdot v_g}{R_o \cdot (d-1)^2} \\ -\dfrac{v_g}{(d-1)} \\ -\dfrac{v_g}{(d-1)} \\ -\dfrac{v_g}{(d-1)} \end{bmatrix} \tag{7}$$

The grid current i_g equals the input inductor current i_L ($i_g = i_L$), where $i_L = \Sigma i_{L_n} n \in \{1, 2, 3, 4\}$, and the output voltage V_o is determined by expression $V_o = \Sigma v_{C_{j,k}}, j \in \{1, 2\}$ and $k \in \{A, B\}$. Therefore, the output variables matrix y results in expression (8).

$$y = \begin{bmatrix} i_g \\ V_o \end{bmatrix} = \begin{bmatrix} \dfrac{6 \cdot v_g}{R_o \cdot (d-1)^2} \\ -\dfrac{4 \cdot v_g}{(d-1)} \end{bmatrix} \tag{8}$$

Solving for it, the static gain can be written by expression (9).

$$G = \frac{V_o}{v_g} = \frac{4}{(1-d)} \tag{9}$$

Therefore, by means of expression (9), the static gain of the proposed converter is four times greater than the conventional boost gain.

C. CURRENT STRESSES ANALYSIS

To determine the semiconductors currents and voltages some considerations were adopted, which are as follows:

TABLE 1. Semiconductors average current to each operational stage.

Semiconductor	1ª stage	2ª stage	3ª stage	4ª stage
$C_{1,A}$	$i'_{C_{1,A}} = \frac{i_g(d^2+d-1)}{2d}$	$i''_{C_{1,A}} = \frac{i_g(d+1)}{2}$	$i'''_{C_{1,A}} = \frac{i_g \cdot d}{2}$	$i''''_{C_{1,A}} = \frac{i_g(d+1)}{2}$
$C_{2,A}$	$i'_{C_{2,A}} = \frac{i_g(d-1)}{2}$	$i''_{C_{2,A}} = \frac{i_g \cdot d}{2}$	$i'''_{C_{2,A}} = \frac{i_g \cdot d}{2}$	$i''''_{C_{2,A}} = \frac{i_g \cdot d}{2}$
$C_{3,A}$	$i'_{C_{3,A}} = \frac{i_g(d-1)}{2d}$	$i''_{C_{3,A}} = -\frac{i_g}{2}$	$i'''_{C_{3,A}} = -\frac{i_g}{2}$	$i''''_{C_{3,A}} = -\frac{i_g}{2}$
D_1	$i'_{D1} = \frac{i_g}{2}$	$i''_{D1} = \frac{i_g}{2}$	blocked	$i''''_{D1} = \frac{i_g}{2}$
D_2	$i'_{D2} = \frac{i_g(d-1)}{2d}$	blocked	blocked	blocked
D_3	blocked	$i''_{D3} = -\frac{i_g}{2}$	$i''_{D3} = -\frac{i_g}{2}$	$i''''_{D3} = -\frac{i_g}{2}$
S1	$i'_{S1} = \sqrt{\frac{i_g^2}{4d}}$	turned off	turned off	turned off
S_3	turned off	turned off	$i'''_{S3} = \frac{\sqrt{(i_g)^2 d}}{2}$	turned off

- The converter operates in continuous conduction mode.
- The switching frequency f_s should be much higher than the grid frequency f_g (voltage grid approximately constant within a switching period T_s).
- The input current ripple is neglected.
- The dc-link voltage is kept constant.
- All capacitance values are sufficiently large to keep their voltages constant over a switching period T_s.
- All components are ideal.

Considering that both input voltage v_g and input current i_g are purely sinusoidal and high-power factor operations, according to the equations in (10).

$$\begin{cases} v_g = V_{gp} \cdot \sin(\omega t) \\ i_g = I_{gp} \cdot \sin(\omega t) \end{cases} \tag{10}$$

where V_{gp} and I_{gp} are the grid peak voltage and the grid peak current, respectively.

Neglecting the average voltage across the input inductor L, which is calculated over a switching period T_s, then $v_g \approx \langle v_{ao} \rangle_{T_s}$, where $\langle v_{ao} \rangle_{T_s}$ is the average voltage between the nodes a and o, that is determined by equation (11) over a switching period T_s.

$$\langle v_{ao} \rangle_{T_s} = \frac{V_o}{4}(1-d) \cdot sign\{i_L\} \tag{11}$$

where d is the duty cycle and $sign\{i_L\}$ is the signal function of i_L. The duty cycle is related with modulation signals v_{modk} $k \in \{A, B\}$, as shown in Fig. 2(b), which is determined through the equation $d = \left(\frac{v_{modk}}{V_T}\right)$, where V_T is the peak of the triangular carrier. Isolating d in equation (11) it results the equation (12), that depicts the duty cycle variations.

$$d = 1 - M \cdot |\sin(\omega t)| \tag{12}$$

where M is the modulation index, that is determined by the equation $M = \left(\frac{4 \cdot V_{gp}}{V_o}\right)$, and V_o is the output voltage.

Therefore, the input inductor current equals the input current ($i_L = i_g$) and it depends on the duty cycle d. Given that, the quasi-instantaneous RMS current expressions are shown in Table 1 as a function of the input current i_g as well as the duty cycle d.

The average current expressions for the semiconductors are listed in Table 1, and the expressions for the RMS current are presented in Table 2 for switches S_1 and S_3, diodes D_1, D_2 and D_3, capacitors $C_{1,A}$, $C_{2,A}$ and $C_{3,A}$. All expressions are defined as functions of the modulation index M as well as the grid peak current I_{gp}.

D. INDUCTOR CURRENT RIPPLE

The envelope of the normalized input current through inductor L is defined by expressions in (13).

$$\overline{\Delta i}_{Lpk-pk} = \begin{cases} \frac{3}{8}Msen(\omega t) - \frac{M^2}{4}sen^2(\omega t) - \frac{1}{8} \ if \ \omega t > \theta_1 \\ \frac{M}{8}sen(\omega t) - \frac{M^2}{4}sen^2(\omega t) \ if \ \omega t < \theta_1 \end{cases} \tag{13}$$

where $\theta_1 = arcsin\left(\frac{1}{2M}\right)$, that corresponds to the boundary of level transition, as shown in Fig. 2(a), and $\overline{\Delta i}_{Lpk-pk}$ represents the normalized input current, that is determined by equation (14).

$$\overline{\Delta i}_{Lpk-pk} = \Delta i_{Lpk-pk} \frac{V_o}{4 \cdot L \cdot f_s} \tag{14}$$

Considering that the maximum current peak occurs when $\omega t = arcsin(\frac{1}{2M})$, leading to the normalized input current to $\overline{\Delta i}_{Lpk-pk} = 0.25$, with modulation index $M > 0.5$, that is one-fourth the input current i_g. Therefore, the input inductance value L is determined by equation (15).

$$L = \frac{V_o}{16 \cdot \Delta i_{Lpk-pk} \cdot f_s} \tag{15}$$

E. DC-LINK VOLTAGE RIPPLE

Considering that the capacitors $C_{3,k}$ $k \in \{A, B\}$ have low capacitance the dc-link voltage ripple Δv_{Co} is defined by the

TABLE 2. Semiconductors RMS current equations over a grid period.

Semiconductor	Effective current expression
$C_{1,A}$	$\mathrm{i}_{C1,A\,rms} = \frac{1}{8}\sqrt{\frac{3\,I_{gp}^2\left[-\frac{16}{3}\arctan\left(\frac{M}{\sqrt{-M^2+1}}\right)+\left[\left(M^4+4\,M^2+\frac{8}{3}\right)\pi-\frac{32}{3}M^3-\frac{16}{3}M\right]\sqrt{-M^2+1}-\frac{8}{3}\pi\right]}{\sqrt{-M^2+1}}}{\sqrt{\pi}\,M}}$
$C_{2,A}$	$\mathrm{i}_{C2,A\,rms} = \frac{\sqrt{-\frac{I_{gp}^2\,M(9\pi M-32)}{192}}}{\sqrt{\pi}}$
$C_{3,A}$	$\mathrm{i}_{C3,A\,rms} = \frac{1}{4}\sqrt{\frac{-\frac{I_{gp}^2\left[-4\arctan\left(\frac{M}{\sqrt{-M^2+1}}\right)+\left(M^2\pi+4\,M+2\pi\right)\sqrt{-M^2+1}-2\pi\right]}{\sqrt{-M^2+1}}}{\sqrt{\pi}M}}$
D_1	$\mathrm{i}_{D1\,rms} = \frac{\sqrt{\frac{I_{gp}^2\,M}{6}}}{\sqrt{\pi}}$
D_2	$\mathrm{i}_{D2\,rms} = \frac{\sqrt{3}}{12}\sqrt{\frac{2\,I_{gp}^2\left[-\frac{3}{2}\arctan\left(\frac{M}{\sqrt{-M^2+1}}\right)+\left(M^3+\frac{3}{8}\pi M^2+\frac{3}{2}M+\frac{3}{4}\pi\right)\sqrt{-M^2+1}-\frac{3}{4}\pi\right]}{\sqrt{-M^2+1}}}{\sqrt{\pi}\,M}}$
D_3	$\mathrm{i}_{D3\,rms} = \frac{\sqrt{\frac{I_{gp}^2\,M}{6}}}{\sqrt{\pi}}$
S_1	$\mathrm{i}_{S1\,rms} = \frac{1}{2}\sqrt{\frac{-\frac{I_{gp}^2\left[-16\arctan\left(\frac{M}{\sqrt{-M^2+16}}\right)+(M+2\pi)\sqrt{-M^2+16}-8\pi\right]}{\sqrt{-M^2+16}}}{\sqrt{\pi}\,M}}$
S_3	$\mathrm{i}_{S3\,rms} = \frac{\sqrt{-\left[\frac{I_{gp}^2(8\,M-3\pi)}{48}\right]}}{\sqrt{\pi}}$

output capacitance C_o through the dc-link capacitors $C_{j,k}$, $j \in \{1, 2\}$ $k \in \{A, B\}$, calculated by equation (16).

$$\Delta v_{Co} = \frac{P_o}{4 \cdot \pi \cdot f_g \cdot V_o \cdot C_o} \tag{16}$$

Considering to the dc-link voltage ripple, the output capacitance C_o is determined by equation (17).

$$C_o \geq \frac{P_o}{4 \cdot \pi \cdot f_g \cdot V_o \cdot \Delta v_{Co}} \tag{17}$$

The capacitance $C_{3,k}$ $k \in \{A, B\}$ are calculated according to partial-charge operation mode, that ensures that there are no current spikes [36]. Over the capacitors switching the current is limited by the series resistance of the capacitors and semiconductors circuit. Therefore, determining the circuit time constant τ, which is calculated using the expression $\tau = (r_{C3,k} \cdot C_{3,k})$, and the capacitor switching time using the expression $T_i = (M \cdot T_s)$ is necessary. Initially, the value of the switching frequency f_s is defined according to the semiconductors and input inductor losses. Subsequently, the values of the capacitors $C_{3,k}$, $k \in \{A, B\}$, and series resistance $r_{C3,k}$, $k \in \{A, B\}$ are defined through the manufacture datasheet. Finally, the condition $\tau > T_i$ must be satisfied to enable the partial-charge operation mode. In conclusion, verifying whether the switching capacitors can withstand the effective circuit current is necessary.

III. CONTROL STRATEGY

The control strategy developed for PFC operation of the proposed converter is shown in Fig. 6. The average current mode method was applied to equate the variables for the control loops of the input current i_g and output voltage V_o.

Owing to the interleaving connection, the input current i_g is divided into four components, which are the currents $i_{L_n}n \in \{1, .., 4\}$ of the interphase transformer inductors L_s. Thus, the input current is the sum of these currents, that is determined by expression $i_g = \Sigma i_{L_n}n \in \{1, .., 4\}$.

The output voltage control monitors the dc-link partial voltages v_{op} and v_{on} because the output voltage V_o is determined by the sum of these voltages, that is $V_o = (v_{op} + v_{on})$.

The measurement of the input voltage v_g is required to generate the control reference signal i_L^{ref}, which is applied to the current-loop to generate the modulation signals v_{mod_k} $k \in \{A, B\}$.

Finally, the modulation signals are compared using two comparators from the PWM scheme, as shown in Fig. 2(b), with the triangular carriers v_{tri_1} and v_{tri_2} to generate the command signals v_{gS_n} for the switches S_n $n \in \{1, .., 4\}$.

A. CURRENT-LOOP CONTROL

Current-loop control is illustrated in Fig. 6, which comprises the generation of the modulation signals $v_{mod,k}$ $k \in \{A, B\}$ following a sinusoidal reference i_L^{ref}, whose waveform is defined by the input voltage v_g and its amplitude is defined by

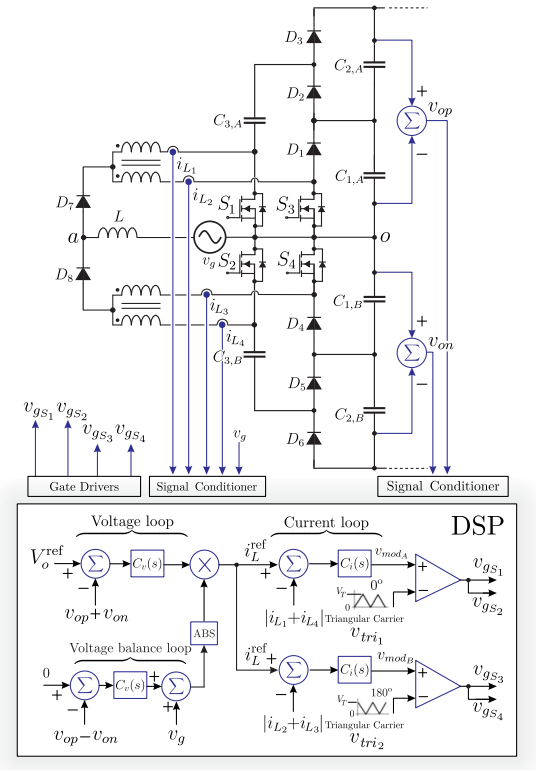

FIGURE 6. Control strategy of the input current i_{L_n} $n \in \{1, .., 4\}$ and partial voltages v_{op} and v_{on}.

voltage-loop control. Subsequently, the modulation signals are compared with the triangular carriers. Finally, the command signals v_{gsn} $n \in \{1, .., 4\}$ are generated for the switch gates.

Therefore, by defining the small-signal model and applying the Laplace transform, the transfer function is obtained in expression (18), that depicts variations in the inductor current with duty cycle.

$$G_i(s) = \frac{\widetilde{i}_L(s)}{\widetilde{d}(s)} = -\frac{V_o}{4 \cdot L \cdot s} \tag{18}$$

B. VOLTAGE-LOOP CONTROL

The voltage-loop control, shown in Fig. 6, generates the signal i_L^{ref}. The dynamics of the voltage-loop control must have a slow action, such that the sinusoidal reference signal does not oscillate.

The voltage balance loop produces a balance between the partial voltages v_{op} and v_{on} through the difference between them. The difference value is applied to a gain and then added to the input voltage signal.

To model the output voltage-loop control, it is assumed that the dc-link capacitors $C_{j,k}$ $j \in \{1, 2\}$ $k \in \{A, B\}$ have much higher capacitance than the capacitors $C_{3,k}, k \in \{A, B\}$. Capacitors $C_{j,k}$ $j \in \{1, 2\}$ $k \in \{A, B\}$ provide a low impedance path to 120 Hz ripples in instantaneous power and low ripple dc-link voltage.

Considering this, by applying the small-signal model and Laplace transform, the voltage-loop transfer function, which describes variations of the output voltage with the inductor current is provided by expression (19).

$$G_v(s) = \frac{\widetilde{V}_o(s)}{\widetilde{i}_L(s)} = \frac{V_{gp} \cdot R_o}{2 \cdot V_o}\left[\frac{1}{R_o \cdot C_o \cdot s + 2}\right] \tag{19}$$

IV. EXPERIMENTAL RESULTS

A. DESIGN CONSIDERATIONS

The experiments were carried out using the specifications of the design parameters presented in Table 3. The prototype was tested operating in a closed loop with control of the input current and output voltage under rated conditions.

TABLE 3. Design parameters.

Specification	Value
Input RMS voltage, $v_{g,rms}$	127 V
Output voltage, V_o	800 V
Grid frequency, f_g / Switching freq., f_s	60 Hz / 50 kHz
Rated output power, P_o	1.25 kW

The component specifications used for the prototype are listed in Table 4. For practical implementation, operating the converter in the partial-charge mode is adequate, as it results in a good relation between the peak current and capacitance [21].

TABLE 4. Laboratory prototype components.

Component	Description
Diode $D_n, n \in \{1, 2, 3, ...8\}$	IDH16S60C SiC Infineon
Input inductor, L	240 μH Magnetic Cor T255-34 Micrometal 54 turns 3x18 AWG
Coupled inductors, L_p	125 μH Magnetic Cor EE65/33/26 Thorton 31 turns 18AWG
Capacitors $C_{j,k}$, $j \in \{1, 2\}, k \in \{A, B\}$	B4345A9477M 470 μF 400 V Epcos
Capacitors $C_{3,k}, k \in \{A, B\}$	M10999100277G 60 μF 800 V Epcos
MOSFET $S_n, n \in \{1, 2, 3, 4\}$	IPW60R041P6 600 V Infineon
Digital signal processor (DSP)	TMS320F28379D Texas Inst.

The capacitors $C_{3,k}$ $k \in \{A, B\}$ have low capacitance value, then film capacitors were employed because they have low resistance and low parasitic inductance, leading to good performance in high frequency. The dc-link capacitors $C_{j,k}$ $j \in \{1, 2\}$ $k \in \{A, B\}$ electrolytic technologies were already used to absorb the oscillating power present at the frequency of 120Hz.

Fig. 7 shows the input voltage v_g, input current i_g, partial voltages v_{op} and v_{on}, and output voltage V_o. The output voltage is according to the desirable value, that is $V_o = 800$ V, with the partial voltages balanced $v_{op} = v_{on} \approx 400$ V, indicating good voltage regulation. In addition, the PFC operation is

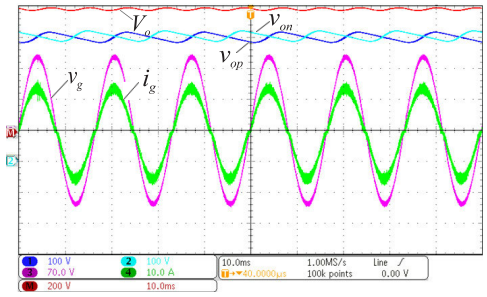

FIGURE 7. Input voltage v_g (70 V/div), input current i_g (10 A/div), partial voltages v_{op} and v_{on} (100 V/div), and output voltage V_o (200 V/div).

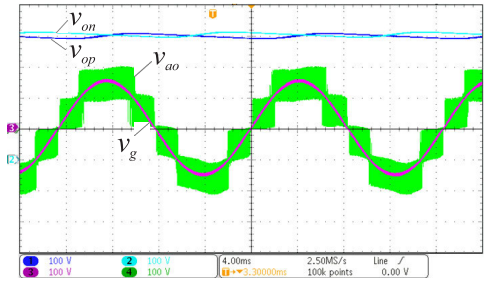

FIGURE 8. Input voltage v_g (100 V/div), switching terminal voltage v_{ao} (100 V/div), and partial voltages v_{op} and v_{on} (100 V/div).

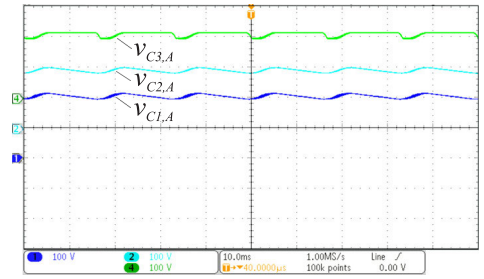

FIGURE 9. Capacitor voltages $v_{C_{1,A}}$, $v_{C_{2,A}}$, and $v_{C_{3,A}}$ (100 V/div).

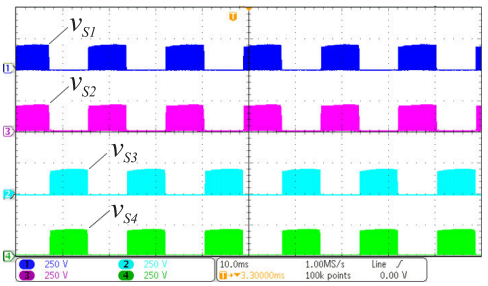

FIGURE 10. Switch voltages v_{Sn} $n \in \{1, .., 4\}$ (250 V/div).

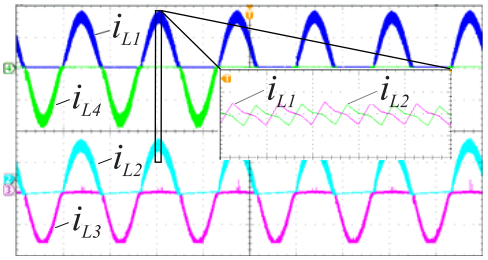

FIGURE 11. Interphase transformer cell current i_{Ln} $n \in \{1, .., 4\}$ (5 A/div).

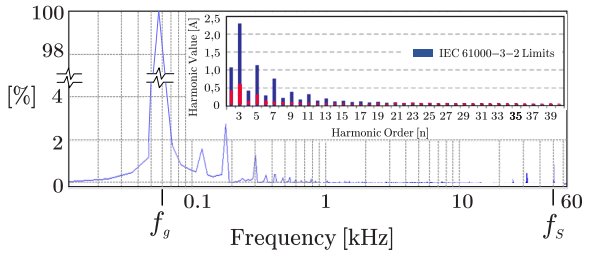

FIGURE 12. Input current harmonic spectrum under rated conditions.

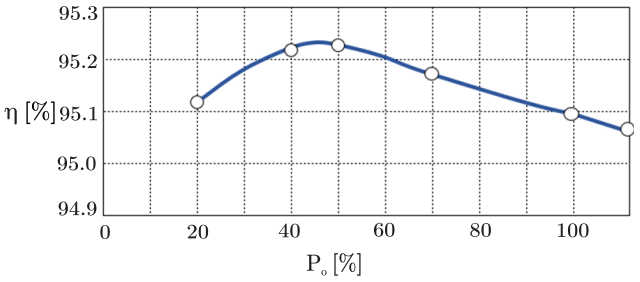

FIGURE 13. Efficiency curve of the laboratory prototype.

confirmed through the current and voltage input experimental waveforms, with a power factor of 0.986.

The switching terminal voltage v_{ao}, input voltage v_g and partial voltages v_{op} and v_{on} are shown in Fig. 8. The converter can impose voltage levels on its terminals, corresponding to $V_o/4 = +200$ V, $V_o/8 = 100$ V, 0, $-V_o/8 =$ -100 V, and $-V_o/4 = -200$ V.

Capacitor voltages are shown in Fig. 9. The voltage is one-fourth of the output voltage, which are $v_{C_{1,A}} = v_{C_{2,A}} = v_{C_{3,A}} = 200$ V.

The switch voltages v_{Sn}, $n \in \{1, .., 4\}$ are shown in Fig. 10 and they are one-fourth of the output voltage.

Fig. 11 represents the interphase transformer cell current i_{Ln} $n \in \{1, .., 4\}$. This confirm the reduction in current efforts owing to the use of the interleaving technique.

Fig. 11 shows the i_{L_1} and i_{L_2} waveforms are out of phase, so they tend to cancel each other out, thereby reducing the high frequency input ripple current, which is caused by the boost switching action.

The input current harmonic spectrum as a percentage of the fundamental component for the proposed converter operating at the rated power is shown in Fig. 12. The current spectrum is obtained from the current shown in Fig. 7, showing a current sinusoidal shape and in phase with the respective voltage. It has a THD $\approx$ 8.5%, that is accordingly IEC 61000-3-2 standard [37], and a power factor of 0.986. The harmonic components are compared with the harmonic limits of the

TABLE 5. Comparison of the proposed converter with other topologies.

Parameter	Topology				
Reference	[33]	[34]	[35]	[21]	Proposed Converter
Switch voltage	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{4}$	$\frac{V_o}{4}$
Capacitor voltage	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{4}$	$\frac{V_o}{4}$
Diode voltage	$\frac{V_o}{2}$	no diode	$\frac{V_o}{2}$	$\frac{V_o}{4}$	$\frac{V_o}{4}$
Active switch	2	5	2	4	4
Capacitor	3	3	3	6	6
Inductor	2	2	2	1	5
Fast diode	3	0	3	6	6
Slow diode	0	0	0	2	2
Static gain	$\frac{2}{(1-d)}$	$\frac{2}{(1-d)}$	$\frac{2}{(1-d)}$	$\frac{4}{(1-d)}$	$\frac{4}{(1-d)}$

IEC 61000-3-2 standard for class A equipment that have been measured for the load condition.

The converter efficiency was measured with a FLUKE Norma 4000 power analyzer and the results are shown in Fig. 13. When the converter operated under the rated condition the maximum efficiency achieved was $\eta \approx 95.1\%$ with an estimated value of conduction losses of 49.64 W and a power factor of 0.986. The experimental results indicate that the proposed converter is viable because it corresponds to the expected values according to the specifications in Table 3.

V. COMPARATIVE AND DISCUSSION

Table 5 presents a qualitative comparison of the proposed converter with other topologies. The topologies presented in [33]–[35] submit the semiconductors to (0.5 V_o), the static gain is twice the conventional boost topology, and are not designed for PFC operation. The converter presented in [21] has higher similarities with the proposed converter. It provides a static gain four times greater than the boost conventional topology, and the voltage across the semiconductors is (0.25 V_o), leading to lower voltage efforts. Although the proposed converter uses more components, owing to the use of the interleaving method the input inductor operates at twice switching frequency, reducing its bulk. The inductors of interphase transformers also have a bulk reduction because they only have a high frequency magnetic flux. In addition, it provides lower current efforts, allowing for higher power applications for PFC operation.

VI. CONCLUSION

In this paper a single-phase HSC interleaved AC-DC boost converter topology is proposed. The topology is derived from a family of high voltage gain single-phase HSC PFC rectifiers. All switches support one-fourth output voltage and low current efforts, owing to the use of the interleaving technique, leading to low conduction losses.

Through an extensive mathematical analysis and experimental results, is demonstrated the feasibility of the converter, that presents a low input current ripple, low harmonic distortion, and regulated output voltage. The converter has an efficiency of $\eta \approx 95.1\%$ under rated conditions.

The proposed converter is suitable for unidirectional applications that require high voltage gain, low current and voltage efforts, PFC operation, and an output voltage above 800 V.

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