Received September 14, 2021, accepted October 4, 2021, date of publication October 8, 2021, date of current version October 18, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3118897

Power Electronics Based on Wide-Bandgap Semiconductors: Opportunities and Challenges

GIUSEPPE IANNACCONE, (Fellow, IEEE), CHRISTIAN SBRANA, (Student Member, IEEE), IACOPO MORELLI, AND SEBASTIANO STRANGIO, (Member, IEEE)

Dipartimento di Ingegneria dell'Informazione, Università di Pisa, 56122 Pisa, Italy

Corresponding authors: Giuseppe Iannaccone (giuseppe.iannaccone@unipi.it) and Sebastiano Strangio (sebastiano.strangio@unipi.it)

This work was supported in part by the following projects: H2020 ECSEL-2017 REACTION under Grant 783158 and H2020 ECSEL-2019 PROGRESSUS under Grant 876868, and in part by the Ministero dell'Istruzione, dell'Università e della Ricerca (MIUR) CrossLab Departments of Excellence Grant.

ABSTRACT The expansion of the electric vehicle market is driving the request for efficient and reliable power electronic systems for electric energy conversion and processing. The efficiency, size, and cost of a power system is strongly related to the performance of power semiconductor devices, where massive industrial investments and intense research efforts are being devoted to new wide bandgap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN). The electrical and thermal properties of SiC and GaN enable the fabrication of semiconductor power devices with performance well beyond the limits of silicon. However, a massive migration of the power electronics industry towards WBG materials can be obtained only once the corresponding fabrication technology reaches a sufficient maturity and a competitive cost. In this paper, we present a perspective of power electronics based on WBG semiconductors, from fundamental material characteristics of SiC and GaN to their potential impacts on the power semiconductor device market. Some application cases are also presented, with specific benchmarks against a corresponding implementation realized with silicon devices, focusing on both achievable performance and system cost.

INDEX TERMS GaN, SiC, wide bandgap semiconductors, power devices, power converters.

I. INTRODUCTION

Silicon carbide (SiC) and gallium nitride (GaN) wide band-gap (WBG) semiconductors have been recently introduced in the power semiconductor market to complement and/or replace silicon devices [1]. In addition to better device-level performance [2], the key properties of these materials can bring advantages at the system level [3]–[5], leading to improved power efficiency, reduced size and weight and, possibly, lower overall cost [6]–[9].

In the application spectrum, two partially overlapping areas for SiC and GaN can be identified on the basis of system power and switching frequency. SiC is preferred for higher output power applications (typically also associated to higher operating voltage): trains and electric vehicles [10], [11], battery chargers for electric vehicles [12], renewable energy [13], [14], industrial automation [8]. GaN, on the other hand, is today suitable for higher switching frequency, lower power/voltage applications [4], [15], such as consumer systems [16], and data centers [17]. GaN devices still suffer from some reliability issues, which is limiting their deployment for high-voltage applications. As the GaN fabrication process will become more mature and the device reliability will correspondingly improve, the GaN application area will expand towards higher voltage and power.

In terms of market penetration in the power semiconductor industry, WBG semiconductor devices enjoy rapid growth but are still limited to niches: probably due to a limited technology maturity, power GaN devices have total annual revenue that is 0.1% of the global power semiconductor market, and more than one order of magnitude smaller than that of SiC devices, according to [18]. However, according to market predictions, both SiC and GaN revenues will increase with a cumulative annual growth rate of 35% and 75% in the next five years, respectively [18]. This means that in 5 years GaN could reach the same market share as the one of SiC today, while SiC could rise to about 10% of the power electronics market.

In this paper we discuss the perspectives of GaN and SiC technology in the power electronics market, ranging from

The associate editor coordinating the review of this manuscript and approving it for publication was Derek Abbott.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

material fundamentals to intrinsic advantages in power converter systems, analyzing technology maturity, device reliability and the power semiconductor market.

II. WIDE BANDGAP MATERIALS: PROPERTIES, TECHNOLOGICAL MATURITY, COST AND DEVICES

We limit our consideration to 4-H SiC and GaN, the most relevant WBG materials from the industrial point of view, and of course we will use silicon technology – the dominant and most mature technology for electronics – as the reference benchmark in our discussion.

A. BASIC PROPERTIES OF WBG MATERIALS

A comparative analysis of fundamental properties of semiconductors for power semiconductors is shown in **Figure 1**. If we look at the meaningful properties for high voltage operations, WBG materials have a wide energy bandgap, above 3 eV, which leads to a large breakdown electric field of about 3 MV/cm, 10 times higher than that of silicon. This is an important property for obtaining large blocking voltage and therefore high-voltage operation.

Baliga FOM = $\mu \varepsilon E_{BD}^3$

	Si CMOS	4H-SiC CMOS	GaN HEMT
Critical Electric Field [MV/cm]	0.3	3	3.5
Energy Bandgap [eV]	1.12	3.23	3.4
Electron Mobility [cm^2/(V s)]	500	35	1500
Electron Saturation Velocity [10^7 cm/s]	1	1.8	3.4
Thermal Conductivity (W/(K cm)]	1.3	3.7	1.5
Melting Point [K]	1412	3103	2500
Baliga Figure of Merit (normalized to Si)	1	59	3916

FIGURE 1. Wide bandgap material fundamentals. Data from [7] and [18].

Mobility and saturation velocity in the two-dimensional (2D) channel of a Field-Effect Transistor (FET) are relevant for high switching frequency. SiC is at disadvantage with respect to silicon because defects at the interface reduce mobility with respect to both the ideal 2D mobility and the bulk mobility [19], [20]. Beyond the effort in improving channel mobility, today one can choose devices in which transport occurs in the bulk, such as JFETs [21], [22]. GaN, instead, has an advantage in terms of the achievable 2D mobility [23], due to a very high density of the 2D electron gas at the GaN/AlGaN interface, and modulation doping using AlGaN piezoelectric properties [24].

In addition, both SiC and GaN have higher saturation velocity than silicon. Regarding the possibility to use a higher switching frequency, there is a clear advantage for GaN FETs and a more limited one for SiC JFETs. In addition to the electrical characteristics, also thermal properties are critical for power systems, that can reach a high operating temperature. Considering this aspect, both SiC and GaN have a significant advantage in terms of both thermal conductivity and melting point with respect to silicon, with SiC very well positioned.

B. MATURITY OF WBG MATERIAL TECHNOLOGIES

Fundamental properties of materials can be translated into device-level figures of merit (FOMs). The comparison of novel devices fabricated after 2015 (Silicon Super-Junctions MOSFETS [25], 4H-SiC MOSFETs [26] and GaN FETs [27]) with ideal limits based on one-dimensional p-n junctions [28] is useful to estimate the maturity of each technology and to evaluate the available room for improvement. For instance, the parameters related to high voltage operation and resistive power loss are well captured by the so-called Baliga FOM (B_{FOM}) [28], which is essentially a normalized breakdown voltage at on-state resistance parity for a unipolar device based on one-dimensional electrostatics. B_{FOM} is proportional to the carrier mobility and to the third power of the breakdown electric field E_{BV}. The B_{FOM} is typically normalized to the one of silicon and is relevant for the operation of unipolar devices such as MOSFETs and High-Electron-Mobility Transistors (HEMTs). The intrinsic advantage of WBG materials with respect to silicon is of orders of magnitude, especially in the case of GaN (**Figure 1**), due to the combined effect of large breakdown field (11.6× higher than the silicon one) and high mobility (3× higher than the silicon one).

The reported fundamentals of WBGs explain the industrial research interest, but a semiconductor technology requires much more than pure potential to be deployed in large-volume applications. Silicon is always the default choice, because of the deep knowledge available, the huge investment already made in the technology, the manufacturing maturity, and the impressive economies of scale. To evaluate how far we are now from the intrinsic potential of WBG materials, following the derivation of B_{FOM}, we can determine an intrinsic limit per each material, which becomes a line in the log-log plot of the on-resistance R_{ON} versus the breakdown voltage V_{BD}, shown in **Figure 2** for silicon, SiC and GaN. One can move the design point of the device along the line by appropriately tuning the thickness of the drift region and the doping. In the same plot, symbols indicate results corresponding to experimental devices.

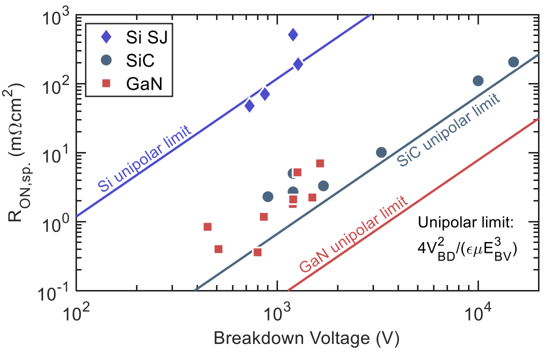
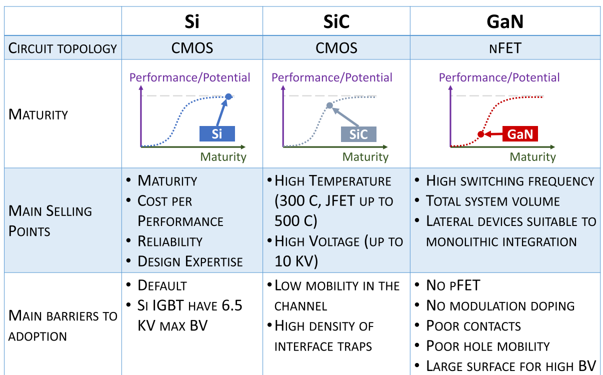


FIGURE 2. Si, SiC, GaN: device performance against theoretical limits. Data from [25] (silicon super-junctions), [26] (SiC MOSFETs) and [27] (GaN FETs). Theoretical limits calculated according to [28].

Commercial silicon devices already reach the so-called limit and, some specific device architectures such as super-junction (SJ) MOSFETs actually can surpass the "silicon limit" [25], [29], [30], because they exploit

sophisticated three-dimensional electrostatics engineering, whereas the Baliga FOM is based on the assumption of basic one-dimensional p-n junctions. SiC is not far from the limit, but still has some room for improvement. In the case of GaN, on the other hand, we are rather far from the limit, even if commercial GaN power devices are already competitive, especially in the low V_{BD}, low R_{ON} region. This lag is motivated by the limited maturity of the GaN technology.

Figure 3 summarizes the advantages and disadvantages of the considered semiconductor options. Silicon of course offers high maturity and reliability, low cost per device and broadly available design expertise, so it is still the default choice. Silicon also offers complementary devices, with all the well-known advantages in terms of flexibility in the choice of the circuit topology. There are some intrinsic limits, due to relatively small bandgap limiting the maximum V_{BD} at a given R_{ON}. SiC comes next, it also offers complementary devices and has almost reached an adult maturity. Given the mobility issues, its main selling point is the operation at high voltage and high temperature. The reduced device size, smaller than silicon at the same V_{BD} due to the higher breakdown field, results in lower switching loss, enabling its operation at higher switching frequency. Still, some barriers to adoption remain, especially due to the low channel mobility and high density of interface traps [31]. These issues are relevant for FETs where the conduction takes place at the semiconductor/oxide interface. This is the reason why SiC JFETs, where the conduction takes place in a buried channel, have found a role in the power device market [2]. Finally, GaN is the extremely promising but still immature player. The main problems are the effective doping, poor contacts, and low hole mobility [3], [18], [32]. Only n-channel devices are industrially available, and there is active research on p-channel devices [33]–[35]. Its main selling points are the high switching frequency and consequently the lower total system volume and, often, the total system cost. In addition, present GaN devices are lateral, therefore are suitable for monolithic integration of devices and other functional blocks (e.g. drivers). For this reason, monolithic integration of power GaN circuits is recently offered also as a foundry service and is still a hot industrial research topic [36], [37].



	Si	SiC	GaN
Circuit topology	CMOS	CMOS	nFET
Maturity	Performance/Potential, Maturity, Si	Performance/Potential, Maturity, SiC	Performance/Potential, Maturity, GaN
Main selling points	• Maturity • Cost per performance • Reliability • Design expertise	• High temperature (300 C, JFET up to 500 C) • High voltage (up to 10 KV)	• High switching frequency • Total system volume • Lateral devices suitable to monolithic integration
Main barriers to adoption	• Default • Si IGBT have 6.5 KV max BV	• Low mobility in the channel • High density of interface traps	• No pFET • No modulation doping • Poor contacts • Poor hole mobility • Large surface for high BV

FIGURE 3. Si, SiC, GaN: comparative table with main features.

WBG semiconductor market size can also provide an indication of their technology maturity. In **Figure 4**, recent market assessment and predictions [18] are shown (Q4 2020, already considering the COVID19 slowdown). The growth of power SiC device market revenue in 2020 has been in the single digit range (∼7%), while the annual growth of the market of SiC devices from 2021 to 2025 is predicted to be in the 20 ∼ 50% range (**Figure 4(a)**), exceeding 3 B$ in 2025 (**Figure 4(b)**). As a reference, in 2020 the global semiconductor market has been in excess of 300 B$ and the power semiconductor market in excess of 30 B$ [18], so in 2020 SiC market represented only 2% of the power semiconductor market, but it is predicted to increase up to 10% in 2025. The market predictions for power GaN devices exhibit a sharp increase, with limited revenue in 2020 (about 40 M$) but growing up to 680 M$ by 2025, which would correspond approximately to a five-year delay with respect to the market for SiC. Most of the revenue is driven by the low-end of the market, consumer products such as chargers and displays [9], and by datacenters [38].

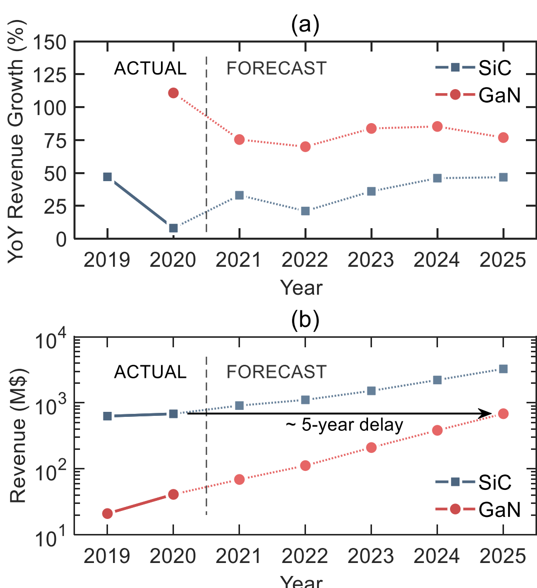


FIGURE 4. Power SiC and GaN market revenue and forecast until 2025. Data from [18].

C. WBG FIELD-EFFECT-TRANSISTORS

Today SiC MOSFETs are available in two main structures, as depicted in **Figure 5**: planar and trench. A critical issue of these devices is the low mobility, due to the relatively high interface trap density, which is limiting the R_{ON}.

In the range 1.2 KV – 6.5 KV, SiC MOSFETs are reliable and can replace silicon MOSFETs. SiC MOSFETs with a breakdown voltage up to 15 kV have been fabricated [39], but the achieved R_{ON} is still too high to make the case for applications. Therefore, to practically move to this voltage range, a significant improvement in channel mobility is

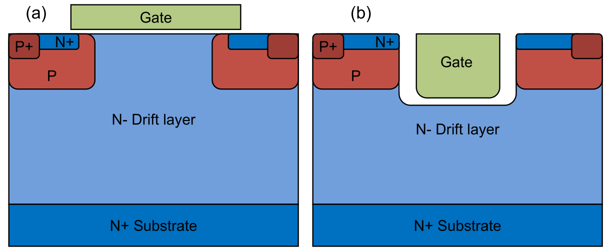


FIGURE 5. Two typical SiC MOSFET flavors: (a) planar and (b) trench. Figure adapted from [8].

needed in SiC MOSFETs. The other option is to rely on SiC IGBTs [39], [40] in order to exploit the advantage of modulation doping. These are both active areas of research, not yet translated to industrial production.

The core of a GaN HEMT is the AlGaN/GaN heterostructure, illustrated in **Figure 6**. Due to a small lattice mismatch, the AlGaN layer is subjected to tensile strain. This has an important effect, because AlGaN is a piezoelectric material and therefore a polarization field is formed in the AlGaN layer, which induces the formation of a 2D electron gas in GaN at the interface with AlGaN. So, with no impurities and with a very smooth interface we have a high electron mobility, reaching up to 1500 $cm^2/(V{\cdot}s)$, coupled with a high 2D carrier density in the order of 10^{13} cm^{-2}.

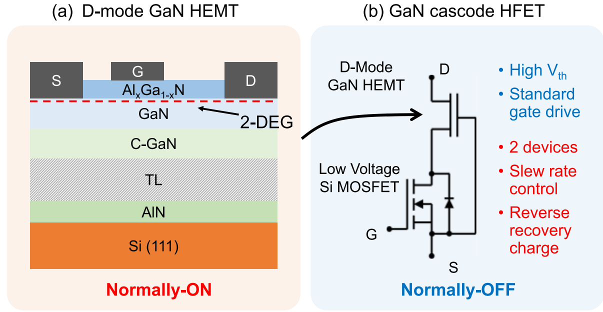


FIGURE 6. (a) Normally ON GaN HEMT and (b) GaN cascode basic topology.

The industrial standard for power applications is to grow GaN on silicon wafers, in order to reduce wafer costs. This involves growth optimization and superlattice engineering to manage the lattice mismatch between Si and GaN, while preserving a high quality GaN/AlGaN interface. The growth process starts from 111 Si wafers, and then a stack of transition layers is grown with gradual lattice mismatch, with the goal of confining the dislocations in the bottom layers and to obtain a high quality GaN layer at the top. The AlGaN layer is also used as a gate dielectric, representing a somewhat good, but suboptimal, insulator. This configuration leads naturally to a depletion-mode FET, commonly known as a "normally-ON" device, with a negative threshold voltage. For basic functional security requirements, a "normally-off" operation is largely preferred in power applications.

There are a few options for achieving normally-off operation. The first one having industrial relevance is the GaN cascode (**Figure 6b**), in which a hybrid Si/GaN circuit block is used, coupling the depletion-mode FET with a low-voltage silicon MOSFET with positive threshold voltage [41], [42]. The GaN HEMT is at the output port of the resulting device, playing the voltage-blocking role. The problem here is that two devices are needed and that there is significant reverse recovery charge during turn-off. In addition, the expected high-temperature behavior of the GaN HEMT is limited by the silicon MOSFET. An alternative option for achieving a normally-off device is the Metal-Insulator-Semiconductor-HEMT (MIS-HEMT), based on a recessed gate obtained by eliminating the AlGaN layer in the underneath region, leading to a depletion of the inversion layer (**Figure 7a**). An additional conformal insulating layer is needed, leading to dielectric reliability issues and instability of the threshold voltage (V_{th}), which are not totally solved issues [43]. A better option is the use of a p-GaN gate [44], [45], by growing an additional p-doped GaN layer before deposition of the gate contact (illustrated in **Figure 7b**). Reliability of the gate in this case is improved, but a large gate leakage can represent a real disadvantage. The additional advantage (compared to the cascode solution) is that the recovery charge is negligible. The concepts based on the AlGaN/GaN heterostructure feature an additional limit at the input port side, due to the limited energy gap of AlGaN, smaller than that of a classic insulating oxide. There is a limit on the maximum voltage that can be applied to the gate (∼5 V) in order to keep the gate leakage current under control, which then poses a tradeoff on the choice of V_{th}: the higher the V_{th}, the lower the ON-state overdrive, and then the higher the R_{ON}.

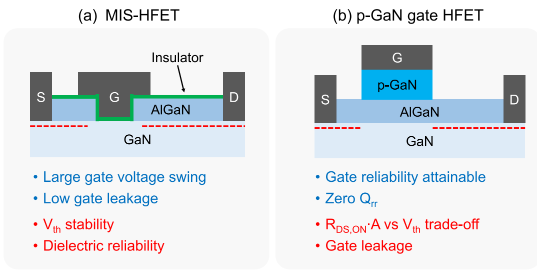


FIGURE 7. Alternative normally-OFF GaN HFET concepts: (a) GaN MIS-HEMT and (b) p-GaN HFET.

D. RECENT GENERATIONS OF POWER DEVICES

Considering the spectrum of traditional circuit converters for power solutions, they are mainly based on silicon MOSFETS and IGBTs [6].

Silicon MOSFETs typically operate at high switching frequency (100-200 kHz) and relatively low voltage range (well below 1 kV), representing the most competitive solution for consumer applications which rely on power converters operating up to 100 W or below. The Infineon CoolMOS superjunction (SJ) MOSFETs [46], for instance, have been recently released and are particularly suited for low-power switched-mode power supply (SMPS) applications [6].

Considering the possible alternatives based on WBG semiconductors, Infineon and Panasonic have recently announced that a second generation of 650 V GaN devices is expected to be released in the first half of 2023 [47].

IGBTs, on the other hand, typically operate at lower switching frequency (10-20 kHz) and are suited for medium-to-high-power applications involving high voltage and current, for instance for inverters driving the electric traction motor of hybrid and electric vehicles (see for example the Infineon TRENCHSTOP IGBT technologies [48]). In this scenario, SiC MOSFETs are gaining momentum: one example is the Infineon CoolSiC family [49], with SiC MOSFETs available in the 650 V, 1200 V and 1700 V classes. As far GaN, although industrial research is directed at devices for these power and voltage ranges, the highest voltage option available today is provided by Transphorm, with a cascode device operating up to 900 V [41].

III. RELIABILITY ISSUES OF GaN-on-Si HEMTs

GaN-on-Si technology still presents significant reliability issues, that are discussed in the literature and are the main reason why the performance available devices is very much below the intrinsic limitations of the material. In the following, we discuss two examples from the recent literature.

A. DEGRADATION OF THE DYNAMIC ON RESISTANCE

During hard switching operation, there is a phase in which the device is in the so-called semi-ON condition, characterized by the simultaneous occurrence of high drain voltage and current. This *semi-ON stress* causes a degradation of the GaN HEMT R_{ON}, that is only slowly recovered, and that has an impact on performance, in terms of higher switching loss, either due to the higher R_{ON} or to the fact that devices are used at lower-than-nominal blocking voltage.

Such degradation is intuitively attributed to negative charge trapping: however, it is important to understand where such charge is localized, why it is trapped and how to mitigate the problem. The latest understanding is that degradation is due to the joint effect of surface and buffer layer charge trapping [48].

This understanding has been gained by fabricating two identical devices S1 and S2 with a different thickness of the low-carbon-doped buffer, corresponding to different distances between the high-carbon doped buffer and the 2D electron gas (smaller for S1, larger for S2 as in **Figures 8a-b**). Effects of semi-ON stress are measured using pulsed stress test. Results after a 10 μs stress corresponding to V_D = 50 V and V_G = 2 V are shown in **Figures 8c-d**: the effect is apparent for both devices, and is much larger for device S1 especially at high temperature. This supports the hypothesis that both surface trapping and trapping in the high-carbon doped layer are responsible for this behavior: in the S2 device the high-carbon doped region is far from the 2DEG, so the increase in R_{ON} is only due to surface trapping, however, the much higher increase of R_{ON} in device S1 can be due to an additional effect, such as trapping in the high-carbon doped layer. This is confirmed by TCAD simulations.

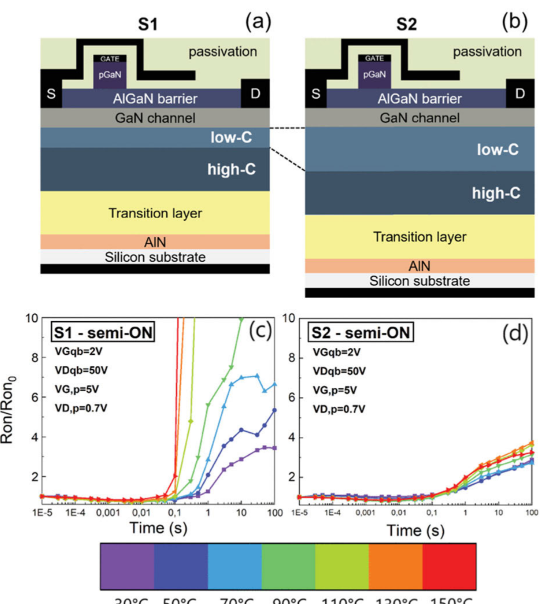


FIGURE 8. Schematic device structure of GaN gate HEMTs. Device S1 (a) has a much smaller thickness of the lowly doped carbon buffer region compared with device S2 (b). Measured dR_{ON} as a function of the stress time for temperatures ranging between 30 °C and 150 °C. (c) S1 semi-ON stress (d) S2 semi-ON stress. Figures from [48].

B. THRESHOLD VOLTAGE INSTABILITY OF pGaN HFETs

Dynamic effects such as the instability of the threshold voltage [44], are critical issues in pGaN HFETs. The instability of the threshold voltage is related to the nature of the ohmic gate contact. Indeed, the pGaN/AlGaN/GaN structure can be modeled as a p-n diode, with the addition of a metal-semiconductor contact represented by the metal gate contact and the pGaN region. In **Figure 9**, two pGaN HFET structures are reported, which feature a different metal gate work-function. The first one has a very low Schottky barrier, so that the metal contact is practically ohmic. The drawback is that significant gate current flows when the p-n diode is directly biased. This practically limits the gate overdrive and therefore the minimum R_{ON}. The second option is to create a Schottky barrier between the metal gate and the pGaN, in order to have a truly rectifying contact: the resulting structure can be modeled by two back-to-back diodes, with gate leakage effectively suppressed irrespective of the applied overdrive needed to achieve low R_{ON}. A critical issue of this second approach is the significant V_{th} instability, which leads either to an effective increase of the R_{ON} (if the V_{th}

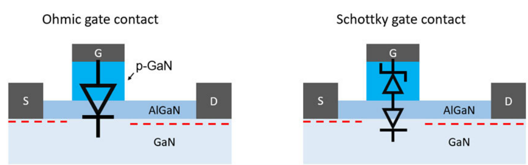


FIGURE 9. pGaN gate HFET structures with (a) ohmic and (b) Schottky contacts between the metal gate and the p-GaN region, depending on the metal gate workfunction considered in [44].

variation is positive), or to a spurious device turn-on (if the V_{th} variation is negative).

A detailed analysis has been performed on device samples fabricated by Infineon Technologies, by coupling both experiments and TCAD simulations [44]. A double pulse (stress and measure) test approach was used, by applying a gate voltage V_{GS} pulse for 1 ms with $V_{DS} = 0$, and then measuring the gate current I_G for a given V_{GS} and low V_{DS} for 1 μs. This cycle was repeated by increasing the V_{GS} in the measurement phase, in order to draw a complete pulse I_D-V_{GS} transfer characteristic of the stressed device and to extract the resulting V_{th} variation (ΔV_{th}). A contour plot of the ΔV_{th} as a function of the gate stress voltage and for variable resulting I_G is reported in **Figure 10(a)** for a Schottky device. In **Figure 10(b)**, experimental results for both ohmic and Schottky contact cases are reported. In addition, by including the essential physical effects involved in the device operation and after a careful calibration of the TCAD simulation deck, similar trends were also reproduced by means of simulations, enabling a microscopic understanding on the underlying physical phenomena. When charge is trapped in the pGaN, a variation of threshold voltage occurs, with a mechanism similar to the basic operation of Flotox nonvolatile memories [51]. When the Schottky diode is inversely biased at a sufficiently high voltage (high V_{GS}), holes can tunnel from the metal into the pGaN, and therefore the V_{th} decreases. When the p-n junction is forward biased, electrons are injected in the pGaN and holes escape the pGaN so the V_{th} increases. The prevailing effect depends on the balance between the current through the Schottky diode and the p-n diode, which is a function of both the Schottky barrier height and the applied voltage. This can be understood by comparing results for the cases of ohmic and Schottky contacts: in the first case, hole injection always dominates, and therefore the ΔV_{th} is always negative and increases (in absolute value) for increasing gate stress; in the latter case, when a high Schottky barrier is created, at low gate voltage stress hole injection prevails ($\Delta V_{th} < 0$), whereas for higher gate voltage stress electron injection through the forward biased p-n junction becomes dominant and the ΔV_{th} becomes positive.

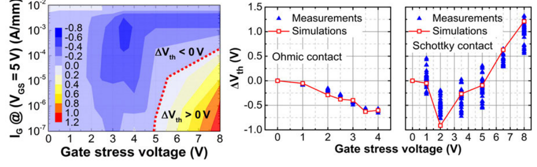


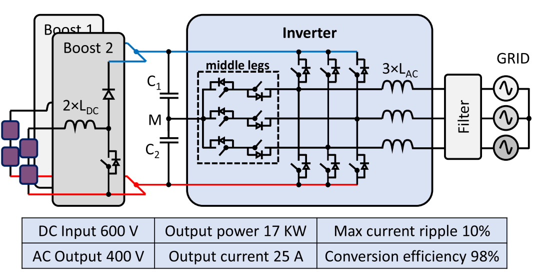
FIGURE 10. **pGaN HFET threshold voltage instability. Color map of the threshold voltage variation ΔV_{th} vs gate stress and gate current (left). Comparison between experiments and simulations of ΔV_nth vs gate stress voltage for the device with ohmic contacts (center) and Schottky contacts (right). Figures from [44] and [45].**

IV. GaN AND SiC EXAMPLE APPLICATIONS

We now discuss specific applications of WBG semiconductor devices, focusing on the possible advantages over similar power converter systems realized with silicon devices. Beyond the possibility to reach high efficiency, which is of course crucial, we consider some case studies to show that the overall cost of a system realized with WBG devices can be lower than the one realized with standard silicon, if the systems are designed for the same specifications. This outcome is counterintuitive, due to the higher cost of WBG devices for a given specification (e.g. V_{BD} or R_{ON}). However, it can be shown that thanks to the capability of WBG to operate at higher frequency and/or at higher temperature, the other system costs can be reduced. One example is represented by the passive components (inductors and capacitors), which can be much smaller and cheaper at higher switching frequency, for similar ripple and power loss conditions; another example is the possibility to save on costs related to heat dissipation, given the higher operating temperature that can be tolerated.

A. SiC INVERTERS FOR PV SYSTEMS

As a first example we consider regenerative energy source applications, as in the case of power converters employed to transfer the DC voltage power provided by photovoltaic (PV) panels to the grid AC voltage. In particular, we illustrate the case of 17 kW inverter options for PV systems which have been designed and reported in [14]. The system schematics and main specifications are reported in **Figure 11**: different PV strings operate in parallel and are connected to the DC input BUS through independent DC/DC converters working under maximum power point tracking (MMPT) conditions; by assuming a DC input bus of 600 V and an AC output bus of 400 V for insertion in the grid, each inverter has been designed to reach a conversion efficiency of 98%. The reference is a state-of-the-art 3-Level topology, provided by many PV inverter manufacturers [52]: realized with Si IGBTs, it can be operated at a switching frequency of 16 kHz by employing an inductance value L_{AC} of 2.5 mH to obtain a maximum peak-to-peak current ripple of 10% of the nominal output current ($I_{out,RMS} = 25$ A). For the same topology and ripple condition, the use of fast switching devices enables an increase of the switching frequency, with a proportional scaling of the output inductance. As a further step, the middle legs can be omitted to get a two-level topology, at the cost of a doubling of the frequency needed to keep the same ripple. Additional design details can be found in [14].



DC Input 600 V	Output power 17 KW	Max current ripple 10%
AC Output 400 V	Output current 25 A	Conversion efficiency 98%

FIGURE 11. **Multi-string PV solar inverter schematic and main specifications considered in Ref. [14].**

Hence, from the devices point of view, the considered options with a blocking voltage V_{BD} of 1200 V are: Infineon silicon IGBTs (High-Speed 3 module, I_{DC} = 80 A), or Infineon SiC JFETs (I_{DC} = 45 A or 60 A) in cascode configuration (connected in series with low-voltage power p-channel MOSFETs) to obtain normally-off behavior. Three different converter architectures are considered: 1) three-level (3L) converter with silicon IGBTs, 2) 3L converter with cascode SiC JFETs (45 A) in the half-bridges and Si IGBTs in the middle legs, 3) two-level (2L) converter with cascode SiC JFETs (60 A). SiC devices are smaller and with smaller intrinsic capacitances, therefore can be operated at 3× and 6× higher switching frequency (for the 3L and 2L case, respectively) with respect to the silicon case, without sacrificing the efficiency (note that the switching loss, extracted by circuit simulations, are actually lower, irrespective of the higher switching frequency). A much smaller inductor can be used at higher switching frequency for the same ripple conditions, implying a relevant cost reduction. Considering that the power loss of SiC inverters is lower than the one realized with Si IGBTs (despite the higher switching frequency), cheaper heat sinks and inverter housings can be adopted, with additional savings.

The main cost factors are summarized in the bar chart in **Figure 12**: the devices (green), the inductor (orange), and the housing (including the sink, blue). Even if SiC devices cost about twice as much as a Si IGBTs, the other costs present a higher absolute reduction, so that total costs are reduced by about 20%. Furthermore, an additional cost advantage could be obtained by scaling the device cost itself, and this aim could be achieved soon for SiC due to the increase of production volume as predicted by market forecast discussed in previous section.

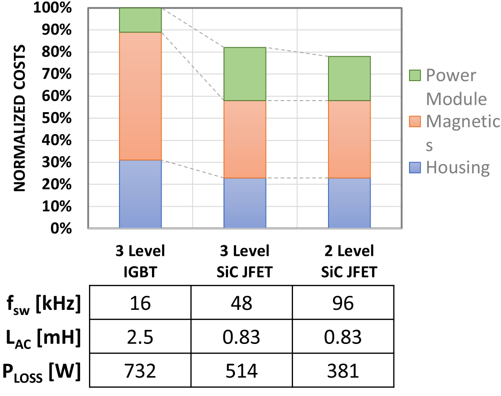
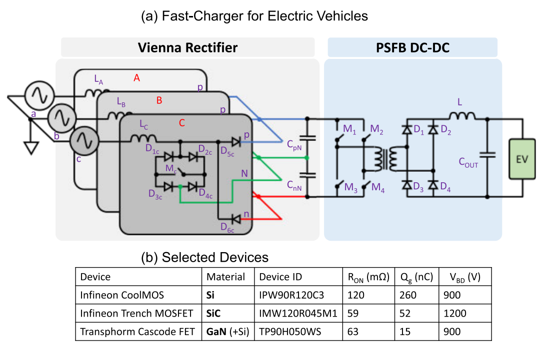


FIGURE 12. Example of SiC system cost analysis using data from [14].

B. GaN AND SiC RECTIFIERS AND DC/DC CONVERTERS FOR ELECTRIC VEHICLE ULTRA-FAST CHARGERS

The electrification of vehicles provides new application cases for power converters. For instance, due to forthcoming explosion of the electric vehicle (EV) market, ultra-fast charging infrastructures are needed, requiring up to 350 kW to be transferred to the EV battery without compromising the converter system reliability and with limited temperature increase due to Joule heating [53]. WBG materials can represent the perfect candidate for these applications, due to the capability to operate at high blocking voltages and to manage the big amount of power which must be transferred from the grid to the EV.

A charger is normally composed by two stages, a three-phase rectifier in boost mode and an isolated DC/DC converter in step-down mode, such as the case depicted in **Figure 13(a)**. Modular approaches are normally exploited to split the total power among several rectifiers and DC/DC converter modules. By referring to a three-switch unidirectional boost converter topology (Vienna [57]) for the rectifier, and to an isolated Phase-Shift Full-Bridge (PSFB) converter topology [58] for the DC/DC converter stage, we have selected both active and passive components for various design proposals and simulated the conversion efficiency as a function of the switching frequency.



(b) Selected Devices

Device	Material	Device ID	R_{ON} (mΩ)	Q_g (nC)	V_{BD} (V)
Infineon CoolMOS	**Si**	IPW90R120C3	120	260	900
Infineon Trench MOSFET	**SiC**	IMW120R045M1	59	52	1200
Transphorm Cascode FET	**GaN** (+Si)	TP90H050WS	63	15	900

FIGURE 13. (a) EV fast charger converter module realized with a Vienna rectifier (left) and a PSFB DC/DC converter (right). (b) Selected transistors for the design examples.

Three versions of each topology have been considered, each based on different power transistors in the 1 kV V_{BD} range, as reported in **Figure 13(b)**: Infineon Si CoolMOSs (IPW90R120C3, V_{BD} = 900 V, I_{DC} = 36 A) [59], Infineon SiC Trench MOSFET (IMW120R045M1, V_{BD} = 1200 V, I_{DC} = 52 A) [60], and Transphorm Cascode GaN FETs (TP90H050WS, V_{BD} = 900 V, I_{DC} = 34 A) [61]. One should note that in the considered V_{BD} scale various options for silicon and SiC devices are available. As for GaN, although there is research efforts on 1200 V FETs [65]–[67], today only the selected 900 V GaN FET is available, realized with a cascode topology where a low-voltage Si MOSFET drives a normally-ON GaN HEMT [61].

We have designed scaled converter modules operating up to 17.5 kW, by assuming to realize a full ultrafast charger system with 20 blocks operating in parallel to reach the 350 kW target. Each design has been optimized depending on the switching frequency, by selecting passive components (capacitors and magnetics) for the same ripple conditions. The resulting full power conversion efficiency as a function of the switching frequency is reported in Figure 14, for the

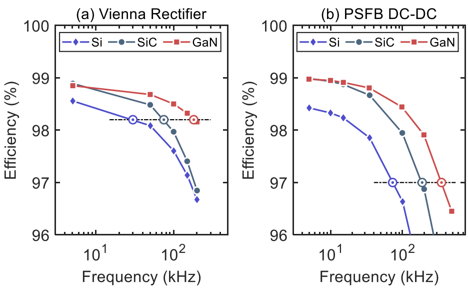


FIGURE 14. Conversion efficiency as a function of the switching frequency for the Vienna rectifier (a) and PSFB DC/DC converter (b) realized with either Si, SiC or GaN transistors.

Vienna rectifier (a) and PSFB DC/DC converter (b). At relatively low frequency, similar efficiency is exhibited by the SiC and the GaN options, due to comparable device R_{ON}, while featuring a 50% reduction of power loss with respect to the silicon counterparts. A higher efficiency is also shown if the frequency is increased, especially for the GaN case, due to smaller intrinsic capacitances. Then, for each converter implementation (that is for any Vienna rectifier and PSFB DC/DC converter), the switching frequency has been selected depending on the considered transistor, as the frequency that enables to reach a conversion efficiency of 98.2% for rectifiers and 97% for the DC/DC converter.

With these assumptions, the three Vienna rectifiers and DC/DC converter implementations can be easily compared in terms of charger total cost and total volume, by neglecting housing and sinks that would be very similar due to fixed power loss, if devices work at the same temperature. In **Figure 15** we have summarized the cost and volume comparison, normalized to the total cost and volume of the whole Si system (Vienna rectifier + DC/DC converter), by including only selected transistors and passive components. Results are reported for three Vienna rectifier cases (cost and volume in (a) and (c), respectively), as well as for three PSFB DC/DC converter cases (cost and volume in (b) and (d), respectively). If we analyze the obtained results, in case of WBG systems the device cost is always higher than the one of the silicon counterpart and represents a big fraction (in the rectifiers) or almost the total cost (in the DC/DC converter) of the components. However, due to higher switching frequency enabled by WBG semiconductor devices (especially for GaN) at similar efficiency conditions, much cheaper and smaller passive components can be selected. For this reason, for both rectifier and DC/DC converter cases, the two options based on Si devices turn out to be the most cumbersome.

C. GaN 48V-12V BIDIRECTIONAL DC/DC CONVERTER

Considering applications of GaN devices, several case studies can be found in the data center segment, where power electronics systems are needed for the power distribution to the racks and to the single boards. We have several DC/DC converters: from 400 V to 48 V, then from 48 V to 12 V, on the board, and then from 12 V to 1 V for the single microprocessors [62]. We can focus on the 48-12 V converter, which is also useful for example for the automotive sector,

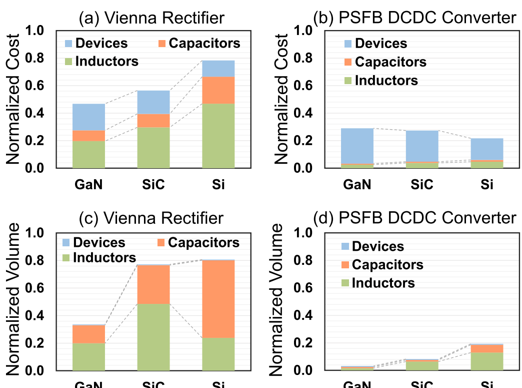
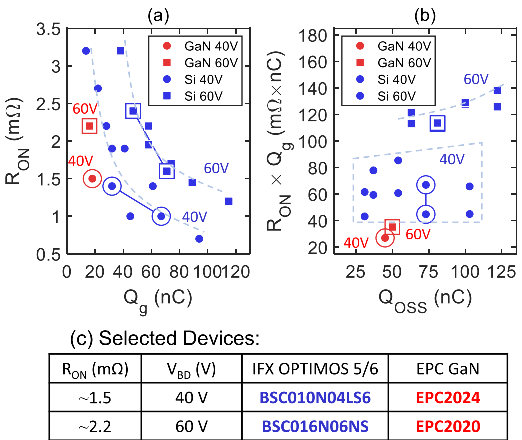


FIGURE 15. Cost and volume analysis for Vienna rectifiers (a and c, respectively) and PSFB DC/DC (b and d, respectively) converter implementations based on Si [59], SiC [60] and GaN [61] devices. Costs (volumes) are normalized to the total cost (volume) of the Si system (rectifier + DC/DC converter).

to connect in a bidirectional way the 48 V and the 12 V batteries for balance charging [63].

We benchmark an implementation with GaN HEMTs with one implemented with Si MOSFETs. As for the switches, both 40 V and 60 V low-voltage power transistors are needed. We have selected the 40/60 V EPC Enhancement-mode GaN FETs [54] and the Infineon OptiMOS5/6 class as best-in-class Si device families for the same blocking voltage level. R_{ON} versus gate charge Q_G and $R_{ON} \times Q_G$ versus Q_{OSS} FOMs are reported in **Figure 16**. A bidirectional converter implemented with the switched-capacitor architecture sketched in **Figure 17** is used for the comparison [62], based on a series-parallel topology augmented with a small inductor to reduce power loss due to charging and discharging of the charge pump flying capacitors.



R_{ON} (mΩ)	V_{BD} (V)	IFX OPTIMOS 5/6	EPC GaN
~1.5	40 V	BSC010N04LS6	EPC2024
~2.2	60 V	BSC016N06NS	EPC2020

FIGURE 16. Considered 40 V and 60 V Si and GaN power devices for the bidirectional power converter.

We have selected Si (BSC010N04LS: $V_{BD} = 40$ V, $I_{DC} = 281$ A and BSC016N06NS, $V_{BD} = 60$ V, $I_{DC} = 225$ A) and GaN (EPC2024: $V_{BD} = 40$ V, $I_{DC} = 90$ A and EPC2020, $V_{BD} = 60$ V, $I_{DC} = 90$ A) transistors with similar R_{ON} (i.e. similar conduction-loss) for both 40 V and 60 V domains.

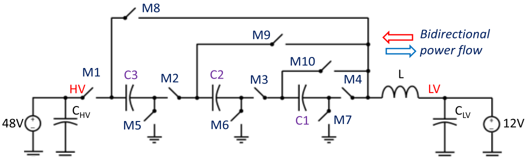


FIGURE 17. Series/parallel hybrid switched-capacitor/inductor 48 V / 12 V bidirectional converter schematic.

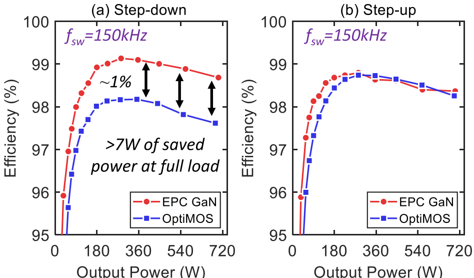


FIGURE 18. Efficiency as a function of the output power of the bidirectional 48 V / 12 V switched-capacitor topology realized with either EPC GaN FETs or Infineon OptiMOS transistors.

However, despite the similar R_{ON} values, for the same breakdown voltage the GaN version always benefits from lower Q_G and Q_{OSS}. One should note that conduction loss in a switched-capacitor DC-DC converter is proportional to an equivalent output resistance [55], depending not only to the R_{ON} of the switches but also on capacitors implementing the particular topology, which dominate at low frequency (slow-switching loss [55]), where the flying capacitors experience a large voltage variation ΔV_{Cf} at each switching cycle. This low-frequency power loss can be reduced by increasing the capacitance or, rather, by adding a small inductor enabling soft-charging of flying capacitors [56] with almost constant current. Finally, at very high switching frequency, switching loss due to charging and discharging of transistor intrinsic capacitances is expected to dominate.

GaN and Si implementations of the DC/DC converter have been operated at 150 kHz: the selected frequency is high enough to render the slow-switching loss negligible, and not so high to highlight differences in switching loss due to different device capacitances. Therefore, the similar device R_{ON} should guarantee a similar performance in terms of conversion efficiency. In **Figure 18** the converter efficiency in step-down (a) and step-up (b) mode is reported for both GaN and Si converters. Only the GaN converter (red curves) achieves the best performance in both operation modes, with a full load efficiency of $\sim$98.5% and peak efficiency close to 99%. The Si converter, instead, can reach similar performance only in one conversion direction, that is in step-up mode. An analysis on the current waveforms has highlighted that Si devices feature slower turn-on and turn-off, then a higher peak current flows through the switches to guarantee the same charge transfer among flying capacitors, leading to overall higher RMS current and then to higher conduction loss, irrespective of the R_{ON} similar to the GaN device.

V. CONCLUSION

The fundamental properties of wide bandgap semiconductors show that GaN and SiC have the potential to push the performance of power electronics well beyond what can be obtained with silicon devices. If the intrinsic limitations of materials are considered, the performance of GaN and SiC devices has much more room for improvement than that of Si devices. Therefore, market penetration of WBG semiconductors is presently limited by the maturity of the corresponding technology, impacting device performance and reliability.

We have shown, however, that even the presently expensive and suboptimal GaN and SiC devices can provide significant cost advantage at performance parity at the system level with respect to Si devices. Indeed, the higher device cost is more than compensated by the lower cost of passive components, enabled by the higher switching frequency at switching loss parity. System cost savings can also increase if WBG devices can be operated at higher temperature, reducing the costs of heat removal and of package and enabling smaller form factors. As fabrication technology improves and defects are reduced, advantages will become larger fostering higher market penetration and an increased silicon replacement.

REFERENCES

[1] P. R. Wilson, B. Ferreira, J. Zhang, and C. DiMarino, "IEEE ITRW: International technology roadmap for wide-bandgap power semiconductors: An overview," *IEEE Power Electron. Mag.*, vol. 5, no. 2, pp. 22–25, Jun. 2018, doi: 10.1109/MPEL.2018.2821938.

[2] J. Millan, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[3] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[4] K. J. Chen, O. Häberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[5] A. Q. Huang, "Power semiconductor devices for smart grid and renewable energy systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2019–2047, Nov. 2017, doi: 10.1109/JPROC.2017.2687701.

[6] M. Parvez, A. T. Pereira, N. Ertugrul, N. H. E. Weste, D. Abbott, and S. F. Al-Sarawi, "Wide bandgap DC–DC converter topologies for power applications," *Proc. IEEE*, vol. 109, no. 7, pp. 1253–1275, Jul. 2021, doi: 10.1109/JPROC.2021.3072170.

[7] S. J. Bader, H. Lee, R. Chaudhuri, S. Huang, A. Hickman, A. Molnar, H. G. Xing, D. Jena, H. W. Then, N. Chowdhury, and T. Palacios, "Prospects for wide bandgap and ultrawide bandgap CMOS devices," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4010–4020, Oct. 2020, doi: 10.1109/TED.2020.3010471.

[8] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017, doi: 10.1109/TIE.2017.2652401.

[9] L. Spaziani and L. Lu, "Silicon, GaN and SiC: There's room for all: An application space overview of device considerations," in *Proc. IEEE 30th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2018, pp. 8–11, doi: 10.1109/ISPSD.2018.8393590.

[10] S. Yu, J. Wang, X. Zhang, Y. Liu, N. Jiang, and W. Wang, "The potential impact of using traction inverters with SiC MOSFETs for electric buses," *IEEE Access*, vol. 9, pp. 51561–51572, 2021, doi: 10.1109/ACCESS.2021.3069268.

[11] C. Zhang, S. Srdic, S. Lukic, Y. Kang, E. Choi, and E. Tafti, "A SiC-based 100 kW high-power-density (34 kW/L) electric vehicle traction inverter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 3880–3885, doi: 10.1109/ECCE.2018.8558373.

[12] H. V. Nguyen, D.-C. Lee, and F. Blaabjerg, "A novel SiC-based multifunctional onboard battery charger for plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5635–5646, May 2021, doi: 10.1109/TPEL.2020.3026034.

[13] M. Abbasi, R. Emamalipour, M. A. M. Cheema, and J. Lam, "A new fully magnetically coupled SiC-based DC/DC step-up LLC resonant converter with inherent balanced voltage sharing for renewable energy systems with a medium voltage DC grid," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 5542–5547, doi: 10.1109/ECCE.2019.8911905.

[14] G. U. Schwarzer, S. Buschhorn, and K. Vogel, "System benefits for solar inverters using SiC semiconductor modules," *Proc. PCIM Eur.*, 2014, pp. 787–794.

[15] Y. Guan, Y. Wang, D. Xu, and W. Wang, "A 1 MHz half-bridge resonant DC/DC converter based on GaN FETs and planar magnetics," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2876–2891, Apr. 2017, doi: 10.1109/TPEL.2016.2579660.

[16] A. Martinez-Perez, A. K. Solomon, A. Castellazzi, and B. Lu, "GaN-based consumer application DC-DC converter for PCB embedment technology integration," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Nov. 2015, pp. 2100–2105, doi: 10.1109/IECON.2015.7392411.

[17] M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48-V VRM with intermediate bus voltage optimization for data centers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 702–715, Feb. 2021, doi: 10.1109/JESTPE.2020.2976107.

[18] (2020). *Yolé Market Forecast for Power semiconductors*. [Online]. Available: http://www.yole.fr/Compound_Semiconductor_Monitor_Q4_2020.aspx

[19] H. A. Moghadam, S. Dimitrijev, J. Han, D. Haasmann, and A. Aminbeidokhti, "Transient-current method for measurement of active near-interface oxide traps in 4H-SiC MOS capacitors and MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2670–2674, Aug. 2015, doi: 10.1109/TED.2015.2440444.

[20] Y. Wang, W. Xu, G. Han, T. You, F. Mu, H. Hu, Y. Liu, X. Zhang, H. Huang, T. Suga, X. Ou, X. Ma, and Y. Hao, "Channel properties of Ga_2O_3-on-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1185–1189, Mar. 2021, doi: 10.1109/TED.2021.3051135.

[21] M. Kaneko and T. Kimoto, "High-temperature operation of n- and p-channel JFETs fabricated by ion implantation into a high-purity semi-insulating SiC substrate," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 723–726, May 2018, doi: 10.1109/LED.2018.2822261.

[22] V. Veliadis, B. Steiner, K. Lawson, S. B. Bayne, D. Urciuoli, H. C. Ha, N. El-Hinnawy, S. Gupta, P. Borodulin, R. S. Howell, and C. Scozzie, "Reliable operation of SiC JFET subjected to over 2.4 million 1200-V/115-A hard switching events at 150 °C," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 384–386, Mar. 2013, doi: 10.1109/LED.2013.2241724.

[23] *NSM Archive—Physical Properties of Semiconductors*. Accessed: Sep. 2, 2021. [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/

[24] V. N. Popok, P. A. Caban, P. P. Michalowski, R. Thorpe, L. C. Feldman, and K. Pedersen, "Two-dimensional electron gas at the AlGaN/GaN interface: Layer thickness dependence," *J. Appl. Phys.*, vol. 127, no. 11, Mar. 2020, Art. no. 115703, doi: 10.1063/1.5142766.

[25] Z. Cao and L. Jiao, "Superjunction LDMOS with dual gate for low on-resistance and high transconductance," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 890–896, 2020, doi: 10.1109/JEDS.2020.3011929.

[26] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Appl. Phys. Rev.*, vol. 2, no. 2, Jun. 2015, Art. no. 021307, doi: 10.1063/1.4922748.

[27] M. F. Fatahilah, K. Strempel, F. Yu, S. Vodapally, A. Waag, and H. S. Wasisto, "3D GaN nanoarchitecture for field-effect transistors," *Micro Nano Eng.*, vol. 3, pp. 59–81, May 2019, doi: 10.1016/j.mne.2019.04.001.

[28] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1811–1823, Sep. 1989, doi: 10.1109/16.34247.

[29] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction power devices, history, development, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 713–727, Mar. 2017, doi: 10.1109/TED.2017.2658344.

[30] H. Kang and F. Udrea, "True material limit of power devices—Applied to 2-D superjunction MOSFET," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1432–1439, Apr. 2018, doi: 10.1109/TED.2018.2808181.

[31] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015, doi: 10.1109/TED.2014.2356172.

[32] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008, doi: 10.1109/TDMR.2008.923743.

[33] N. Chowdhury, J. Lemettinen, Q. Xie, Y. Zhang, N. S. Rajput, P. Xiang, K. Cheng, S. Suihkonen, H. W. Then, and T. Palacios, "p-channel GaN transistor based on p-GaN/AlGaN/GaN on Si," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1036–1039, Jul. 2019, doi: 10.1109/LED.2019.2916253.

[34] H. Hahn, B. Reuters, A. Pooth, B. Holländer, M. Heuken, H. Kalisch, and A. Vescan, "p-channel enhancement and depletion mode GaN-based HFETs with quaternary backbarriers," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3005–3011, Oct. 2013, doi: 10.1109/TED.2013.2272330.

[35] Z. Zheng, W. Song, L. Zhang, S. Yang, J. Wei, and K. J. Chen, "High I_{ON} and I_{ON}/I_{OFF} ratio enhancement-mode buried *p*-channel GaN MOSFETs on *p*-GaN gate power HEMT platform," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 26–29, Jan. 2020, doi: 10.1109/LED.2019.2954035.

[36] H.-Y. Chen, Y.-Y. Kao, Z.-Q. Zhang, C.-H. Liao, H.-Y. Yang, M.-S. Hsu, K.-H. Chen, Y.-H. Lin, S.-R. Lin, and T.-Y. Tsai, "A fully integrated GaN-on-silicon gate driver and GaN switch with temperature-compensated fast turn-on technique for improving reliability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 460–462, doi: 10.1109/ISSCC42613.2021.9365828.

[37] A. Li, M. Cui, Y. Shen, Z. Li, W. Liu, I. Z. Mitrovic, H. Wen, and C. Zhao, "Monolithic comparator and sawtooth generator of AlGaN/GaN MIS-HEMTs with threshold voltage modulation for high-temperature applications," *IEEE Trans. Electron Devices*, vol. 68, no. 6, pp. 2673–2679, Jun. 2021, doi: 10.1109/TED.2021.3075425.

[38] K. George and S. Ang, "Topology survey for GaN-based high voltage step-down single-input multi-output DC-DC converter systems," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2016, pp. 340–343, doi: 10.1109/WiPDA.2016.7799964.

[39] M. Kim, J. J. Forbes, E. A. Hirsch, J. Schrock, S. Lacouture, A. Bilbao, S. B. Bayne, H. K. O'Brien, and A. A. Ogunniyi, "Evaluation of long-term reliability and overcurrent capabilities of 15-kV SiC MOSFETs and 20-kV SiC IGBTs during narrow current pulsed conditions," *IEEE Trans. Plasma Sci.*, vol. 48, no. 11, pp. 3962–3967, Nov. 2020, doi: 10.1109/TPS.2020.3030295.

[40] S. Chowdhury and T. P. Chow, "Performance tradeoffs for ultra-high voltage (15 kV to 25 kV) 4H-SiC n-channel and p-channel IGBTs," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Jun. 2016, pp. 75–78, doi: 10.1109/ISPSD.2016.7520781.

[41] *Transphorm USA, GaN Technology: Cascode vs. e-mode*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.transphormusa.com/en/gan-technology/#casecode-vs-e-mode

[42] P. Parikh, Y. Wu, L. Shen, R. Barr, S. Chowdhury, J. Gritters, S. Yea, P. Smith, L. McCarthy, R. Birkhahn, M. Moore, J. McKay, H. Clement, U. Mishra, R. Lal, P. Zuk, T. Hosoda, K. Shono, K. Imanishi, and Y. Asai, "GaN power commercialization with highest quality-highest reliability 650 V HEMTs-requirements, successes and challenges," in *IEDM Tech. Dig.*, Dec. 2018, pp. 19.7.1–19.7.4, doi: 10.1109/IEDM.2018.8614579.

[43] N. Zagni, M. Cioni, A. Chini, F. Iucolano, F. M. Puglisi, P. Pavan, and G. Verzellesi, "Mechanisms underlying the bidirectional V_T shift after negative-bias temperature instability stress in carbon-doped fully recessed AlGaN/GaN MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2564–2567, May 2021, doi: 10.1109/TED.2021.3063664.

[44] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018, doi: 10.1109/TED.2018.2828702.

[45] L. Savadi, G. Iannaccone, S. Sicre, S. Lavanza, G. Fiori, O. Haberlen, and G. Curatola, "Charge injection in normally-off p-GaN gate AlGaN/GaN-on-Si HFETs," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2018, pp. 18–21, doi: 10.1109/ESSDERC.2018.8486899.

[46] *Infineon: 500V-950V N-Channel Power MOSFET*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/500v-950v/

[47] *Infineon Market News: Infineon and Panasonic Accelerate GaN Technology Development for 650 V GaN Power Devices*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.infineon.com/cms/en/about-infineon/press/market-news/2021/INFPSS202109-094.html
[48] *Infineon: IGBTs—Insulated Gate Bipolar Transistors*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/
[49] *Infineon: Silicon Carbide CoolSiC MOSFETs*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/
[50] A. Minetto, B. Deutschmann, N. Modolo, A. Nardo, M. Meneghini, E. Zanoni, L. Sayadi, G. Prechtl, S. Sicre, and O. Häberlen, "Hot-electron effects in AlGaN/GaN HEMTs under semi-ON DC stress," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4602–4605, Nov. 2020.
[51] C. Papadas, G. Ghibaudo, G. Pananakakis, C. Riva, and P. Ghezzi, "Model for programming window degradation in FLOTOX EEPROM cells," *IEEE Electron Device Lett.*, vol. 13, no. 2, pp. 89–91, Feb. 1992, doi: 10.1109/55.144968.
[52] (2018). *Texas Instruments Design Guide TIDA-01606: 10-kW, Bidirectional Three-Phase Three-Level (T-Type) Inverter and PFC Reference Design*. [Online]. Available: https://www.ti.com/lit/pdf/tidue53
[53] X. Liang, S. Srdic, J. Won, E. Aponte, K. Booth, and S. Lukic, "A 12.47 kV medium voltage input 350 kW EV fast charger using 10 kV SiC MOSFET," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 581–587, doi: 10.1109/APEC.2019.8722239.
[54] A. Lidow, M. D. Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*, 3rd ed. Hoboken, NJ, USA: Wiley, 2019.
[55] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008, doi: 10.1109/TPEL.2007.915182.
[56] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015, doi: 10.1109/TPEL.2014.2377738.
[57] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004, doi: 10.1109/TIE.2004.825341.
[58] R. Ramachandran, M. Nymand, C. Østergaard, C. Kjeldsen, and G. Kapino, "High efficiency 20 kW SiC based isolated DC-DC converter for battery charger applications," in *Proc. 20th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, 2018, pp. 1–9.
[59] *Infineon IPW90R120C3*. Accessed: Oct. 9, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/500v-950v/ipw90r120c3/
[60] *Infineon IMW120R045M1*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/discretes/imw120r045m1/
[61] *Transphorm TP90H050WS*. Accessed: Sep. 2, 2021. [Online]. Available: https://www.transphormusa.com/en/product/tp90h050ws-2/
[62] S. Saggini, O. Zambetti, R. Rizzolatti, M. Picca, and P. Mattavelli, "An isolated quasi-resonant multiphase single-stage topology for 48-V VRM applications," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6224–6237, Jul. 2018, doi: 10.1109/TPEL.2017.2740058.
[63] T. Kim and S. Kwak, "A flexible voltage bus converter for the 48-/12-V dual supply system in electrified vehicles," *IEEE Trans. Veh. Technol.*, vol. 66, no. 3, pp. 2010–2018, Mar. 2017, doi: 10.1109/TVT.2016.2570817.
[64] S. Strangio and G. Iannaccone, "A 700 W bidirectional 48V/12V switched capacitor converter realized with GaN FET transistors," Dept. Inf. Eng., Univ. Pisa, Pisa, Italy, Tech. Rep., 2021.
[65] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V normally off GaN-on-Si field-effect transistors with low dynamic on-resistance," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 632–634, May 2011, doi: 10.1109/LED.2011.2118190.
[66] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, "1200 V GaN vertical fin power field-effect transistors," in *IEDM Tech. Dig.*, Dec. 2017, pp. 9.2.1–9.2.4, doi: 10.1109/IEDM.2017.8268357.
[67] Y. Wang, G. Lyu, J. Wei, Z. Zheng, J. He, J. Lei, and K. J. Chen, "Characterization of static and dynamic behavior of 1200 V normally off GaN/SiC cascode devices," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10284–10294, Dec. 2020, doi: 10.1109/TIE.2019.2959512.

GIUSEPPE IANNACCONE (Fellow, IEEE) received the M.S. and Ph.D. degrees in EE from the University of Pisa, in 1992 and 1996, respectively. He is currently a Professor of electronics with the University of Pisa. He has coordinated several European and national projects involving multiple partners and has acted as principal investigator in several research projects funded by public agencies at the European and national level, and by private organizations. He co-founded the academic spinoff Quantavis s.r.l. and is involved in other technology transfer initiatives. He has authored or coauthored more than 230 articles published in peer-reviewed journals and more than 160 papers in proceedings of international conferences, gathering more than 8500 citations on the Scopus database. His research interests include quantum transport and noise in nanoelectronic and mesoscopic devices, development of device modeling tools, new device concepts and circuits beyond CMOS technology for artificial intelligence, cybersecurity, implantable biomedical sensors, and the Internet of Things. He is a fellow of the American Physical Society.

CHRISTIAN SBRANA (Student Member, IEEE) received the B.S. and M.S. degrees *(cum laude)* in electronic engineering from the University of Pisa, Italy, in 2018 and 2021, respectively. He is currently pursuing the Ph.D. degree in electronics with the University of Pisa, working on the industrial IoT sensors for harsh environments and analog-based physical unclonable functions (PUFs). Starting from his master's thesis titled "Analysis and Design of DC/DC Converters for Electric Vehicles Fast Charging Applications Implemented With Wide Bandgap Semiconductor Devices." He is also with Quantavis s.r.l. His research interests include power management and integrated design on WBG materials, analog and mixed-signal ICs design and sensors for the IoT systems.

IACOPO MORELLI received the B.S. and M.S. degrees in electronic engineering from the University of Pisa, in 2018 and 2021, respectively, with a master's thesis on a three-phase rectifier stage for fast chargers of electric vehicles. He worked on the design of rectifier modules realized with GaN and SiC devices to improve the system performance. He is currently working as a Test Development Engineer with Microtest.

SEBASTIANO STRANGIO (Member, IEEE) received the B.S. and M.S. degrees *(cum laude)* in EE, and the Ph.D. degree from the University of Calabria, Cosenza, Italy, in 2010, 2012, and 2016, respectively. He was with IMEC, Leuven, Belgium, as a Visiting Student, in 2012, working on the electrical characterization of resistive-RAM memory cells. From 2013 to 2016, he was a Temporary Research Associate with the University of Udine, and with the Forschungszentrum Jülich, Germany, as a Visiting Researcher, in 2015, researching on TCAD simulations, design, and characterization of TFET-based circuits. From 2016 to 2019, he was with LFoundry, Avezzano, Italy, where he worked as a Research and Development Process Integration and Device/TCAD Engineer, with main focus on the development of a CMOS Image Sensor Technology Platform. He is currently a Researcher in electronics with the University of Pisa. He has authored or coauthored over 30 articles, most of them published in IEEE journals and conference proceedings. His research interests include technologies for innovative devices (e.g. TFETs) and circuits for innovative applications (CMOS analog building blocks for DNNs), as well as CMOS image sensors, power devices and circuits based on wide-bandgap materials.