

Received September 27, 2021, accepted October 2, 2021, date of publication October 8, 2021, date of current version November 11, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3119039

Comprehensive and Simplified Numerical Design Procedure for Class-E Switching Circuits

WENQI ZHU¹, (Graduate Student Member, IEEE),
YUTARO KOMIYAMA¹, (Graduate Student Member, IEEE),
KIEN NGUYEN¹, (Senior Member, IEEE), AND
HIROO SEKIYA¹, (Senior Member, IEEE)

Graduate School of Science and Engineering, Chiba University, Chiba 263-8522, Japan

Corresponding author: Hiroo Sekiya (hiroo.sekiya@ieee.org)

This work was supported by the Ministry of Internal Affairs and Communications of Japan through a grant entitled “Research and Development of Wireless Control Technology in the Millimeter-Wave Band for Wire-Free Robots” under Grant JPJ000254.

ABSTRACT This paper proposes comprehensive and simplified numerical design procedures for the class-E switching circuits with the Particle Swarm Optimization (PSO) algorithm. The PSO algorithm does not require approximate solutions and partial differentiation derivations. Therefore, the proposed design method has higher convergence stability than Newton’s method-based design. It is also a feature that the PSO algorithm allows the mismatch between the design condition and the design parameter numbers. As a design example, we successfully draw the multiple design curves of the class-E amplifier and frequency multipliers by one-time optimization execution with the modified PSO algorithm. Besides, we show a pretty simple design procedure of the class-E amplifier, which uses only one evaluation function for determining three design parameters. The design accuracy of the proposed design method does not deteriorate compared with the previous design method. We carried out circuit experiments, which achieved power-conversion efficiency of 94.0%. The circuit experiment showed agreement with numerical predictions, which confirmed the validity and usefulness of the proposed design method.

INDEX TERMS Resonant inverters, resonant converters, wireless power transmission, soft switching, class-E inverter.

I. INTRODUCTION

High frequency amplifiers have been used in a wide range of applications, such as wireless power transfer (WPT) systems [1]–[5], resonant power converters [6]–[13], and induction heating [14], [15]. It is effective to increase the switching frequency for the size reduction of the magnetic components. With the development of the next-generation wide-bandgap semiconductors such as Gallium Nitride (GaN), it becomes possible to push the switching frequency up to the ISM-frequency band, such as 6.78 MHz and 13.56 MHz [1]–[4], [12], [13].

At high-frequency operations, switching loss dominates and results in low efficiency. For reducing the switching loss, the soft-switching technique is mandatory. The class-E switching circuit families, such as

class-E [1], [3]–[5], [7]–[10], [14], [16]–[28], class-DE [13], [29], and class-EF [1], [30] amplifiers, have gained researcher’s interest in recent years. This is because they can achieve the class-E zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions, which reduces the switching loss significantly. One of the main research topics of the class-E switching circuits is to establish the design method according to different operating modes since the class-E switching circuit was invented about 40 years ago.

Generally, the design methods of the class-E switching circuits can be divided into two approaches: the analytical design [1]–[3], [16], [17], [23], [29] and the numerical one [7], [18]–[20], [31]. By adopting analytical design procedures, we can explicitly comprehend the relationship between circuit component values and parameters, which helps to intuitively and comprehensively understand the circuit characteristics. However, specialized knowledge and strenuous efforts are necessary to derive the analytical equations.

The associate editor coordinating the review of this manuscript and approving it for publication was Sze Sing Lee¹.

For example, the class-E switching circuits have different operation modes with identical circuit topology, including the class-E amplifier and frequency multipliers [26]–[28]. It is necessary to derive analytical equations with hard effort according to the amplifier and the frequency multiplier types individually despite the same circuit topology. Additionally, the assumptions for idealizations are needed to express the circuit characteristics in mathematical formulas, which causes the lack of design accuracy. At ISM-band frequencies, however, the designers require more accurate component values.

The numerical design procedures [7], [18]–[20], [31] can consider complicated circuit characteristics. Therefore, the accuracies of the numerical design results are improved compared with the analytical designs. In the designs of the class-E inverter, the algebraic equation solver, such as Newton's method, is widely used for obtaining the nominal design values [7], [18]–[20]. However, there are several limitations and issues in Newton's method-based designs. Because Newton's method is an equation solver, the number of design conditions should be the same as the adjustable parameters. Besides, it is impossible to give the design conditions, which are expressed by inequality. Newton's method requires approximate solutions for algorithm convergence as initial algorithm values in the computation algorithm, which are not easy to obtain. Additionally, the partial differentiation of the algebraic equations is also required in the algorithm, which needs complicated computations to derive [31]. The accuracies of the initial values and the partial differentiation affect the convergence stability of Newton's method algorithm. Additionally, it is hard to comprehend the relationship between parameters and circuit characteristics because Newton's method provides only one "optimal point" in the parameter space with one algorithm execution. A comprehensive and straightforward design method is expected. For example, the design procedure, which simultaneously provides design curves of all the operation modes with one-time algorithm execution, is user-friendly.

This paper proposes comprehensive and simplified numerical design procedures of the class-E switching circuits with a heuristic optimization algorithm. Our idea is to apply the Particle Swarm Optimization (PSO) algorithm to the class-E switching circuit designs. By utilizing the features of the PSO algorithm, the proposed design method does not rely on the initial values or partial differentiation of the evaluation function. By modifying the PSO algorithm, we can draw design curves of the class-E amplifier and frequency multipliers simultaneously with the one-time execution of the algorithm. Additionally, we can derive the component values satisfying the class-E ZVS/ZDS conditions by setting only one evaluation function: power-conversion efficiency. Though the computation algorithm and evaluation functions are straightforward, the design accuracy does not deteriorate compared to Newton's method-based designs. We performed circuit experiments, which achieved power-conversion efficiency of 94.0%. The circuit experiment showed agreement

with numerical predictions, which confirmed the validity and usefulness of the proposed design method.

This paper is organized as follows: Section II introduces the circuit topology, parameter definitions, and system modeling of the class-E amplifier and multipliers. Section III discusses the advantage and disadvantages of previous design methods. Additionally, the proposed PSO-based design method is introduced in Section III. Two design examples are denoted in this paper: Section IV proposes a comprehensive design of the class-E amplifier and rectifiers based on the modified PSO algorithm. Section V gives a design example of the class-E amplifier with only one evaluation function. Finally, Section VI gives the conclusion of this research.

II. INTRODUCTION OF THE CLASS-E SWITCHING CIRCUITS

A. CIRCUIT DESCRIPTION

Figure 1 shows a circuit topology of the class-E amplifier and class-E frequency multiplier [26]–[28]. It consists of dc-voltage source V_I , RF-choke dc-feed inductance L_C , switching device S , shunt capacitance C_S , series resonant filter L_0 - C_0 , and load resistance R_L . Figure 2 shows example waveforms of the class-E switching circuits, where f_s is the switching frequency, and $\theta = \omega t = 2\pi f_s t$ is the angular displacement. Table 1 gives the definitions of all circuit parameters.

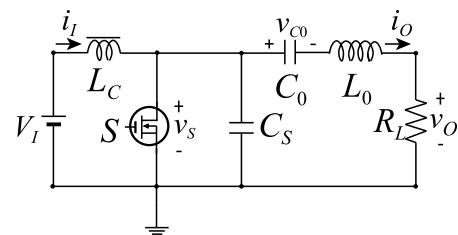


FIGURE 1. Circuit topology of the class-E amplifier.

B. CLASS-E AMPLIFIER

Figure 2(a) shows example waveforms of the class-E amplifier. Because of the dc-voltage source and RF-choke, the input current i_i is regarded as direct current. Additionally, the loaded quality factor of the series resonant filter, which is defined as

$$Q_0 = \frac{2\pi f_s L_0}{R_L}, \quad (1)$$

is sufficiently high. Therefore, the output current i_o becomes sinusoid, as shown in Fig.2(a).

During the switch ON state, the difference between the input and output currents flows through the switching device, and the voltage across the switch becomes almost zero. When the switch is in the OFF state, the current flows through the shunt capacitance, which generates the pulse-shape switch voltage. In the nominal operation of the class-E amplifier,

TABLE 1. Circuit parameter definitions.

Notation	Definition	Notation	Definition
C_{ds}	Drain-to-source capacitance.	r_{L0}	ESR of the resonant inductance.
C_{ext}	External shunt capacitance.	r_{ON}	On-state resistance of the switch.
C_S	Total shunt capacitance.	R_L	Load resistance.
C_0	Resonant capacitance.	v_{C1}	Voltage of resonant capacitance.
D_S	Switch on-duty ratio.	V_I	Input voltage.
f_S	Switching frequency.	v_S	Drain-to-source voltage of the switch.
H	$2\pi f_S L_C / R_L$.	v_O	Inverter output voltage.
i_I	Input current.	V_O	RMS output voltage.
i_O	Output current.	γ_S	$2\pi f_S C_S R_L$.
L_C	Input choke inductance.	η	Power-conversion efficiency.
L_0	Resonant inductance.	θ	Angular time, $\theta = 2\pi f_S t$.
Q_0	$2\pi f_S L_0 / R_L$.	ω_0^*	$1 / (2\pi f_S \sqrt{L_0 C_0})$.
r_{Lc}	ESR of the input inductance.		

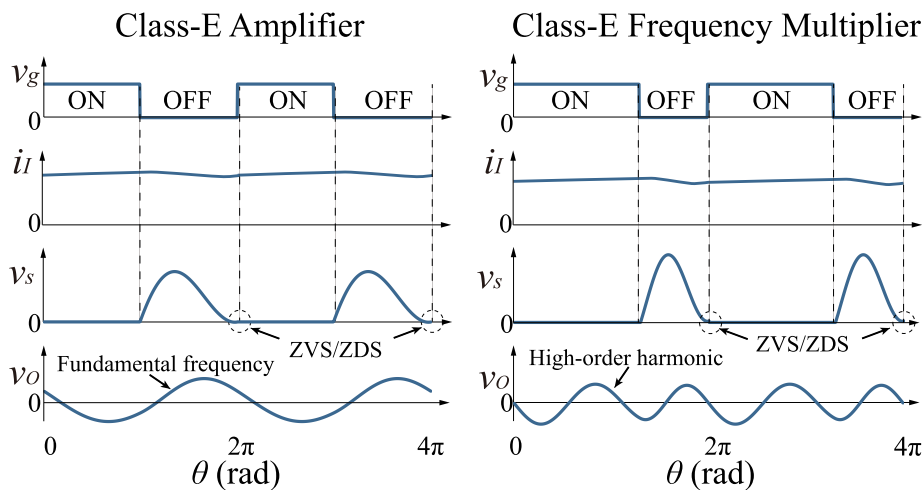


FIGURE 2. Example waveforms of two operating modes of the class-E switching circuit. (a) The class-E amplifier. (b) The class-E frequency multiplier.

the switch voltage satisfies the class-E ZVS/ZDS conditions at the turn-on instant, namely,

$$\begin{aligned} v_S(2\pi) &= 0, \\ \left. \frac{dv_S}{d\theta} \right|_{\theta=2\pi} &= 0. \end{aligned} \quad (2)$$

By achieving the class-E ZVS/ZDS conditions, the class-E amplifier can suppress switching losses effectively. Therefore, the class-E amplifier works with high power-conversion efficiency at high frequencies. Because of this characteristic, the class-E amplifier is suitable for applications such as WPT systems [1], [2], [4], [5], [25], resonant power converters [7]–[12], and induction heating systems [14].

1) THE CLASS-E AMPLIFIER

For the class-E amplifier, the resonant frequency of the output resonant network $f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}}$ is approximately the same as the switching frequency f_S . In this case, the resonant filter extracts a fundamental frequency component of the switch

voltage, as shown in Fig. 2(a). This is the class-E amplifier operation.

2) THE CLASS-E FREQUENCY MULTIPLIER

When the resonant filter is tuned to the high-order harmonic components, the harmonic-frequency output voltage can be obtained. These circuits are known as the class-E frequency multipliers [26]–[28]. The class-E frequency multiplier has the same circuit topology as the class-E amplifier, as shown in Fig. 1. The component values and parameters of the class-E frequency multiplier are, however, different from the amplifier. The switch voltage needs to include sufficient harmonic components, which are extracted by the resonant filter. Figure 2(b) shows example waveforms of the class-E frequency doubler.

As shown in Fig. 2(b), the on-duty ratio of the class-E frequency doubler D_S is about 0.75. For generating the b -th harmonic components, it is usually that the duty ratio of the switch is

$$D_S \approx 1 - \frac{1}{2}b. \quad (3)$$

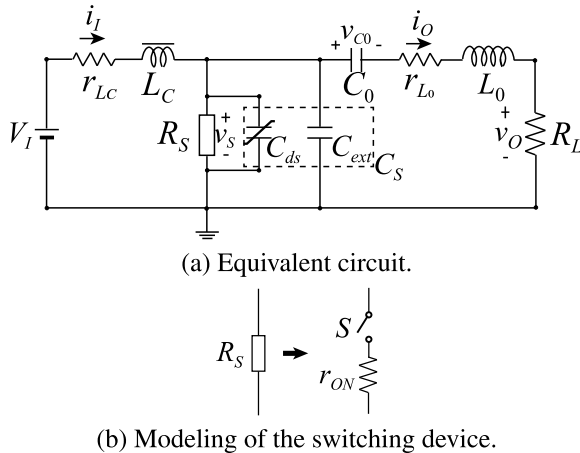


FIGURE 3. Equivalent circuit of the proposed class-E amplifier and modeling of the switching device. (a) Equivalent circuit. (b) Modeling of the switching device.

Like the class-E amplifier, the input current is also direct current because of the dc-feed inductance. Additionally, the output current is sinusoid because of high quality factor Q_0 of the output filter.

It is noted that the frequency multipliers also satisfy the class-E ZVS/ZDS conditions at the switch turn-on instant, as shown in Fig. 2.

C. CIRCUIT EQUATIONS

Because the circuit topology of the class-E amplifier is the same as that of the class-E frequency multiplier, their circuit equations are formulated as identical expressions. In this paper, we express the circuit equations by the normalized and dimensionless quantities. Concretely, all the voltage variables are normalized by input voltage V_I , e.g., $v_s^* = v_s/V_I$, where superscript ‘*’ means a normalized variable. Additionally, all the current variables are normalized by V_I and load resistance R_L , e.g. $i_l^* = i_l R_L/V_I$. By adopting the normalized variables, the class-E switching circuit is expressed by

$$\begin{cases} \frac{di_l^*}{d\theta} = \frac{R_L}{\omega L_C} \left(1 - \frac{r_{LC}}{R_L} i_l^* - v_s^* \right), \\ \frac{dv_s^*}{d\theta} = \frac{1}{\omega(C_{ds} + C_{ext})R_L} \left(i_l^* - \frac{R_L}{R_S} v_s^* - i_o^* \right), \\ \frac{dv_{C1}^*}{d\theta} = \frac{1}{\omega C_0 R_L} i_o^*, \\ \frac{di_o^*}{d\theta} = \frac{R_L}{\omega L_0} \left[v_s^* - v_{C1}^* - \left(1 + \frac{r_{L0}}{R_L} \right) i_o^* \right], \end{cases} \quad (4)$$

where R_S is the equivalent resistance of the MOSFET, which is expressed as

$$R_S = \begin{cases} r_{ON}, & \text{for } 0 \leq \theta < 2\pi D_s, \\ \infty, & \text{otherwise.} \end{cases} \quad (5)$$

C_{ext} is the drain-to-source parasitic capacitance of the switch, and C_{ds} is the external capacitance. r_{ON} is the on-resistance of the GaN-FET, and r_{LC} and r_{L0} are equivalent series resistances (ESRs) of the dc-feed inductance and

resonant inductance, respectively. Generally, the FET drain-to-source capacitance works as the nonlinear capacitance, depending on the drain-to-source voltage.

III. DESIGN METHODS OF THE CLASS-E SWITCHING CIRCUITS

In the class-E switching circuits designs, it is necessary to achieve the class-E ZVS/ZDS conditions in the steady-state. Namely, we need to find a proper combination of component values, which satisfy two conditions in (2) simultaneously. One of the major research topics of the class-E switching circuits has been to establish the design methods since the class-E switching circuit was invented about 40 years ago.

Generally, the design methods of the class-E switching circuit can be divided into two kinds, namely analytical designs [1]–[3], [16], [17], [23], [29], [32] and numerical ones [5], [7]–[9], [18], [20], [21].

A. ANALYTICAL DESIGN APPROACHES

Through the analyses of the class-E circuits, circuit component values can be expressed as functions of circuit parameters explicitly. In the earliest papers on class-E amplifier analysis, some idealizations are given, e.g., pure sinusoidal output current, direct input current, ideal switching device operation, and 50% duty-ratio [24], [26]. After that, circuit analyses have been performed with any duty ratio [23], finite RF-choke [28], [33], and any quality factor [33], which relief the initial assumptions gradually. Additionally, class-E amplifier analysis considering the nonlinearity of MOSFET parasitic capacitances was also presented in recent years [34], [35]. Using these analytical equations, we can explicitly express the relationship between circuit component values and circuit parameters, which helps to intuitively and comprehensively understand the characteristics of the class-E switching circuits.

However, it takes a long time to derive the analytical equations. Specialized knowledge is necessary for carrying out the analyses. The assumptions for idealizations cause the lack of design accuracy. With the development of the next-generation semiconductors, such as GaN-FET devices, the switching frequency can be pushed up to ISM-band. At high frequencies, however, designers require accurate component values.

The class-E amplifier topology is the same as the frequency multiplier topologies. Besides, all the amplifier and frequency multiplier satisfies the class-E ZVS/ZDS conditions. This means that there are many combinations of the circuit parameters to achieve the class-E ZVS/ZDS with different operation modes such as the class-E amplifiers and frequency multipliers. These parameter sets become the ‘‘design curves.’’ For obtaining the design curves on the parameter space, however, we have to derive the analytical expression of each operation mode individually.

B. NUMERICAL DESIGN APPROACHES

By adopting numerical design procedures, complicated circuit characteristics can be reflected in the design values.

As far as the authors know, the numerical design method of the class-E amplifier was firstly proposed in [19]. In [19], the state variable vector $\mathbf{x} = [x_1, x_2, x_3, x_4]^T = [i_C, v_S, v_{C0}, i_O]^T$ and circuit parameters vector $\boldsymbol{\lambda} = [D_S, \omega_0^*, \gamma_S]^T$ are considered. Then, the circuit equations in (4) can be expressed as

$$\frac{d\mathbf{x}}{d\theta} = f(\theta, \mathbf{x}, \boldsymbol{\lambda}). \quad (6)$$

The design problem of the class-E switching circuits narrows down to solve the equations:

$$\mathbf{F}(\boldsymbol{\lambda}, \mathbf{x}_0) = \begin{bmatrix} \mathbf{x}(2\pi) - \mathbf{x}_0 \\ v_S(2\pi) \\ \left. \frac{dv_S}{d\theta} \right|_{\theta=2\pi} \end{bmatrix} = 0, \quad (7)$$

for \mathbf{x}_0 and $\boldsymbol{\lambda}$, where $\mathbf{x}_0 = \mathbf{x}(0)$. The first line of \mathbf{F} ensures the circuit operates in the steady state, the second and third lines express the class-E ZVS/ZDS condition achievements. In [19], the function $\mathbf{F}(\boldsymbol{\lambda})$ is regarded as algebraic equations. When we determine $\boldsymbol{\lambda}$ and \mathbf{x}_0 as solutions of (7), the parameter set of $\boldsymbol{\lambda}$ becomes component values for satisfying the class-E ZVS/ZDS conditions. (7) is solved numerically by applying Newton's method in [19]. The iterative computations of Newton's method can be expressed as

$$\mathbf{u}^{\kappa+1} = \mathbf{u}^{\kappa} - \frac{\mathbf{F}(\mathbf{u}^{\kappa})}{\mathbf{F}'(\mathbf{u}^{\kappa})}, \quad (8)$$

where $\mathbf{u} = [\mathbf{x}_0^T, \boldsymbol{\lambda}^T]^T$ is the unknown variable vector of the algebraic equations. κ is the iteration number, and \mathbf{F}' is the Jacobian matrix of \mathbf{F} . Numerical design methods can provide the design parameters even if the design circuit is complicated to analyze. Therefore, designs of many types of the class-E switching circuits, which had been considered impossible to design due to complexity, were succeeded [5], [7]–[9], [18]–[20], [22].

However, there are still some limitations in Newton's method-based designs.

- It is necessary to derive the approximate solutions used for the initial values of Newton's method. We often obtain the approximate solutions from the analytical expressions or need to execute trial-and-error simulations. In both ways, it is a tedious task and takes a long time.
- The derivations of the elements in the Jacobian matrix \mathbf{F}' also require tedious and complicated calculations. Special mathematics skills, such as variational equations, are needed [19]. In [31], an approximate derivation method of the Jacobian matrix is proposed. However, in that case, the convergence stability of Newton's method deteriorates.
- Newton's method is an algebraic equation solver. Therefore, the number of the adjustable parameter should be the same as the equation number. Namely, Newton's method provides the "optimal point." Therefore, it is not easy to comprehend the relationship between parameters

and circuit characteristics intuitively. For comprehensive understanding, it is necessary to derive many 'points' in the parameter spaces [8], which increases the calculation cost.

- It is difficult to obtain the component values to satisfy 'maximum' and 'minimum' conditions. Besides, we cannot obtain the optimal values when the design conditions are expressed by inequality. A parameter design technique that maximizes the power transmission efficiency of WPT systems was proposed in [5], where the maximization of the power-conversion efficiency was derived using the derivative of efficiency, namely $d\eta/d\boldsymbol{\lambda} = 0$. However, partial differentiation with respect to this derivative is required for obtaining the Jacobian matrix, whose computation is too complicated and makes the algorithm unstable.

C. PROPOSED DESIGN METHOD

This paper proposes a numerical design of the class-E switching circuits for addressing the issues mentioned above. Our idea is to solve design equations in (7) by applying heuristic algorithms. In this paper, we adopt the PSO algorithm, which is one of the familiar heuristic algorithms, for the class-E switching circuit designs.

In the PSO algorithm, many particles travel in the parameter space and find the global minimum of the evaluation function. The particle k moves its position in the parameter space iteratively, which is determined by

$$\mathbf{u}_k(\kappa + 1) = \mathbf{u}_k(\kappa) + \mathbf{v}_k(\kappa + 1), \quad (9)$$

where κ is the iteration number, and the velocity of the particle k is

$$\mathbf{v}_k(\kappa + 1) = w\mathbf{v}_k(\kappa) + \alpha_1 a_1 (\mathbf{u}_k^{pbest}(\kappa) - \mathbf{u}_k(\kappa)) + \alpha_2 a_2 (\mathbf{u}^{gbest}(\kappa) - \mathbf{u}_k(\kappa)). \quad (10)$$

In (10), w denotes the inertia weight, \mathbf{u}_k^{pbest} and \mathbf{u}^{gbest} are the individual and global best-known positions, respectively. Additionally, α_1 and α_2 are random numbers in the uniform distribution from 0 to 1, and a_1 and a_2 are the social and individual acceleration coefficients, respectively. Table 2 gives the definitions of all algorithm parameters. We can see from (9) and (10) that the movement of each particle is determined by its individual best-known position and the global one.

In this research, all numerical calculation programs are made by ourselves. For deriving the circuit waveforms, we developed the differential equation solver to solve (4) based on the Runge-Kutta method. The differential equation solver is embedded into the PSO algorithm for calculating the evaluation function.

D. RESEARCH COMPARISON

Table 3 gives brief comparisons between the PSO-based design method and Newton's method-based one [19], [20].

TABLE 2. Algorithm parameter definitions.

Notation	Definition	Notation	Definition
a_1	Acceleration coefficient for personal best.	\mathbf{u}^{gbest}	Global best-known location.
a_2	Acceleration coefficient for global best.	\mathbf{v}	Particle velocities.
F	Evaluation function.	w	Inertia weight.
\mathbf{F}	Design conditions matrix.	\mathbf{x}	State variables vector.
\mathbf{J}'	Jacobian matrix of \mathbf{F} .	\mathbf{x}_0	Initial-state vector.
k	Particle index.	α_1, α_2	Random values with uniform distribution in $[0, 1]$.
K	Number of particles.	λ	Adjusting parameters vector.
\mathbf{u}	Vector of unknown values to be solved.	κ	Iteration number.
\mathbf{u}^{pbest}	Personal best-known location.	κ_{Max}	Maximum iteration number.
\mathbf{u}^{fbest}	Friend best-known location.		

TABLE 3. Research comparisons between the PSO-based design method and Newton’s method-based one.

Researches	[19], [20]	This work
Algorithm	Newton’s method	PSO
Jacobian matrix derivation	Necessary	Unnecessary
Initial values derivation	Necessary	Unnecessary
# of adjusting param.	Same as # of conditions	No restriction
Design conditions	Algebraic equations	Evaluation functions

As seen from this table, the proposed design method has the following features.

- 1) It is unnecessary to give the accurate initial values though it is necessary to determine the search range of the parameters.
- 2) We do not have to derive the partial differentiation of the evaluation function.
- 3) The number of design conditions does not need to be equal to that of adjusting design parameters. In addition, ‘maximization’ and ‘minimization’ can be executed without affecting the computation complexity.
- 4) In the PSO algorithm, many particles travel in the parameter space. Therefore, there is a possibility that the PSO can find the multiple best positions in the parameter spaces within the one-time execution of the computation program.

This paper presents two examples of the class-E switching circuits by using the above features.

IV. COMPREHENSIVE DESIGN OF THE CLASS-E SWITCHING CIRCUITS

In this section, a comprehensive design of the class-E switching circuits is proposed. The design curves of the class-E amplifier and frequency multipliers are obtained simultaneously in one-time optimization execution.

As stated in Section II, there are many nominal parameter sets that can satisfy the class-E ZVS/ZDS conditions at the class-E amplifier topology. When the multiple particles are trapped at different nominal points on the parameter spaces, it may be possible to draw the design curves by connecting trapped particles in one-time optimization execution, which is our idea. It can be stated that this design approach uses feature 4) of the PSO algorithm effectively.

A. CIRCUIT EQUATIONS

This section aims to obtain the design curves of the class-E amplifier and the class-E multipliers simultaneously with one-time optimization executions. For having the generality of design curves, the following assumptions are given.

- 1) The switch S is considered as the ideal switching device with infinity off-resistance, zero on-resistance, and zero drain-to-source parasitic capacitance.
- 2) The ESRs of all circuit components are ignored.

Based on the assumptions, (4) is rewritten as

$$\begin{cases} \frac{di_I^*}{d\theta} = \frac{1}{H}, \\ \frac{dv_{C1}^*}{d\theta} = \omega_0^{*2} Q_0 i_1^*, \\ \frac{di_O^*}{d\theta} = \frac{1}{Q_0} \left(-v_{C1}^* - i_1^* \right). \text{for } 0 \leq \theta < 2\pi D_s, \end{cases} \quad (11)$$

and

$$\begin{cases} \frac{di_I^*}{d\theta} = \frac{1}{H} \left(1 - v_S^* \right), \\ \frac{dv_S^*}{d\theta} = \frac{1}{\gamma_S} \left(i_I^* - i_1^* \right), \\ \frac{dv_{C1}^*}{d\theta} = \omega_0^{*2} Q_0 i_1^*, \\ \frac{di_O^*}{d\theta} = \frac{1}{Q_0} \left(v_S^* - v_{C1}^* - i_1^* \right). \text{for } 2\pi D_s \leq \theta < 2\pi, \end{cases} \quad (12)$$

where $H = \omega L_C / R_L$, $\omega_0^* = \frac{1}{\omega \sqrt{L_0 C_0}}$ and $\gamma_S = \omega C_S R_L$.

The circuit equations (11) and (12) are independent of the switching frequency, input voltage, and load resistance. In this design, only $Q_0 = 5$ and $H = 150$ are given as design specifications. The other circuit-equation parameters are the adjusting parameters for optimization, namely

$$\lambda = [D_s, \omega_0^*, \gamma_S]^T. \quad (13)$$

B. EVALUATION FUNCTION

The purpose of the design is to satisfy the class-E ZVS/ZDS conditions at the steady state. The design conditions in (7) are

rewritten into the evaluation function, which is

$$F(\mathbf{u}) = \left| v_S(2\pi, \mathbf{u}) \right| + \left| \frac{dv_S(\theta, \mathbf{u})}{d\theta} \Big|_{\theta=2\pi} \right| + \sum_{j=1}^n \left| x_j(2\pi) - x_j(0) \right|. \quad (14)$$

Namely, the design problem can be replaced to the optimization problem, which is

$$\min_{\mathbf{u}} F(\mathbf{u}). \quad (15)$$

C. PSO ALGORITHM FOR COMPREHENSIVE DESIGN

As stated in Section II, there are multiple solutions of \mathbf{u} that satisfy $F(\mathbf{u}) = 0$. These solutions are continuous in parameter space, shaping each ‘design curve.’

However, the design-curve range depends on the harmonic frequency. The particle tends to move the area that many particles are located. Namely, most of the particles go to the largest ‘valley’ area and converges to one point. Because the class-E amplifier design curve is the longest, all the particles converge to one point on the class-E amplifier design curve, for example, the green point in Fig. 4.

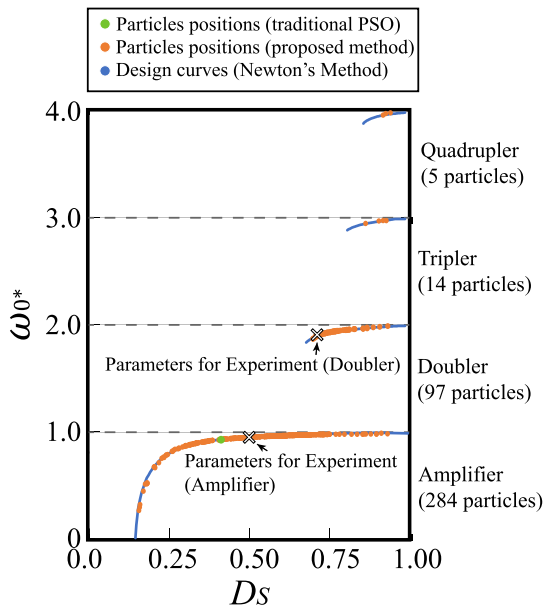


FIGURE 4. Design results plotted in $D_S - \omega_0^*$ parameter space.

For realizing a comprehensive design, it is necessary to modify the PSO algorithm. The reason for one-point convergence is that all the particles are connected to others in the algorithm. Therefore, the connection strength among the particles should be weakened. Concretely, each particle shares information with only two others. For achieving that, K particles are labeled from one to K . Besides, the particles $(k - 1)$ and $(k + 1)$ are defined as the friends of particle k .

In the proposed PSO algorithm, (10) is rewritten as

$$v_k(\kappa + 1) = wv_k(\kappa) + \alpha_1 a_1 (\mathbf{u}_k^{pbest}(\kappa) - \mathbf{u}_k(\kappa)) + \alpha_2 a_2 (\mathbf{u}_k^{nfbest}(\kappa) - \mathbf{u}_k(\kappa)), \quad (16)$$

where

$$\mathbf{u}_k^{fbest} = \arg \min_{\mathbf{u} \in \{\mathbf{u}_{k-1}, \mathbf{u}_k, \mathbf{u}_{k+1}\}} F(\mathbf{u}), \quad (17)$$

is the friend best-known position. The modified PSO makes particles travel in a wide range of parameter space and find optimal points in the entire parameter space. Because each particle is trapped at different optimal points, the design curves can be drawn by connecting the particles with the one-time execution of the algorithm.

We performed the modified PSO with following parameters: number of particles $K = 400$, maximum iteration number $\kappa_{Max} = 200$, inertia weight $w = 0.729$, acceleration coefficients $a_1 = a_2 = 1.494$. Table 4 gives the ranges of the adjusting parameters.

TABLE 4. Parameter ranges.

Parameter	Range
D_S	[0, 1]
ω_0^*	[0, 5]
γ_S	[0, 1]
$v^*(0)$	[-100, 100]
$i^*(0)$	[-100, 100]

D. DESIGN RESULTS DISCUSSION

Figure 4 shows 400 particle positions on the parameter space of $D_S - \omega_0^*$ after the optimization execution. For the design result with the traditional PSO algorithm, all particles converged into one point finally. On the other hand, for the proposed design procedure with the modified PSO algorithm, we confirm that 400 particles are trapped at many optimal points where the class-E ZVS/ZDS conditions are achieved. The solid lines in Fig. 4 are design curves of the class-E amplifier and frequency multipliers obtained from the algorithm in [20]. We can see from Fig. 4 that all the particles are trapped in the range of $0 < \omega_0^* < 4$, which can be divided into four groups. By connecting the particles for each group, we can simultaneously obtain the design parameter curves of the class-E amplifier, doubler, tripler, and quadrupler. It can be seen from Fig. 4 that the plots are overlapped with the design curves completely, which proves the accuracy of the proposed design procedure.

We would like to emphasize that four design curves can be obtained by the one-time optimization execution. Additionally, only circuit equations in (11) and (12), evaluation function in (14), and the parameters ranges as given in Table 4 are given for the design. The modified PSO algorithm is also simple in the sense that there is no initial value estimation or no partial-differentiation derivation.

E. EXPERIMENTAL VERIFICATION

For confirming the validity of the proposed design method, circuit experiments of the class-E amplifier and frequency doubler were carried out. The measured component values of the class-E amplifier and frequency doubler are given in Tables 5 and 6, whose design points are plotted as shown in Fig.4.

TABLE 5. Numerical and measured circuit components of the class-E amplifier.

Parameter	Designed	Measured	Difference
L_C	35.2 μH	34.3 μH	-2.56 %
L_0	1.17 μH	1.16 μH	-0.85 %
C_{ext}	249 pF	249 pF	0.00 %
C_{ds}	110 pF	-	-
C_0	269 pF	265 pF	-0.15 %
r_{LC} (DC)	-	0.058 Ω	-
r_{L0} (6.78 MHz)	-	0.261 Ω	-
r_{ON}	0.016 Ω	-	-
R_L	10.0 Ω	10.0 Ω	0.00 %
f_s	6.78 MHz	6.78 MHz	0.00 %
D_s	0.50	0.50	0.00 %
η	-	93.0 %	-

TABLE 6. Numerical and measured circuit components of the class-E frequency doubler.

Parameter	Designed	Measured	Difference
L_C	35.2 μH	34.3 μH	-2.56 %
L_0	1.17 μH	1.16 μH	-0.85 %
C_{ext}	29.6 pF	29.0 pF	-2.03 %
C_{ds}	110 pF	-	-
C_0	69.4 pF	67.5 pF	-2.74 %
r_{LC} (DC)	-	0.058 Ω	-
r_{L0} (13.56 MHz)	-	0.367 Ω	-
r_{ON}	0.016 Ω	-	-
R_L	10.0 Ω	10.0 Ω	0.00 %
f_s	6.78 MHz	6.78 MHz	0.00 %
D_s	0.70	0.70	0.00 %
η	-	82.0 %	-

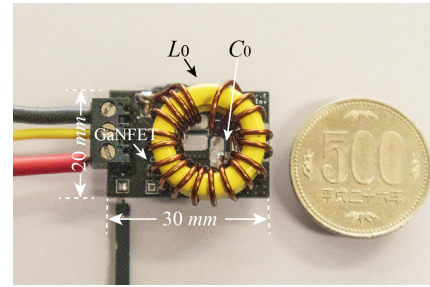
For the circuit experiments, the design specifications are set as $V_I = 20\text{ V}$, $f_s = 6.78\text{ MHz}$, and $R_L = 10\ \Omega$. We selected GS61004B enhancement-mode GaN-FET from GaN Systems as the switching device. We used a Keysight E4990A impedance analyzer to measure all the component values.

The gate driving signal was generated by a Tektronix AFG3022C function generator. A Texas Instruments UCC27512DRST low-side gate driver was adopted. All the waveforms were measured by a Tektronix MSO46 oscilloscope.

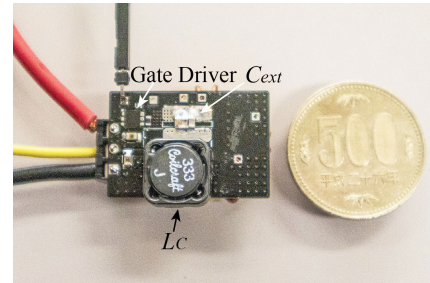
In experimental measurements, the power-conversion efficiency was obtained from

$$\eta = \frac{P_O}{P_I} = \frac{V_O^2}{R_L V_I I_I}, \quad (18)$$

where the RMS value of the output voltage V_O and dc-feed current I_I were measured by a Tektronix MSO46 oscilloscope. Figure 5 shows the photos of the implemented class-E amplifier prototype.

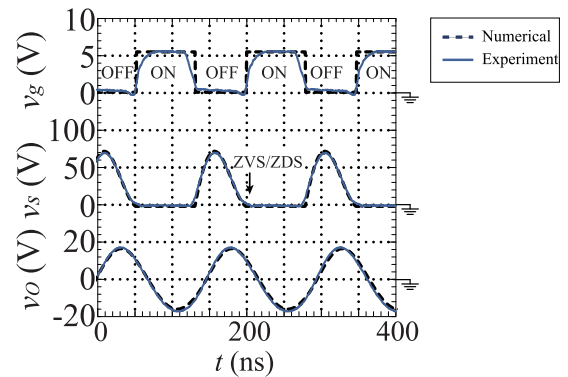


(a) Top-side view.

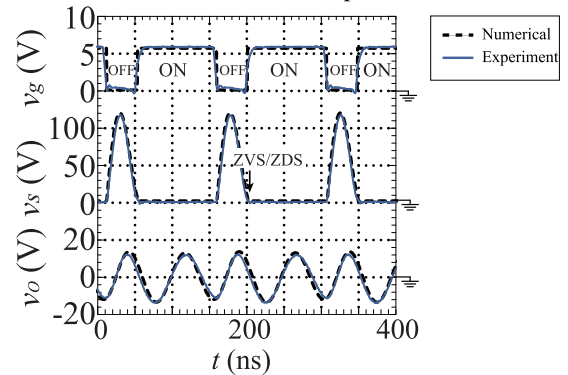


(b) Bottom-side view.

FIGURE 5. Photos of the implemented class-E switching circuit. (a) Top-side view. (b) Bottom-side view.



(a) Class-E amplifier.



(b) Class-E frequency doubler.

FIGURE 6. Numerical and experimental circuit waveforms. (a) Class-E amplifier. (b) Class-E frequency doubler.

Figure 6 show the numerical predictions and experimental waveforms of the class-E amplifier and the frequency doubler. It is seen from Fig. 6 that the class-E ZVS/ZDS

conditions were achieved for both experiments. Besides, we can confirm from Fig. 6 that the numerical and experimental results showed agreement with each other. These results proved the validity and usefulness of the circuit model in (11) and (12) and the proposed design method.

V. DESIGN EXAMPLE OF THE CLASS-E AMPLIFIER WITH POWER-CONVERSION EFFICIENCY MAXIMIZATION

The class-E ZVS/ZDS aims to achieve high power-conversion efficiency at high frequencies due to the switching-loss elimination. Therefore, the class-E amplifier may be designed only by maximizing the power-conversion efficiency. However, there is no design example with this approach because the number of adjusting design parameters is more than the design restrictions.

The PSO algorithm, however, allows the mismatch of the design parameter and the evaluation function numbers, described in the PSO feature 3). In this section, we design the class-E amplifier by evaluating only the power-conversion efficiency.

A. CIRCUIT EQUATIONS

The design specifications are set as follows: $f_s = 6.78$ MHz, $Q_0 = 5$, $R_L = 10 \Omega$, and $V_I = 20$ V. From Q_0 and R_L , the resonant inductance is determined as $L_0 = 1.17 \mu\text{H}$. A hand-made toroidal coil was adopted for the resonant inductance L_0 with Micrometals T-80-6 iron-powder core. The measured equivalent series resistance (ESR) was $r_{L0} = 0.261 \Omega$ at 6.78 MHz. As the input inductance L_C , we adopted the MSS1246-333MLB inductor from Coilcraft, whose self-inductance and ESR were $L_C = 33 \mu\text{H}$ and $r_{LC} = 0.058 \Omega$, respectively.

We also adopted GS61004B enhancement-mode GaN-FET from GaN Systems as the switching device, whose on-resistance is 0.016Ω from the datasheet. Additionally, according to the Spice model of the GaN-FET [36], the non-linear drain-to-source parasitic capacitance is expressed as

$$C_{ds} = \frac{3.15 \times 10^{-10}}{v_S} \log(1 + e^{0.5(v_S+16)}) + \frac{1.69 \times 10^{-10}}{v_S} \log(1 + e^{0.03(v_S+31)}). \quad (19)$$

In this design, we adopt the circuit equations in (4). The adjusting design parameters are set as $\lambda = [D_S, \omega C_{ext} R_L, 1/(2\pi f_s \sqrt{L_0 C_0})]^T$.

B. EVALUATION FUNCTION

Because we consider only the power-conversion efficiency for the class-E amplifier design, the evaluation function is defined as

$$F'(\mathbf{u}) = \left| 1 - \eta(\mathbf{u}) \right| + \sum_{j=1}^n \left| x_j(2\pi) - x_j(0) \right|. \quad (20)$$

In the power-conversion efficiency equation in (18), V_o and I_I are calculated by

$$V_o = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} v_o^2(\theta) d\theta}, \quad (21)$$

and

$$I_I = \frac{1}{2\pi} \int_0^{2\pi} i_I(\theta) d\theta, \quad (22)$$

respectively. The traditional PSO-algorithm optimization was performed with the evaluation function in (20). The PSO algorithm searches the global best with the following parameters: number of the particles $K = 200$, maximum iteration number $\kappa_{Max} = 200$, inertia weight $w = 0.729$, acceleration coefficients $a_1 = a_2 = 1.494$.

C. DESIGN RESULTS AND DISCUSSION

Table 7 shows the component values obtained from the PSO optimization. Figure 7 shows the optimal design point and the contours of power-conversion efficiency on the D_S - ω_0^* space, where the contours are derived by brute-force calculations.

TABLE 7. Numerical and measured circuit components of the class-E amplifier with power-conversion efficiency maximization.

Parameter	Designed	Measured	Difference
L_C	35.2 μH	34.3 μH	-2.56 %
L_0	1.17 μH	1.16 μH	-0.85 %
C_{ext}	347 pF	345 pF	-0.57 %
C_{ds}	110 pF	-	-
C_0	299 pF	303 pF	1.33 %
r_{LC} (DC)	-	0.058 Ω	-
r_{L0} (6.78 MHz)	-	0.261 Ω	-
r_{ON}	0.016 Ω	-	-
R_L	10.0 Ω	10.0 Ω	0.00 %
f_s	6.78 MHz	6.78 MHz	0.00 %
D_s	0.39	0.39	0.00 %
η	95.2 %	94.0 %	-

We can see from Fig. 7 that the maximum power-conversion efficiency can be obtained at $D = 0.39$ in this design. Besides, it can be confirmed that the proposed algorithm can find the component values, which provides the highest power-conversion efficiency.

D. EXPERIMENTAL VERIFICATION

Based on the obtained design result, the experimental circuit of the class-E amplifier was implemented. Table 7 gives the designed and measured component values of the optimal class-E amplifier. The experiment setup was the same as that in Section IV.

Figure 8 shows the waveforms of the designed class-E amplifier. It is seen from this figure that the implemented inverter almost achieved the class-E ZVS/ZDS conditions. This result includes evidence that the class-E ZVS/ZDS lead to high power-conversion efficiency. In the opposite view, the class-E inverter, satisfying the class-E ZVS/ZDS conditions, can be designed by giving only one evaluation function, namely power-conversion efficiency maximization.

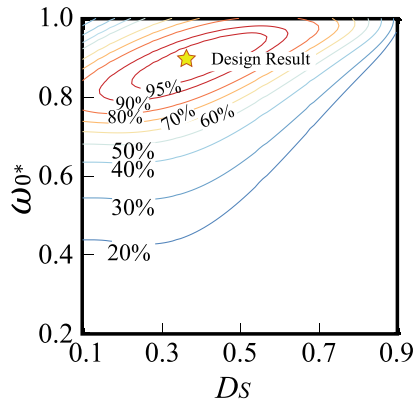


FIGURE 7. Efficiency contour in the D_s - ω_0^* space.

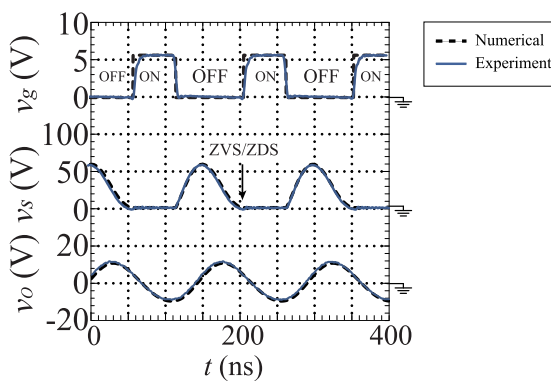


FIGURE 8. Numerical and experimental circuit waveforms of the class-E amplifier with power-conversion efficiency maximization.

Additionally, it can be confirmed from Fig. 8 and Table 7 that all the experimental results quantitatively agreed with numerical ones. The power-conversion efficiency achieved 94.0%, which is 1.0% higher than the class-E amplifier designed in Section IV. This result shows the validity and effectiveness of the proposed design method.

VI. CONCLUSION

This paper has proposed comprehensive and simplified numerical design procedures for the class-E switching circuits with the PSO algorithm. The PSO algorithm does not require approximate solutions and partial differentiation derivations. Therefore, the proposed design method has higher convergence stability than Newton's method-based design. It is also a feature that the PSO algorithm allows the mismatch between the design condition and the design parameter numbers. As a design example, we successfully draw the multiple design curves of the class-E amplifier and frequency multipliers within one-time optimization execution with the modified PSO algorithm. Besides, we showed a pretty simple design procedure of the class-E amplifier, which uses only one evaluation function for determining three design parameters. The design accuracy of the proposed design method does not deteriorate compared with the previous design method. By carrying out circuit experiments,

the validity and usefulness of the proposed design method were confirmed.

The limitation of the proposed design method is that the circuit topology is fixed, which is determined by the given circuit equations. Nevertheless, as stated in Section I, there are many kinds of derived topologies in the class-E families with different features, including class-E, class-DE, class-EF, etc. If the automatic topology derivation can be achieved in the design stage, not only the circuit parameters but also the most suitable circuit topology can be found for the given design specification. However, automatic topology derivation is a challenging research topic, which we will address in the future.

REFERENCES

- [1] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Load-independent class E/EF inverters and rectifiers for MHz-switching applications," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8270–8287, Oct. 2018.
- [2] A. Pacini, A. Costanzo, S. Aldhaher, and P. D. Mitcheson, "Load and position-independent moving MHz WPT system based on GaN-distributed current sources," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5367–5376, Dec. 2017.
- [3] L. Zhang and K. Ngo, "Design methodology of a ZVS Class-E inverter with fixed gain," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 2752–2758.
- [4] S. Liu, M. Liu, S. Han, X. Zhu, and C. Ma, "Tunable class E^2 DC-DC converter with high efficiency and stable output power for 6.78-MHz wireless power transfer," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6877–6886, Aug. 2018.
- [5] K. Inoue, T. Nagashima, X. Wei, and H. Sekiya, "Design of high-efficiency inductive-coupled wireless power transfer system with class-DE transmitter and class-E rectifier," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 613–618.
- [6] F. Lin, X. Zhang, and X. Li, "Design methodology for symmetric CLLC resonant DC transformer considering voltage conversion ratio, system stability, and efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10157–10170, Sep. 2021.
- [7] W. Zhu and H. Sekiya, "A 1 MHz class-E² single-stage PFC converter with frequency control," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2020, pp. 2041–2047.
- [8] S. Saito, S. Mita, W. Zhu, H. Onishi, S. Nagaoka, T. Uematsu, K. Nguyen, and H. Sekiya, "Novel design approach of soft-switching resonant converter with performance visualization algorithm," *IEEE Access*, vol. 8, pp. 59922–59933, 2020.
- [9] H. Sekiya, J. Lu, and T. Yahagi, "Design of generalized class E^2 DC/DC converter," *Int. J. Circuit Theory Appl.*, vol. 31, no. 3, pp. 229–248, 2003.
- [10] Y. Wang, J. Huang, W. Wang, and D. Xu, "A single-stage single-switch LED driver based on class-E converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2618–2626, May 2016.
- [11] J. M. Rivas, O. Leitermann, Y. Han, and D. J. Perreault, "A very high frequency DC-DC converter based on a class- ϕ_2 resonant inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2980–2992, Jan. 2011.
- [12] Y. Yanagisawa, Y. Miura, H. Handa, T. Ueda, and T. Ise, "Characteristics of isolated DC-DC converter with class Phi-2 inverter under various load conditions," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10887–10897, Nov. 2019.
- [13] P. Thummala, D. B. Yelaverthi, R. A. Zane, Z. Ouyang, and M. A. E. Andersen, "A 10-MHz GaNFET-based-isolated high step-down DC-DC converter: Design and magnetics investigation," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 3889–3900, Jul. 2019.
- [14] H. Sarnago, O. Lucia, A. Mediano, and J. M. Burdío, "A class-E direct AC-AC converter with multicycle modulation for induction heating systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2521–2530, May 2014.
- [15] J. Yeon, K. Cho, and H. Kim, "A 3.6 kW single-ended resonant inverter for induction heating applications," in *Proc. Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–7.

- [16] R. E. Zulinski and K. J. Grady, "Load-independent class E power inverters. I. Theoretical development," *IEEE Trans. Circuits Syst.*, vol. 37, no. 8, pp. 1010–1018, Aug. 1990.
- [17] N. Obinata, W. Luo, X. Wei, and H. Sekiya, "Analysis of load-independent class-E inverter at any duty ratio," in *Proc. 45th Annu. Conf. Ind. Electron. Soc.*, Oct. 2019, pp. 1615–1620.
- [18] W. Luo, X. Wei, H. Sekiya, and T. Suetsugu, "Design of load-independent class-E inverter with MOSFET parasitic capacitances," in *Proc. IEEE 62nd Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2019, pp. 529–532.
- [19] H. Sekiya, I. Sasase, and S. Mori, "Computation of design values for class E amplifiers without using waveform equations," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 7, pp. 966–978, Jul. 2002.
- [20] H. Sekiya, T. Ezawa, and Y. Tanji, "Design procedure for class E switching circuits allowing implicit circuit equations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3688–3696, Dec. 2008.
- [21] Y. Tanji, H. Matsushita, and H. Sekiya, "Particle swarm optimization for design of class-E amplifier," *IEICE Nonlinear Theory Appl.*, vol. 3, no. 4, pp. 586–595, 2012.
- [22] R. Miyahara, X. Wei, T. Nagashima, T. Kousaka, and H. Sekiya, "Design of class- E_m oscillator with second harmonic injection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2456–2467, Apr. 2012.
- [23] M. K. Kazimierczuk, *Resonant Power Converters*. Hoboken, NJ, USA: Wiley, 2015.
- [24] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. JSSC-10, no. 3, pp. 168–176, Jun. 1975.
- [25] M. Fu, H. Yin, M. Liu, Y. Wang, and C. Ma, "A 6.78 MHz multiple-receiver wireless power transfer system with constant output voltage and optimum efficiency," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5330–5340, Jun. 2018.
- [26] R. E. Zulinski and J. W. Steadman, "Idealized operation of class E frequency multipliers," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 12, pp. 1209–1218, Dec. 1986.
- [27] M. Albulet, "Analysis and design of the class E frequency multipliers with RF choke," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 42, no. 2, pp. 95–104, Feb. 1995.
- [28] R. Zulinski and J. Steadman, "Class E power amplifiers and frequency multipliers with finite DC-feed inductance," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 9, pp. 1074–1087, Sep. 1987.
- [29] K. Shinoda, T. Suetsugu, M. Matsuo, and S. Mori, "Idealized operation of class DE amplifier and frequency multipliers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 45, no. 1, pp. 34–40, Jan. 1998.
- [30] M. Thian and V. F. Fusco, "Analysis and design of class- E_3F_2 and transmission-line class- E_3F_2 power amplifiers," *IEEE Trans. Circ. Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 902–912, Dec. 2011.
- [31] T. Kousaka, T. Ueta, and H. Kawakami, "Bifurcation of switched nonlinear dynamical systems," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 7, pp. 878–885, Jul. 1999.
- [32] Z. Yang, M. Li, Z. Dai, C. Xu, Y. Jin, T. Li, and F. Tang, "A generalized high-efficiency broadband class-E/ F_3 power amplifier based on design space expanding of load network," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3732–3744, Sep. 2020.
- [33] G. H. Smith and R. E. Zulinski, "An exact analysis of class E amplifiers with finite DC-feed inductance at any output Q," *IEEE Trans. Circuits Syst.*, vol. 37, no. 4, pp. 530–534, Apr. 1990.
- [34] X. Wei, H. Sekiya, S. Kuroiwa, T. Suetsugu, and M. K. Kazimierczuk, "Design of class-E amplifier with MOSFET linear gate-to-drain and nonlinear drain-to-source capacitances," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2556–2565, Oct. 2011.
- [35] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and design of class-E power amplifier with MOSFET parasitic linear and nonlinear capacitances at any duty ratio," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5222–5232, Nov. 2013.
- [36] GaN System. (2021). *GS61004B Spice Model*. [Online]. Available: <https://gansystems.com/gan-transistors/gs61004b/>



WENQI ZHU (Graduate Student Member, IEEE) was born in Hefei, Anhui, China. He received the B.E. degree from Anhui University, China, in 2016, and the M.E. degree from the Graduate School of Advanced Integration Science, Chiba University, Japan, in 2020, where he is currently pursuing the Ph.D. degree.

His current research interests include dc/dc, ac/dc power converters, and WPT systems.



YUTARO KOMIYAMA (Graduate Student Member, IEEE) was born in Nagano, Japan, in June 1998. He received the B.E. degree from Chiba University, Japan, in 2021, where he is currently pursuing the degree with the Graduate School of Science and Engineering.

His research interest includes high-frequency high-efficiency ac/dc inverter.



KIEN NGUYEN (Senior Member, IEEE) received the Ph.D. degree in informatics from the Graduate University for Advanced Studies, Japan, in 2012. He is currently an Assistant Professor with the Graduate School of Science and Engineering, Chiba University. He has published more than 90 publications in peer-reviewed journals and conferences. His research interests include the Internet, the Internet of Things technologies, and wired and wireless communications. He is a member of IEICE. He also involves in IETF activities.



HIROO SEKIYA (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in electrical engineering from Keio University, Yokohama, Japan, in 1996, 1998, and 2001, respectively.

Since April 2001, he has been with Chiba University, Chiba, Japan, where he is currently a Professor with the Graduate School of Science and Engineering. His research interests include high-frequency high-efficiency tuned power amplifiers, resonant dc/dc power converters, dc/ac inverters, and digital signal processing for wireless communications.

Dr. Sekiya is a Senior Member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan, and a member of the Institute of Electronics, Information Processing Society of Japan (IPSI) and the Research Institute of Signal Processing (RISP), Japan.

•••