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Self-Rectifying Characteristics Observed in O-Doped ZrN Resistive Switching Memory Devices Using Schottky Barrier Type Bottom Electrode

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ABSTRACT In this study, we investigated the self-rectifying characteristics of *p*-Si/O-doped ZrN/TiN structures in order to overcome a disturbance between neighboring cells in array structures. The proposed device shows a nonlinear selection characteristic and a Schottky diode property in the positive bias region. We also observed the rectifying region within −2 V, which suppresses the interference with neighboring cells that occurs during a reading operation. Any RS phenomena is not observed especially for the reverse bias sweep to reset the proposed device, which indicated that the proposed device has an intrinsic rectifying property. The proposed device shows the highest current ratio of 6×10^2 at −4.5 V and a maximum current limiting capability in the bias region above −2 V. In addition, the O-doped ZrN memory device shows a stable retention up to 10^4 seconds at 125 °C as well as a high read margin of 380. Therefore, the proposed device suppresses interference in the read operation without additional selector elements, enabling stable memory operation.

INDEX TERMS O-doped ZrN, self-rectifying RRAM, Schottky barrier type bottom electrode, read margin.

I. INTRODUCTION

In recent years, resistive random-access memory (RRAM) has gained a lot of attention as one of the next-generation nonvolatile memory (NVM) devices due to its excellent memory performances, such as low-power consumption, fast operating speed, high density possibility using crossbar arrays, and three-dimensional (3D) architecture [1]–[3]. In addition, as the interest in the artificial neural network (ANN) increases, RRAM-based ANN has also drawn attention [4], [5]. Therefore, research and improving RRAM characteristics, such as reliability, and endurance are essential. In terms of material research, various transition metal nitrides (TMNs), such as HfN, CuN, NiN, ZrN, VN, SiN, and BN have been used as either a resistive switching (RS) layer or an insertion layer between the electrode and the RS layers [6]–[10]. Particularly, in the reported literature [11], [12], ZrN films with high thermal conductivity (50W/mK) and a semiconductor phase was applied as an active layer of RRAM [13], which reported low voltage operation and the feasibility of stable RS characteristics. In addition, in our previous work [14], we reported that oxygen doping with in the ZrN films could improve the reliability of the memory cell by lowing the operating current level especially for the reset current for filament erasure. Nevertheless, in order to realize the high-density crossbar array (CBA) configuration, the reading errors that are caused by the sneak current should be suppressed. Therefore, a device with both functions of a memory cell and a nonlinear access element is required in order to solve the problem. In this regard, several solutions have been tried to solve this problem, which include 1 diode and 1 resistor (1D-1R) [15], 1 transistor and 1 resistor (1T-1R) [16], and 1 selector and 1 resistor (1S-1R) [17]. However, in the case of 1T-1R, which has a similar structure

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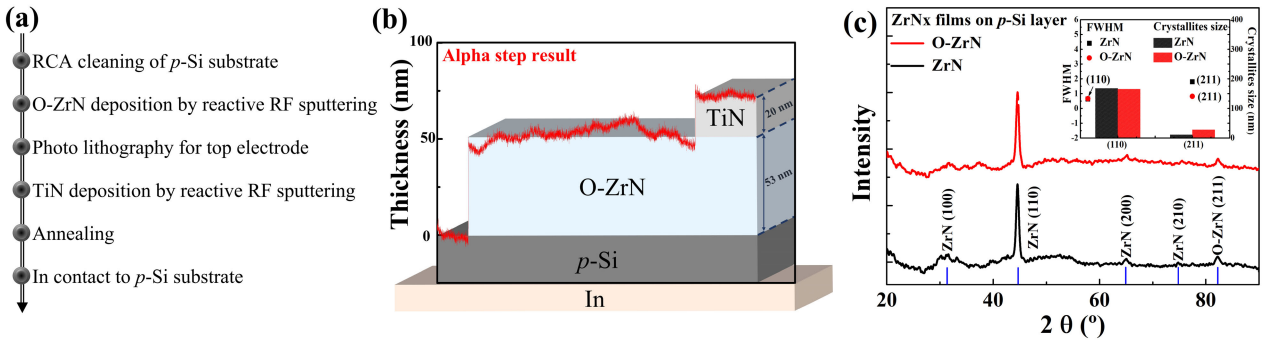

FIGURE 1. (a) Fabrication procedure and (b) device structure of the *p*-Si/O-ZrN/TiN RRAM cell. (c) X-ray diffraction (XRD) peaks in the range of 20° to 90° of the ZrN and O-ZrN films. The inset figure shows the half-width and crystallite size for the ZrN and O-ZrN films.

to the DRAM, the size of the unit cell is increased because MOSFET is normally used to suppress snack current, which requires a high temperature process in RRAM production. In the case of the 1S-1R, the 1S-1R, which has a two-terminal selector of Metal/Insulator/Metal (MIM) structure, consists of MIM (Selector) + MIM (Resistor) structure in series. In terms of device integration, since the 1S1R structure can be fabricated in a vertical structure, it regarded as one of the candidates for high-density 3D integration. Nevertheless, the 1S-1R structure still has limitations in regard to high-density integration compared to the 1R structure due to the limitation in a vertical integration. Similarly, in the case of 1D-1R, it has a similar vertical structure to 1S-1R, which also limits a vertical integration. In order to solve above mentioned issues, we reported here the self-rectifying RS characteristics of Metal/Insulator/Semiconductor (MIS) based RRAM devices, possible to simple structure and low process temperature. Compared to the 1D-1R, 1T-1R, and 1S-1R, the proposed self-rectifying RRAM has similar rectifying characteristic with a simpler structure. Therefore, we expect that it will be considered as the preferable structure for high-density RRAM device.

Therefore, we proposed a *p*-Si/O-doped ZrN(O-ZrN)/TiN structure to fabricate self-rectifying RRAM devices in this study and demonstrated its nonlinear RS property for an array application. As an experimental result, we observed a self-rectifying characteristic that does not require a selector and stable endurance. In order to further understand the RS characteristics when applying it to an array, the maximum read margin (RM) value that can protect data was then investigated.

II. EXPERIMENTAL DETAILS

First, a *p*-Si substrate cleaned by a radio corporation of America (RCA) process was prepared for the sample fabrication. A 53 nm O-ZrN layer was then deposited by reactive radio frequency (RF) magnetron sputtering with a Zr target at room temperature (RT), which was in a mixed gas ambient of $Ar/N_2/O_2$ (20/5/1 sccm). Next, the TiN top electrodes with a thickness of 20 nm and a size of 150 × 150 μm^2 were deposited by RF magnetron sputtering via the photolithography process. After that, the fabricated device was annealed at 450 °C for 30 seconds using the MILA-5000 (Ulvac, Inc) rapid thermal annealing (RTA) equipment for the crystallization of the O-ZrN film. Finally, in order to make ohmic contact on the Si substrate, indium contact metal was used. Figure 1(a) shows the fabrication procedure in detail and the proposed device for the *p*-Si/O-ZrN/TiN

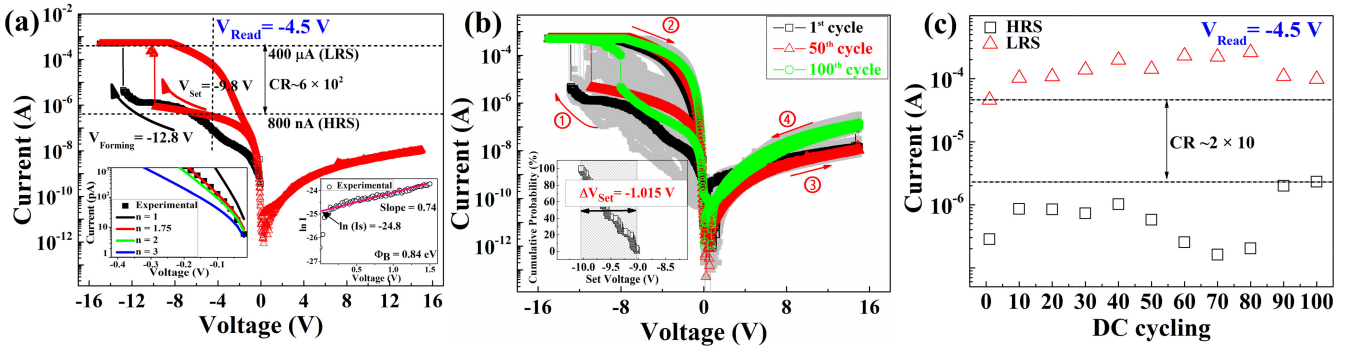

FIGURE 2. (a) The RS characteristics and (b) the repetitive RS characteristics for 100 times for p-Si/O-ZrN/TiN self-rectifying RRAM devices. The insets of Fig. 2(a) are the ideality factor (n) (left side) and Schottky barrier height (ϕB) (right side). The inset of Fig. 2(b) is the cumulative distribution of the set voltage. (c) The DC cycling characteristics for 100 cycles for the proposed devices.

metal-insulator-semiconductor (MIS) structures. Figure 1(b) shows the schematic drawings of the proposed *p*-Si/O-ZrN/TiN RRAM cell, and the thickness of each layer was measured using the alpha step (KLA Tencor). We then investigated the electrical characteristics of the *p*-Si/O-ZrN/TiN RRAM cell.

III. RESULTS AND DISCUSSION

First, in order to evaluate the structural characteristics of the O-ZrN film, we measured the X-ray diffraction (XRD) peaks with the scan range of 20° ∼ 90° and analyzed them using the Joint Committee on Powder Diffraction Standards (JCPDS) card, which is shown in Fig. 1(c). The measured diffraction peaks were observed at 31°, 44°, 64°, 73°, and 82°, which corresponded to the ZrN (100), ZrN (110), ZrN (200), ZrN (210), and O-ZrN (211) planes [18-20], respectively. Compared to the undoped films, such as the ZrN films, we found a disappearance or reduction of the diffraction peaks at 31°, 64°, and 73°, which might indicate the improvement of crystallinity of the ZrN films via the oxygen doping process. In order to further understand the crystallization properties of the ZrN and O-ZrN films, we calculated the full width at half maximum (FWHM) for the (110) and (211) main planes [21]. As a result, after the oxygen doping process, we observed slightly increased FWHM for the (110) plane related to ZrN, whereas the FWHM for the (211) plane related to O-ZrN was decreased about 35 %. In addition, as a calculation result of the crystallite size before and after the oxygen-doping process [22], we found a decrease of 2 % in the ZrN but also an increase of 60 % in the O-ZrN after the oxygen-doping process.

In order to investigate the RS characteristics of the *p*-Si/O-ZrN/TiN memory cell, we then measured the current–voltage (*I*–*V*) curve characteristics in the direct current (DC) mode. After the forming process with −12.8 V, it indicated a change of the resistance from a high resistive state (HRS) to a low resistive state (LRS), which is illustrated in Fig. 2(a). Also, with a reverse bias sweep up to +15 V, the resistance state is then switched back from LRS to HRS, which is the reset process, it indicates that the device operates in a bipolar RS mode with a rectifying region, which include the current limiting regions, in the positive bias. Afterward, when a forward bias is applied, the device is set to LRS at near −9.8 V. In addition, when using the read voltage (V_R) = −4.5 V, the largest current ratio (CR) is 6×10^2. Especially, the proposed device shows a rectifying region within −2 V, which suppresses interference with the neighboring cells that occurs during a reading operation.

Especially, for the reverse bias sweep to reset the proposed device, any RS phenomena could not be observed, which means that the proposed MIS memory cell has an intrinsic rectifying property. In order to further discuss this rectifying phenomenon, the band structures of the *p*-Si/O-ZrN/TiN RRAM, which depend on the polarity of applied voltage, were depicted in Fig. 3. Figure 3(a) shows the band structure of the proposed *p*-Si/ O-ZrN/TiN RRAM cell at 0 V. When negative bias is applied to the TiN top electrode of the RRAM cell, the negative bias lowers the barrier height, which results in high current, which is shown in Fig. 3(b). On the other hand, in reverse bias conditions, the current is suppressed by a higher barrier height, which is shown in Fig. 3(c). As a result, the *I*–*V* curve well matched with the Schottky emission model [23]. In addition, to quantitatively analyze the difference between LRS and HRS, the Schottky barrier height was calculated using the Schottky emission equation, which is $I = I_s\{\exp(qV_d/nkT)-1\}$ and $I_s = AA^*T^2 \exp(-q\phi_B/kT)$, where I_s is the reverse saturation current, ϕ_B is the Schottky barrier height, and A^* is the Richardson constant. The applied voltage, which is V_d, can be positive or negative, and kT/q is 25.9 meV at RT. *n* is the ideality factor. In an ideal diode, *n* is 1, whereas the value might differ from 1 to 6 depending on the fabrication or materials, which is shown in the inset (left side) of Fig. 2(a). By solving the equation, the closely matched ideality factor of the proposed device is calculated

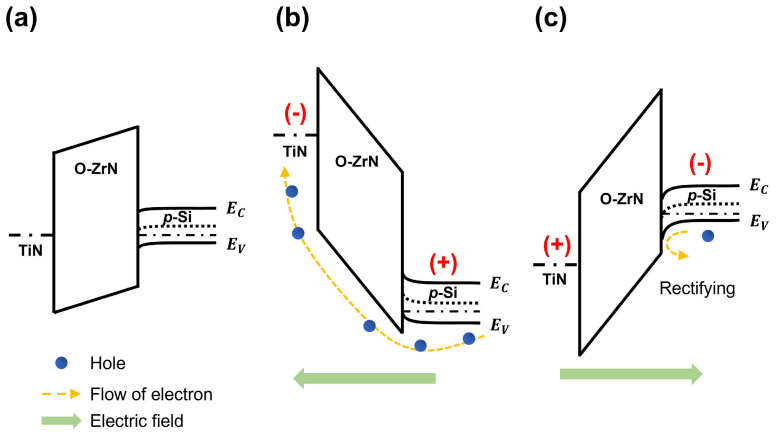

FIGURE 3. Energy band diagram of the p-Si/O-ZrN/TiN RRAM cell. (a) 0 V, (b) positive bias, and (c) negative bias.

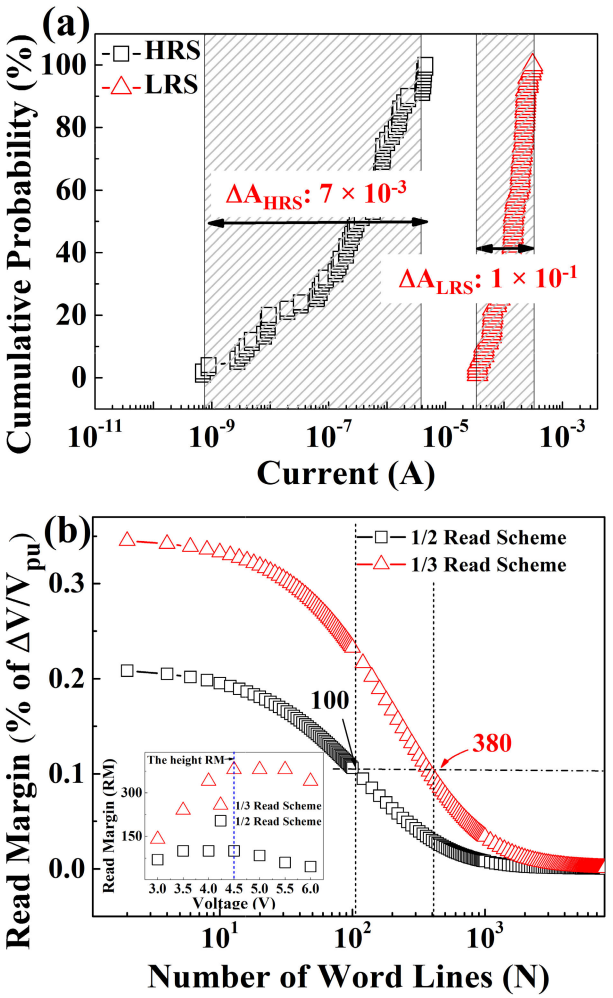

FIGURE 4. (a) Current cumulative distribution at the HRS and at the LRS. (b) The read margin calculated with a 1/2, 1/3 read scheme. The inset figure is the read margin results according to the read voltage.

to be 1.75 when the I_s as low as 2.5×10^{-12} A for the HRS and 16×10^{-12} A for the LRS using exp (−26.7) for the HRS and exp (−24.8) for the LRS. From this result, it is found that it can suppress the forward bias current, such as the diode even if the resistance state for the LRS is switched. In order to further understand the current limiting characteristics in the negative bias region, we then analyzed the ϕ_B for both resistance states, which is shown in the inset (right side) of Fig. 2(a). In this study, the Schottky contact area was 150×150 μm^2, and the values of the ϕ_B for each state were extracted to be 0.89 eV for the HRS and 0.84 eV for the LRS. As a result, this result shows that after the resistance change from the HRS to the LRS, the barrier height between *p*-Si and O-ZrN layers is lowered by 5.6 %, so the flow of the current has increased for the LRS.

Next, in order to examine the variation properties of the proposed device, we investigated the repetitive RS characteristics in the dc mode. As shown in Fig. 2(b), we observed the stable RS characteristics 100 times with the self-rectifying behavior in the $I - V$ characteristic curves. In addition, the inset of Fig. 2(b) shows the statistical distribution of the set voltage (V_{SET}), and the narrow variation in the V_{SET} was −1.015 V with $V_R = -4.5$ V. In addition, as shown in Fig. 2(c), for 100 cycles, the resistance window between HRS and LRS remains at least 20, which is shown in Fig. 4(a). To evaluate the endurance characteristic in pulse mode, we investigated pulse conditions for set and reset operations by controlling the pulse width/height, as shown in inset of Fig. 5. In the set operation, the HRS was changed to the LRS when applying −12 V / 4 μs to the top electrode. Especially, when raising the set pulse height to −14 V, at 700 ns, the device is capable of set operation (or program operation). In reset operation, the LRS was changed to the HRS when applying the reset pulses of 15 V / 40 μs and 16 V / 6 μs, respectively. Then, in order to evaluate using the optimized set/reset pulse conditions, an endurance test was conducted on the proposed self-rectifying O-ZrN RRAM device, as shown in Fig. 5. As a result, we observed that the memory device was maintained for 100 cycles with a current ratio of about 2×10^2, as shown in Fig. 5.

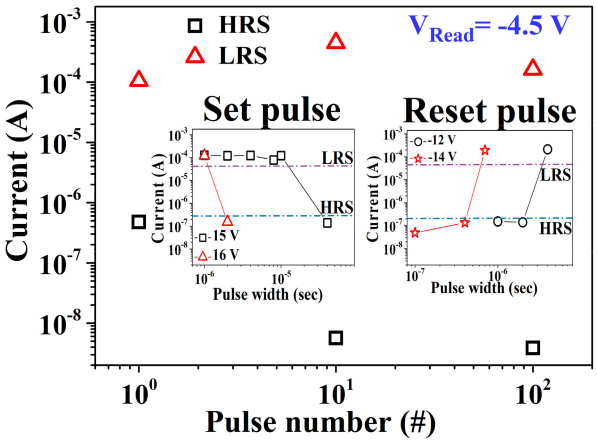

FIGURE 5. Pulse endurance characteristics for the proposed device. Inset shows the resistive switching condition in pulse mode depending on the pulse width and height.

In order to further evaluate the variation at the HRS and the LRS of the device, we analyzed the statistical distribution of each resistance state, which is shown in Fig. 4(a). As a result, we observed a variation of 7×10^{-3} for the HRS and 1×10^{-1} for the LRS with mean values of 9 nA and 100 μA. Compared to the variation on the LRS, the variation is relatively large on the HRS, which can be explained by the filament formation being more irregular than that of the rupture of filament [24].

Next, we investigated the RM characteristic in order to estimate the read disturb phenomena in the CBA during the reading process. Note that a typical RRAM element with bipolar RS has poor nonlinearity in the $I - V$ curve characteristics especially at the LRS, which leads to sneak path problems through the neighboring unselected cells in the array structures. Therefore, reducing the current level of the unselected cells in the LRS to solve the interference phenomenon from sneak path is required.

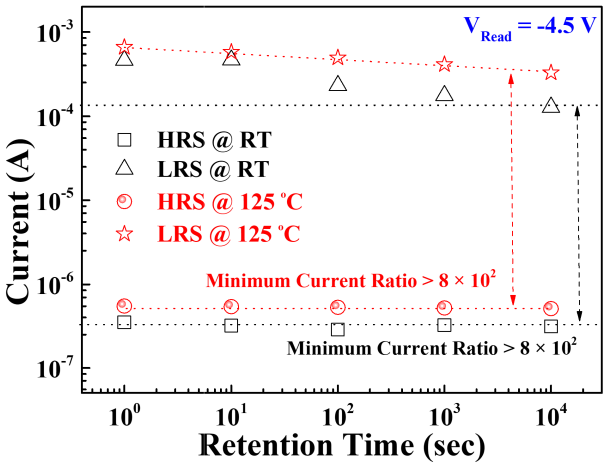

FIGURE 6. Retention characteristics of the memory device for 10^4 s at room temperature and high temperatures.

In order to estimate the maximum array size without interference with the neighboring cells, we calculated the practical RM under the worst conditions for cell selection in the CBA during the read process. This means that it was assumed that all the unselected cells were in the LRS, and the selected cell was in the HRS.

When the V_R was applied to the selected bit line, the read current (I_{read}) flows through the selected cell. At the same time, the unselected cells allow a sneak current (I_{sneak}) to flow together [25]–[27].

Figure 4(b) shows the calculated RM as a function of the number of word lines for the proposed device. In this evaluation, in order to obtain the optimum RM condition, we used various V_R and both read schemes of 1/2 and 1/3, which is shown in Fig. 4. As a result, the height RM was −4.5 V for both read schemes, which is shown in the inset of Fig. 4(b). In $V_R = -4.5$ V, RM was estimated to be 100 in a 1/2 read scheme, whereas an increased RM to 380 was obtained using a 1/3 read scheme. Therefore, when applied to a CBA, it is confirmed that the proposed RRAM can reliably protect the stored data without disturbance up to 19×19 CBA structures.

Finally, the retention property of the memory was conducted in order to evaluate the data storage ability. For the evaluation of the retention characteristics in the extreme environment, we measured it for 10^4 s at RT and at a high temperature of 125 °C. Figure 6 depicts the retention characteristics of the *p*-Si/O-ZrN/TiN RRAM device. As a result, the device had a slight decrease as time passed for the LRS, and the current value for both states increased at high temperatures. Nevertheless, the CR maintained at least 8×10^2 or higher. Consequently, these results show that the proposed device can stably maintain the stored data for a long time without deterioration even at high temperatures.

IV. CONCLUSION

We proposed an O-ZrN based self-rectifying RRAM device using a *p*-Si bottom electrode in this study. In the experiment results, the proposed device shows asymmetric resistive switching hysteresis in $I - V$ characteristics, which provides current limiting regions below $1/3V_R$ and suppresses the interference phenomenon during the reading operation up to the 19×19 arrays. Further optimization of the device performance with higher nonlinearities and lower variations is likely to apply these devices to low-power and high-density crossbar memory arrays in the future.

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(Jinsu Jung and Doowon Lee contributed equally to this work.)

REFERENCES

[1] Z. Wang, H. Wu, G. W. Burr, C. S. Hwang, K. L. Wang, Q. Xia, and J. J. Yang, "Resistive switching materials for information processing," *Nature Rev. Mater.*, vol. 5, no. 3, pp. 173–195, Mar. 2020, doi: 10.1038/s41578-019-0159-3.

[2] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Mater.*, vol. 6, no. 11, pp. 833–840, Nov. 2007, doi: 10.1038/nmat2023.

[3] H.-D. Kim, M. J. Yun, and S. Kim, "All ITO-based transparent resistive switching random access memory using oxygen doping method," *J. Alloys Compounds*, vol. 653, pp. 534–538, Dec. 2015, doi: 10.1016/j.jallcom.2015.09.076.

[4] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 211–221, Jan. 2012, doi: 10.1109/TCSI.2012.2215714.

[5] J. Sun, J. Han, Y. Wang, and P. Liu, "Memristor-based neural network circuit of emotion congruent memory with mental fatigue and emotion inhibition," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 3, pp. 606–616, Jun. 2021, doi: 10.1109/TBCAS.2021.3090786.

[6] M. H. Kim, S. Kim, S. Bang, T. H. Kim, D. K. Lee, S. Cho, and B. G. Park, "Uniformity improvement of sinx-based resistive switching memory by suppressed internal overshoot current," *IEEE Trans. Nanotechnol.*, vol. 17, no. 4, pp. 824–828, 2018. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/8369124

[7] Y. Bai, H. Wu, R. Wu, Y. Zhang, N. Deng, Z. Yu, and H. Qian, "Study of multi-level characteristics for 3D vertical resistive switching memory," *Sci. Rep.*, vol. 4, no. 1, pp. 1–7, May 2015. [Online]. Available: https://www.nature.com/articles/srep05780

[8] Y.-R. Jeon, Y. Abbas, A. S. Sokolov, S. Kim, B. Ku, and C. Choi, "Study of *in situ* silver migration in amorphous boron nitride CBRAM device," *ACS Appl. Mater. Interfaces*, vol. 11, no. 26, pp. 23329–23336, Jul. 2019. [Online]. Available: https://pubs.acs.org/doi/abs/10.1021/acsami.9b05384

[9] A. B. Mei, O. Hellman, N. Wireklint, C. M. Schlepütz, D. G. Sangiovanni, B. Alling, A. Rockett, L. Hultman, I. Petrov, and J. E. Greene, "Dynamic and structural stability of cubic vanadium nitride," *Phys. Rev. B, Condens. Matter*, vol. 91, no. 5, Feb. 2015, Art. no. 054101, doi: 10.1103/PhysRevB.91.054101.

[10] S. Kim, Y. F. Chang, M. H. Kim, and B. G. Park, "Improved resistive switching characteristics in Ni/SiN_x/p^{++}-Si devices by tuning x," *Appl. Phys. Lett.*, vol. 111, Jul. 2017, Art. no. 033509, doi: 10.1063/1.4985268.

[11] Q. Zheng, A. B. Mei, M. Tuteja, D. G. Sangiovanni, L. Hultman, I. Petrov, J. E. Greene, and D. G. Cahill, "Phonon and electron contributions to the thermal conductivity of VNx epitaxial layers," *Phys. Rev. Mater.*, vol. 1, no. 6, Nov. 2017, Art. no. 065002, doi: 10.1103/PhysRevMaterials.1.065002.

[12] M. D. Re, R. Gouttebaron, J. P. Dauchot, P. Leclere, G. Terwagne, and M. Hecq, "Study of ZrN layers deposited by reactive magnetron sputtering," *Surf. Coat. Technol.*, vol. 174, pp. 240–245, 2003, doi: 10.1016/S0257-8972(03)00679-0.

[13] A. Rizzo, M. A. Signore, L. Mirenghi, and E. Serra, "Properties of ZrNx films with x>1 deposited by reactive radiofrequency magnetron sputtering," *Thin Solid Films*, vol. 515, no. 4, pp. 1307–1313, Dec. 2006, doi: 10.1016/j.tsf.2006.03.020.

[14] D. Kumar, U. Chand, L. W. Siang, and T. Y. Tseng, "ZrN-based flexible resistive switching memory," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 705–708, May 2020, doi: 10.1109/LED.2020.2981529.

[15] F. Gül, "Addressing the sneak-path problem in crossbar RRAM devices using memristor-based one Schottky diode-one resistor array," *Results Phys.*, vol. 12, pp. 1091–1096, Mar. 2019, doi: 10.1016/j.rinp.2018.12.092.
[16] Z.-R. Wang, Y. T. Su, Y. Li, Y. X. Zhou, T. J. Chu, K. C. Chang, and X. S. Miao, "Functionally complete Boolean logic in 1T1R resistive random access memory," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 179–182, Feb. 2017, doi: 10.1109/LED.2016.2645946.
[17] Y.-C. Chen, C.-C. Lin, S.-T. Hu, C.-Y. Lin, B. Fowler, and J. Lee, "A novel resistive switching identification method through relaxation characteristics for sneak-path-constrained selectorless RRAM application," *Sci. Rep.*, vol. 9, no. 1, pp. 1–6, Dec. 2019, doi: 10.1038/s41598-019-48932-5.
[18] W. Lee, J. Park, S. Kim, J. Woo, J. Shin, G. Choi, S. Park, D. Lee, E. Cha, B. H. Lee, and H. Hwang, "High current density and nonlinearity combination of selection device based on $TaO_x/TiO_2/TaO_x$ structure for one selector–one resistor arrays," *ACS Nano*, vol. 6, no. 9, pp. 8166–8172, Sep. 2012, doi: 10.1021/nn3028776.
[19] H.-D. Kim, M. J. Yun, S. M. Hong, H.-M. An, and T. G. Kim, "Improved reliability of Ti/ZrN/Pt resistive switching memory cells using hydrogen postannealing," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectronics: Mater., Process., Meas., Phenomena*, vol. 31, no. 4, Jul. 2013, Art. no. 041205, doi: 10.1116/1.4813792.
[20] J. Čyvienė and J. Dudonis, "Zr, zrN and zr/Al thin films deposition using arc evaporation and annealing," *Acta Phys. Polonica A*, vol. 114, no. 4, pp. 769–777, Oct. 2008, doi: 10.12693/APhysPolA.114.769.
[21] E. S. Andres, A. D. Prado, I. Martil, G. G. Diaz, F. L. Martinez, D. Bravo, and F. J. Lopez, "Rapid thermal annealing effects on plasma deposited SiOx:H films," *Vaccum*, vol. 67, nos. 3–4, pp. 531–536, 2002, doi: 10.1016/S0042-207X(02)00244-0.
[22] R. Elmoubarki, F. Z. Mahjoubi, A. Elhalil, H. Tounsadi, M. Abdennouri, M. Sadiq, S. Qourzal, A. Zouhri, and N. Barka, "Ni/Fe and Mg/Fe layered double hydroxides and their calcined derivatives: Preparation, characterization and application on textile dyes removal," *J. Mater. Res. Technol.*, vol. 6, no. 3, pp. 271–283, Jul. 2017, doi: 10.1016/j.jmrt.2016.09.007.
[23] C. R. Crowell, "The Richardson constant for thermionic emission in Schottky barrier diodes," *Solid-State Electron.*, vol. 8, no. 4, pp. 395–399, Apr. 1965, doi: 10.1016/0038-1101(65)90116-4.
[24] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal-oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012, doi: 10.1109/JPROC.2012.2190369.
[25] C.-L. Lo, T.-H. Hou, M.-C. Chen, and J.-J. Huang, "Dependence of read margin on pull-up schemes in high-density one selector–one resistor crossbar array," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 420–426, Jan. 2013, doi: 10.1109/TED.2012.2225147.
[26] C. J. Amsinck, N. H. D. Spigna, D. P. Nackashi, and P. D. Franzon, "Scaling constraints in nanoelectronic random-access memories," *Nanotechnology*, vol. 16, no. 10, pp. 2251–2260, Aug. 2005, doi: 10.1088/0957-4484/16/10/047.
[27] Y. Kim, Y. J. Kwon, J. Kim, C. H. An, T. Park, D. E. Kwon, H. C. Woo, H. J. Kim, J. H. Yoon, and C. S. Hwang, "Novel selector-induced current-limiting effect through asymmetry control for high-density one-selector–one-resistor crossbar arrays," *Adv. Electron. Mater.*, vol. 5, no. 7, Jul. 2019, Art. no. 1800806, doi: 10.1002/aelm.201800806.

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