Ultra-High Step-Up DC-DC Converters Based on Center-Tapped Inductors

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ABSTRACT In this paper, a new family of ultra-high step-up DC-DC converters based on a center-tapped coupled inductor (CI) is proposed. These single-switch converters employ different inductive and capacitive power transfer techniques by utilizing multi-winding CIs, intermediate capacitor links and simple switched-capacitors to improve the transferred power rate, harvest magnetizing and leakage inductance energies, and enhance power density. Achieving high voltage gain in low duty cycle values enables the proposed converters to operate under wide output voltage ranges; meanwhile, distributing the output voltage on two or three output ports alleviates the voltage stress on output terminal components. Low input current ripple, simple pulse width modulation control, low switch voltage stress and operation without circulating current can be listed as other features. In this paper, the proposed family is introduced, theoretically analyzed and compared with other state-of-the-art researches. Finally, the accuracy of analyses are evaluated with some experimental tests of a 1.25 kW experimental prototype.

INDEX TERMS DC-DC converter, high step-up power converter, center-tapped coupled inductor.

I. INTRODUCTION

In the massive energy harvesting technologies development today, using different types of renewable energies, such as photovoltaic and fuel cells, is inevitable due to the deficiency in fossil fuels and alarming conditions of environmental issues [1], [2]. High performance high step-up DC-DC converters are indispensable for such applications in which the low output voltage (typically lower than 50 V) should be boosted to a desired level [3]. Among different approaches to achieve high voltage gain converters, interleaving and utilizing coupled inductors (CI) and/or voltage multiplier cells (VMC)s obtain the merits of low duty cycle requirement and high efficiency operation for reaching the desired high gain ratio [4]–[7]. Furthermore, numerous features should be considered during a high step-up DC-DC converter's design, among which, amount of power loss, control complexity,

number of operational modes, converter's size, imposed inrush current on semiconductors, required CI turns, power density and desired duty cycle range are the most crucial ones. For example, as a practical consideration, the high voltage gain converter presented in [8] suffers from high conduction loss due to its high operation duty cycle range and high number of components. In addition, using high number of power switches increases the complexity in control system, the problem that is also existed in the suggested converters in [9]–[11].

Reduced input current ripple and continuous input current are the vital specifications of the converters that are utilized in renewable energy-based systems due to the harmful impacts of large and pulsating input current on the energy interfaces. The converters introduced in [12]–[16] suffer from large input current ripple owing to their input-side CI. Adopting interleaving technique and avoiding input CI are the effective solutions for the input current ripple problem. The suggested converter in [17] utilizes interleaving and CI techniques in

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addition to an active clamp circuit to achieve high output voltage and low current stress values, simultaneously. However, high number of semiconductors and large output voltage ripple limit its industrial applications. The interleaved converters introduced in [18]–[20] focus on the inductor coupling approach alongside with the VCMs to increase voltage gain ratio. Nevertheless, their high number of components, especially the passive ones, causes high size and low reliability. Scholars try to reduce the components' current stress and recycle the CI leakage energy in [21], [22], but the complex control system restricts their chance in real life applications. The converters presented in [23], [24] are suitable for high voltage applications; however, their disability of recycling leakage inductance energy and employing four inductors' cores are their main drawbacks. In [25] and [26], two interleaved DC-DC converters are proposed with passive and active clamp circuits, respectively, in order to solve switch voltage spikes. However, their need for high duty cycle values to enhance output voltage gain is their main disadvantage. The multi-stage high gain converter suggested in [27] utilizes conventional interleaved boost converter in each stage. Unfortunately, this method increases the power losses and circulating current.

The multi-input converter introduced in [28] utilizes a modified VMC in order to increase voltage gain ratio, but it cannot achieve such a high experimental output voltage ratio due to its high loss VMC. The SEPIC-based high step-up converter introduced in [29] uses CI and VMC to increase voltage gain ratio, but it suffers from low efficiency and high components count. In [30], authors tried to achieve high voltage gain and reduced input current ripple by adopting interleaving and switched-capacitor techniques, but the high number of components, either passive or active components, is its main drawback. Authors introduced a non-isolated high gain DC-DC converter and tried to achieve soft-switching performance in [31], but its high input current ripple and the need for high duty cycle are its main disadvantages that restrict its applications and increase conduction loss. In [32], scholars proposed an ultra-high gain DC-DC converter and used the interleaving technique to reduce the size of filter components and switching loss. However, utilizing two three-winding CIs, nine diodes, eight capacitors, and two switches are its main drawbacks that increase its cost and volume.

In order to fulfill the desired factors and resolve the problems of the above-mentioned converters, a family of center-tapped inductor based DC-DC converters are introduced in this paper that are able to provide ultra-high voltage gain ratio. Their low input current ripple makes them suitable for renewable energy-based systems. Additionally, the ability to optimize output voltage ripple is another feature of the proposed single-switch converters. In this paper, the proposed converters are introduced, analyzed and designed comprehensively. Then, they are evaluated by the comparison of operational characteristics with other state-of-the-art researches. Eventually, the theoretical analytics are validated through some experimental results of a 1.25 *kW* prototype.

II. PROPOSED CONVERTERS

Fig. 1 indicates the circuit of the proposed single-switch converters which are named as Pro1 ∼ Pro4. The converter Pro1 is the basic proposed topology and Pro2 ∼ Pro4 are the improved versions. Operation principle of all the proposed converters are almost the same with some differences that will be explained in the following. As shown in Fig. 1 (a)-(d), all introduced converters consist of some similar components such as: one two-, three- or four-winding center-tapped CI, that is modeled with an ideal transformer in addition to a parallel magnetizing inductor (L_m) and leakage inductances (L_{r1} and L_{r2}), one input inductor (L), one intermediate link capacitor (C_1), one power switch (S), one switched capacitor (C_2), some diodes ($D_{(i)}$) and output capacitors ($C_{o(i)}$). The fourth topology (Pro4) is assumed as the main converter in this paper; so the comprehensive analysis of Pro4 is provided besides a brief analysis of other topologies.
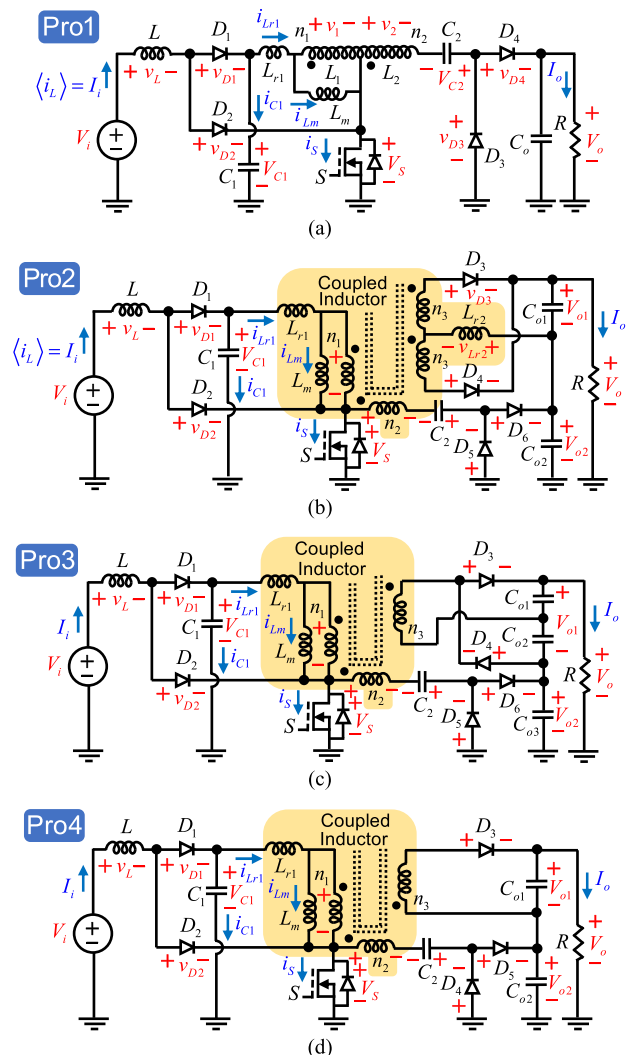

FIGURE 1. Classification of the DC-DC converters.

A. FIRST PROPOSED CONVERTER (PRO1)
Current flow paths of the Pro1 converter in its two operational intervals of continuous conduction mode (CCM) are shown

in Fig. 2. The operational modes of this converter are evaluated as follows:

1) MODE 1 ($0 < t < DT_S$) [FIG. 2(a)]

In this time interval, the switch S is turned ON; therefore, the input and magnetizing inductors are charged with the energy of the input source and C_1, respectively. Diodes D_3 and D_4 are forward and reverse biased, respectively, and C_2 is charged through the secondary winding of the CI, consequently. Considering $n_2/n_1 = N_2$ and $n_3/n_1 = N_3$, voltages of L and L_m are calculated as

$$v_L = V_i \tag{1}$$

$$v_{Lm} = V_{C1} \tag{2}$$

$$V_{C2} = N_2 V_{Lm} \tag{3}$$

2) MODE 2 ($DT_S < t < T_S$) [FIG. 2(b)]

Finishing the switch ON-state leads to the forward bias of D_1 and D_4. Hence, the current paths are changed according to Fig. 2(b).

$$v_L = V_i - V_{C1} \tag{4}$$

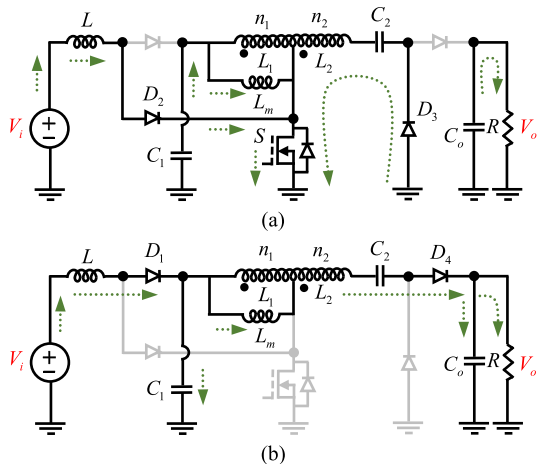$$v_{Lm} = \frac{1}{N_2 + 1}(V_{C1} + V_{C2} - V_o) \tag{5}$$

(a)

(b)

FIGURE 2. Equivalent circuits of Pro1 in; (a) Mode 1. (b) Mode 2.

B. FOURTH PROPOSED CONVERTER (PRO4)

Equivalent circuits of the proposed double-output port Pro4 converter are demonstrated in Fig. 3, which result in the key voltage and current waveforms of Fig. 4.

1) MODE 1 ($0 < t < DT_S$) [FIG. 3(a)]

At first, the power switch S is turned ON, so the diodes D_1 and D_2 are revere and forward biased, respectively, and L is magnetized with V_i, consequently. In this condition, the capacitor C_1 is discharged to the L_m and the capacitor C_2 is charged with the transferred power of the CI in its secondary winding.

$$v_L = V_i \tag{6}$$

$$v_{Lm} = V_{C1} \tag{7}$$

$$V_{C2} = N_2 V_{Lm} = N_2 V_{C1} \tag{8}$$

2) MODE 2 ($DTs < t < T_S$) [FIG. 3(b)]

At $t = DT_s$, the power switch duty cycle is completed and the diodes D_1 and D_5 start conducting; hence, the stored energies of L, L_m, and C_2 are transferred to the C_1, C_{o1} and C_{o2}, respectively. The main equations of this mode are listed as

$$v_L = V_i - V_{C1} \tag{9}$$

$$v_{Lm} = \frac{1}{N_2 + 1}[V_{C1} + V_{C2} - V_{o2}] \tag{10}$$
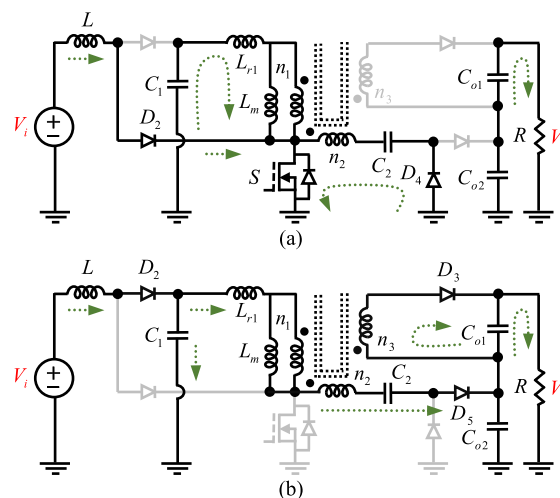
$$V_{o1} = -N_3 V_{Lm} \tag{11}$$

(a)

(b)

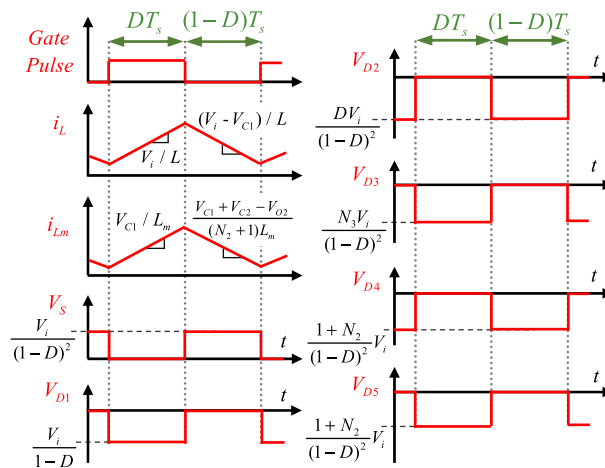FIGURE 3. Equivalent circuits of Pro4 in; (a) Mode 1. (b) Mode 2.

FIGURE 4. Typical voltage and current waveforms of Pro4 in CCM operation.

III. STEADY-STATE PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTERS

A. VOLTAGE GAIN CALCULATION

Voltage gain of the Pro4 converter is calculated by volt-second balance law and the resulted equations of

the previous section as

$$DV_i + (1-D)(V_i - V_{C1}) = 0 \qquad (12)$$

$$DV_{C1} + (1-D)(\frac{V_{C1} + V_{C2} - V_{o2}}{1 + N_2}) = 0 \qquad (13)$$

Using (12), the voltage of C_1 can be expressed as follows:

$$V_{C1} = \frac{V_i}{1-D} \qquad (14)$$

By substituting (14) into (8), the voltage of capacitor C_2 is obtained as

$$V_{C2} = \frac{N_2 V_i}{1-D} \qquad (15)$$

Then, substituting (14) and (15) into (13) leads to

$$V_{o2} = \frac{(N_2 + 1)V_i}{(1-D)^2} \qquad (16)$$

Regarding to Mode 2, and (11) and (14)-(16), the voltage across C_{o1} is calculated as

$$V_{o1} = \frac{N_3 D V_i}{(1-D)^2} \qquad (17)$$

Due to the attained output capacitors' voltages, the voltage gain of the Pro4 converter in CCM operation is concluded as

$$M_{Pro4} = \frac{V_{o1} + V_{o2}}{V_i} = \frac{1 + N_2 + N_3 D}{(1-D)^2} \qquad (18)$$

Voltage gain of the Pro1, Pro2, and Pro3 converters are calculated with the same procedure and the results are given in Table. 1 and Fig. 5. It is worth to mention that volt-second balancing law should be applied on L_{r2} as well as L and L_m to obtain voltage gain of the Pro2 converter.

TABLE 1. Voltage gain of pro1~Pro3.

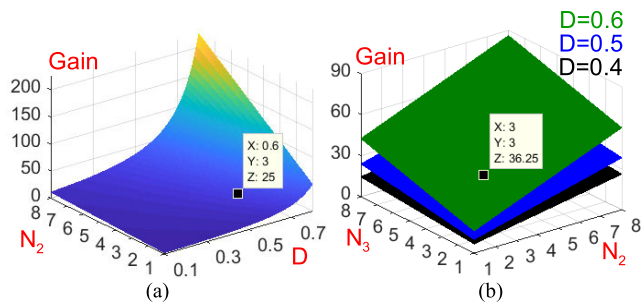| Converter	Voltage Gain
Pro1	$M_{Pro1} = \dfrac{1+N_2}{(1-D)^2}$
Pro2	$M_{Pro2} = \dfrac{1+N_2}{(1-D)^2} + \dfrac{2N_3 D}{1-D}$
Pro3	$M_{Pro3} = \dfrac{1+N_2+N_3}{(1-D)^2}$

FIGURE 5. Voltage gain. (a) Pro1. (b) Pro4.

TABLE 2. Voltage stress analysis of Pro1~Pro3.

Voltage stress	Pro1	Pro2	Pro3
V_S		$\dfrac{1}{(1-D)^2}V_i$	
V_{D1}		$\dfrac{1}{1-D}V_i$	
V_{D2}		$\dfrac{D}{(1-D)^2}V_i$	
V_{D3}	$\dfrac{1+N_2}{(1-D)^2}V_i$	$\dfrac{2DN_3}{(1-D)^2}V_i$	$\dfrac{N_3}{(1-D)^2}V_i$
V_{D4}		$\dfrac{2N_3}{1-D}V_i$	
V_{D5}	--	$\dfrac{1+N_2}{(1-D)^2}V_i$	
V_{D6}	--		

B. VOLTAGE AND CURRENT STRESS ANALYSES

The equivalent circuit of the Pro4 converter during switch OFF-state (Mode 2) should be analyzed to obtain switch voltage stress. According to (15), (16) and Fig. 4(b), the switch voltage stress can be calculated as

$$V_S = \frac{1}{(1-D)^2}V_i \qquad (19)$$

Similarly, voltage stress of the diodes are given as

$$V_{D1} = \frac{1}{1-D}V_i \qquad (20)$$

$$V_{D2} = \frac{D}{(1-D)^2}V_i \qquad (21)$$

$$V_{D3} = \frac{N_3}{(1-D)^2}V_i \qquad (22)$$

$$V_{D4} = V_{D5} = \frac{1+N_2}{(1-D)^2}V_i \qquad (23)$$

In addition, voltage stress of the semiconductors in Pro1~Pro3 are tabulated in Table. 2, and their normalized values are plotted in Fig. 6. In order to calculate current stress of the semiconductors, the current paths during their on-state should be analyzed. Hence, according to Fig. 4, average current of the switch and diodes of the Pro4 converter are obtained as

$$I_S = I_i + I_{Lr1} + \frac{1}{N_2}(I_{Lr1} - I_{Lm}) \qquad (24)$$

$$I_{D1} = I_{D2} = I_i \qquad (25)$$

$$I_{D3} = \frac{1}{N_3}I_{Lm} \qquad (26)$$

$$I_{D4} = \frac{1}{N_2}(I_{Lr1} - I_{Lm}) \qquad (27)$$

$$I_{D5} = I_{Lr1} \qquad (28)$$

where, I_{Lr1} and I_{Lm} are the average values of leakage and magnetizing inductance currents, respectively. The same procedure can be followed to obtain current stress of active components of Pro1~Pro3.
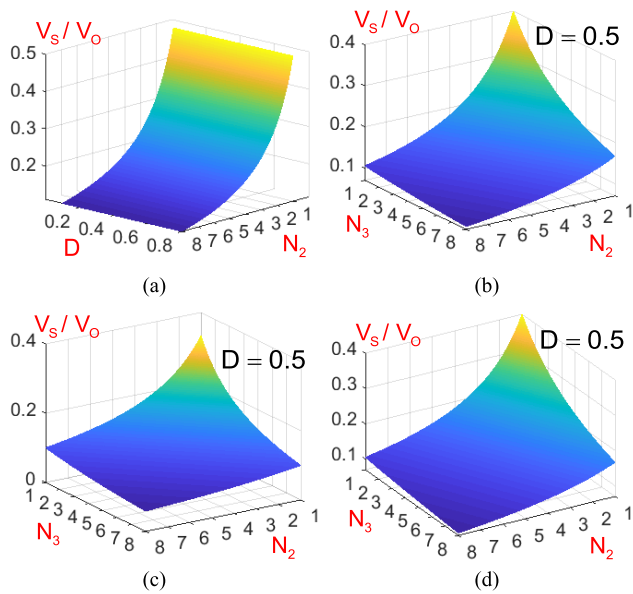
FIGURE 6. Normalized switch voltage stress. (a) Pro1. (b) Pro2. (c) Pro3. (d) Pro4.

C. DISCONTINUOUS CONDUCTION MODE (DCM) BOUNDARY

In the DCM-CCM boundary of the proposed converters, their average input current in the boundary conduction mode (I_{iB}) is equal to

$$I_{iB} = \frac{\Delta i_L}{2} \tag{29}$$

According to the proposed converters' voltage gain, output load and the current path during switch ON-state, output current and load resistance in the boundary conduction mode (I_{oB}) is obtained as

$$I_{oB} = \frac{DV}{2f_S LM^2} \tag{30}$$

$$R_B = \frac{2f_S LM^2}{D} \tag{31}$$

Normalized form of the boundary conduction mode output current and load resistance of the proposed converters are plotted in Fig. 7 with respect to the duty cycle and the CI turns ratio to identify the CCM and DCM operation regions. As can be seen, the larger the duty cycle and the turns ratio, the wider the solution area in CCM for normalized load resistance and output current, respectively.

IV. DESIGN CONSIDERATIONS

According to the CCM performance of the Pro4 converter, and the desired voltage and current ripple values of passive components, they can be designed as

$$L = \frac{DV_i}{f_S \Delta i_L} \tag{32}$$

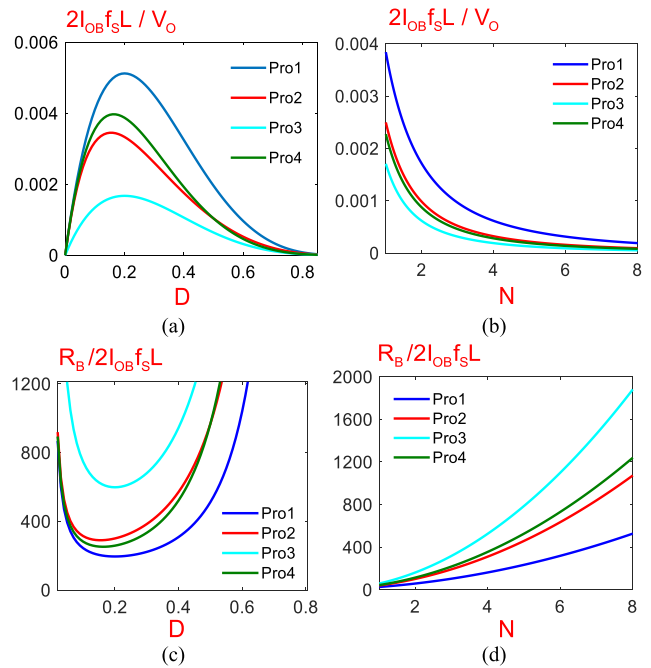$$L_m = \frac{DV_i}{f_S \Delta i_{Lm}(1 - D)} \tag{33}$$

FIGURE 7. Normalized boundary conduction mode output current with respect to: (a) duty cycle in $N_2 = N_3 = N = 3$, and (b) turns ratio in $D = 0.6$. Normalized load resistance with respect to (c) duty cycle in $N_2 = N_3 = N = 3$, and (b) turns ratio in $D = 0.6$.

$$C_1 = \frac{DI_{Lr1}}{f_S \Delta V_{C1}} \tag{34}$$

$$C_2 = \frac{(1 - D)I_{Lr1}}{f_S \Delta V_{C2}} \tag{35}$$

$$C_{o1} = \frac{DI_o}{f_S \Delta V_{Co1}} \tag{36}$$

$$C_{o2} = \frac{DI_o}{f_S \Delta V_{Co2}} \tag{37}$$

Continuous input current with low ripple is a feature of the proposed converters that makes them suitable for renewable application. In order to achieve minimum input current ripple, the effects of different parameters such as turns ratio and duty cycle should be analyzed. According to Fig. 3, the input current ripple of the Pro4 converter is obtained as

$$\Delta i_L = \frac{DV_o}{f_S LM} \tag{38}$$

Substituting (18) into (38) leads to

$$\Delta i_L = \frac{V_O}{f_S L} \frac{D(1 - D)^2}{1 + N_2 + N_3 D} \tag{39}$$

Fig. 8 illustrates the variation of the input current ripple with respect to CI turns ratio and duty cycle in different $B = V_o/f_S L$ values, where B is utilize to normalize the calculated input current ripple with respect to the converters' output voltage, switching frequency and input inductor. This helps to compare the converters in the same operation and design conditions. It is clear in Fig. 8 that (i) Δi_L reduces by the turns ratio rise, and (ii) Δi_L reaches to its maximum

value in a particular duty cycle. Fig. 9 shows the duty cycle values which belong to the Δi_L maximum points with respect to the turns ratios. Due to this figure, the duty cycle values that lead to maximum Δi_L are less than 0.302; therefore, it does not restrict the operational duty cycle range of the proposed converters. In other words, it is mostly preferred to utilize the high step-up converters in $D > 0.4$ to reach high voltage gain which does not coincide with the maximum input current ripple area. This makes the proposed converter an appropriate candidate for renewable energy applications such as photovoltaics and fuel cells. Fig. 10 presents the desired operation region for duty cycle and turns ratio to achieve specific normalized input current ripple ($\Delta i_L f_S L/RI_i = D/M^2$). According to this figure, high N and D values, which are preferred in high step-up converters, are located in the desired operation area.
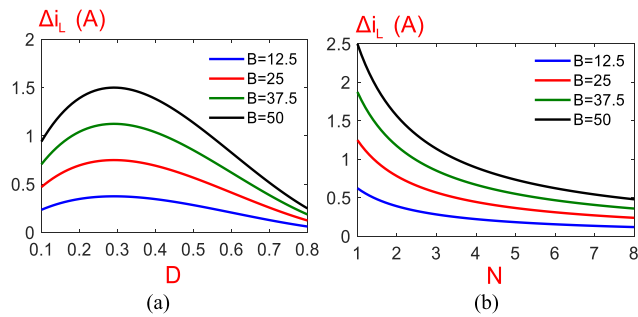

FIGURE 8. Variation of input current ripple in Pro4 with respect to B and: (a) duty cycle in $N_2 = N_3 = N = 3$. (b) turns ratio in $D = 0.5$.
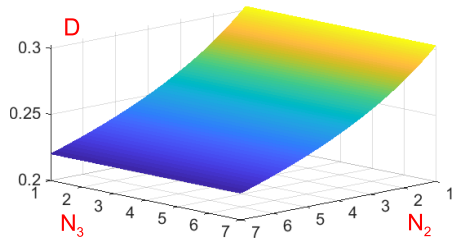

FIGURE 9. Maximum input current ripple realization in Pro4 with respect to duty cycle and CI turns ratios.

V. EFFICEINT INDUCTIVE OPERATION

In order to enhance the performance of the proposed converters, the stored energies in all capacitive and inductive circuit components are recycled and transferred to the output capacitors due to the performance of semiconductors during operational modes. Power flow paths of the Pro4 converter are depicted in Fig. 11, where (i) the stored energy in L is transferred to C_1 in $(1-D)T_s$ (blue path), (ii) the energy of C_1 is discharged to C_2 via n_1 and n_2 in DT_s (purple path), (iii) the energy of L_{r1} is recycled to C_{o2} in $(1-D)T_s$ (green path), (iv) the magnetizing energy is guided to C_{o1} via n_1 and n_3 in $(1-D)T_s$ (red path), and (v) the energy of L_{r2} is transferred to C_{o1} in $(1-D)T_s$ (yellow path).
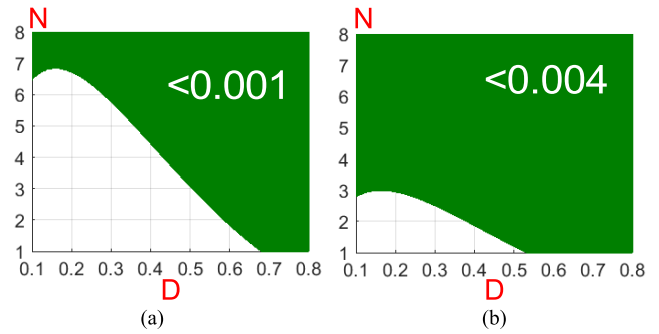

FIGURE 10. Desired operation region of normalized input current ripple ($\Delta i_L f_S L/RI_i$) with respect to duty cycle and turn ration in Pro4.
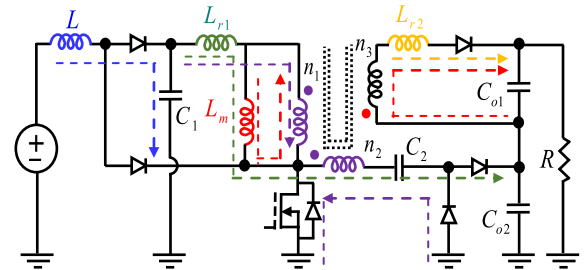

FIGURE 11. Power flow paths in Pro4 converter.

VI. COMPARISON

In real industrial applications, introducing a flawless converter is not possible due to the existence of numerous evaluation parameters and desired factors. However, in this study, it is tried to achieve a family of converters with acceptable parameters and valuable features that make them suitable for different industrial applications.

In this section, a fair comparison is performed between the proposed converters and recently introduced ones to clarify their pros and cons. For this purpose, the converters are classified into three categories based on the count of utilized windings in their coupled inductors, and the results are presented in Table 3 and Figs. 12 and 13. Quantities of active and passive components are considered as the first factor in Table 3 since it affects the volume, cost, efficiency, and power density of the converters. From this point of view: (i) [12], [29], [40], [43], [44] and the proposed converters have the least number of power switches and gate drivers, (ii) although the number of semiconductors in [12], [38] and [44] is the lowest, they present low voltage gain. Therefore, by considering the realized voltage gain of the converters, the number of utilized semiconductors is not high in the proposed converters, (iii) [9], [17], [23], [25] and [34] have the highest number of magnetic cores, and (iv) [11], [12], [17], [23], [25], [31], [34]–[38], [40], [42], [44] and Pro1 have the least number of capacitors. Hence, the proposed converters employ acceptably low number of components.

Input current ripple is another significant parameter that specifies whether the converter is suitable for some application such as renewable sources or not. Therefore, low input

TABLE 3. Comparison of proposed converter with other state-of-the-art researches.

	Refs.	S/D/C/CI+L	LICR	NOM	Voltage Gain (M)	Voltage Stress of Switch(s) (ΣV_S)	Voltage Stress of Diodes (ΣV_D)
Topologies with Two-winding CI	[11]	$4/0/2/1^{2w}+0$	No	2	$\dfrac{1}{(1-D)^2}$	$\dfrac{4-2D}{1-D}V_o$	0
	[12]	$1/2/2/1^{2w}+0$	No	5	$\dfrac{N+1}{1-D}$	V_o	$\dfrac{1+2N}{1+N}V_o$
	[17]	$4/4/3/1^{2w}+2$	Yes	8	$\dfrac{N+1}{1-D}$	$\dfrac{4V_o}{1+N}$	$4V_o$
	[23]	$2/4/3/1^{2w}+2$	No	4	$\dfrac{2}{1-D}+ND$	$\dfrac{2V_o}{2+ND-ND^2}$	$\left(\dfrac{3}{2}+\dfrac{4N-3ND}{2M}\right)V_o$
	[29]	$1/4/5/1^{2w}+1$	Yes	5	$\dfrac{N+D+2}{1-D}$	$\dfrac{V_o}{2+N+D}$	$\dfrac{4+2N}{2+N+D}V_o$
	[31]	$2/2/3/1^{2w}+0$	No	10	$\dfrac{N+1}{1-D}$	$\dfrac{2V_o}{1+N}$	$\dfrac{2N}{1+N}V_o$
	[33]	$2/2/4/1^{2w}+1$	Yes	6	$\dfrac{N}{1-D}$	$\dfrac{2V_o}{N}$	$2V_o$
	[34]	$4/0/3/1^{2w}+2$	No	5	$\dfrac{2N-1}{(N-1)(1-D)}$	$2V_o$	0
	[35]	$4/0/3/1^{2w}+0$	No	5	$\dfrac{N+1}{1-D}$	$\dfrac{2+3N-2ND}{1+N}V_o$	0
	[36]	$4/0/3/1^{2w}+0$	No	5	$\dfrac{N+2}{1-D}$	$2V_o$	0
	Pro1	$1/4/3/1^{2W}+1$	Yes	2	$\dfrac{1+N_2}{(1-D)^2}$	$\dfrac{V_o}{(1-D)^2 M_{Pro1}}$	$\dfrac{3+2N_2}{(1-D)^2 M_{Pro1}}V_o$
Topologies with Three-winding CI	[9]	$4/6/9/2^{3w}+2$	No	11	$\dfrac{2(N+1)}{1-D}$	$\dfrac{2V_o}{1+N}$	$\dfrac{3+4N}{1+N}V_o$
	[25]	$2/4/3/1^{3w}+2$	Yes	10	$\dfrac{N+2}{1-D}$	$\dfrac{2V_o}{2+N}$	$\dfrac{4+N}{2+N}V_o$
	[37]	$4/1/3/1^{3w}+0$	No	8	$\dfrac{2+N_1 D+N_2}{1+N_2-D(1+N_2)}$	$\left[2+\dfrac{1}{(1-D)M}\right]V_o$	---
	[38]	$3/0/2/1^{3w}+0$	No	7	$\dfrac{1+D(n+n_a)}{1-D}$	---	0
	[39]	$4/2/4/1^{3w}+0$	No	9	$\dfrac{1+N+D}{1-D}$	$\dfrac{4V_o}{1+N+D}$	$\dfrac{2N}{1+N+D}V_o$
	[40]	$1/3/3/1^{3w}+0$	No	4	$\dfrac{2+N_3 D+N_2}{1-D}$	$\dfrac{V_o}{2+N+ND}$	$\dfrac{3+3N}{2+N+ND}V_o$
	[41]	$2/3/4/1^{3w}+0$	No	9	$\dfrac{Dn_t+n_s+2}{1-D}$	$\dfrac{2V_o}{2+N+ND}$	$\dfrac{2+ND+2N}{2+N+ND}V_o$
	Pro3	$1/6/5/1^{3W}+1$	Yes	2	$\dfrac{1+N_2+N_3}{(1-D)^2}$	$\dfrac{V_o}{(1-D)^2 M_{Pro3}}$	$\dfrac{3+2N_2+2N_3}{(1-D)^2 M_{Pro3}}V_o$
	Pro4	$1/5/4/1^{3w}+1$	Yes	2	$\dfrac{1+N_2+N_3 D}{(1-D)^2}$	$\dfrac{V_o}{(1-D)^2 M_{Pro4}}$	$\dfrac{3+2N_2+N_3}{(1-D)^2 M_{Pro4}}V_o$
Topologies with Four-winding CI	[42]	$4/0/3/1^{4w}+0$	No	4	$\dfrac{2(1+nD)}{1-D}$	$\dfrac{(2+N)V_o}{1+ND}$	0
	[43]	$1/9/8/1^{4w}+0$	No	5	$\dfrac{(1+2n)(1+D)+2}{1-D}$	$\dfrac{2V_o}{(1+2N)(1+D)+2}$	$\dfrac{8+6N}{(1+2N)(1+D)+2}V_o$
	[44]	$1/2/3/1^{4w}+0$	No	4	$\dfrac{1+(1+2n)D}{1-D}$	$\dfrac{V_o}{1+(1+2n)D}$	$\dfrac{2+2N}{1+(1+2n)D}V_o$
	[45]	$2/6/6/1^{4w}+0$	No	6	$\dfrac{2N-1.5}{(N-1)(1-D)}$	$\dfrac{N-1}{2N-1.5}V_o$	$\dfrac{3N-2}{2N-1.5}V_o$
	Pro2	$1/6/4/1^{4W}+1$	Yes	2	$\dfrac{1+N_2}{(1-D)^2}+\dfrac{2N_3 D}{1-D}$	$\dfrac{V_o}{(1-D)^2 M_{Pro2}}$	$\dfrac{3+2N_2+2N_3+2DN_3}{(1-D)^2 M_{Pro2}}V_o$

* **Note:** In the CI count, a^{bw} indicates "a" coupled inductor coils with "b" windings.

current ripple (LICR) is considered as the second evaluation parameter. For this purpose, the converters with discontinuous input current, voltage fed input port and coupled input inductor are considered as the converters with higher input current ripple. On the other hand, the converters with a single-winding inductor or single-winding interleaved inductors in
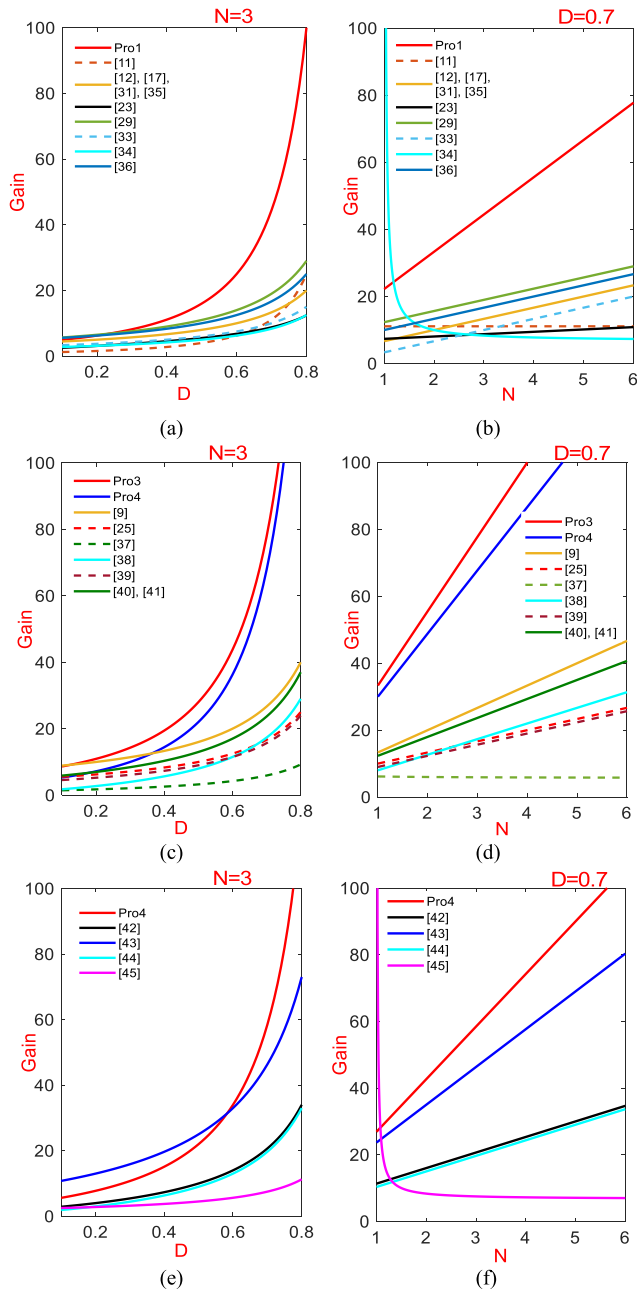
FIGURE 12. Comparison of converters' voltage gain with:
(a, b) a two-winding coupled inductor. (c, d) a three-winding coupled inductor. (e, f) a four-winding coupled inductor.

current ripple and NOM. In addition, voltage gain and normalized accumulative switch voltage stress of the converters are plotted in Fig. 12 and Fig. 13 with respect to the duty cycle and turns ratio. As can be seen, the proposed converters achieve the highest voltage gain and the lowest normalized accumulative switch voltage stress in both conditions.
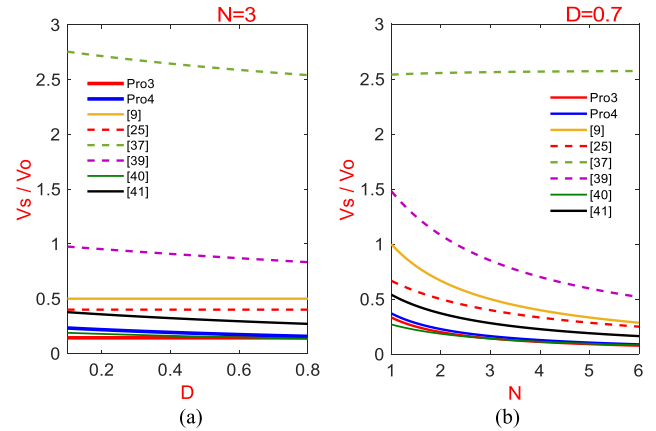

FIGURE 13. Normalized switch voltage stress comparison of converters' with a three-winding coupled inductor with respect to: (a) duty cycle. (b) coupled inductor turns ratio.
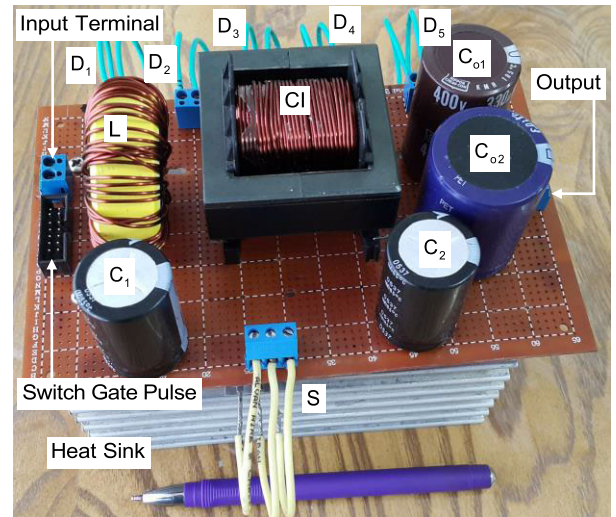

FIGURE 14. Experimental prototype of Pro4. (The switch and diodes are implemented under the board.)

the input port are considered as the LICR converters. According to Table 3, [17], [25], [29], [33] and the proposed converters operate with the lowest input current ripple. The number of operational modes (NOM) is the next parameter evaluated in Table 3, which affects on the converter control complexity and duty cycle range. The last columns of Table 3 are dedicated to the voltage gain ratio, accumulative switch(s) voltage stress, and accumulative diodes voltage stress, respectively. According to Table 3, the comparison of the above-mentioned parameters clarify the superiority of the proposed converters with less active and passive components, and low input

VII. EXPERIMENTAL RESULTS
In order to validate the performance and theoretical analytics of the proposed converters, the Pro4 topology is selected for experimental prototyping, where the experimental circuit and the obtained results are shown in Fig. 14 and Fig. 15, respectively. This circuit is designed for the nominal power of $P_o = 1.25 \ kW$ and the experimental results are obtained in the test point of $P_o = 1014 \ W$. The switching frequency is equal to $50 \ kHz$, and $N_2 = N_3 = 2$. The passive components are designed as $L = 122 \mu H$, $n_1 = 12$, $n_2 = n_3 = 24$, $C_1 = C_2 = 470 \ \mu F$, $C_{o1} = 330 \ \mu F$ and $C_{o2} = 150 \ \mu F$.
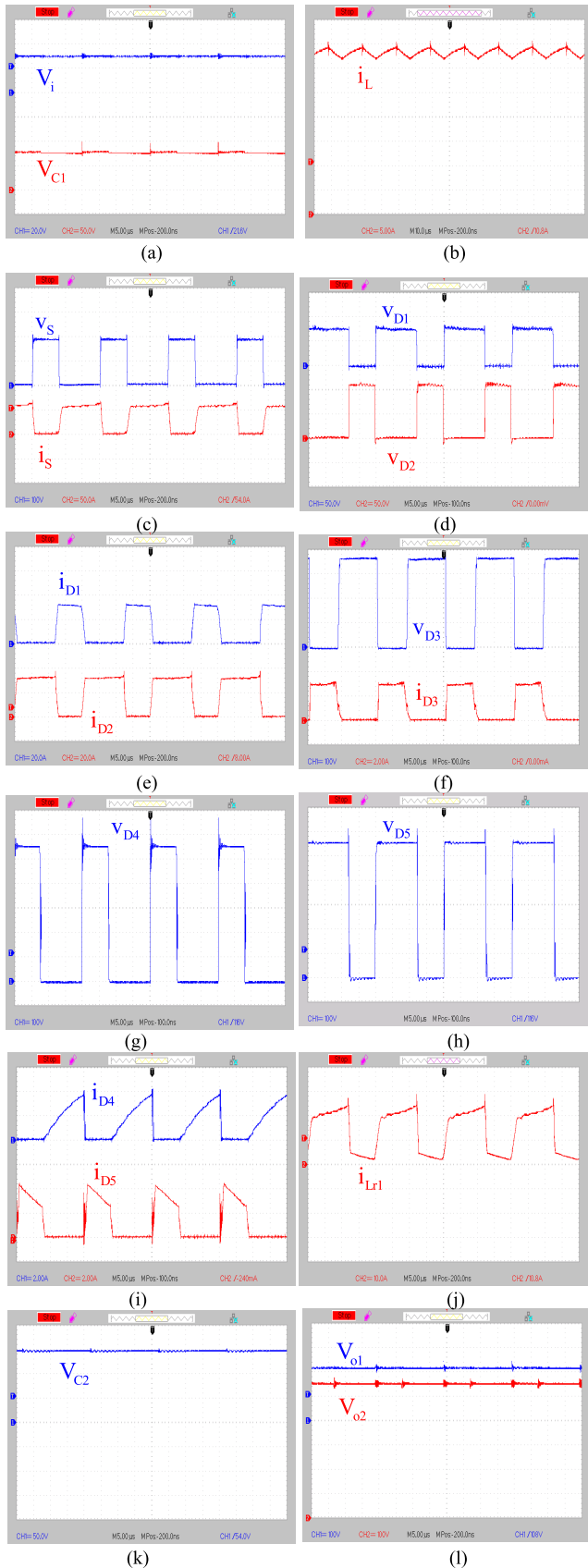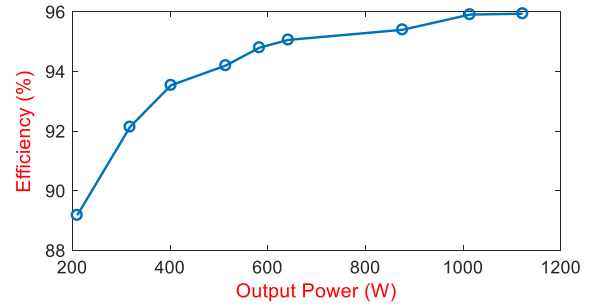
FIGURE 15. Experimental results.

FIGURE 16. Efficiency with respect to the output power.

Furthermore, the specifications of semiconductors are listed as follows: UJ4C075018K3S for S, VS-60EPU06-N3 for D_1 and D_2, MUR1560 for D_3 and DSEP30-12AR for D_4 and D_5.

Fig. 15(a) shows the input voltage and voltage across C_1 with $V_i = 30 \, V$ and $V_{C1} = 73.9 \, V$, which verifies (14). Input current ($I_i = I_L$) with the approximate 10% peak-peak ripple value is depicted in Fig. 15(b). In order to evaluate the switch performance, its drain-source voltage and current are illustrated in Fig. 15(c). As expected, its voltage stress is approximate $185 \, V$ that confirms (19). Voltage and current of diodes are shown in Figs. 15(d)-(i). As can be seen, the applied voltage stress across the diodes match with the results in (20)-(23). One of the significant features of this experiment is the absence of the high-voltage spikes during the switching transitions. Current profile of the leakage inductance is also demonstrated in Fig. 15(j). Using (15)-(17), V_{C2}, V_{o1}, and V_{o2} are calculated as $150 \, V$, $225 \, V$, and $562 \, V$, respectively. As shown in Fig. 15(k)-(l), the experimental voltage across $C1$, C_{o1}, and C_{o2} are measured as $145.5 \, V$, $220 \, V$, and $556 \, V$, respectively. Eventually, the efficiency of the Pro4 converter is measured in different output power values which is shown in Fig. 16. According to this figure, the maximum efficiency of this converter is equal to 95.94%.

VIII. CONCLUSION

A new family of high step-up DC-DC converters was proposed in this paper, which employs a center-tapped coupled inductor. Wide output voltage gain, low input current ripple, low normalized voltage stress across switching components, recycling all inductive and capacitive energies, no circulating current, simple control, low switching voltage spikes and operation of the coupled inductor with high power density are the main features of the proposed converters. Specifically, the main operational characteristic of these converters is employing different capacitive and inductive approaches to harvest the stored energies in capacitors and inductors such as leakage and magnetizing inductances, and transfer them toward output load. In this paper, comprehensive theoretical analytics, design considerations, comparison study and experimental results were provided to validate the performance and applicability of the proposed converters. The experimental results showed the approximate efficiency range of 89.18% to 95.94% from light to nominal test points.

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