IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received September 1, 2021, accepted September 21, 2021, date of publication September 29, 2021,
date of current version October 13, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3116160

A Low-Power Quadrature LO Generator With Mutual Power-Supply Rejection Technique

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This work was supported in part by Singapore Ministry of Education Academic Research Fund Tier 2 under Grant MOE2019-T2-1-114, and in part by China Scholarship Council.

ABSTRACT This paper presents a supply-insensitive low-power quadrature local oscillation (LO) generator based on the current-reused voltage-controlled oscillator (VCO) and divide-by-two frequency divider (FD). By utilizing the mutual power-supply rejection (M-PSR) technique, a voltage regulator is embedded into the FD to provide a supply-insensitive voltage for VCO. Meanwhile, the feedback loop provides a supply-insensitive current and time constant compensation for FD. The M-PSR technique does not require extra voltage headroom, thus the proposed quadrature LO generator can work under the supply of 0.9 V. A prototype of the proposed quadrature LO generator is implemented in a 28-nm CMOS process. Measurement results indicate that the LO generator achieves a phase noise of −110.5 dBc/Hz@1MHz at the carrier of 5.9 GHz and the power consumption is 1.8 mW. This work has a competitive figure of merit in supply sensitivity or in area (FOM_{ss} or FOM_a respectively) among the state-of-the-art works.

INDEX TERMS CMOS, current-mode-logic (CML), frequency divider (FD), low-power consumption, mutual power-supply rejection (M-PSR), supply sensitivity, quadrature local oscillation (LO) signal generator, voltage-controlled oscillator (VCO).

I. INTRODUCTION

Quadrature local oscillation (LO) signal generator is a power-hungry circuit, and its signal integrity and spectrum purity are critical in RF system. Challenges exist in the LO designs of being low-power and low-jitter to meet the reliability and power saving requirements in modern communication applications, for example, vehicle-to-everything (V2X) communication [1]. The power-supply induced noise degrades the circuits performance, especially when many circuits share the supply in the integrated systems. Thus, there is a strong demand to develop a reliable quadrature LO generator with low-power consumption and low supply sensitivity.

There are several methods to generate quadrature LO signals. The quadrature voltage-controlled oscillator (QVCO) can provide four phases directly with good driving capability [2] [3], but it has risks of phase inaccuracy and phase ambiguity. The poly-phase filter-based structure is a more reliable choice. However, the phase shift network in it introduces additional noise and causes power loss [4]. Quadrature LO signal can also be generated from a structure of a differential LC-VCO operating at double frequency followed by a divide-by-two current-mode-logic frequency divider (CML-FD) [5]. It avoids phase ambiguity and has better phase noise and power efficiency. The current-reused technique [6] can be adopted to further reduce the power consumption. However, the voltage headroom is limited which makes it hard to implement power supply rejection function with conventional methods.

Adding a fully integrated CMOS low-dropout regulator (LDO) is the most straightforward and popular method to reject power supply noise. However it adds noise from devices [7] and requires supply headroom of several hundred millivolts. Without occupying voltage headroom, the devices for generating tail current are reused to suppress supply noise with an amplified ripple replica in [8]. Nevertheless, it is only applicable in the structure with a tail current source. The compensation [9] and cancellation [10] techniques based on

The associate editor coordinating the review of this manuscript and approving it for publication was Teerachot Siriburanon.

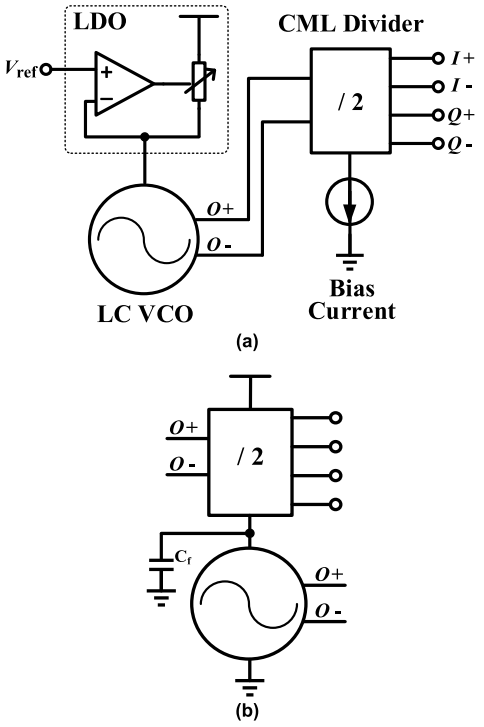

FIGURE 1. (a) The conventional quadrature LO generator and (b) the current-reused structure.

characteristics of devices can reject supply noise, which is applicable for circuits with or without the tail current source. However, the power supply rejection capability is achieved in open loop which requires tuning to optimize the accuracy.

In this paper, a mutual power-supply rejection (M-PSR) quadrature LO generator based on low-power current-reused structure without scarifying voltage headroom is proposed. The principle of the proposed M-PSR technique and the circuit implementation are discussed in section II. Section III shows the measurement results and comparisons. Finally, section IV presents the conclusion.

II. DESIGN AND ANALYSIS

A. PRINCIPLE OF THE MUTUAL POWER-SUPPLY REJECTION TECHNIQUE

Fig. 1(a) presents the conventional architecture of a quadrature LO generator based on an LC-VCO and a CML-FD. Since the LC-VCO suffers from AM-FM conversion [11], an LDO is usually adopted to suppress the AM noise from power supply at the expense of voltage headroom, area and power consumption. Moreover, for a CML-FD, the output frequency is locked by signals injected from VCO. The low frequency power supply noise is reflected in the quadrature outputs as fluctuations of the self-oscillation frequency which is related to the working current and time constant τ. A tail current source is usually adopted for better supply immunity, but the problem of τ decreasing still exists [12]. The above problems are more severe in the low-power current-reused architecture as shown in Fig. 1(b). The devices with small

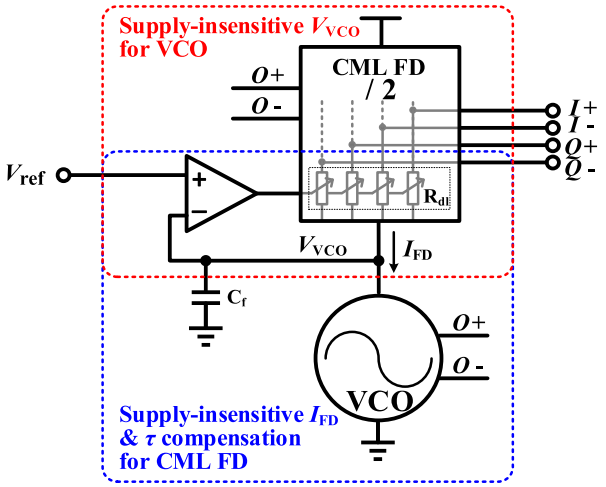

FIGURE 2. Diagram of the proposed quadrature LO generator with M-PSR technique.

voltage headroom would enter undesired working region due to supply ripple which degrades the linearity.

The proposed M-PSR technique is applied on the current-reused structure without demanding voltage headroom, as shown in Fig. 2. Instead of a fixed load, a variable load (R_{dl}) is adopted for CML-FD. A voltage regulator is implemented by reusing the variable load to suppress AM noise from V_{DD} for the VCO. At the same time, since the V_{VCO} has been stabilized, the bias current IFD also has the supply noise immunity. Moreover, the R_{dl} increases with supply voltage increases because of the feedback loop, which compensates the τ decreasing of CML-FD. The proposed M-PSR technique reuses devices to suppress supply noise for the stacked VCO and FD, thus achieves low-power consumption and supply insensitivity at the same time.

B. CIRCUIT DESIGN

The schematic of the proposed quadrature LO generator is shown in Fig. 3. The CML-FD is stacked with the LC VCO to reuse current. The distribution of voltage for each block is critical as the voltage headroom is limited. The supply voltage V_{VCO} for the LC-VCO is 450 mV. Only the NMOS transistors (MN5, MN6) are employed in the cross-coupled pair to compensate for the loss of LC-tank. Meanwhile, the bias voltage of the NMOS devices in LC-VCO has been set to around the threshold voltage to get high power efficiency [13], which makes it well-suited for low-power applications with limited voltage headroom. The output swing of the signals which are injected to CML-FD is around 800mV. The supply rails for the divide-by-two CML-FD are from V_{DD} (900 mV) to around 450 mV. It is consisted of CML master-slave flip-flops, which converts differential signals from the VCO into quadrature LO signals. Four PMOS devices (MP1-MP4) are switched by the differential outputs of the VCO directly. No level shifters or buffers are required as the common-mode voltage and swing can be matched properly. Therefore, no additional noise sources are

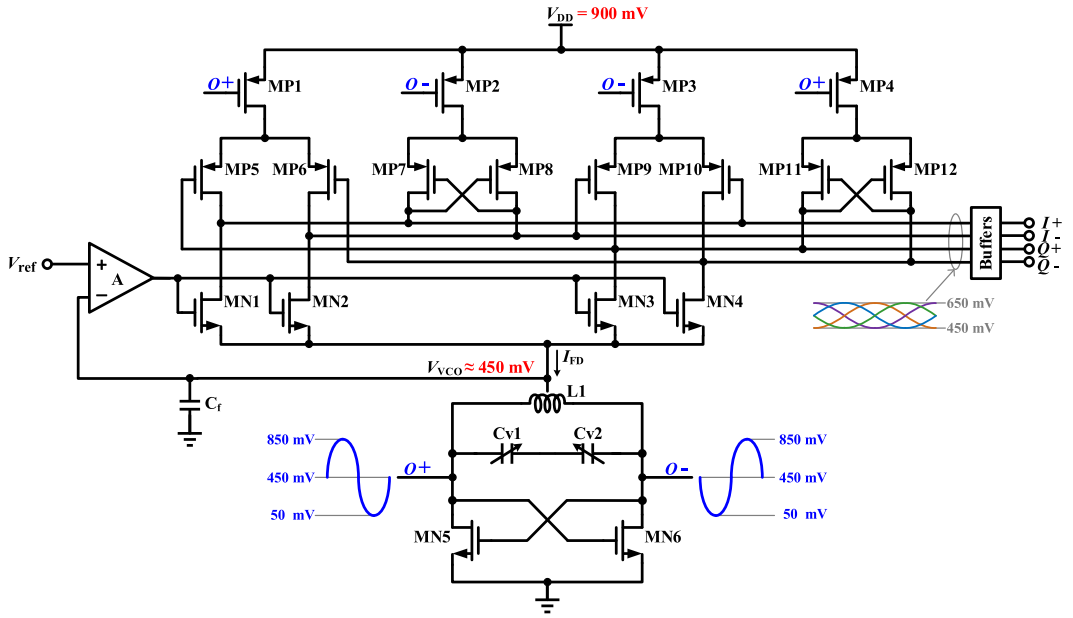

FIGURE 3. Schematic of the proposed M-PSR quadrature LO generator.

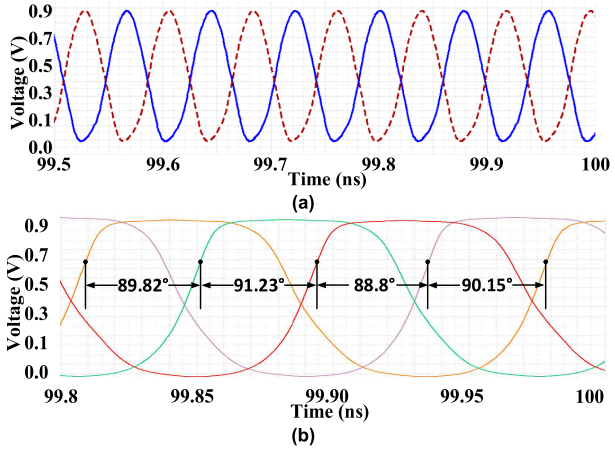

FIGURE 4. The post-layout simulations of (a) differential outputs and (b) quadrature outputs with phase differences.

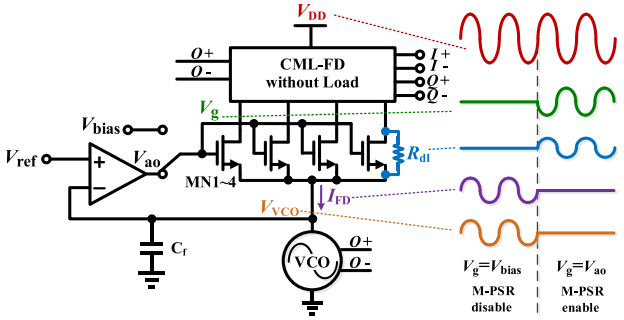

FIGURE 5. Block diagram showing the supply regulation principle graphically.

introduced. The simulated differential outputs of LC-VCO with the frequency around 12 GHz are shown in Fig. 4(a). The swing of CML-FD outputs is around 200 mV. Buffers are followed to enlarge the swing to around 800 mV. The post-layout simulation of quadrature outputs after buffers are shown in Fig. 4(b). The LO core consumes 1.4 mA, and the total current including buffers is 1.8 mA.

When V_{DD} increases, the variation of the V_{VCO} can be suppressed if the equivalent resistance of MN1 to MN4 increases. Conventional structure with a fixed bias voltage is not capable to provide such suppression as shown in Fig. 5. Instead, in the proposed structure, the voltage ripple is continuously sensed to adjust variable load resistance. This voltage sensing and load regulation is achieved by negative feedback to dynamically adjust the gate voltage of MN1 to MN4.

To verify the power supply rejection capability, the load condition can be simplified by considering the quadrature output signals as square waves each with 90° phase shifting. Four identical NMOS devices (MN1 to MN4) are adopted as the variable load of CML-FD. Hence there are always two transistors turned on and the other two turned off, and the equivalent resistance of MN1 to MN4 is a constant at stable state. The whole circuit can be simplified as shown in Fig. 6(a). The ratio of variation of V_{VCO} to V_{DD} is calculated as

$$\frac{\Delta V_{VCO}}{\Delta V_{DD}} = \frac{R_{vco}}{R_{dl} + (A+1)\, gm R_{dl} R_{vco} + R_{vco} + R'_{fd}} \quad (1)$$

where R_{dl}, R_{vco}, R'_{fd} are the equivalent resistances of variable load, LC-VCO and CML-FD (without load) respectively, gm is the equivalent transconductance of MN1 to MN4, and A is the gain of the amplifier.

An amplifier with loop gain of around 28 dB and phase margin of more than 70° was designed. The power consumption of the proposed M-PSR structure is 0.27 mW

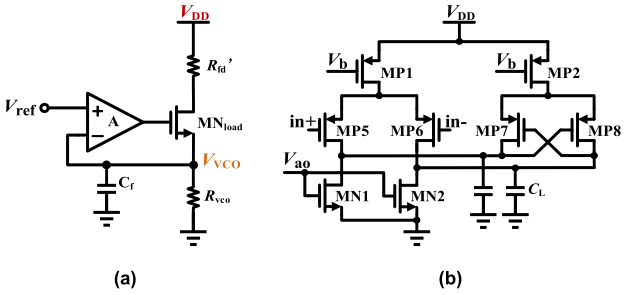

FIGURE 6. Diagram of (a) the simplified model of voltage regulator and (b) single CML cell.

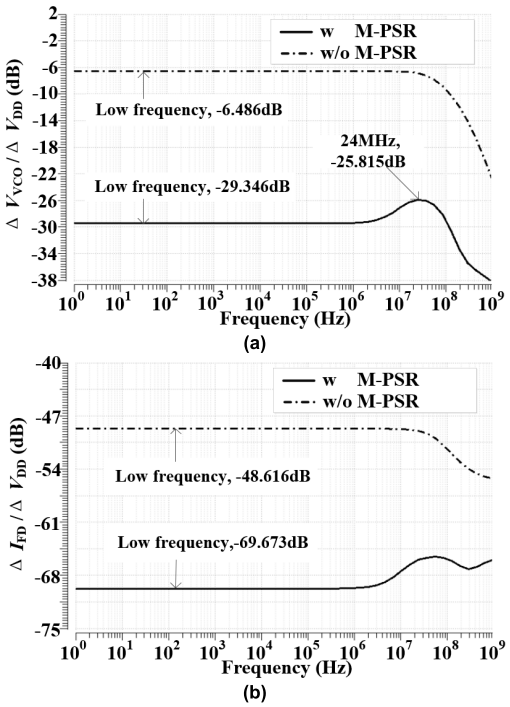

FIGURE 7. Simulated (a) V_{VCO} variations, (b) I_{FD} variations versus supply variations.

and the area is 0.004 mm^2. The simulated power supply rejection ratio of the V_{VCO} to V_{DD} is improved from −6.48dB to −29.34dB at low frequency range compared to structure with fixed biased load as shown in Fig. 7(a). Meanwhile, since V_{VCO} is well regulated and the VCO shares the current with CML-FD, the simulated variation of I_{FD} with V_{DD} is improved from −48.62dB to −69.67dB as shown in Fig. 7(b). Power supply noise suppression capability can be improved by increasing the amplifier gain and the transconductance of MN1 to MN4, but with the sacrifices of power consumption and area. Besides, if the equivalent resistance of MN1 to MN4 is too low, then the quadrature output swing may not be sufficient.

Apart from the voltage regulation function, the variable load also compensates the decreasing time constant of CML-FD. Conventional CML-FD has a positive supply voltage sensitivity as described in [12]. The CML cell used in the proposed work is shown in Fig. 6(b). The time constant

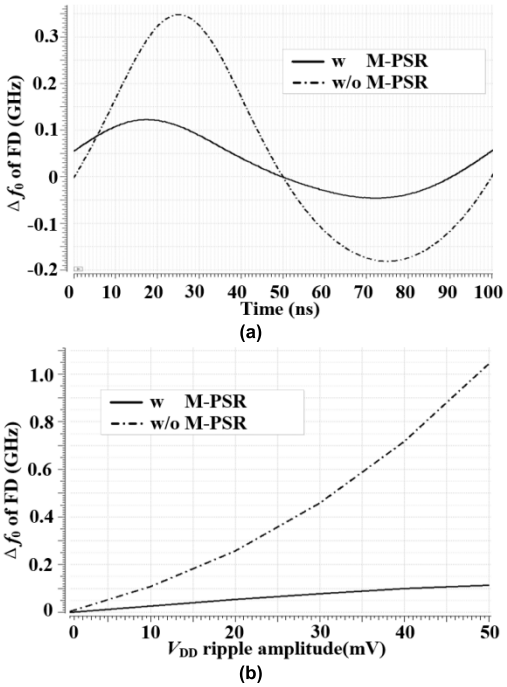

FIGURE 8. Simulated (a) self-oscillation frequency variations with 50 mVpp supply noise at 10 MHz and (b) self-oscillation frequency variations versus supply noise amplitude at 10 MHz.

τ of CML-FD is defined by

$$\tau = (C_{\text{par}} + C_{\text{L}})(R_{\text{dl}} // \frac{1}{g_{\text{ds}}}) \tag{2}$$

where C_{par} is the total parasitic capacitance of input transistors, C_{L} is the load capacitance, R_{dl} is the equivalent load resistance, and g_{ds} is the conductance of input transistors.

According to [12], The C_{db} decreases and g_{ds} increases with V_{DD} which means the frequency increases as V_{DD} increases. While in the proposed structure, the variable load resistor R_{dl} has a positive coefficient as supply voltage increasing,

$$\partial R_{\text{dl}}/\partial V_{\text{DD}} > 0 \tag{3}$$

which compensates the time constant τ. The locking range of CML-FD also varies with V_{DD} because of the variable load. However, due to the large input swing from the VCO, the locking range of CML-FD structure can cover input frequency range from 4 GHz to 15 GHz. Simulation results verify that the time constant of CML-FD is compensated with proposed M-PSR technique, which is reflected as the variation of the self-oscillation frequency as shown in Fig. 8 (a) and (b).

III. MEASUREMENT RESULTS

The proposed M-PSR quadrature LO generator was designed in a charge-pump PLL with 28nm CMOS process. The die photograph of the chip is shown in Fig. 9. The whole chip area is 0.7 × 0.7 mm^2, in which the proposed quadrature LO generator occupies 0.072 mm^2.

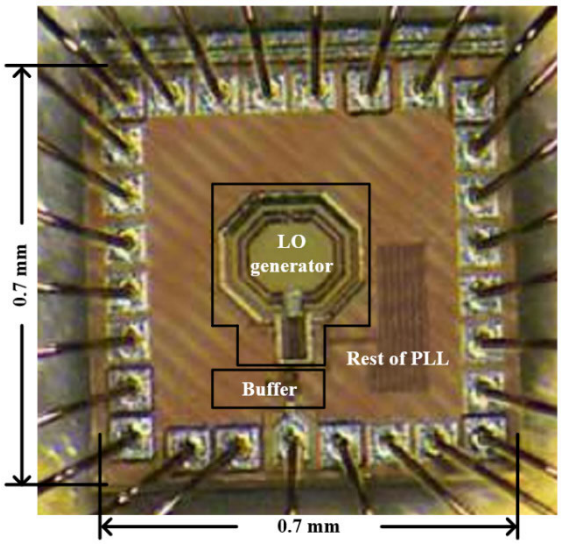

FIGURE 9. Die photograph.

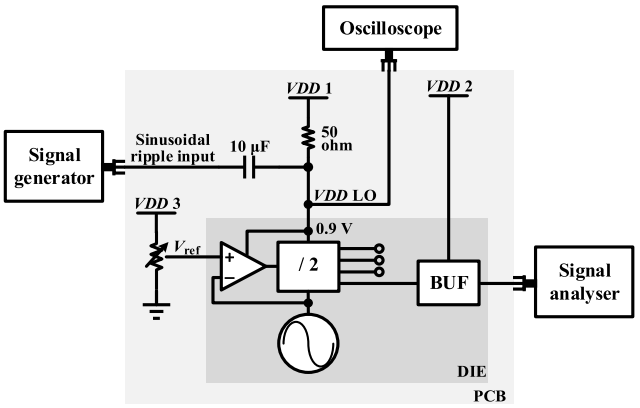

FIGURE 10. Diagram of measurement setup.

The measurement setup is shown in Fig. 10. The remained parts of PLL were turned off, and the proposed LO generator was measured individually. The supply voltage of the proposed quadrature LO generator is 0.9 V. The measured current consumption is less than 2 mA, which corresponds to a power consumption of around 1.8 mW. The tuning range of the proposed LO generator is from 5.7 GHz to 6.1 GHz. Fig. 11 shows the measured phase noise is −110.52 dBc/Hz@1MHz at 5.9 GHz. The bumps in between 10 kHz to 1 MHz offset region are noise caused by open loop testing where the remaining part of PLL especially the charge pump and multi-mode divider may not be completely turned off. It can be filtered if measured in closed loop.

It has a figure of merit (FOM) [14] of −184.4 dB calculated by

$$\text{FOM} = L(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P_{\text{dc}}}{1\text{mW}}\right) \quad (4)$$

where $\Delta\omega$ is the offset frequency from the oscillation frequency ω_0 and P_{dc} is the power consumption.

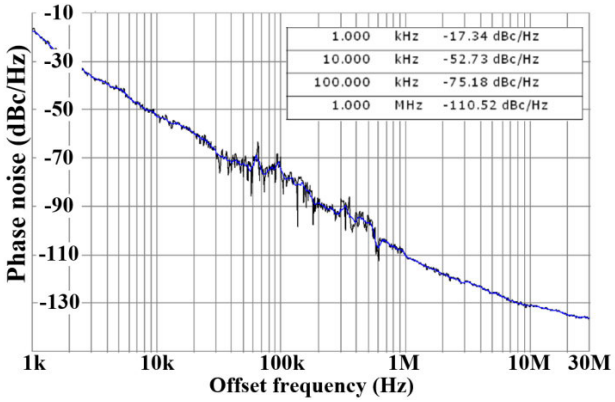

FIGURE 11. Measured phase noise of VCO at 5.9 GHz.

To evaluate the power-supply rejection performance, the supply voltage of the LO generator was provided separately. As shown in Fig. 10, through an RC network, the sinusoid ripple was ac-coupled onto the chip supply voltage. The oscilloscope was to monitor that the actual power supply applied to LO generator is 0.9 V DC with the generated ripple.

By measuring the power levels of outputs at center frequency and supply-noise induced side tones through the signal analyzer, the supply sensitivity was evaluated [9]. Fig. 12(a) shows that with 50 mVpp supply noise at 10 MHz superimposed on the power supply, the power ratio at center frequency of 5.9 GHz (P0) to that at offset frequency (P1) is 40.05 dB with the proposed M-PSR structure. If the amplitude of supply noise at 10 MHz increases to 100 mVpp, the power ratio is 33.85 dB as shown in Fig. 12(b).

The mutual rejection function was disabled by increasing the reference voltage to make the amplifier output saturated. Hence the feedback circuitry worked as a fixed voltage bias, the LO generator structure is then considered as a conventional current-reused structure. Fig. 12(c) shows the power ratio is 20.67 dB with M-PSR disabled with 50 mVpp supply noise. With 100 mVpp supply noise, the power ratio is decreased to 15.62 dB with M-PSR technique disabled, as shown is Fig. 12(d). The periodic jitter introduced by supply noise in UI can be deduced based on P0/P1 [12] as

$$\hat{J}_{p-p} = \frac{2}{\pi\sqrt{\frac{P_0}{P_1}}} \quad (5)$$

The single-tone supply noise also causes the real-time sinusoidal frequency variations. This type of frequency variation is defined as

$$\Delta f = 2\pi \cdot f_{\text{noise}} \cdot \hat{J}_{\text{p-p}} = \frac{4f_{\text{noise}}}{\sqrt{\frac{P_0}{P_1}}} \quad (6)$$

where f_{noise} is the supply ripple frequency. Fig. 13(a) shows the periodic jitter when the ripple frequency is tuned from 1 MHz to 10 MHz. Normalized peak-to-peak jitter is inversely proportional to noise frequency as the accumulation

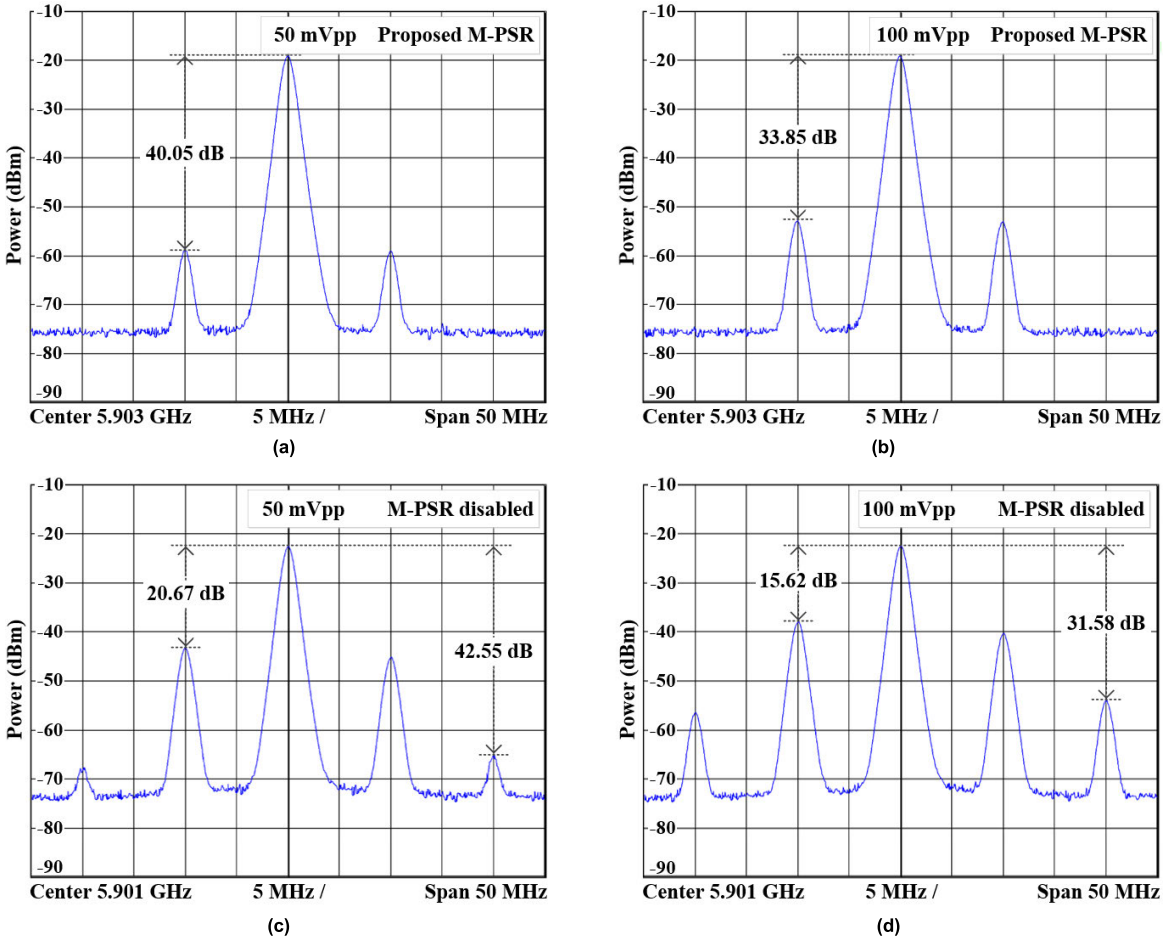

FIGURE 12. Measured output spectra of the proposed M-PSR LO generator with the supply ripple of (a) 50 mVpp and (b) 100 mVpp respectively. Measured output spectra of the M-PSR disabled LO generator with the supply ripple of (c) 50 mVpp and (d) 100 mVpp respectively.

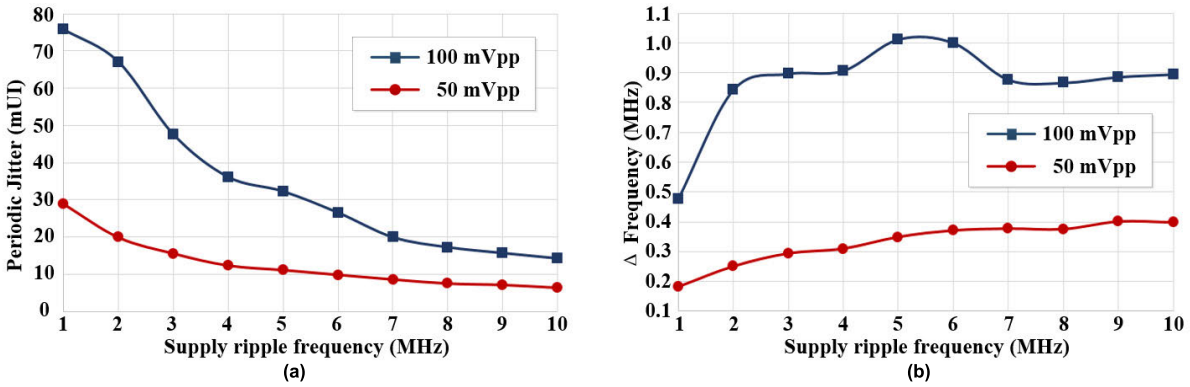

FIGURE 13. Measurement results of (a) jitter and (b) frequency variation versus supply noise frequency.

time of jitter is the period of supply noise. Fig. 13(b) presents the frequency variation calculated by equation (6) with different supply ripple frequencies and amplitudes. The nonlinearity parts of the circuit such as varactors affects the frequency heavily with larger amplitude of supply ripple.

The overall performance of the proposed M-PSR LO generator is compared with state-of-the-art supply-insensitive designs as shown in Table 1. Supply sensitivity can be further deduced based on P0/P1 and intuitively reflected as the normalized supply noise induced jitter and frequency variation which are defined as

$$supply\ sensitivity\left(\frac{\text{mUI}}{\text{mV}}\right)=\frac{\hat{J}_{\text{p-p}}}{V_{\text{p-p\_ripple}}} \tag{7}$$

TABLE 1. Performance summary and comparison to state-of-the-art works.

	[8]	[9]	[10]	[16]	This work	
Process	40nm	180nm	65nm	65nm	**28nm**	
Structure type	LC	LC	Ring	Ring	**LC+CML**	
Number of output phases	2	2	4	10	**4**	
Supply voltage (V)	1	1.8	0.85	1	**0.9**	
Power consumption (mW)	0.8	0.9	2.25	1.55	**1.8**	
Area (mm^2)	0.23	N.A.	0.0189	0.093	**0.072**	
Frequency (GHz)	4.9-5.7	4.3-4.8	0.9-1.4	3.2	**5.8-6.3**	
Phase noise (dBc/Hz)	-110.9 @1MHz	-111.51 @1MHz	-96.5 @1MHz	-104.3 @10MHz	**-110.5 @1MHz**	
Supply ripple frequency (MHz)	10	10	10	1	**10**	
Supply ripple amplitude (mVpp)	50	50	50	25	**50**	**100**
Supply Sensitivity (mUI/mV)	0.0127	0.544	0.476	0.299	**0.127**	**0.129**
Supply Sensitivity ($\%f/\%V_{DD}$)	0.00014	0.0136	0.0204	0.000587	**0.00121**	**0.00124**
FOM (dB)	-186.9	-186.2	-154.9	-152.4	**-183.4**	
FOM_{ss} (dB)	-262.9	-223.2	-188.7	-217.1	**-241.7**	**-241.5**
FOM_a (dB)	-193.3	N.A.	-172.1	-162.7	**-194.8**	

$$supply\ sensitivity\left(\frac{\%f}{\%V_{\mathrm{DD}}}\right)=\frac{\Delta f/f_{\mathrm{osc}}}{V_{\mathrm{p-p\_ripple}}/V_{\mathrm{DD}}} \tag{8}$$

$\mathrm{FOM_{ss}}$ [9] and $\mathrm{FOM_a}$ [15] are defined as:

$$FOM_{ss}=\mathrm{FOM}+20\log(supply\ sensitivity\left(\frac{\%f}{\%V_{\mathrm{DD}}}\right)) \tag{9}$$

$$FOM_a=\mathrm{FOM}+10\log\left(\frac{\mathrm{Area}}{1\mathrm{mm}^2}\right) \tag{10}$$

It takes into consideration of the FOM for normalized supply sensitivity and for area respectively together with the standard FOM for phase noise, working frequency and power consumption [9]. The proposed LO generator achieves a competitive $\mathrm{FOM_{ss}}$ and $\mathrm{FOM_a}$ among state-of-the-art works.

IV. CONCLUSION

In this paper, a low-power and supply-insensitive quadrature LO generator is implemented and measured in 28nm CMOS process. Simulation and measurement results show that the proposed architecture can effectively enhance the supply noise immunity compared to the conventional current reuse architecture. It exhibits a good noise performance, and the overall merits are favorably comparable to state-of-the-art supply-insensitive works.

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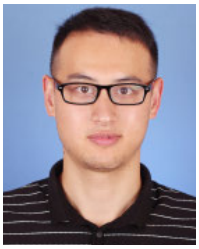

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