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Modeling and Experimental Evaluation of Z-Source Modular Multilevel Converter Using Reduced Inserted Cells Technique

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ABSTRACT The integration of a Z-source network with a modular multilevel converter (MMC) to provide voltage step-up function is proposed in this paper. The proposed Z-source modular multilevel converter (ZS-MMC) uses a Z-source network connected between the DC source and the DC-link terminals of the MMC. The operation principle of the ZS-MMC is presented utilising the reduced inserted cells (RICs) modulation technique. Compared to the quasi ZS-MMC previously developed by the authors, the ZS-MMC has small fundamental frequency component in the ZS inductor current which requires a smaller inductor size for the Z-source network and is also more efficient. The ZS-MMC is compared to other topologies that can accomplish buck and boost capabilities, such as the quasi Z-source MMC, the quasi Z-source cascaded multilevel converter and the full-bridge based MMC, to validate the viability of the proposed converter. The operation of the ZS-MMC employing the RICs technique is confirmed experimentally.

INDEX TERMS Modular multilevel converter, modulation technique, reduced inserted cells, voltage step-up, Z-source network.

I. INTRODUCTION

Renewable energy sources are gaining a lot of attention around the world as a way to minimise CO₂ emissions [1]. The wind energy system (WES) is one of the most rapidly expanding renewable energy sources [2]. Among various generator types used with WES, the permanent magnet synchronous generator (PMSG) has gained significant interest due to the absence of the gearbox, leading to lower system failure, greater efficiency, and higher system dependability [3]. Diagram of the WES using direct drive PMSG is shown in Fig. 1. A power converter is necessary to connect the WES to the electric grid because the generator output voltage and frequency vary with the wind speed. Back-to-back (BTB) converter is one of the available power converter solutions, which consists of a controlled rectifier that creates a regulated DC voltage at the DC-link terminals and a PWM inverter that generates an AC voltage synchronised to the grid. The typical BTB converter configurations are the two-level voltage source converter (2L-VSC) [4], the neutral point

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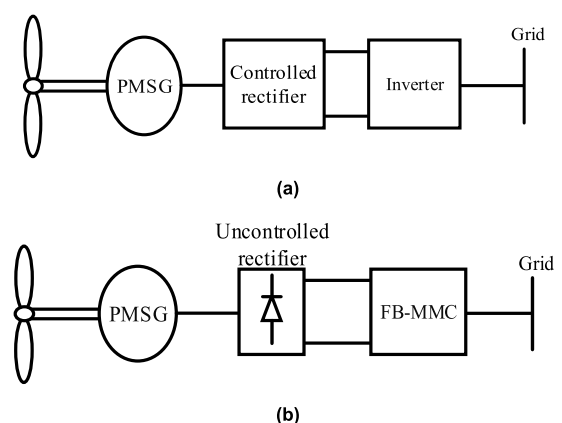


FIGURE 1. Diagram of wind energy system with PMSG using a) BTB converter, and b) FB-MMC.

clamped (NPC) [4] converter, and the modular multilevel converter (MMC) [5]. Because MMC has features of multilevel converters such as reduced harmonic distortion and improved handling of medium and high voltage/power [6] as well as its unique features of modularity, voltage/power scalability, and redundancy, BTB converters utilising MMC

are the most promising [5], [7]–[11]. However, using two forced commutated converters of BTB converter leads to a high cost and low efficiency [12].

Various configurations of the MMC have been investigated. Half bridge inverter sub-modules (HBSMs) [13] and full bridge inverter sub-modules (FBSMs) [12] are extensively used in MMC construction. Each design has weaknesses and strengths. For instance, the HBSM employs half as many switches as the FBSM, resulting in lower power loss and lower cost [14]. The FBSM, on the other hand, can provide higher levels of output voltage (voltage boost function) than the HBSM [15] and can handle DC-faults whereas the HBSM cannot [14].

The usage of a FBSMs based MMC (FB-MMC) to interface the WES to the electric grid was suggested in [12] which is rated at 6.6 kV, 5 MW. This integration was achieved by connecting the AC output terminals of PMSG to the FB-MMC’s input terminals with a simple three-phase uncontrolled diode rectifier, as shown in Fig. 1b. This circuit has a benefit over the BTB arrangement in that it replaces the controlled rectifier stage (which might be a 2L-VSC, NPC, or MMC) with a three-phase diode rectifier, resulting in cheaper cost, higher reliability, and improved efficiency [12].

A boost converter stage or an impedance-source converter can be used instead of the FB-MMC depicted in Fig. 1. A topology of quasi Z-source MMC (qZS-MMC) that can provide voltage buck and boost functions and also enables DC-fault blocking has been proposed in [16], [17]. The operating principles together with two deriving PWM modulation techniques known as simultaneously shorted (SS) and reduced inserted cells (RICs) are presented. The concept was expanded in [18] by providing in-depth analysis to the previously mentioned modulation techniques, and design guidelines for different components that were experimentally validated. The qZS-MMC uses HBSMs which reduces the number of switches compared to the FB-MMC. Using the RICs technique with the qZS-MMC resulted in lower stress voltage on the qZS-network switches than using the SS technique [18]. The RICs, on the other hand, creates a large fundamental frequency component in the qZS inductor current, resulting in a larger inductor size [18]. This is due to implementing the concept of partial shoot-through during half of the fundamental frequency cycle.

To overcome the need for large inductors, the integration of the single Z-source (ZS) network with the MMC started in [19] where the basic operating principles were presented. In which, applying the concept of partial shoot-through to the ZS-MMC allows for a lower fundamental component in the inductor current and thus a smaller inductor size. In this paper, the operation of the proposed ZS-MMC is confirmed experimentally. Furthermore, the study has been extended to include the proper control for suppression of the AC components in the circulating current. Also, the viability of the ZS-MMC has been compared with other existing topologies to highlight the features and weaknesses of the proposed one.

This paper is organized as follows. The operation principle of the ZS-MMC is firstly presented. Then, the reduced inserted cells (RICs) modulation technique, used to derive the proposed converter, is explained in detail. Following that, the control objectives used to provide a proper operation are illustrated. Also, the design guideline of the ZS inductors is presented by studying the signature of the inductor current and voltage waveforms. To illustrate the weaknesses and strengths of the proposed converter (ZS-MMC), it has been compared with the other three power converters, that are able to provide voltage buck and boost functions, is carried out. The performance of the proposed converter is validated using the experimental prototype. Finally, the work done in this paper has been concluded.

II. PROPOSED Z-SOURCE MODULAR MULTILEVEL CONVERTER (ZS-MMC)

A. CIRCUIT CONFIGURATION

Fig. 2 shows the proposed single-phase Z-source modular multilevel converters (ZS-MMC) topology, where a single Z-source impedance network is employed. The operation of the ZS-network relies on producing shoot-through (ST) at its output terminals [20]. This will increase the energy stored in its storage components (inductors and capacitors) thus boosting the DC-link voltage seen by the MMC half bridge stage. The DC source needs to have a midpoint to allow the connection of the AC load as well as for the asymmetric shoot-through to be performed. This can be achieved also by using only one DC supply with two capacitors in series connection. The MMC leg contains an upper and lower arm, each has N_{SM} half-bridge sub-modules (SMs) in a series connection with an arm inductor (L_o) to limit the circulating and fault currents. Each SM has a floating capacitor C_{SM} (with a voltage of V_{CSM}) and two switches (S_1 , and S_2) as depicted in Fig. 2. The two switches (S_1 , and S_2) are complementary controlled, where its terminals have a voltage of V_{CSM} or zero.

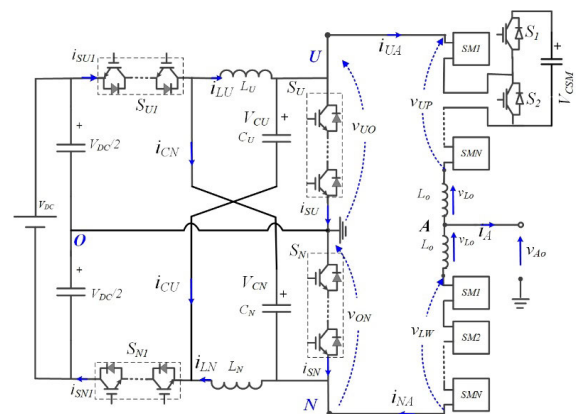


FIGURE 2. Structure of a Z-source modular multilevel converter.

B. MMC OPERATION PRINCIPLES

The AC output voltage v_{Ao} is given by (1), where v_{UO} and v_{ON} are the upper and lower DC-link voltages respectively, v_{UP}

and v_{LW} are the upper and the lower arm voltages respectively.

$$v_{AO}(t) = \frac{v_{LW}(t) - v_{UP}(t)}{2} + \frac{v_{UO}(t) - v_{ON}(t)}{2} - \frac{L_O}{2} \cdot \frac{di_{AO}}{dt} - \frac{r_O}{2} \cdot i_{AO} \quad (1)$$

It can be seen that the output AC voltage can be influenced by the difference between the upper and lower DC-link voltages, the difference between the upper and lower arm voltages and also by the output current i_{AO} that causes a voltage drop on the arm inductance. The voltage drop across the arm inductance will cause a slight variation in the output voltage levels where this part can be completely ignored or removed by using coupled arm inductor configuration [21]. Since L_O and r_O are small, the effect of i_{Ao} on the output voltage can be ignored. Therefore, the AC output voltage v_{Ao} is expressed by:

$$v_{AO}(t) = \frac{v_{LW}(t) - v_{UP}(t)}{2} + \frac{v_{UO}(t) - v_{ON}(t)}{2} \quad (2)$$

According to the current direction shown in Fig. 2, the arm currents i_{UA} and i_{NA} can be expressed by:

$$\begin{aligned} i_{UA}(t) &= i_{AO}(t)/2 + i_{cir}(t) \\ i_{NA}(t) &= -i_{AO}(t)/2 + i_{cir}(t) \end{aligned} \quad (3)$$

where

$$\begin{aligned} i_{cir}(t) &= i_{2f}(t) + I_{UN} \\ i_{2f}(t) &= (i_{UA}(t) + i_{NA}(t))/2 - I_{UN} \end{aligned} \quad (4)$$

The arm currents i_{UA} and i_{NA} are composed of the load i_{Ao} and the circulating current component i_{cir} . The circulating current i_{cir} flows through the upper and lower arms without affecting the load current. This current has a DC component I_{UN} and even low order harmonics, with the 2nd harmonic i_{2f} component being the dominant, causing more current stress and loss, which needs to be well suppressed. i_{cir} and i_{2f} can be calculated by (4).

A voltage balancing strategy is required to balance the SM capacitor voltages in each arm. There are different strategies for ensuring capacitor voltage balancing [7], where the sorting method [13], which is considered the most wide strategy, is applied in this paper.

C. Z-SOURCE NETWORK OPERATION PRINCIPLES

ZS-network requires shoot-through (ST) at its output terminals to increase the energy stored in the ZS-inductors, which is later transferred to the ZS-capacitors during non-shoot-through (NST) state and consequently, the voltage boosting capability can be attained.

To provide an ST current path, a switch S_U is connected between U and O terminals, while S_N is connected between O and N terminals, as shown in Fig. 2. This is necessary because it is difficult to make ST with both the upper and lower arms by allowing all of the SMs to generate zero voltage. This would cause a significant temporary loss of voltage and hence distorting the output voltage. Moreover, the feature of having

a multilevel functionality will be affected. The number of switches needed in each chain-link will be explained later.

The ZS-network requires series diodes and/or active switches which are essential for providing the voltage step-up capability and cannot be removed. As demonstrated in [22], an active semiconductor device should be antiparallel connected to the diodes, otherwise, undesired operation modes will appear. The two switches S_{U1} and S_{N1} should be gated in complementary with gating signals of S_N and S_U respectively.

The ZS-network can be working with partial ST by gating on only upper or lower chain-link switches separately and can be fully shorted by gating on both. The different operation modes are presented as follows.

1) UPPER ST OR/AND LOWER ST MODE

In case of the upper switch S_U is turned on, the S_{N1} should be turned off. Also, if the lower switch S_N is turned on, the S_{U1} should be turned off. The upper ST (UST) and lower ST (LST) equivalent circuits are illustrated respectively in Fig. 3a and Fig. 3b, and Fig. 3c shows the equivalent circuit in case of full ST (FST) mode. In these modes, the energy of the two Z-source inductors increases, and therefore ZS inductor currents increase, while the capacitors discharge causing the capacitor voltage to decrease. The inductor voltages are given by (5) for UST or LST modes and given by (6) for FST mode:

$$v_{LU} = v_{LN} = V_{DC}/2 \quad (5)$$

$$v_{LU} = v_{LN} = V_C \quad (6)$$

Considering the ZS-capacitor voltages are V_{CU} and V_{CN} and both equal to V_C and DC source voltage is V_{DC} , the DC-link voltages v_{UO} and v_{ON} for UST, LST and FST modes are given by (7), (8), and (9) respectively.

$$v_{UO} = 0 \quad v_{ON} = -V_{DC}/2 + V_C \quad (7)$$

$$v_{UO} = -V_{DC}/2 + V_C \quad v_{ON} = 0 \quad (8)$$

$$v_{UO} = 0 \quad v_{ON} = 0 \quad (9)$$

2) NON-SHOOT-THROUGH MODE (NST)

In NST mode, the switches (S_U , or S_N) are turned off and as a result, the series switches (S_{U1} , or S_{N1}) are turned on. The equivalent circuit is shown in Fig. 3d. The two ZS inductors start to de-energize where the inductor currents decrease. From Fig. 3d, the inductor voltages and the DC-link voltages during this mode can be given by:

$$\begin{aligned} v_{L1} &= v_{L2} = V_{DC} - V_C \\ v_{UO} &= v_{ON} = V_{UN}/2 = -V_{DC}/2 + V_C \end{aligned} \quad (10)$$

where V_{UN} is the peak value of the DC-link voltage. In this mode, the ZS-capacitors are charging or discharging according to the direction of ZS capacitor currents and can be defined by (11).

$$\begin{aligned} i_{CU}(t) &= i_{LU}(t) - i_{UA}(t) \\ i_{CN}(t) &= i_{LN}(t) - i_{NA}(t) \end{aligned} \quad (11)$$

If the upper/lower arm current i_{UA}/i_{NA} is higher than upper/lower inductor current i_{LU}/i_{LN} , the capacitor C_U/C_N charges and the capacitor voltage V_{CU}/V_{CN} increases, if not the capacitor voltage decreases.

With reference to the switching cycle T , the NST duration T_{nst} , the UST T_u and LST T_n durations, can be calculated:

$$\begin{aligned} T_{nst} + T_u + T_n &= T \quad T_u = T_n = T_{sh}/2 \\ D_{sh} &= T_{sh}/2T \end{aligned} \quad (12)$$

where D_{sh} is the average value of the ST duty ratio. Considering that over one switching period, the average value of the inductor voltage is equal to zero and using (5), (10), and (12), the ZS-capacitor voltages have an average value of:

$$V_C = V_{DC} \times (1 - D_{sh}) / (1 - 2D_{sh}) \quad (13)$$

Substituting from (13) into (10), the peak value of the DC-link voltages V_{UO} and V_{ON} are given by:

$$V_{UO} = V_{ON} = V_{UN}/2 = \frac{1}{1 - 2D_{sh}} V_{DC}/2 \quad (14)$$

Gating on one of the DC-link devices S_U or S_N will cause a change in the number of the levels of the output voltage, which should be compensated using a proper modulation method. This is further explained in the next section.

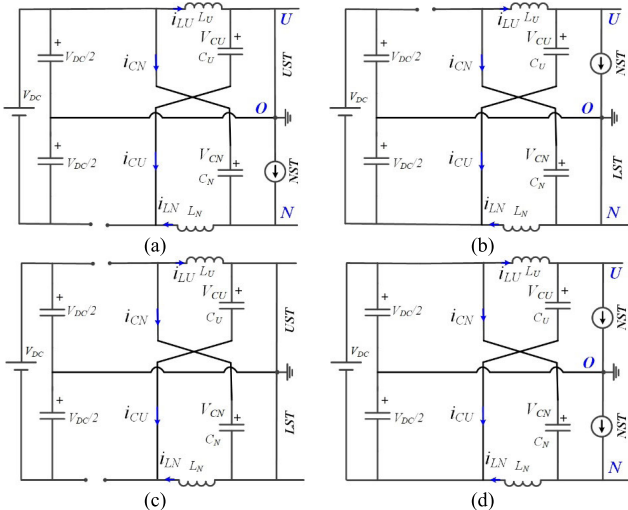


FIGURE 3. Operation modes of ZS-network: a) UST, b) LST, c) FST, and d) NST modes.

III. MODULATION TECHNIQUE AND CONTROL OBJECTIVES

A. REDUCED INSERTED CELLS TECHNIQUE

In this work, the level-shift SPWM with two opposite modulating signals, one for the upper arm and one for the lower arm, is used as illustrated in Fig.4. For N_{SM} sub-modules per arm, N_{SM} level-shifted carriers are required. As a result, a $(N_{SM} + 1)$ and $(2 N_{SM} + 1)$ level waveform is produced on the arm voltage and the AC output voltage.

According to (1), the instant output voltage depends on the arm voltages and the DC-link voltages. In MMC, the second term in (1) equals zero for normal operation conditions

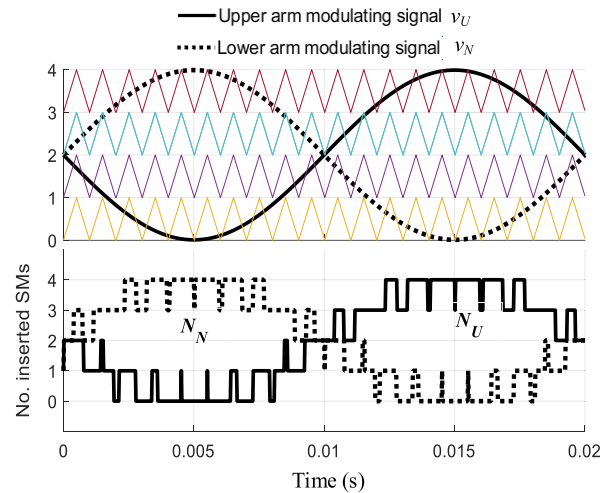


FIGURE 4. PWM modulation technique at $N_{SM} = 4$ (a) The upper and lower modulating signals with level-shifted triangles, and (b) The number of inserted cells for the upper and lower arms.

because $v_{UO} = v_{ON} = V_{DC}/2$. For the proposed ZS-MMC, the FST mode can be applied by turning on both S_U and S_N , and consequently the second term in (1) is still equal to zero. The FST mechanism was applied previously in [17] and referred to as the “simultaneously shorted (SS)” technique which is investigated in detail in [18] for a quasi Z-source MMC (qZS-MMC) topology. This technique considers simple but has high voltage stress on qZS passive and active components and high switching loss. This is because the fundamental output voltage is limited to the average value of the half DC-link voltage. The same drawbacks will be found also when applying FST with the ZS-MMC, therefore this technique is not used in this paper.

On the other hand, if only one of the DC-link switches (upper or lower) is gated on, the second term in (1) will become significant (equal to $V_{UN}/2$). Consequently, the output voltage waveform will be disturbed, and the voltage magnitude during this case will change by $V_{UN}/2$. This reflects on the corresponding level number to change by step of $\pm N_{SM}/2$. Therefore, the arm voltages should be modified to compensate for the shooting-through of the upper or lower DC-link. In which, the upper/lower arm voltage v_{UP}/v_{LW} should be changed by an amount of $V_{UN}/2$ to maintain the output voltage at its magnitude and level number.

For more clarification, if the upper shoot-through (UST) is introduced to the ZS-network, $N_{SM}/2$ SMs that are initially inserted (SM output voltage = V_{CSM}) in the upper arm should be selected to be bypassed (SM output voltage = zero) causing the upper arm voltage v_{UP} to decrease by $V_{UN}/2$. The lower shoot-through (LST) will be similar. Therefore, to introduce the upper or lower ST signals, the upper or/and lower arm should have at least $N_{SM}/2$ inserted SMs.

This technique is named “Reduced Inserted Cells” (RICs). As shown in Fig. 5, during the second half-cycle of the upper arm modulating signal (i.e., the negative half cycle of the output voltage), the number of upper inserted SMs N_U is greater than or equal to $N_{SM}/2$. While during the first half-cycle of

the lower arm modulating signal (i.e., the positive half cycle of the output voltage), the number of lower inserted cells N_N is greater than or equal to $N_{SM}/2$. Hence, the UST can be introduced during the negative half cycle of the output voltage, and the LST can be introduced during the positive half cycle of the output voltage.

Considering that the ST carrier has a unity height as shown in Fig. 5a, the ST reference signals for the upper and the lower arms (v_{sh-U} and v_{sh-N}) are expressed by:

$$v_{sh-U} = \begin{cases} 0 \\ 2D_{sh} \end{cases} \quad \& \quad v_{sh-N} = \begin{cases} 2D_{sh} \rightarrow 0 : \pi \\ 0 \rightarrow \pi : 2\pi \end{cases} \quad (15)$$

To avoid any disturbance in the output voltage, the reference signal for the upper/lower DC-link switches is set to zero in the first/second half cycle, as illustrated in (15). In addition, to get the average ST duty ratio over one output frequency cycle to be D_{sh} , the height of ST reference signals should be $2D_{sh}$. By comparing the reference signals v_{sh-U} and v_{sh-N} with the carrier signal shown in Fig. 5a, the ST gating signals of S_U and S_N can be obtained as shown in Fig. 5b. The upper and lower arms modulating signals have been corrected corresponding to the actual ST gating signals as shown in Fig. 5c, where the amplitude of original modulating signals is dropped by $N_{SM}/2$ units of SMs carrier during the ST intervals.

The arm inductor voltage during the upper or lower ST intervals is given by (16). While, the arm inductor voltage is given by (17) during the NST interval.

$$v_{LO} = V_{UN}/4 - (N_U + N_N - N_{SM}/2) \cdot V_{CSM}/2 \quad (16)$$

$$v_{LO} = V_{UN}/2 - (N_U + N_N) \cdot V_{CSM}/2 \quad (17)$$

Using (16) and (17), the arm inductor voltage has zero average value at steady state condition as follows.

$$v_{LO}(t) = D_{sh} \cdot [V_{UN}/4 - (N_U + N_N - N_{SM}/2) \cdot V_{CSM}/2] + (1 - D_{sh}) \cdot [V_{UN}/2 - (N_U + N_N) \cdot V_{CSM}/2] = 0 \quad (18)$$

As the number of inserted SMs in both arms is $N_U + N_N$ with an average of N_{SM} during the switching frequency cycle, the SMs average capacitor voltage is given by:

$$V_{CSM} = \frac{1}{N_{SM} \cdot (1 - 2D_{sh})} V_{DC} = \frac{V_{UN}}{N_{SM}} \quad (19)$$

From (19), the average value of SM capacitor voltages is equal to the peak of the DC-link voltage V_{UN} divided by N_{SM} . This is leading to smaller voltage stresses on the active and passive components compared to FST technique (named as SS technique) [18], in which the SMs capacitor voltage is equal to the average value of the DC-link voltage V_{UN} divided by N_{SM} . The load voltage and current are assumed to be sinusoidal functions:

$$v_{AO}(t) = V_m \sin \omega \cdot t \quad i_{AO}(t) = I_m \sin(\omega \cdot t - \varphi) \quad (20)$$

where I_m is the peak of fundamental phase current and ω is the fundamental output angular frequency. φ is the phase shift

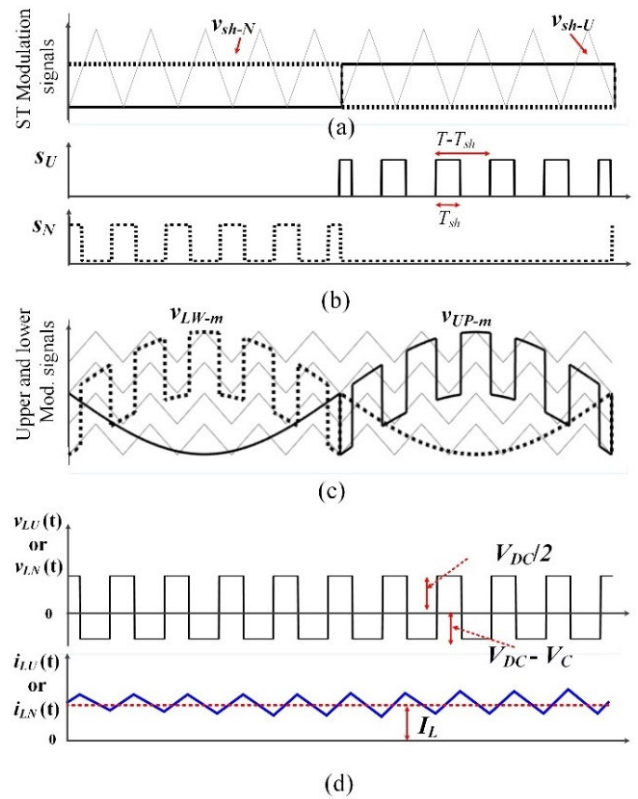


FIGURE 5. The circuit waveforms showing a) shoot-through reference signals, b) gating signals of S_U and S_N , c) arm modulating signals, and d) voltage and current waveforms of the ZS-MMC inductor (LU, LN).

between v_{AO} and i_{AO} . By using Fourier series and according to Fig. 5c, the upper and lower arm voltages and then the upper and the lower DC-link voltages are derived as (21) and (22) respectively.

$$v_{UP} = (1 - D_{sh} - (m - 4D_{sh}/\pi) \cdot \sin \omega \cdot t) \cdot V_{UN}/2$$

$$v_{LW} = (1 - D_{sh} + (m - 4D_{sh}/\pi) \cdot \sin \omega \cdot t) \cdot V_{UN}/2 \quad (21)$$

$$v_{UO} = (1 - D_{sh} + 4D_{sh} \cdot \sin \omega \cdot t/\pi) \cdot V_{UN}/2$$

$$v_{ON} = (1 - D_{sh} - 4D_{sh} \cdot \sin \omega \cdot t/\pi) \cdot V_{UN}/2 \quad (22)$$

where m is the converter modulation index. From (20), (21) and (22), the peak fundamental output phase voltage is:

$$V_m = \frac{m}{2} \cdot V_{UN} = \frac{m}{2} \cdot N_{SM} \cdot V_{CSM} = m \cdot G \cdot \frac{V_{DC}}{2} \quad (23)$$

where G is the converter gain due to using ST mode, and is defined by:

$$G = 1/(1 - 2D_{sh}) \quad (24)$$

By neglecting the converter power loss, the arm current DC component I_{UN} and ZS-inductor current I_L can be expressed by:

$$I_{UN} = m_{RIC} \cdot \cos \varphi \cdot I_m/4$$

$$I_L = m \cdot G \cdot \cos \varphi \cdot I_m/4 \quad (25)$$

where

$$m_{RIC} = \frac{2 \cdot \pi \cdot m \cdot G - 4 \cdot (G - 1)}{\pi \cdot (G + 1)} \quad (26)$$

1) CONTROL OBJECTIVES

The important goal is to keep the SMs capacitor voltages balanced otherwise, the MMC may become unstable owing to an imbalance problem between the SMs [21]. Based on the level-shift PWM technique, the number of inserted SMs in both arms is changed between $N_{SM} + 1$, N_{SM} , and $N_{SM} - 1$ with an average of N_{SM} during a switching frequency cycle ensuring that the sum of the upper and lower arm voltage always equals $N_{SM} V_C$. To ensure that the average SM voltage is well distributed among all SM capacitors, the sorting algorithm strategy for capacitor voltage balance reported in [13] is implemented here. The implementation of this method depends on the sorting of the SM capacitor voltage and the direction of the arm current. If the arm current is positive (negative), the SMs with smaller (higher) capacitor voltage is chosen to be inserted for charging (discharging).

Inherent even low order harmonics exist in the circulating current, with the double line frequency harmonic being the dominant component. When the arm inductance is low, these harmonics need to be suppressed or well-regulated to a small value, otherwise these components will add more loss and current stress on the circuit. Moreover, due to the presence of some sources of imbalance, such as asymmetry (due to manufacturing tolerance) between the ZS-networks components and between the two MMC arms, the AC fundamental current will be unequally distributed between both arms. This will appear as a fundamental frequency current component in the circulating current resulting a difference in the DC voltages produced by the two arms.

For AC circulating current controller, a proportional resonant (PR) controller, which is widely applied for single-phase converters [23], [24], is considered here. The controller is used to detect and eliminate the undesired harmonics. The PR controller can achieve a high gain at the selected frequency in the circulating current, which are double-line frequency and fundamental frequency components, and then eliminate the steady-state error. The open loop transfer function of the PR controller has two parts, one part for double line frequency and the other part for the fundamental frequency.

$$G_{PR}(s) = K_{PR1} + \frac{2\omega_c \cdot K_{iR1} \cdot s}{s^2 + 2\omega_c s + (\omega_o)^2} + K_{PR2} + \frac{2\omega_c \cdot K_{iR2} \cdot s}{s^2 + 2\omega_c s + (2\omega_o)^2} \quad (27)$$

where ω_o is the angular fundamental output frequency, $2\omega_o$ is the angular double line harmonic frequency to be eliminated, and $\omega_c \ll \omega_o$ represents the cut-off frequency. Fig. 6 shows the control block diagram for the two circulating current controllers. Fig. 7 shows the bode diagram of the two PR controllers together with the following set of parameters: $\omega_c = 5$ rad/s, $K_{PR1} = 0.5$, $K_{PR2} = 0.5$, $K_{iR1} = 50$, and $K_{iR2} = 50$. It is seen that this controller achieves the expected high gain peaks at the selected frequencies $2\pi \times 50$ rad/s and $2\pi \times 100$ rad/s and small gain for the other frequencies.

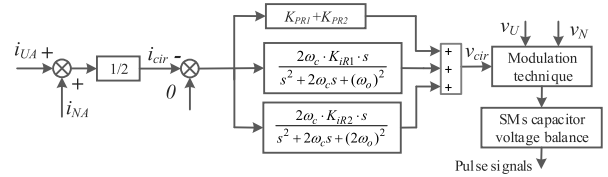


FIGURE 6. The control diagram for suppressing the double line frequency and fundamental frequency components in the circulating current.

IV. ESTIMATING THE ZS-MMC INDUCTOR SIZE

The RICs technique is based on the partial ST concept, in which the upper DC-link switches can shoot through for half of the fundamental frequency cycle while the lower DC-link switches do so for the other half. The two ZS inductors in the ZS-MMC topology charge together in any of LST and UST modes and discharge in NST mode, causing the inductor current to have the largest ripple at the switching frequency. On the other hand, this method has been previously used with the qZS-MMC [18], in which the upper or lower qZS-inductor is only energized during UST or LST respectively. As a result, the inductors will be de-energized for one half of the output frequency cycle causing high fundamental frequency component in the inductor current requiring a larger inductance. Therefore, the RICs technique with ZS-MMC has the benefit of requiring a substantially much smaller inductor size than qZS-MMC. The size reduction potential will be explored next.

The waveforms of the ZS-MMC inductor voltages and currents are shown in Fig. 5d. The inductance is often calculated by:

$$L = \frac{v_L \cdot \Delta t}{\Delta i_L} \quad (28)$$

$$\Delta t = 2D_{sh}/f_s, \quad \Delta i_L = k_{i-ZS} I_L \quad (29)$$

where during ST mode, the inductor voltage v_L is given by (5), k_{i-ZS} is the ZS inductor current ripple ratio, and f_s is the switching frequency. Using (24), (28) and (29), the ZS inductances are given as a function of D_{sh} and gain G (30) and (31) respectively.

$$L_U = L_N = \frac{D_{sh} \cdot V_{DC}^2}{K_{i-ZS} \cdot f_s \cdot P} \quad (30)$$

$$L_U = L_N = \frac{(G - 1) \cdot V_{DC}^2}{2K_{i-ZS} \cdot f_s \cdot G \cdot P} \quad (31)$$

where $P = V_{DC} \cdot I_L$, is the converter input power.

Referring to [18], the qZS inductances (L_U , L_N) and the source inductance can be expressed as a function of D_{sh} or G by (32) and (33) respectively.

$$L_U = L_N = \frac{D_{sh} \cdot V_{DC}^2}{4 \cdot k_{i-qZS} \cdot (1 - 2D_{sh}) \cdot f_o \cdot P} = \frac{(G - 1) \cdot V_{DC}^2}{8 \cdot f_o \cdot k_{i-qZS} \cdot P} \quad (32)$$

$$L_s = \frac{D_{sh} \cdot V_{DC}^2}{2 \cdot k_{i-qZS} \cdot f_s \cdot P} = \frac{(G - 1) \cdot V_{DC}^2}{4 \cdot k_{i-qZS} \cdot f_s \cdot G \cdot P} \quad (33)$$

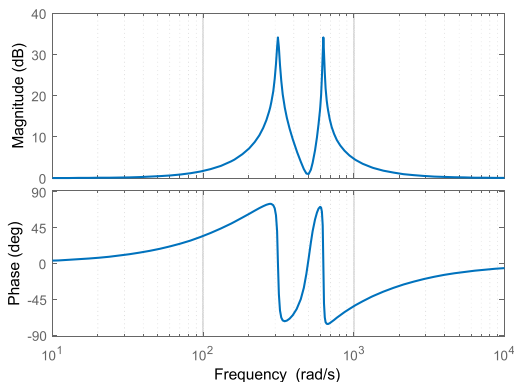


FIGURE 7. Bode diagram of the PR control for filtering 2nd order harmonic and fundamental components in the circulating current.

where k_{i-qZS} is the inductor current ripple ratio of qZS-MMC, and f_o is the output frequency.

From (31) and (33), the inductances L_U and L_N depend on f_s and f_o for the ZS-MMC and qZS-MMC respectively. Dividing (31) by (33), the ratio between the inductances required for ZS to qZS is given (34).

$$\frac{L(ZS)}{L(qZS)} = \frac{4 \cdot f_o \cdot K_{i-qZS}}{K_{i-ZS} \cdot f_s \cdot G} \quad (34)$$

From (34), for the same inductor current ripple $k_{i-ZS} = k_{i-qZS}$ in both ZS-MMC and qZS-MMC, ZS-MMC requires much lower inductances compared with qZS-MMC. For example, the inductance required for qZS-MMC is about 20 times of that required for ZS-MMC, at $f_s = 2$ kHz, $f_o = 50$ Hz and $D_{sh} = 0.25$. Considering a case study of the RMS output voltage equals 3.8 kV, $P = 1.4$ MW, $G = 2$, $V_{DC} = 5.5$ kV, $f_s = 2$ kHz, $f_o = 50$ Hz and $L_U = L_N = 13$ mH, the inductor current ripple k_{i-ZS} of ZS-MMC (31) becomes 20% while the ripple k_{i-qZS} of qZS-MMC (33) becomes 400%. Therefore, the RICs technique is more beneficial with ZS-MMC because the inductor currents have lower ripple, allowing for a smaller inductor size. Moreover, the qZS-MMC requires two more source inductors (which can be merged in one inductor or magnetically coupled) compared with ZS-MMC. This will be on the account of the source current, where the source current in qZS-MMC will be continuous, while it is discontinuous for ZS-MMC.

V. COMPARISON WITH COMPETING TOPOLOGIES

The performance of the proposed ZS-MMC is compared with a range of similar MMC arrangements with similar voltage boosting capability: (1) The qZS-MMC using symmetrically shorted (SS) modulation technique [18], (2) The more established MMC topologies based on FBSMs (FB-MMC) [12], and (3) The quasi Z-source cascaded multilevel converter (qZS-CMI) [25]. The single-phase inverter AC side is designed for an RMS voltage of 3.8 kV and 1.4 MW.

In the previous section, the proposed ZS-MMC has been compared with qZS-MMC [18] when both converters were using the RICs technique in terms of inductor sizes. This differentiating factor is important since the two converters

have the same number of semiconductor devices and the same voltage and current stresses for their semiconductor devices, leading to approximately equal switching and conduction loss for the same rating of the switching devices, leading to similar converter efficiencies. Also, the qZS-MMC has a much higher fundamental frequency component in the qZS-inductor currents compared with the ZS-MMC, which consequently requires larger inductor sizes. Therefore, the qZS-MMC with RICs technique is excluded from this comparison.

Table 1 summarizes the number of semiconductor devices, inductors and capacitors, and DC voltage sources. For the same number of levels ($2N_{SM} + 1$) and magnitude of the output AC voltage for a gain $G = 2.0$, N_{SM} SMs per arm are required for ZS-MMC, qZS-MMC, and FB-MMC, while $3N_{SM}/2$ SMs are required for qZS-CMI. The number of devices per chain-link required for ZS-MMC is $N_{SM}/2$ while $2N_{SM}/3$ for the qZS-MMC. Taking the number of the IGBTs in the FB-MMC as a reference, the total number of IGBTs required by the ZS-MMC decreases to a minimum of 75%. This number reduces to only 87.5% and 93.7% for qZS-MMC and qZS-CMI respectively. Regarding the usage of passive components, the ZS-MMC provides a saving of two inductors and two capacitors compared to the qZS-MMC. But when compared to the FB-MMC, the ZS-MMC uses two more inductors and capacitors. The qZS-CMI would require a greater number of inductors and capacitors especially with increasing N_{SM} . The ZS-MMC, qZS-MMC and FB-MMC require only one DC source but the qZS CMI requires more isolated DC sources, depending on N_{SM} .

Table 2 describes the ratio of the voltage stresses of the switching devices and the capacitor voltages relative to the peak fundamental AC voltage. The relations have been derived to be as a function of G and N_{SM} . The voltage stresses of the series and the chain-link switches of the ZS-MMC are lower than that of the qZS-MMC and both are higher than that of qZS-CMI. The SM switches stress voltages are equal for ZS-MMC, qZS-MMC and FB-MMC, and all of them are higher than that of qZS-CMI. Although ZS-MMC has a higher voltage across the ZS capacitors than the qZS capacitors of the qZS-MMC, the summation of the voltage stress for the two ZS capacitors in the ZS-MMC and for the four qZS capacitors are the same. The qZS capacitor voltage of the qZS-CMI is lower than the ZS capacitor voltage of ZS-MMC. Although the qZS-CMI switches get the lowest voltage stress, the number of the required switches is higher than that of ZS-MMC and qZS-MMC.

Regarding the current stress, Table 3 describes analytically the ratio of the current stress of the switching devices and the inductors relative to the peak fundamental AC current as a function of G , $\cos \varphi$ and m . The current stress of the series and DC-link switches are approximately equal in both ZS-MMC and qZS-MMC, where $m_{RIC} = 0.91$ at $G = 2$. The current stress of the series switch of qZS-CMI is higher than ZS-MMC with a ratio of 1.6 times at $G = 2$, $m = 1$ and $\cos \varphi = 1$. The qZS-CMI gets higher SMs current stress

TABLE 1. Comparison of active and passive components requirements.

| | ZS-MMC | qZS-MMC | FB-MMC | qZS-CMI |
|-------------------------|--------------|--------------|------------|--------------|
| SMs | $2 N_{SM}$ | $2 N_{SM}$ | $2 N_{SM}$ | $3 N_{SM}/2$ |
| IGBTs | $4 N_{SM}$ | $4 N_{SM}$ | $8 N_{SM}$ | $6 N_{SM}$ |
| ZS/qZS IGBTs | $2 N_{SM}$ | $3 N_{SM}$ | 0 | $3 N_{SM}/2$ |
| Total IGBTs | $6 N_{SM}$ | $7 N_{SM}$ | $8 N_{SM}$ | $7.5 N_{SM}$ |
| Inductors | 4 | 6 | 2 | $3 N_{SM}$ |
| Capacitors | $2 N_{SM}+2$ | $2 N_{SM}+4$ | $2 N_{SM}$ | $3 N_{SM}$ |
| DC sources (split caps) | 1 (2) | 1 | 1 (1) | $3N_{SM}/2$ |

TABLE 2. Comparison of voltage stresses relative to the peak output voltage.

| | ZS-MMC | qZS-MMC | FB-MMC | qZS-CMI | |
|-------------------|---------------|----------------|-----------------------|-------------------------------|--------------|
| DC-link Switches | 1 | $(2G - 1) / G$ | N/A | N/A | |
| Series Switches | 1 | $(2G - 1) / G$ | N/A | $\frac{(2G - 1)}{(N_{SM} G)}$ | |
| SMs Switches | $2 / N_{SM}$ | $2 / N_{SM}$ | $2 / N_{SM}$ | | |
| ZS/qZS Capacitors | $(G + 1) / G$ | C_1 | 1 | C_1 | $1 / N_{SM}$ |
| | | C_2 | $\frac{(G - 1)}{(G)}$ | N/A | C_2 |
| SMs Capacitors | $2 / N_{SM}$ | | | N/A | |

than the FB-MMC and both are higher than qZS-MMC and ZS-MMC. The current stress of the ZS inductors of the ZS-MMC is approximately equal to that of the qZS-MMC and both are half of the value of qZS-CMI. Also, the FB-MMC gets a higher current stress on the arm inductor compared to the qZS-MMC. Therefore, it can be concluded that the ZS-MMC has the lowest current stresses.

In addition, the comparison has been carried out in terms of conduction and switching loss and it is found that:

- For the conduction loss: in both buck and boost modes, the ZS-MMC has the lowest loss, while qZS-CMI has the highest loss, and the conduction loss of FB-MMC is higher than the qZS-MMC.
- For the switching loss: the ZS-MMC, qZS-MMC and the FB-MMC have equal switching loss in buck mode, and all these have higher switching loss than the qZS-CMI. In boost mode, the ZS-MMC has lower switching loss than the qZS-MMC and both converters have higher switching loss than qZS-CMI. The FB-MMC has the lowest switching loss.
- For the total loss (conduction and switching): the ZS-MMC has the lowest total loss in buck mode. On the other hand, the FB-MMC has the lowest total loss in boost mode. The qZS-MMC has higher total loss than the qZS CMI, and both have higher total loss than the ZS-MMC, causing the ZS-MMC the second-best, in boost mode.

TABLE 3. Comparison of current stresses relative to the peak output current.

| | ZS-MMC | qZS-MMC | FB-MMC | qZS-CMI |
|------------------|---|--|--|---------------------|
| Series Switches | $\frac{m \cdot G}{2} \cos \varphi - \frac{m_{ric}}{4} \cos \varphi + \frac{1}{2}$ | $\frac{m_{ric}}{4} \cos \varphi + \frac{1}{2}$ | N/A | G |
| DC-link Switches | | | N/A | N/A |
| SMs Switches | $\frac{m_{ric}}{4} \cdot \cos \varphi + \frac{1}{2}$ | $\frac{m}{4} \cdot \cos \varphi + \frac{1}{2}$ | $\frac{m \cdot G}{4} \cdot \cos \varphi + \frac{1}{2}$ | $\frac{(G + 1)}{2}$ |
| ZS/qZS Inductors | $\frac{m \cdot G}{4} \cdot \cos \varphi$ | $\frac{m \cdot G}{4} \cdot \cos \varphi$ | N/A | $\frac{G}{2}$ |
| Arm Inductors | $\frac{m_{ric}}{4} \cdot \cos \varphi + \frac{1}{2}$ | $\frac{m}{4} \cdot \cos \varphi + \frac{1}{2}$ | $\frac{m \cdot G}{4} \cdot \cos \varphi + \frac{1}{2}$ | N/A |

TABLE 4. Prototype parameters.

| Parameter | Value |
|---|-----------|
| Peak AC output voltage (V) | 170 |
| DC-source voltage (V) | 225 |
| Number of SMs N_{SM} | 2 |
| Load resistance (Ω) / Load inductance (mH) | 15.2 / 4 |
| SMs capacitances (mF) / Arm inductance (mH) | 3.3 / 2.5 |
| ZS capacitances (mF) / ZS inductances (mH) | 3.3 / 15 |
| Switching frequency (kHz) | 10 |

VI. EXPERIMENTAL EVALUATION

The proposed concept is suitable for medium voltage applications which makes the experimental evaluation of this concept at full voltage and power scale very difficult. Therefore, a laboratory prototype of the proposed ZS-MMC, where the schematic diagram of the prototype is shown in Fig. 8, was constructed on a small scale to test its behavior and performance. The circuit parameters are summarised in Table 4 and Fig. 9 illustrates a photo of the prototype actual hardware.

The modulation technique and control algorithm are implemented on a 225-MHz TMS320C6713 floating-point DSP which works in conjunction with an FPGA platform for the data acquisition and PWM gating pulse generation. A daughter card is connected to the DSP through a host port interface (HPI) connector and used for real-time data capture by MATLAB. There are two ways of displaying the experimental results: screen captures from the oscilloscope or, for data that requires post-processing, download the data points acquired with the 200-MHz oscilloscope as Excel files which are re-drawn using MATLAB and processed for retrieving the frequency spectrum data. The DSP sampling and the PWM carrier switching frequency are set to 10 kHz.

The experimental results have been obtained when the proposed topology was supplied with 225V DC source voltage. The modulation index m of 0.98 and an ST duty ratio D_{sh} of 0.17 were used to obtain a 1.5 voltage gain G . The output voltage v_{AO} and current i_{AO} and their FFT spectrums are illustrated in Fig. 10. Although the expected peak value of the fundamental output voltage component according to (23) is 167 V, the value revealed by the FFT is smaller which is 162 V. This difference is a result of voltage drops across the

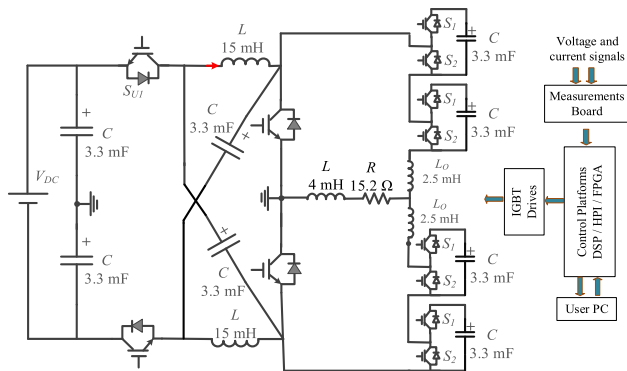


FIGURE 8. Experimental system schematic diagram of the ZS-MMC.

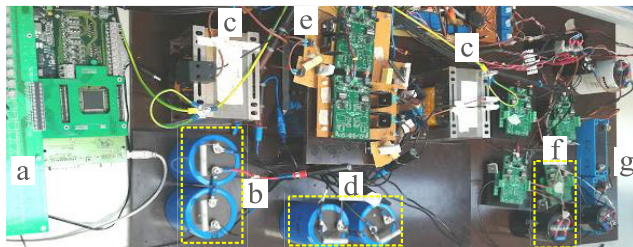


FIGURE 9. Photo of the experimental prototype including, a) control platform TMS320C6713 DSP and FPGA, b) decoupled DC-capacitors c) ZS-inductors, d) ZS-capacitors, e) ZS-switches, f) sub-module, and g) MMC arm inductors.

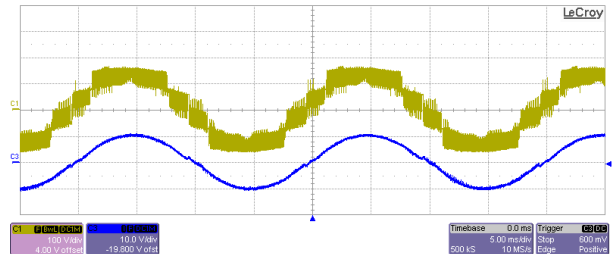
power circuit components. The output voltage and current have a negligible low-order harmonics.

The DC-link voltages (upper voltage v_{UO} and lower voltage v_{ON}) are shown in Fig. 11 with peak values of 168 V which is a little lower than the theoretical value (14) due to the voltage drops across the power circuit components. The normalized stress voltage ($V_{UN}/(V_{DC}/2)$) on the chain-link switches in ZS-MMC has a percentage of 1.49 ($2 * 168V/225V$). According to [18], the normalized stress voltage on the DC-link switches for qZS-MMC is 1.49 and 1.96 for RICs and SS techniques respectively. It is clear that, the stress voltage on the DC switches in ZS-MMC is equal to that of qZS-MMC [18] when using the RICs technique and both are lower than that of the qZS-MMC when using SS technique. Fig. 11 shows the experimental waveforms of the ZS-capacitor voltages (v_{CU} and v_{CN}). The average value of the two ZS-capacitor voltages v_{CU} and v_{CN} are 281 V, which equals the expected value obtained from (13).

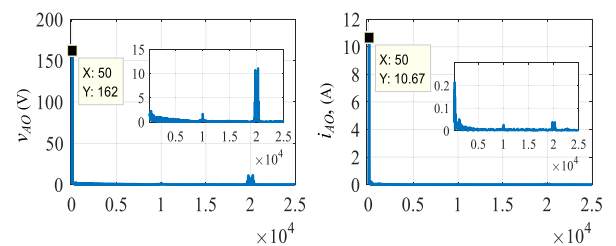
In order to compare with qZS-MMC, the ZS inductance is used in this work to be equal the qZS inductance used in [18]. Fig. 12 shows the ZS-inductor currents (i_{LU} and i_{LN}). It can be observed that the ZS inductor currents have a low value of 50 Hz harmonic component. Comparing with [18] for qZS-MMC, applying the RICs technique to qZS-MMC causes the inductor currents i_{LU} and i_{LN} to have a high ripple at fundamental frequency where their peak-to-peak equals twice of the average value (8A). In contrast, for the proposed converter ZS-MMC, the inductor currents have a low ripple at fundamental frequency, where their peak-to-peak equals 0.2 (0.8A) of the average value. Therefore, the RICs technique is more advantageous when it is applied with

ZS-MMC compared with qZS-MMC due to the significantly lower value of the fundamental frequency component ripple and consequently ability to use a low inductor size.

Fig. 13 shows the ZS series switch currents i_{SU1} and i_{SN1} , which also represents the DC voltage source currents. The switch S_{U1} and S_{N1} are reverse biased during the LST and UST modes respectively. It is noted that the source current is discontinuous.



(a)

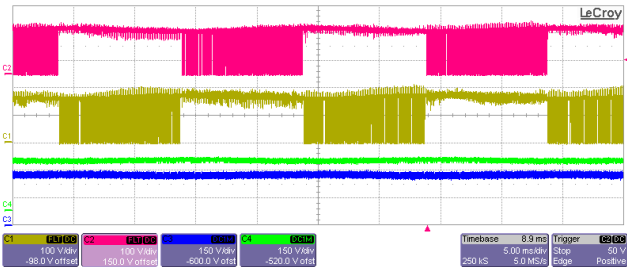


(b)

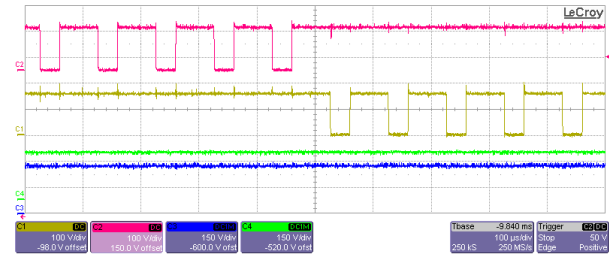
FIGURE 10. Experimental waveforms for the converter output voltage (yellow) and current (blue) and their FFT spectrum.

From Fig. 10, it has been highlighted that the actual output voltage is slightly lower than the expected output value due to the voltage drop on the circuit components, such as switches and inductors. Therefore, Fig. 14 shows the theoretical and experimental voltage gains of the proposed ZS-MMC where the voltage gain is defined as the ratio of the measured peak value of the fundamental output voltage and half value of the DC source voltage. The experimental voltage gain curves have been drawn at four different values of DC source voltage which are 75 V, 100 V, 150 V and 200 V at the same load. All the experimental gain curves are lower than the theoretical curve due to voltage drops across the power circuit components which are not considered in the theoretical model. Increasing the DC source voltage yields a higher gain value at the same ST duty ratio.

Fig. 15 indicates the experimental efficiency curves of the ZS-MMC prototype when using the RICs technique, which has been compared with the qZS-MMC when using RICs and SS technique at different output power at $G = 1.5$ and supply voltage V_{DC} of 225 V. While the output voltage is maintained constant, the output power is modified by adjusting the load resistance value to emulate the conditions of a grid-connected inverter increasing its loading. The input power was calculated by measuring the source voltage and current readings whilst the load power was determined by using the measured load current in the I^2R power relation. The maximum efficiency is approx 94% at a load power of



(a)



(b)

FIGURE 11. Experimental waveforms showing (from top to the bottom) a) the upper and the lower DC-link voltages v_{U0} and v_{ON} (100 V/div) and the ZS capacitor voltages v_{CU} and v_{CN} (150 V/div) and b) Zoom.

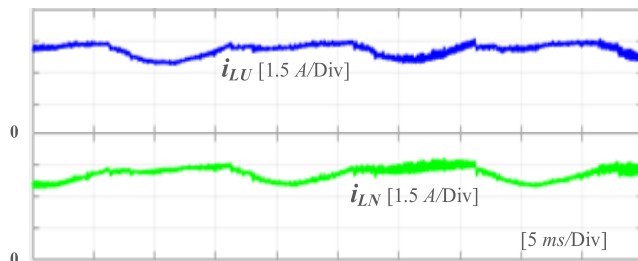


FIGURE 12. Experimental waveforms for ZS inductor currents i_{LU} and i_{LN} (1.5 V/div).

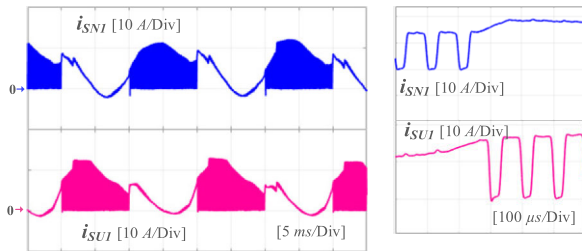


FIGURE 13. Experimental waveforms for the upper and lower ZS series switch currents i_{SN1} and i_{SU1} (10 A/div) at 5ms/div (left) and at 0.1ms/div (right).

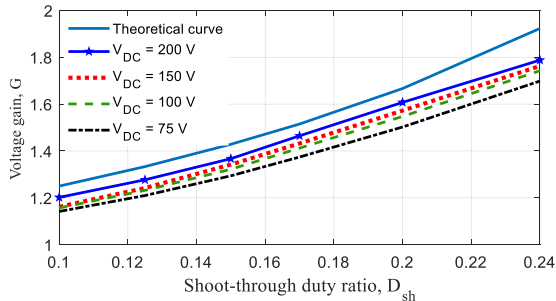


FIGURE 14. Output voltage gains with the variation of D_{sh} at $m = 0.98$.

880 W for both converters when using the RICs technique. This is because that the ZS-MMC and qZS-MMC have the same number of semiconductor devices with the same voltage

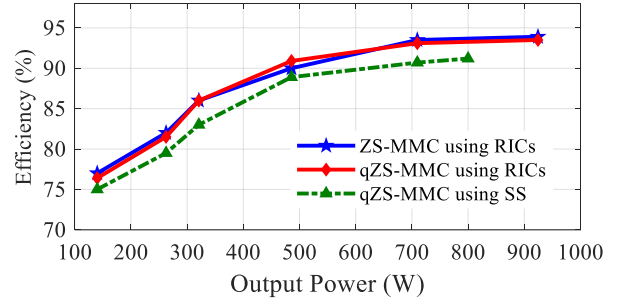


FIGURE 15. Efficiency of the ZS-MMC and qZS-MMC prototypes at $G = 1.5$.

and current stresses, leading to approximately equal switching and conduction loss for the same semiconductor devices rating, leading to similar converter efficiencies. While in the case of the SS technique, due to higher stress voltage on the DC-switches compared to RICs technique, and also applying full ST principle, the qZS-networks loss is higher when using SS technique compared to RICs technique and consequently, the converter efficiency is lower when using SS technique.

VII. CONCLUSION

A new converter, Z-source MMC (ZS-MMC), that can provide both buck and boost voltage capabilities, is presented. The converter operation principles are discussed. The reduced inserted cells (RICs) modulation technique has been derived and implemented. Design guideline for the ZS required inductors has been presented and compared with the requirement for the quasi ZS-MMC (qZS-MMC). It is found that the RICs technique is more beneficial when used with the ZS-MMC because the ZS inductor currents have a much lower fundamental frequency component allowing for a smaller inductor size, when compared to the qZS inductor currents in qZS-MMC. Also, the proposed ZS-MMC has been compared with qZS-MMC, the full-bridge sub-modules based MMC (FB-MMC) and the quasi Z-source cascaded multilevel inverter (qZS-CMI), showing that:

- The ZS-MMC requires the smallest number of semiconductor devices, and it is considered the second-best candidate for the number of passive components following the FB-MMC.
- The ZS_MMC has the lowest total loss in buck mode, the lowest conduction loss in both buck and boost modes. Also, it is the second-best candidate in terms of total loss in boost mode following the FB-MMC.
- The ZS-MMC has the lowest current stress and the second-best candidate regarding the stress voltage after the qZS-CMI.

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