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A Design of 44.1 fJ/Conv-Step 12-Bit 80 ms/s Time Interleaved Hybrid Type SAR ADC With Redundancy Capacitor and On-Chip Time-Skew Calibration

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ABSTRACT A 12-bit 80 MS/s hybrid type analog-to-digital converter (ADC) for high sampling speed and low power applications is presented in this paper. It has a subranging architecture with a front end of 6-bit Flash ADC with five channels of 6-bit time interleaved synchronous Successive Approximation Register (SAR) ADC. The proposed architecture with a shared 6-bit Flash ADC and time interleaved SAR ADC provides a power and area efficient high speed ADC. The proposed Time-skew calibration is implemented to minimize the discrepancy between the output of Flash ADC and SAR ADC's channels. To rectify the decision error of the Flash ADC and extract the time-skew information, 1-bit redundancy is included in the CDAC of the SAR conversion. The decision error between the Flash ADC and the SAR ADC is covered with designed redundancy and the mismatch between the ADCs is covered with the time-skew calibration. To reduce the offset mismatch between Flash and SAR ADC and within SAR ADCs, all comparators are calibrated to minimize their absolute offset by utilizing background offset calibration. The modified dynamic strong ARM comparator is used for flash ADC and dynamic latched comparator is used for SAR ADCs. For fine offset calibration and low power consumption, the comparator's offset calibration circuit is implemented. To reduce the kickback noise and enhance the overall energy efficiency for fast operation of SAR ADCs, rail-to-rail dynamic latch comparator with modified adaptive power control (APC) is implemented. The proposed ADC structure has been implemented in 130 nm CMOS process. The ADC has an effective number of bit (ENOB) of 10.97 bits while consuming 7.08 mW current consumption from the 1.2 V supply voltage.

INDEX TERMS Adaptive power control (APC), comparator offset calibration, hybrid type time interleaved SAR ADC, low power consumption, redundant capacitor, time-skew calibration, time-skew error.

I. INTRODUCTION

Flash analog-to-digital converter (ADC) has been frequently used in previous years for low-resolution and high-speed applications, which include satellite receivers, ultra wide-band (UWB) receives. Successive approximation register (SAR) ADC structure replaces the Flash ADC structure by employing a time interleaving algorithm, as submicron CMOS technologies help in accelerating the speed of transistor operation in low power [1]–[4]. Four channels of time-interleaved SAR ADC has been used for 600 MHz and 12-bit ADC architecture [5]. Since the traditional SAR ADC uses the binary search algorithm, for n-bit decision it requires n + 1 clock cycles. However, in Time interleaved ADCs, adding more channel is not advisable because of the time mismatch, offset, and gain errors between them.

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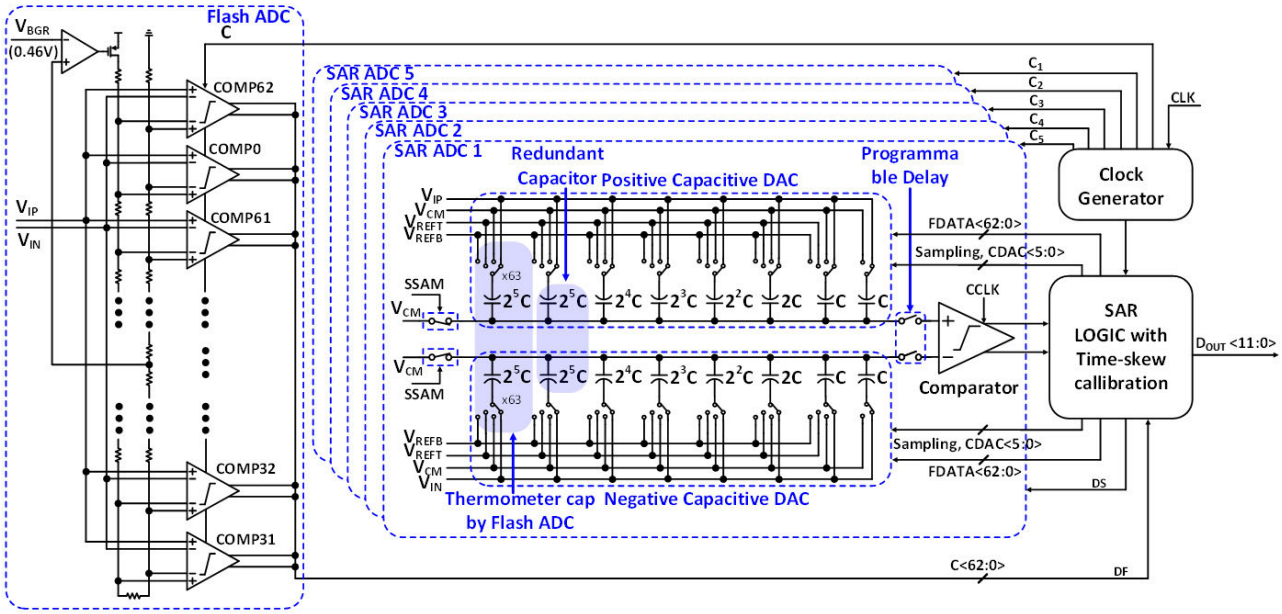

FIGURE 1. The top-block diagram of the proposed hybrid flash follower time interleaved SAR ADC.

Hence, a time-interleaving structure with a large number of channels often requires redundant channel or mismatch calibration schemes [6]. The speed limitation factor in SAR ADC can be overcome by 2-bits per cycle decision algorithm in time-interleaved SAR ADC [7, [8]. However, the hardware complexity of 2-bit/cycle is about 3 times more than the traditional SAR ADC operation.

For medium speed and medium resolution, SAR ADCs are the most energy-efficient architecture. The time-interleaved architecture is frequently used to improve the SAR ADCs bandwidth. However, time-interleaved ADC structures have several issues, which are the result of mismatches between the channels, such as time skew error, offset mismatch, and gain mismatch. Time skew error caused by the increasing input signal frequency, unlike the other errors. Time skew error is dominant in time-interleaved ADCs architecture as it is employed to increase bandwidth. Many types of researches have presented different background timing skew calibrations by using an additional channel taking it as a reference. To decrease the number of channels from the time-interleaved ADCs, hybrid type time-interleaved SAR ADC [9] architecture can be used, which improves the SAR ADC conversion speed by front end Flash ADC which provides the multi-bit MSB.

This paper presents an 80 MS/s time-interleaved hybrid ADC structure based on a shared Flash ADC and time-interleaved SAR. Front end 6-bit Flash ADC helps to achieve the MSBs in a single clock cycle, which decreases many clock cycles from the SAR logic operation. In addition, the total conversion time is greatly reduced by employing the time interleaving technique to presented architecture. The overall power consumption can be lowered by sharing the 6-bit Flash ADC with the 5 channels 6-bit time-interleaved SAR ADCs. To solve the offset mismatch between SAR ADC and Flash ADC and within SAR ADCs, all comparators are calibrated to minimize their absolute offset by utilizing background offset calibration. A modified strong-arm latched comparator is used in Flash ADC and a dynamic latched comparator is used in SAR ADCs and for fine offset calibration and low-power consumption comparator offset calibration is implemented. Time skew calibration is used to reduce the time error between the SAR ADCs.

The proposed paper is organized as follows. Section II explains the architecture of hybrid type time-interleaved SAR ADC with time-skew calibration. Section III discuss about the circuit implementation and the sub-blocks, including flash ADC, sub-blocks of time-interleaved SAR ADC such as, capacitive DAC, mismatch between flash and SAR ADC, time-skew logic, dynamic latch comparator with modified APC. Complete measurement results are discussed in section IV and finally we conclude in section V.

II. PROPOSED HYBRID TIME INTERLEAVED SAR ADC ARCHITECTURE

The top block diagram of the proposed hybrid type time-interleaved SAR ADC architecture is depicted in Figure 1. The ADC is composed of a 6-bit Flash ADC, a 6-bit synchronous SAR ADC, a clock generator, and a SAR logic for multiplexing and bit combining. The clock generator contains the programmable delay circuit to correct the timing skew which is controlled by the timing-skew estimator. The 6-bit Flash ADC in the proposed design does not affect

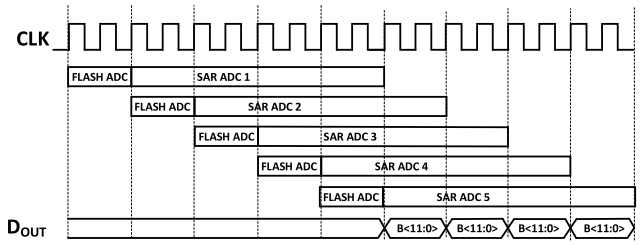

FIGURE 2. The timing diagram of the proposed hybrid flash follower time interleaved SAR ADC.

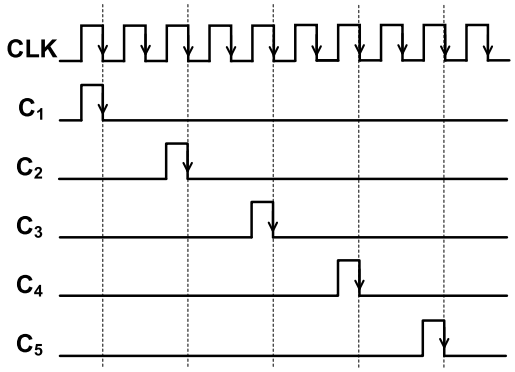

FIGURE 3. The timing diagram of clock generation.

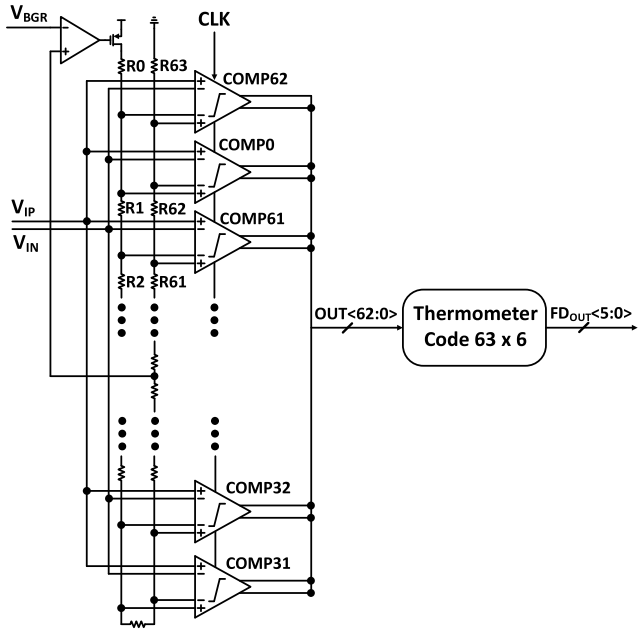

FIGURE 4. Architecture of the proposed SAR ADC.

from time-skew errors, because it operates at the full speed of the proposed ADC to resolve the MSBs for each SAR channel [10]. To estimate the time skew and resolve the 6 LSBs with 1-bit redundancy of SAR channels, the output from the Flash ADC is also taken as a timing reference at 1/5 of sampling speed. Figure 2 represents the timing diagram of the proposed hybrid time-interleaved SAR ADC. A single sampling clock is used to minimize the timing skew error between the SAR ADC and Flash ADC as illustrated in Figure 3. The sampling clock for each channel is generated by the global clock CLK. In order to reduce the logic delay mismatch, the sampling clock is designed with a sharp transition slope based on post-layout simulation. While CDAC settles down, each SAR ADC operates synchronously to avoid undesirable reference Variation from SAR ADC channels. The input is sampled for one clock cycle, and Flash ADC provides the 6-bit MSBs during the following one clock cycles. Then 7-bit LSBs, with 1-bit redundancy are determined by 1 channel SAR ADC for seven clock cycles. Offset and time-skew calibration will be collectively performed in the final two clock cycles.

In the proposed paper, we implemented a time-skew calibration to minimize the discrepancy between the output of Flash ADC and SAR ADC's channels. Time-skew calibration operates at a principle that helps in aligning the falling edge of the clock used in Flash ADC with the SAR ADCs sampling clock falling edge. The falling edge of the sampling clock of SAR ADC can be adjusted to align the falling edge of the sampled signal from SAR ADC with the Flash ADC clock signal considering the sampling switching threshold variation. To correct the Flash ADC error, 1-bit redundancy is added in the SAR conversion process. The difference between the output of Flash ADC and the output of the corresponding SAR channel is precisely represented as SAR conversion lower output bits. Thus, the lower output bits of SAR conversion corresponds to the minimum time-skew. According to output bits of Flash ADC, the lower output bits of SAR will be first sorted, then the sampling clock of SAR minimize the discrepancy of lower output bit of SAR is computed. It is because of the computation which only processes the small-signal represented in output bit of SAR conversion, and computation is a simple process than expanding correlation-based calibration to multiple bit timing references [11]–[13]. This calibration operates in the background to trace voltage and temperature variation and this calibration does not intersperse the ADC operation and it does not affect the input signal.

III. CIRCUIT IMPLEMENTATION

A. FLASH ADC

6-bit Flash ADC contains 63 comparators and a resistor string to define the reference voltage for each comparator. To complement the reference-settling period with the decision phase, we implemented a modified comparator that has differential dual input in 6-bit Flash ADC as shown in Figure 4.

When reference voltages settle down, then comparators will enable and start the comparison. The input signal can be directly compared with the reference voltages in the conventional Flash ADC comparators [9]. Conventional fully differential implementation includes the rail-to-rail input pair and zeroes static power. Conventional Flash ADC comparators suffer from low power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) when

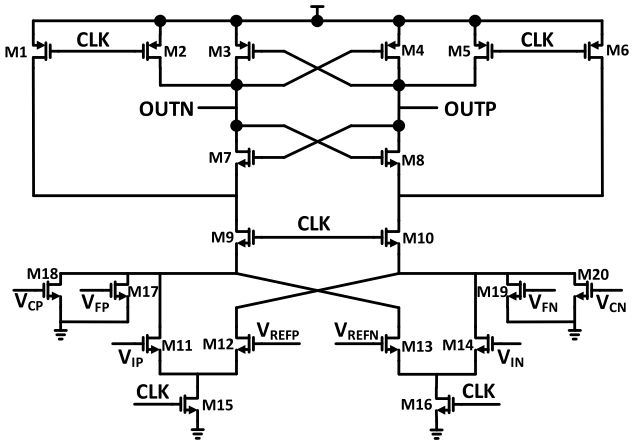

FIGURE 5. Schematic of modified strong ARM comparator for flash ADC.

reference voltages or input are large in fully differential topology. In conventional architecture, the sampled signal between Flash and SAR ADC are matched because the Flash ADC's sampling circuit is a scaled version. In the proposed architecture to minimize the timing skew correction range, the clock of Flash ADC is closely aligned with the sampling signal of SAR ADC.

The fully differential topology of 6-bit Flash ADC has 63 comparators and 64 resistors, which compares differential reference voltages with the input signal. The schematic of the modified strong ARM comparator for the 6-bit Flash ADC is represented in Figure 5. Comparator architecture is implemented without a preamplifier, resulting in reducing the power consumption and satisfying high-speed operation. At the Flash ADC input, high kickback noise is caused due to the absence of a preamplifier. We place the transistor M9 and M10 between the regenerative back-to-back inverter transistors M3, M4, M7, M8, and input pair M11 – M14 to reduce the kickback noise from the input pair of comparator [11], [14]. During the reset phase, the drain of input transistors is floating with the implemented kickback reduction technique while in the conventional case it is precharged to VDD. During the comparator's operation, due to this less voltage variation is caused at the drain of transistors M11 – M14, thereafter kickback noise-reducing at the input stage. The kickback noise is reduced from the comparator in the implemented architecture of Flash ADC. One way to reduce the mismatch offset is to increase the size of input transistors, but it results in increasing the kickback noise and the total input capacitance. Another way is to use preamplifiers, but they increase the overall power consumption. We have adopted a digital calibration for offset error in flash ADCs as digitally designed techniques are proven to be more useful against the process variation and provide flexibility in a system level design. An intentional imbalance in current is generated by adjusting the sizes of transistor M17, M18 and M19, M20 to correct the offset error of the comparators in flash ADC. When compared to the capacitance based techniques, this current injection technique is more useful in reducing the parasitic capacitance because it does not involve large capacitor.

B. TIME INTERLEAVED SAR ADC

The 12-bit time-interleaved hybrid type SAR ADC for the single channel is shown in Figure 1. To ensure the linearity, bottom plate sampling is used and apart from CDAC, 32C redundancy capacitor is used for high sampling speed. During the sampling phase, input is sampled at the bottom plate and VCM is connected to the top plate of capacitors. The size of MSB capacitor is decided for addition-only digital error correction and Flash ADCs sign code transferred to MSB capacitor [13]. Flash ADC's 6-bit MSB in the form of 63 thermometers is transferred to 32C capacitor of SAR ADC. The proposed IMCS switching has an additional 32C*63 capacitors for redundancy between SAR ADC and Flash ADC which is controlled by output signals from the Flash ADC. MSB DAC have 63 unary weighted capacitors, which are controlled by the output of the flash ADC. 1bit redundancy added between the flash ADC and SAR ADCs to cover the error from flash ADC and to extract the timing skew information as explained in the timing skew mismatch. SAR ADC is composed of a 6-bit CDAC with a 1-bit redundancy capacitor, a comparator, and SAR logic. SAR logic controls the 6-bit LSB of CDAC which is distributed as binary-weighted capacitors. To estimate the timing-skew information and to compensate for the Flash ADC error, we use 1-bit redundancy in between Flash ADC and SAR ADC. The weighted sum of the output from Flash ADC (DF) and the output from SAR ADC (DS) is the output of each channel (DC), DC = 32*DF + DS. To optimize the power consumption, a dynamic latch comparator with modified adaptive power control is used in SAR ADC.

The bandwidth mismatch occurring in the sampling switches and the capacitors among various channels will lead to the overall bandwidth mismatch. This modulate the overall continuous-time input signal, and after the signal being sampled in to C the operation of the remaining part of the S/H is in discrete-time and all the mismatches will appear as offset and gain-mismatches that were already fully characterized before. Assuming that R and C are the on-resistance switches and the sampling capacitance of the five channels respectively, then the sampling time constant would be represented as:

$$T_5 = R_5C_5 = T(1 + r_5) \tag{1}$$

where T corresponds to its mean/ nominal value and r5 is the percentage of the time-constant mismatch. The bandwidth mismatch is calibrated with the programmable bias current for each input buffer. The input buffer has two main purposes, first is to reduce the input impedance to drive a large ADC array and improves bandwidth and the second is to reduce the non-linear current drawn by the sample-and-hold circuit from the input source. We want to have high output bandwidth, low capacitance and harmonic distortion. We use

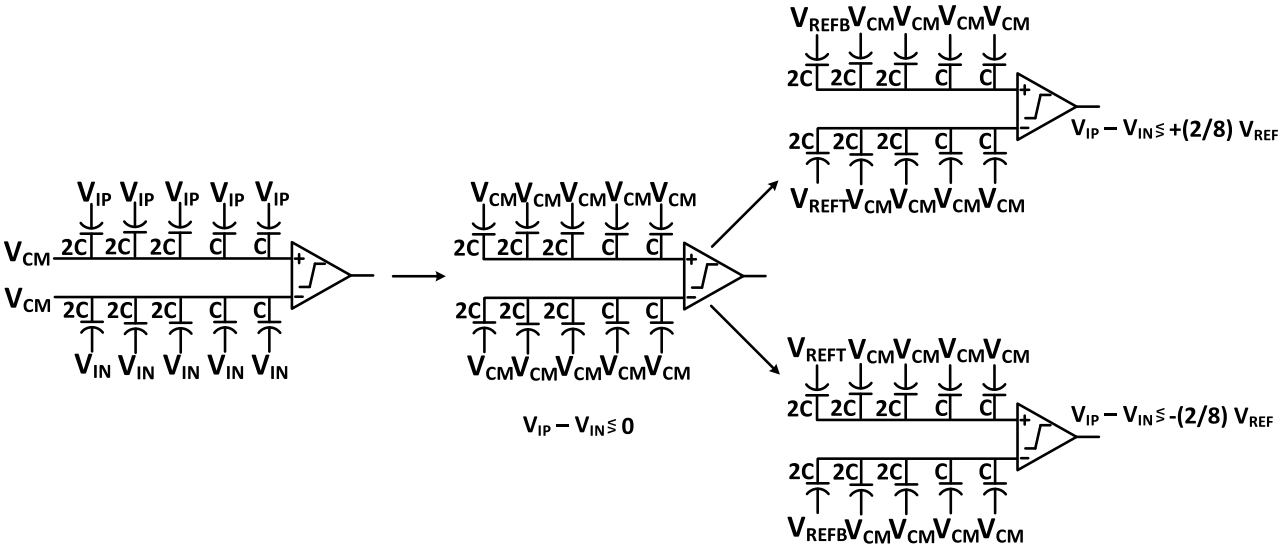

FIGURE 6. Proposed redundancy implementation using common mode charge recovery algorithm.

the programmable bias current for input buffers to calibrate the bandwidth mismatch.

1) CAPACITIVE DAC WITH REDUNDANCY IMPLEMENTATION

In the presented prototype, the IMCS algorithm is incorporated with redundancy as shown in Figure 6. During the sub-binary search, stepping size is proportional to the size of capacitors in the IMCS algorithm. When the first comparison is finished, the stepping size is equal to the DAC's first size and the input will compare with $\pm 2/8 V_{REF}$. Without an extra complexity, if the redundancy is implemented with the conventional switching, the stepping size will be asymmetric [15], [16]. In the proposed IMCS switching algorithm, the error-tolerance and the stepping size are symmetric for each decision level, while in the conventional switching error tolerance and the stepping size both are asymmetric for decision levels. In conventional asymmetric switching, decision error occurs in a direction that can be compensated but the same decision error in another direction cannot be compensated. In the proposed IMCS switching implementation, the input has an equal chance of making decision error in any direction. In the asymmetric error tolerance, the redundancy algorithm is less tolerance for correcting the dynamic error than symmetric error tolerance.

During the search algorithm, the proposed architecture implements the redundancy to DAC by adjusting the capacitor size to the desired stepping sizes. During the search process, symmetry is required to allow the same tolerance to decision settling error regardless of its direction ''up'' or ''down''. The proposed IMCS switching with redundancy avoids the complex digital circuitry, delays included by decoders and arithmetical units, and extra power, but it does not have the capability to adjust the redundancy amount after fabrication [15]. As compared to the conventional switching algorithm [17], the proposed IMCS switching technique is 94% more energy efficient.

2) MISMATCH BETWEEN FLASH AND SAR ADC

To design a FATI_SAR ADC, all mismatches [18], not only between SAR ADCs but also between the Flash and SAR ADCs, should be taken into consideration due to the lack of decision redundancy. Since the Flash and SAR ADCs have different input sampling and also can have different references, a remedy of gain error is needed. To remove the mismatch, bottom plate sampling is used for SAR ADCs. To remove the mismatch, bottom plate sampling is used for SAR ADCs. The custom designed unit capacitor used. It is a combination of MIM and MOM structures. The benefit of capacitor arrays with the MIM structure is that the top and bottom plates are shielded from each other in a capacitor array and each element can be accessed without adding parasitic capacitance. The capacitance from VIAs is covered by using little wider metal strips for M4 instead of minimum size. To ensure the small parasitic capacitance at the input of the comparator, bottom plate of capacitor is implemented with metal M5. Although the input of the comparators in the Flash and SAR ADCs have different attenuation, decision gain error does not occur because both sampled input and DAC levels are reduced at the same rate. Gain matching between SAR ADCs is also resolved in this manner with the bottom-plate sampling.

To solve the offset mismatch issue between the Flash and SAR ADCs as well as within SAR ADCs, all comparators are calibrated to minimize their absolute offset by utilizing background offset calibration. The modified dynamic strong ARM comparator is used for Flash ADC and the dynamic latched comparator is used for SAR ADCs. Additionally, for fine offset calibration and low-power consumption, the comparator's offset calibration circuit is implemented as shown in Figure 7. The comparator in calibration mode is retired from the normal operation, and to get a zero-input condition, its differential inputs are tied together. The results from the offset polarity sensing with zero input

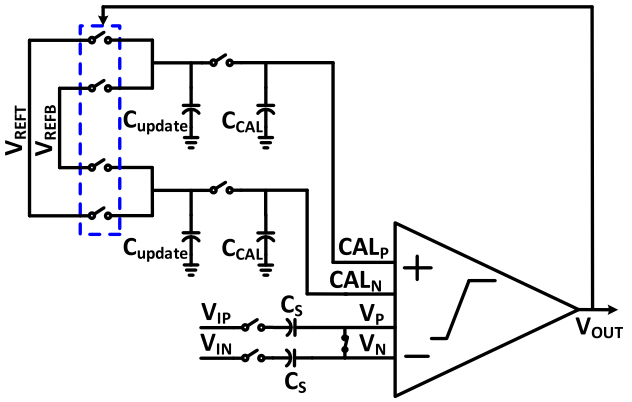

FIGURE 7. Block diagram of comparator offset calibration technique.

are reflected in the calibration technique to update offset control information. The comparator offset calibration is performed continuously in a round-robin manner, and thus the offset of all comparators are minimized with the step size determined by calibration technique and transconductance of the additional input pair for calibration. An extra reference switch is added in each comparator to eradicate the necessity of the comparator in calibration mode. When the first comparator is in calibration mode, the i^{th} comparator is connected to i + 1 so that the second comparator can operate for the first comparator and so on. Three clock cycles are required for the offset correction: sensing the offset polarity, charging and discharging C_{update}, and CCAL update. During offset polarity sensing Flash, ADC comparators can be retired. Similarly, all comparators enter in the calibration mode sequentially. A SAR ADC stays in the calibration mode for 5 clock cycles. The offset correction for the SAR ADC is also done through the three clock cycles of sensing the offset polarity, C_{update}, and CCAL updating. To minimize the power consumption from the SAR channel, all unnecessary blocks such as CDAC and SAR logics are disabled during the calibration mode.

3) SAR LOGIC WITH TIMING-SKEW CALIBERATION

A theoretical diagram of ADC time skew operation is represented in Figure 8. In this figure, C indicates the Flash ADC clock and C_x indicates SAR ADCs clock. The middle scale shows the corresponding Flash ADC's reference voltages according to the SAR ADC's MSB DAC level. The SAR ADC's LSB DAC code is on the right. In Figure 8(a), C and C_X are aligned and sampled the input signal simultaneously. Assuming the Flash ADC is correct and the coarse estimation from Flash ADC is accurate, as both ADCs sample the same input. Here the output of Flash ADC is 12. If there is no noise or inaccuracy, the final output always lies in the nominal range which is 16 to 48. In Figure 8(b) Flash ADC and SAR ADC do not sample the input simultaneously as C and C_X are not aligned. In this case the coarse estimation from Flash ADC is incorrect and its output is 11. The SAR ADC starts the conversion process from different

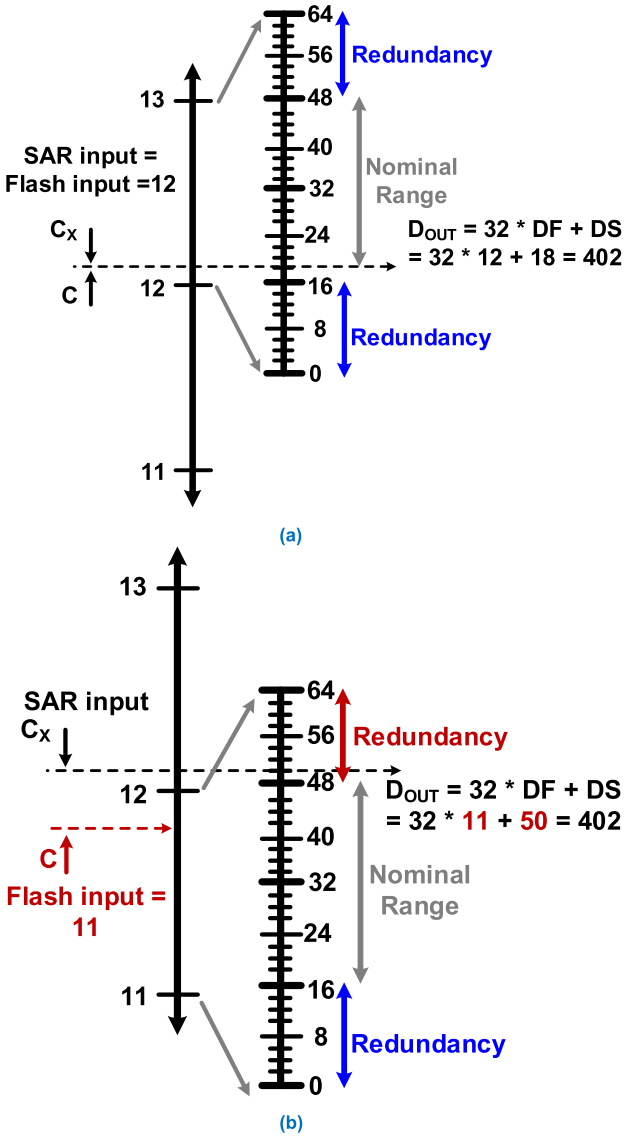

FIGURE 8. Theoretical diagram of the ADC operation (a) ideal case without timing-skew (b) realistic case with timing skew.

place. But, due to added redundancy the final output is correct.

The proposed timing-skew calibration can be explained by the following equations. If we assume the time-skew is not so large and it can be corrected through the SAR ADC redundancy, the output of a complete channel is determined by the SAR ADC's sampled value. Then, the Flash ADCs output and a complete channel output can be represented by the equation (2) and (3) respectively:

$$DF[n] = V_{IN}(nT) + QF[n] \quad (2)$$

$$DC[n] = V_{IN}(nT + \Delta t) + QC[n] \quad (3)$$

where QF[n] denotes the quantization noise and DF[n] denotes the digital output of flash ADC. While the quantization noise and digital output of a channel is represented as QC[n] and DC[n], respectively. The timing-skew between each ADC channel and the Flash ADC is denoted by Δt.

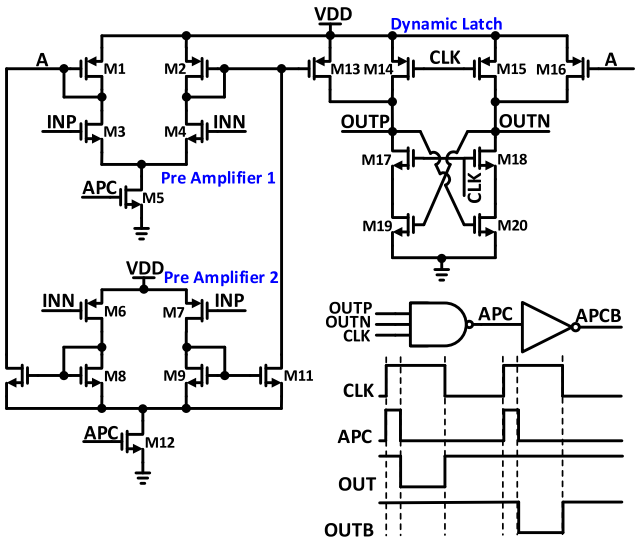

FIGURE 9. The rail-to-rail dynamic latch comparator with modified APC.

The variance of the DS can be written as:

$$\begin{aligned}&\mathrm{VAR}\,[\mathrm{DS}\,[n]]\\&= \mathrm{VAR}\,[\mathrm{DC}\,[n] - \mathrm{DF}\,[n]] \quad (4)\\&= \mathrm{VAR}\,[V_{IN}\,(nT + \Delta t) + \mathrm{QC}\,[n] - V_{IN}\,(nt) - \mathrm{QF}\,[n]] \quad (5)\\&= \mathrm{E}\left[(V_{IN}\,(nT + \Delta t) - V_{IN}\,(nt) + \mathrm{QC}\,[n] - \mathrm{QF}\,[n])^2\right] \quad (6)\\&= \mathrm{E}\left[(V_{IN}\,(nT + \Delta t) - V_{IN}\,(nt))^2\right] + Q^2C,\,\mathrm{rms} + Q^2F,\mathrm{rms} \quad (7)\end{aligned}$$

where Q^2C, rms and Q^2F, rms are the quantization noise power of each channel ADC and the flash ADC. Equation XX shows that the VAR[DS[n]] is a function of Δt and it is minimized when Δt is zero. Above equation also indicated that minimizing VAR[DS[n]] is equivalent to find LMS (least mean square) error approximation between the two signal.

4) DYNAMIC LATCH COMPARATOR WITH MODIFIED ADAPTIVE POWER CONTROL

The comparator is a crucial building block in a medium resolution SAR ADC, because the noise of the comparator dominates the ADC performance. The implemented rail-to-rail dynamic latch architecture of the comparator with modified APC is shown in Figure 9. The comparator architecture implemented in the proposed ADC consists of a dynamic latch, two preamplifiers, and an APC block to increase the decision operation and resolution [23]–[25]. At the input stage, the preamplifier is used to reduce the kickback noise and in addition, to reduce the current consumption of the comparator a modified APC technique is implemented in the comparator. When the comparator output comes, the APC signal turns off the comparator, hence the active time of the comparator reduced by the APC signal, which results in the reduction of the overall power consumption.

Modified APC topology is shown in Figure 9. The implemented APC circuit consists of one inverter and one NAND gate. In the operation of the modified APC block, when the comparison is made, output triggers the APC block. In the reset phase, when the clock is low and the outputs OUTP and OUTN go to high by the reset transistors and the NAND output goes to high. The output of NAND goes to low as the clock is changing from low to high. When the evaluation phase is completed, one output terminal of the comparator is at VDD and another output terminal of the comparator is at VSS, as a result, the NAND gate output goes to high. In the preamplifier, the DC power supply controlling switches invert the NAND output to get the final APC signal, which will be the input to the M5 and M12 transistors.

C. CLOCK GENERATOR AND VBGR CIRCUIT

Figure 10 shows the block diagram of clock generator with the input as clock signal CLK which is provided externally. Programmable delay block corrects the average mismatch between the SAR clocks (C1 - C5) and flash clock (C). These programmable delay blocks have an equal effect on SAR clocks and results in no change in timing skew among them as they are implemented before the clock divider. The delay between the inverters is controlled with the help of a capacitor bank and switches. Capacitance at the output of the first inverter controls the coarse delay while capacitance at the output of the second inverter controls the fine delay. The next two inverters help in recovering the sharpness of the transition edge. A clock divider circuit is used to feed the interleaved SAR channels with divided clocks C1 – C5 as shows in Figure 10. Clock divider circuit is designed with the help of D flip-flops to divide the high frequency clock. Dummy logic gates are used in the Flash clock (C) path to avoid the mismatch between SAR clock and flash clock.

Band-gap reference voltage (VBGR) has been used as input of the reference voltage generator and to compensate the variation and mismatch, trimming controls have been added for each reference voltage. Schematic of BGR is shown in Figure 3. The feedback from Error amplifier tends to keep the same voltage level at the both inputs, R3 generates the voltage difference ΔVBE between two Bipolar Junction Transistors (BJTs) and causes I2b to flow. ΔVBE with proportional to absolute temperature (PTAT) characteristics makes I2b as a current component with the PTAT characteristics. Similarly, the due to the inverse PTAT (IPTAT) characteristics of VBE, the current I2a which flows through R3 behaves as an IPTAT. Therefore, by tuning the resistance component and I2 BJT ratio, a constant current component can be created switch is independent of temperature, and by flowing the current through M6 through mirroring, it is possible to output a constant voltage also for temperature change.

A Soft Start circuit is added to the output, when the Power Enable (PEN) signal is high, a current starts to flow through the PMOSs, M11, M12 and M13 connected in diode fashion. It slowly charges the capacitor C3, then M10‘s gate voltage

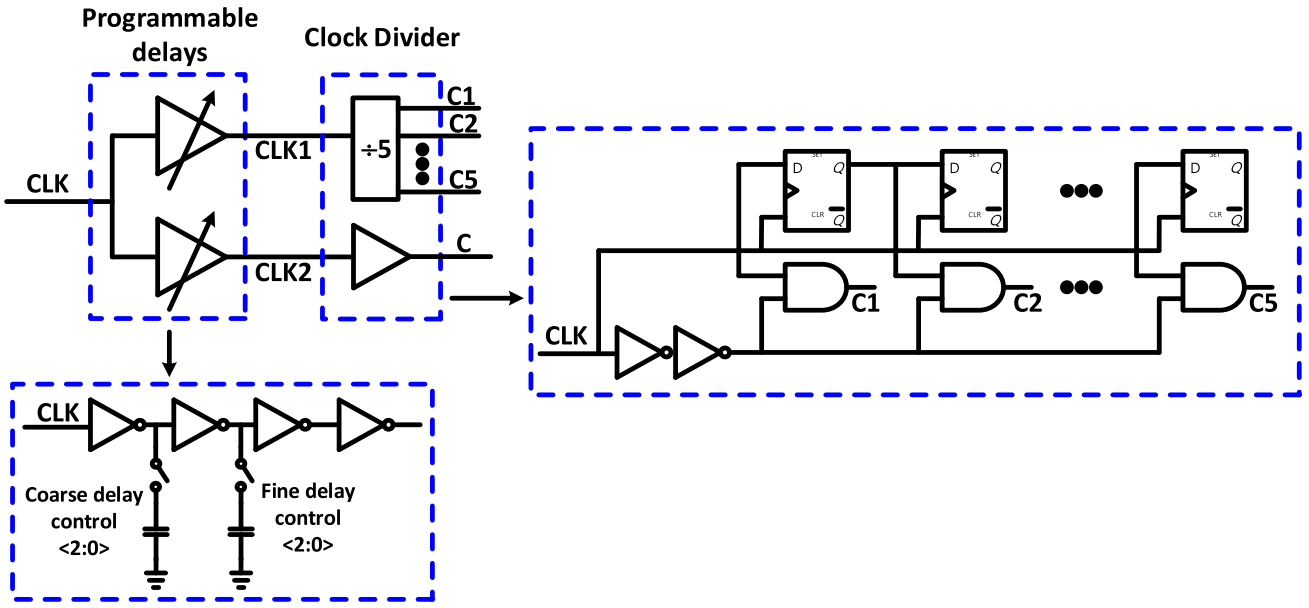

FIGURE 10. Block diagram of clock generator circuit.

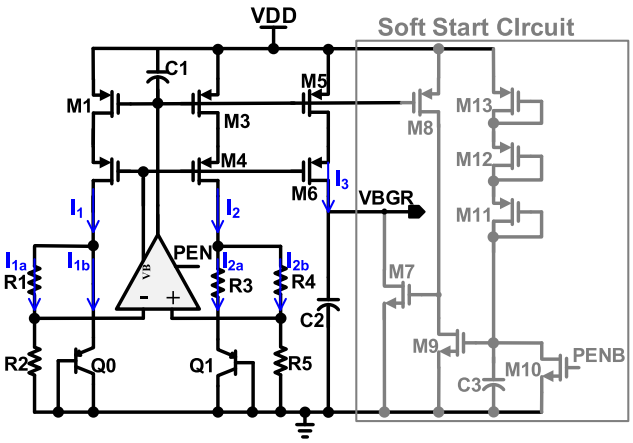

FIGURE 11. Band-gap reference generator schematic.

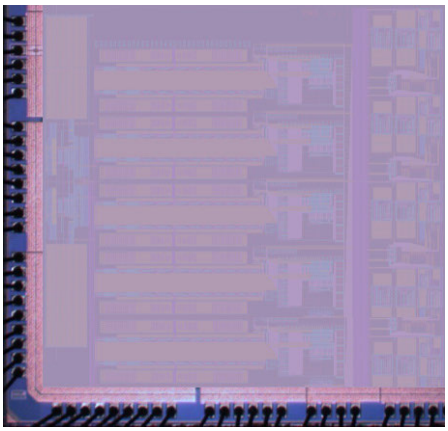

FIGURE 12. Die photograph of the proposed time interleaved hybrid type SAR ADC.

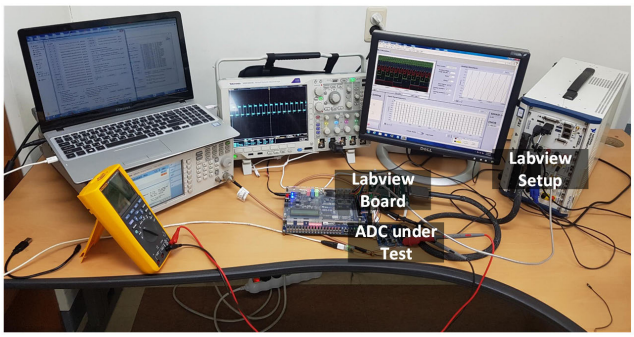

FIGURE 13. Measurement setup for the proposed ADC.

becomes higher or equals than its threshold voltage, and to prevent the BGR peak voltage, BGR output voltage rises.

IV. MEASUREMENT RESULTS

The proposed time interleaved hybrid SAR ADC is fabricated and tested with 130 nm CMOS process. The die photograph and measurement setup is shown in Figure 12 and Figure 13, respectively. The implemented ADC is operated under 1.2 V supply and the differential input range of the ADC is 0.8 Vpp with reference voltages 0.2 V $\sim$ 1 V.

The measured FFT performance without offset and time skew calibration is shown in Figure 14. The ADC performance is limited because of offset error between Flash and SAR channels. However, without offset and time skew calibration, the ADC achieved SNDR of 58.49 dB and effective number of bits (ENOB) of 9.42 bits with input frequency of 20.07 MHz at 80 MS/s sampling speed as shown in Figure 14 (a), and at nyquist rate input frequency 38.98 MHz, it achieved SNDR of 54.38 dB and ENOB of 8.74 bits as shown in Figure 14 (b).

The measured FFT performance with offset and time skew calibration is shown in Figure 15. The error correction of

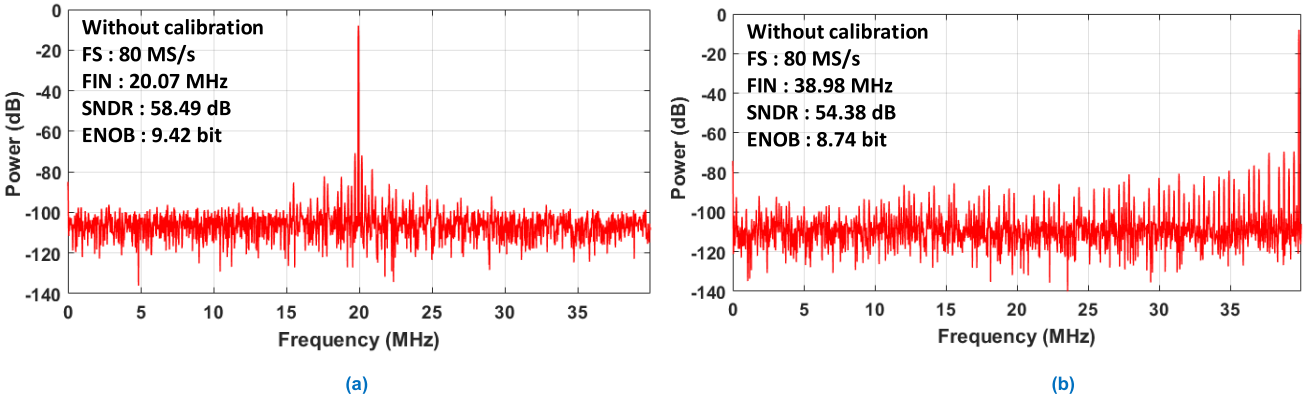

FIGURE 14. Measured FFT spectrum without offset and time skew calibration for different input frequencies at the sampling rate of 80 MS/s (a) for input frequency 20.07 MHz (b) for nyquist input frequency 38.98 MHz.

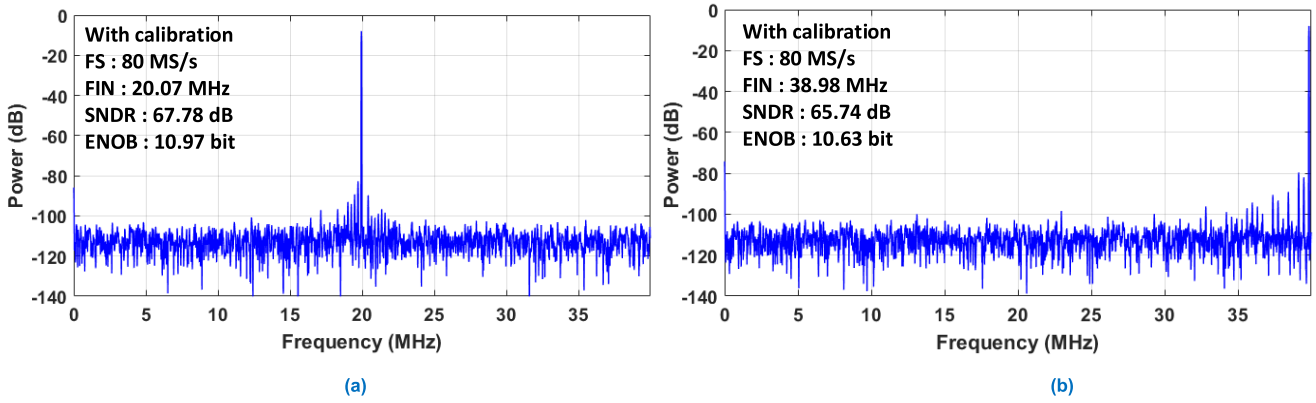

FIGURE 15. Measured FFT spectrum with offset and time skew calibration for different input frequencies at the sampling rate of 80 MS/s (a) for input frequency 20.07 MHz (b) for nyquist input frequency 38.98 MHz.

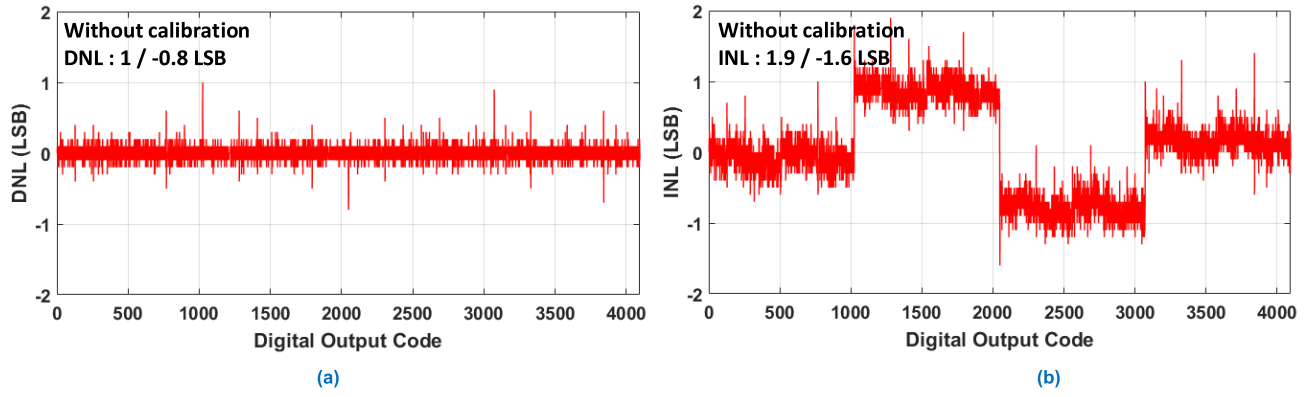

FIGURE 16. Measured static performance without offset and time skew calibration (a) differential non-linearity (DNL) is 1 / −0.8 LSB (b) integral non-linearity (INL) is 1.9 / −1.6 LSB.

ADC is covered with designed redundancy and the mismatch between SAR channels is covered with the time skew calibration and the results are shown in Figure 15. However, with offset and time skew calibration, the ADC achieved SNDR of 67.78 dB and effective number of bits (ENOB) of 10.97 bits with input frequency 20.07 of MHz at 80 MS/s sampling speed shown in Figure 15(a), and at nyquist rate input frequency 38.98 MHz, it achieved SNDR of 65.74 dB and ENOB of 10.63 bits as shown in Figure 15(b).

The measured static performance without offset and time skew calibration is shown in Figure 16. Differential non-linearity (DNL) without calibration is 1 / −0.8 LSB as shown in Figure 16 (a), and integral non-linearity (INL) without calibration is 1.9 / −1.6 LSB and is shown in Figure 16 (b).

The measured static performance of proposed ADC architecture with offset and time skew calibration is shown in Figure 17. The DNL with offset and time skew calibration is 0.6 / −0.4 LSB as shown in Figure 17 (a), and INL with

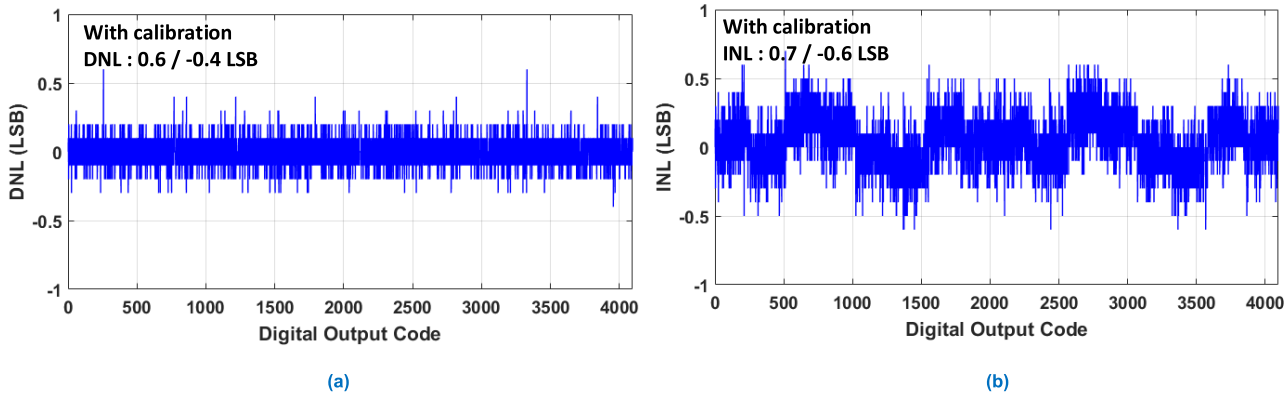

FIGURE 17. Measured static performance with offset and time skew calibration (a) differential non-linearity (DNL) is 0.6 / −0.4 LSB (b) integral non-linearity (INL) is 0.7 / −0.6 LSB.

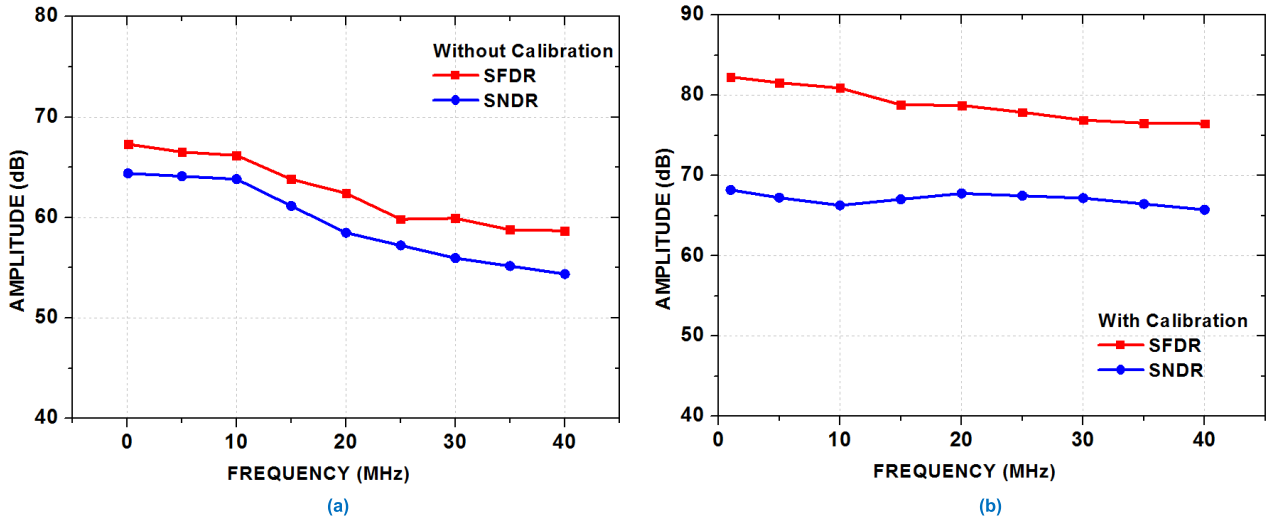

FIGURE 18. Measured SFDR and SNDR levels versus input frequency at 80 MS/s (a) without offset and time skew calibration (b) with offset and time skew calibration.

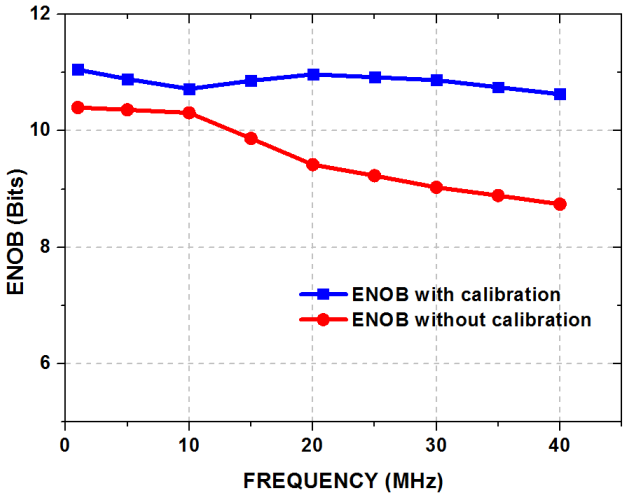

FIGURE 19. Measure ENOB versus input frequency comparison with and without offset and time skew calibration at sampling rate 80 MS/s.

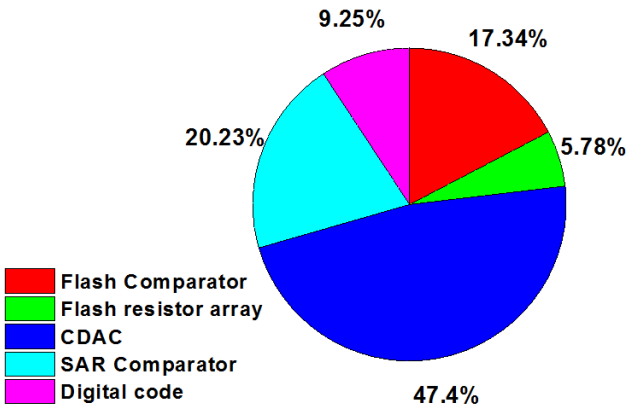

FIGURE 20. Power consumption breakdown of ADC.

offset and time skew calibration is 0.7 / −0.6 LSB and is shown in Figure 17(b).

Figure 18 shows the dynamic performance for the proposed ADC with input frequency sweep with the sampling speed of 80 MS/s. Without offset and time skew calibration, the SNDR is limited below to 65 dB, because of the error between the Flash and ADC and time mismatch between

TABLE 1. Performance summary and comparison.

Parameter	JSSC [13]	IEEE [5]	JSSC [26]	TCAS [27]	IEEE [8]	This work
Technology (nm)	130	40	65	40	130	130
Resolution (bit)	10	12	10.5	12	8	12
Supply (V)	1.2	-	1.2	1.3 V	-	1.2
Sampling Rate (MS/s)	40	600	100	125	1000	80
SNDR (dB)	50.6	61.7	56.6	62.98	46.16	67.78
ENOB (bit)	8.11	9.95	9.11	10.17	7.37	10.97
DNL (LSB)	0.72 / -0.78	-	-	0.51 / -0.55	-	0.6 / -0.4
INL (LSB)	0.90 / -1.5	-	-	0.80 / -0.85	-	0.7 / -0.6
Power (mW)	550 µ	23	2.46	10.71	13.29	7.08
FOM (fJ/step)	50	38.7	44.5	74.4	80.3	44.12
On-chip calibration	-	Yes	-	Yes	Yes	Yes

SAR channels and is shown in Figure 18 (a). However after offset and time skew calibration, the proposed prototype of hybrid time interleaved ADC achieved more than 65 dB of SNDR upto nyquist frequency and is shown in Figure 18 (b). Figure 19 shows the measured ENOB trend at different input frequencies by sweeping the input frequency of ADC with and without offset and time skew calibration at the sampling rate of 80 MS/s. The power breakdown of ADC is represented in Figure 20.

The measured performance summary of the proposed: hybrid type time interleaved ADC and comparison with the other state-of-the art ADC structures [5], [8], [13], [26], and [27] is shown in Table 1. Figure-of-merit (FOM), and resolution at different sampling rates is essential to compare the presented hybrid type time interleaved 12-bit, 80 MS/s ADC to compare with the other ADCs. The formula to calculate the FOM is given as [1]:

$$\text{FOM} = \frac{\text{Power}}{\min\{\text{F}_\text{S}, 2 \times \text{ERBW}\}2^{\text{ENOB}}} \tag{8}$$

where, Power represents the power consumption of the ADC architecture, FS represent the sampling rate of ADC, and ERBW is the effective resolution bandwidth.

The proposed hybrid time interleaved ADC achieves a FOM of 44.12 fJ/step. The power consumption of the proposed structure includes a Flash ADC and 5 channels time interleaved SAR ADC with redundancy, comparator offset and time skew calibration.

V. CONCLUSION

The proposed paper presents a hybrid type 12-bit, 80 MS/s, time interleaved SAR ADC with comparator offset and time-skew calibration. The implemented ADC prototype is fabricated in 130 nm CMOS process. The proposed time-skew calibration is implemented to minimize the discrepancy between the output of Flash ADC and SAR ADC's channels. To rectify the decision error of the Flash ADC and extract the time-skew information, 1-bit redundancy is included in the CDAC of the SAR conversion. To solve the offset mismatch between SAR ADC and Flash ADC and within the SAR ADC channels, all comparators are calibrated to minimize their absolute offset by utilizing background offset calibration. The modified dynamic strong ARM comparator is used for Flash ADC and dynamic latched comparator is used for SAR ADCs. For fine offset calibration and low power consumption, the comparator offset calibration circuit is implemented. The decision error between the Flash ADC and SAR ADC is covered with designed redundancy and the mismatch between the ADCs is covered with the time-skew calibration. To enhance the overall energy efficiency and for fast operation, a rail-to-rail dynamic latch comparator with modified APC circuit is used. The implemented prototype of the ADC with 80 MS/s sampling rate and 1.2 V power supply achieves the ENOB of 10.97 bits and SNDR of 67.78 dB in the measurement. The FoM of the proposed architecture is 44.12 fJ/ step.

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