IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received August 27, 2021, accepted September 13, 2021, date of publication September 24, 2021, date of current version October 11, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3115660

A Switched-DC Source Sub-Module Multilevel Inverter Topology for Renewable Energy Source Applications

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This work was supported in part by the Agencia Nacional de Investigación y Desarrollo (ANID) through the Project Fondo Nacional de Desarrollo Científico y Tecnológico (FONDECYT) under Grant 1191028 and Grant FONDAP SERC Chile 15110019.

ABSTRACT This article presents a sub-module topology for switched DC source cascaded multilevel inverter configurations that require fewer switching devices and can generate a high number of voltage levels that are suitable for renewable energy sources. The proposed sub-module topology comprises eight semiconductor switches and four DC voltage sources that generate fifteen voltage levels. Furthermore, the cascaded topology is presented to increase the output voltage levels and to minimize the number of components. The proposed sub-module inverter and its cascaded topology are compared with several multilevel inverters to indicate the advantages and drawbacks of the proposal. The comparison studies show that the proposed topologies require fewer switching devices and gate drivers in comparison with other multilevel inverter topologies. In addition, the proposed cascaded topology reduces the cost of the inverter when compared to other multilevel inverter configurations. Furthermore, the power loss calculations and the implementation of the proposed topology in grid-connected photovoltaic applications are simulated and analyzed. Finally, the performance of the proposal is verified by simulation and experimental results for both symmetric and asymmetric sub-module topologies as well as for the proposed cascaded topology.

INDEX TERMS DC-AC power converters, multilevel inverters, grid-connected PV inverters, photovoltaic systems, renewable energy sources.

I. INTRODUCTION

Multi-level inverter (MLI) technology is developing quickly due to several advantages over conventional two-level inverters. These topologies are capable of generating low voltage total harmonic distortion (THD) by increasing the number of voltage levels. Furthermore, MLI topologies reduce the voltage rating of power switches by sharing the DC link voltage on power switches, and they can operate at low switching frequencies for a given output waveform quality. As a result, MIL can be used in grid-connected applications such as Photovoltaic (PV) Systems, Wind, Fuel Cell, Flexible Alternating Current Transmission System (FACTS) devices, and Electrical Vehicles (EV) [1]–[4]. The basic operation principles of MLIs can be found in the neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) configurations [5]–[7].

The cascaded MLI configurations in the literature have been presented in three categories: switched DC source multilevel inverters (SDC-MLIs), switched-diode multilevel inverters (SD-MLIs), and switched capacitor multilevel inverters (SC-MLIs). The SDC-MLIs use multiple independent DC voltage sources, the SD-MLIs use lots of discrete diodes which are replaced by switches and SC-MLIs use

The associate editor coordinating the review of this manuscript and approving it for publication was Md. Rabiul Islam.

several capacitors with one DC source to reduce the number of power switches [8]–[11]. In this article, the focus is on the presented topologies of SDC-MLIs, with the weaknesses and strengths being discussed in the following. To achieve a large number of voltage levels, all types of multilevel inverters and their cascaded topologies require a high number of components which causes some technical issues, such as: increasing the final system cost, increasing the probability of device failure, and requiring a switch to each driver circuit. To overcome these issues, there has been carried out the design of alternative MLI configurations [8]–[11]. These configurations lead to a reduction in the active component count over conventional cascaded MLI configurations. Several reduced single-phase SDC-MLI configurations have been published in the literature [12]–[16]. An improved configuration of the modified T-type inverter has been presented by Samadaei et. al. in [12], which generates seventeen-levels in asymmetrical mode with a reduced number of switches in the symmetrical pattern in comparison with other MLIs. The benefit of this topology is, low voltage stress because using bidirectional power switches. Despite the fact that this MLI generates a large number of levels (17), the number of power switches, driver circuits and DC sources remains high. The presented structure by Samadaei et. al. [13] is an advanced topology [12] called a K-type inverter. The K-type MLI generates 13 voltage levels with 14 switches, 11 drivers, 2 unequal DC sources and 2 capacitors. This topology aimed to reduce the amount of DC power supplies by replacing two capacitors with two DC power supplies. The drawback of this topology is a high number of components (IGBTs, drivers) when a large number of levels are needed. Furthermore, the number of On-switches is high, resulting in high conduction losses. In [14], Alishah et. al. have recommended a topology based on a developed H-bridge module for general multilevel inverter topologies. The benefit of this MLI is a reduction in the number of components as well as reduced voltage stress of the switches. The topology presented in [14] is a general topology that can operate in both symmetric and asymmetric modes. The benefit of this topology is the use of bidirectional switches to reduce voltage stress, but it still requires a large number of DC sources and components when a large number of levels are required. In [15] by Sathik et. al., a reduced generalized multilevel converter topology has been presented based on a basic unit which is able to develop as two states (extended basic unit and cascade connection) to decrease blocking voltage and components. The given basic unit of this topology is an asymmetric structure and uses 10 unidirectional power switches and 4 DC power supplies to generate 9-level. Using 10 switches to produce 9 levels is a large number of switches that results in the need for a complex modulation technique. In [16], by Sathik et. al. A SDC-MLI structure has been presented with the same circuit as in [15]. This topology was developed for the asymmetric topology to increase the number of voltage levels from 9-level to 17-level using the same components. This topology uses two unidirectional switches instead of one bidirectional switch to reduce the voltage stress. Although this MLI decreases the voltage stress, it requires a high quantity of components to produce high voltage levels.

In addition to the discussed above MLIs, recently, new multilevel inverters have been presented based on different objectives: reduced switches count, reduced DC sources, the reduced voltage stress on power switches, etc.) [17]–[21]. In [17]–[21], five different 15-level reduced MLI configurations have been reported. Siddique *et al.*'s presented reduced MLI topology in [17] that handles ten power switches to switch three DC sources to make fifteen-voltage levels. The drawback of this topology is using a high number of switches. A modular topology for symmetric MLI configurations has been presented by Nasiri et. al. in [18]. It uses ten switches (bidirectional and unidirectional) and seven DC sources to make 15-level. The disadvantage of this topology is the large number of DC sources; in a real application each DC source requires a capacitor which increases the system's power loss. A modified packed U-cell multilevel inverter has been presented by Hosseinzadeh et. al. in [19] which reduced the number of switches to generate fifteen voltage levels. The drawback of this topology is that it cannot handle the backflow current due to the use of diodes in its circuit. Presented topology by Majumdar et. al. in [20] combines a classical five-level T-type inverter with a three-level H-bridge inverter to reduce voltage stress on the switches. It requires nine power switches with four extra diodes. A cascaded multilevel inverter topology based on an extendable basic unit has been developed by C. Dhanamjayulu et. al. in [21]. This multilevel inverter is a symmetric topology that uses an H-bridge converter to change the polarity of the output voltage. The H-bridge inverter that is used should endorse the maximum output voltage magnitude that leads to an increase in the power losses and cost of the inverter. Using two basic units of this topology, with 16 power switches and 7 DC sources, it can produce 15-level. Therefore, this MLI requires a high number of components making it less efficient and unaffordable.

Regarding switched capacitor MLIs, a new K-type MLI has been reported by Zeng et. al in [22]. This topology handles one DC source and four capacitors with ten power switches to generate 13-level. The benefit of this MLI is the self-balancing of the capacitor's voltages; it still needs a high number of switching devices. Bana et. al have introduced two hybrid MLI configurations in [23]. These hybrid MLIs can make 13-level and 19-level with nine and eleven power switches with six DC-sources and one capacitor, respectively. Khan et. al have developed a symmetric step-up switch capacitor MLI in [24] that creates 2n+1 voltage levels. The benefit of this MLI is the self-balancing of capacitors and using one DC source; in contrast, it uses a high number of power switches and capacitors to generate a high number of levels.

This article aims to propose a new symmetric and asymmetric switched DC source MLI using fewer switching devices and gate drivers making the control system of the proposed topology simpler. The different arrangements of

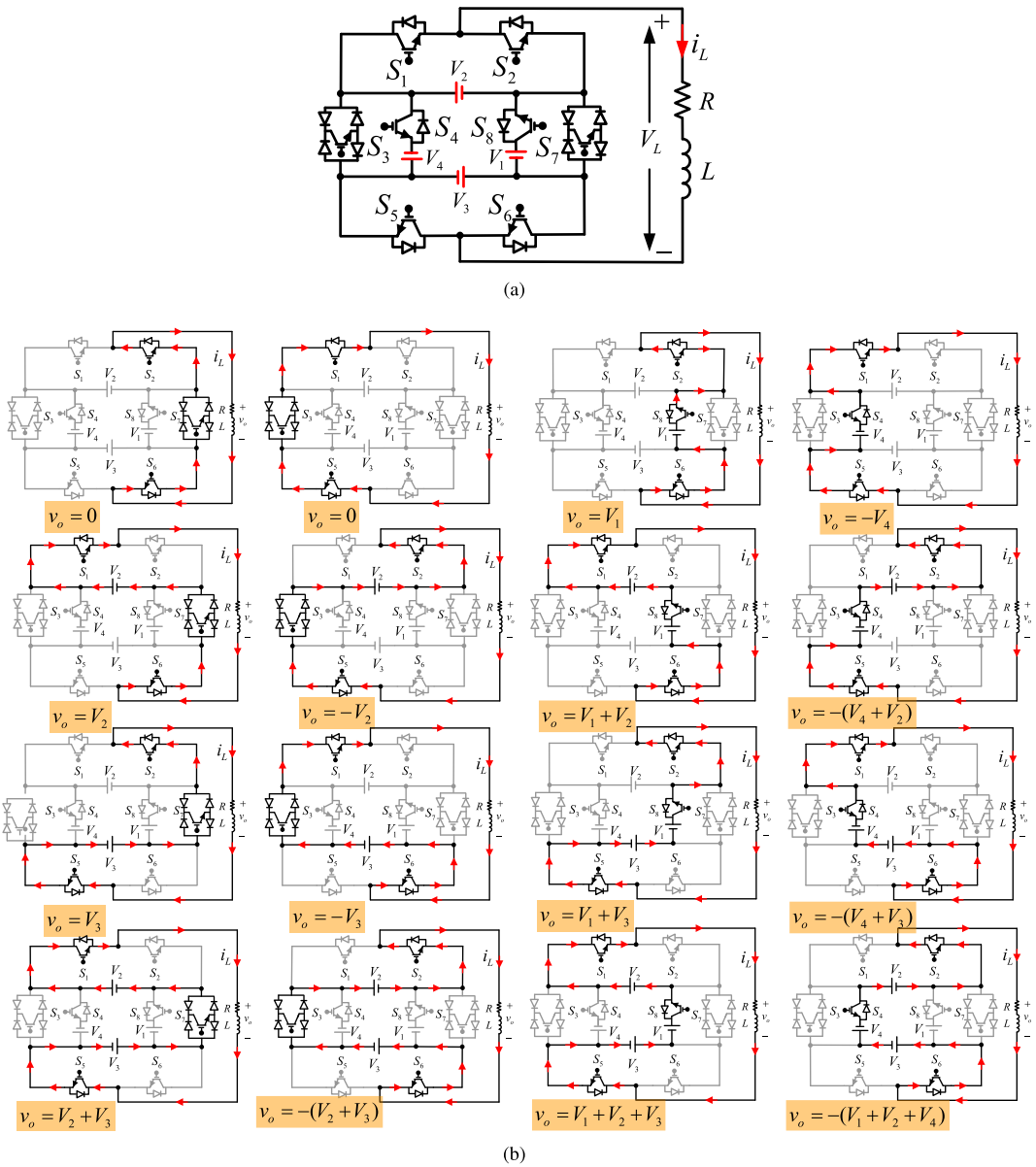

FIGURE 1. (a) Proposed sub-module topology; (b) all operation modes of sub-module inverter.

DC power supplies are presented for the extended cascaded topologies. The comparison studies are performed in terms of the number of elements (switches, drivers, diodes), isolated DC power supplies, and total blocking voltages. The power loss analysis of the proposed topology, the grid-connected PV application, and selection of power switch voltage rating are discussed. Finally, simulation and experimental results are presented to validate the proposal.

II. PRINCIPLE OPERATION OF THE PROPOSED SUB-MODULE TOPOLOGY

A. CIRCUIT DESCRIPTION

Fig. 1(a) indicates the power circuit of the proposed sub-module topology. As can be seen from this figure, the numbers of switches and DC power supplies in the proposed topology are eight and four, respectively. The type of power switches $S_1, S_2, S_4, S_5, S_6, S_8$ in the proposed topology are unidirectional, along with an insulated gate bipolar transistor (IGBT) and an anti-parallel diode while two power switches S_3, S_7 are bidirectional each with an IGBT and four diodes to conduct the back-flow current in both directions. The circuit of the proposed asymmetric sub-module topology is designed in such a way that only three DC supplies of V_1, V_2, V_3 can combine to generate positive levels. The DC power supply of V_4 is used for making more negative levels, and it connects with V_2 and V_3 but cannot connect with V_1 due to short-circuiting.

B. OPERATION MODES

The proposed topology has various operating modes that are generated by the activation of the different switching devices. Fig. 1(b) shows the operation modes for the proposed

TABLE 1. All Switching States of the Proposed 15-level Sub-Module Topology.

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_L	
1	1	0	1	0	1	0	0	0	0	0
2	0	1	0	0	0	1	1	0		
3	0	1	0	0	0	1	0	1	V_1	V_{dc}
4	1	0	0	0	0	1	1	0	V_2	$2V_{dc}$
5	1	0	0	0	0	1	0	1	V_1+V_2	$3V_{dc}$
6	0	1	0	0	1	0	1	0	V_3	$4V_{dc}$
7	0	1	0	0	1	0	0	1	V_1+V_3	$5V_{dc}$
8	1	0	0	0	1	0	1	0	V_2+V_3	$6V_{dc}$
9	1	0	0	0	1	0	0	1	$V_1+V_2+V_3$	$7V_{dc}$
10	1	0	0	1	1	0	0	0	$-V_4$	$-V_{dc}$
11	0	1	1	0	1	0	0	0	$-V_2$	$-2V_{dc}$
12	0	1	0	1	1	0	0	0	$-(V_2+V_4)$	$-3V_{dc}$
13	1	0	1	0	0	1	0	0	$-V_3$	$-4V_{dc}$
14	1	0	0	1	0	1	0	0	$-(V_3+V_4)$	$-5V_{dc}$
15	0	1	1	0	0	1	0	0	$-(V_2+V_3)$	$-6V_{dc}$
16	0	1	0	1	0	1	0	0	$-(V_2+V_3+V_4)$	$-7V_{dc}$

TABLE 2. Magnitudes of DC Power Supplies for the Proposed Sub-Module Topology.

Methods	$\mathbf{V}_1$	$\mathbf{V}_2$	$\mathbf{V}_3$	$\mathbf{V}_4$	$\mathbf{V}_{omax}$	$\mathbf{N}_L$
$\mathbf{M}_{1sub}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$3V_{dc}$	$7-Level$
$\mathbf{M}_{2sub}$	V_{dc}	$2V_{dc}$	V_{dc}	V_{dc}	$4V_{dc}$	$9-Level$
$\mathbf{M}_{3sub}$	V_{dc}	$2V_{dc}$	$2V_{dc}$	V_{dc}	$5V_{dc}$	$11-Level$
$\mathbf{M}_{4sub}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	V_{dc}	$6V_{dc}$	$13-Level$
$\mathbf{M}_{5sub}$	V_{dc}	$2V_{dc}$	$4V_{dc}$	V_{dc}	$7V_{dc}$	$15-Level$

sub-module topology (corresponding to Table 1). Table 1 gives the synthesis of the state of the switches to generate each level, where the 16 switching states are shown by the different on and off switches. As can be seen in Table 1, there is one redundancy for making zero levels. Some of the operation modes of the proposed topology are explained as follows:

There are two states for generating zero levels in the first mode, so switches S_1, S_3, S_5 or S_2, S_6, S_7 are turned on to generate zero levels.

The second mode is for generating $\pm V_{dc}$, so by turning on the three switches S_2, S_6, S_8 the voltage level of $-V_{dc}$ is created, and for generating $-V_{dc}$ the three switches S_1, S_4, S_5 are turned on.

In the sixteenth mode for generating the maximum voltage level in positive and negative $\pm 7V_{dc}$, switches S_1, S_5, S_8 are turned on for generating the voltage level of $+7V_{dc}$, and for generating $-7V_{dc}$ the switches S_2, S_4, S_6 are turned on. From this mode, it is clear that all DC voltages ($V_1 + V_2 + V_3$) are summed together to create maximum voltage levels. Similarly, the remaining levels are obtained based on a valid switching pattern as given in Table 1.

Dependent on the choosing magnitudes of DC power supplies, the proposed topology can generate different voltage levels, however, the sub-module topology creates seven voltage levels in symmetric mode by considering the same magnitudes of DC power supplies of ($V_1 = V_2 = V_3 = V_4 = V_{dc}$). The 9, 11, 13, and maximum 15 voltage levels are obtained in asymmetric modes by considering the magnitudes of the DC power supplies differently, as shown in Table 2.

C. TOTAL BLOCKING VOLTAGE

The maximum total blocking voltage (TBV) is an essential factor in the design of multilevel inverter topologies. The maximum TBV in the proposed sub-module topology is the sum of the blocking voltages in which the power switches suffer. The maximum TBV of the proposed sub-module topology is obtained as follows:

$$TBV_{sub} = V_{S1} + V_{S2} + \ldots + V_{S8} \tag{1}$$

The magnitude of the maximum blocking voltage on each switch is:

$$V_{S1} = V_{S2} = V_2 \tag{2}$$
$$V_{S3} = V_1 + V_2 + V_4 \tag{3}$$
$$V_{S4} = 2V_1 + V_2 + V_4 \tag{4}$$
$$V_{S5} = V_{S6} = V_3 \tag{5}$$
$$V_{S7} = V_1 + V_2 + V_3 \tag{6}$$
$$V_{S8} = 2V_1 + V_2 + V_3 \tag{7}$$

According to the magnitudes of the maximum blocking voltage by each switch, the value of the maximum TBV for the proposed sub-module topology is obtained as:

$$TBV_{sub} = \sum_{i=1}^{8} V_{Si} = 6(V_1 + V_2 + V_3) \tag{8}$$

The value of TBV can be rewritten according to the number of levels of the proposed sub-module topology as follows:

$$TBV_{sub} = 3(N_{level} - 1) \tag{9}$$

III. EXTENDED CASCADED CONFIGURATIONS

A cascaded topology is the connection of an n number of sub-module topologies as series. Then, the output voltage is obtained by the sum of the output voltage of each sub-module topology. The proposed cascaded topology based on the sub-module topology is indicated in Fig. 2. The cascaded topologies are separated into two configurations: symmetric and asymmetric topologies. In this way, the proposed cascaded topologies based on the proposed sub-module topology are analyzed in two shapes: symmetric and asymmetric. In the symmetric cascaded topology, the magnitudes of all DC supplies are equal to each other. As mentioned in section II, the proposed sub-module topology generates 7-level in the symmetric mode. Therefore, the number of levels for symmetric cascaded topology is expressed as follows:

$$N_L = 6n + 1 \tag{10}$$

Here n is the number of the sub-module topology.

In an asymmetric cascaded topology, the magnitudes of all DC supplies are different. Depending on the choosen methods of determination of DC supplies, the proposed cascaded topology generates different voltage levels. Table 3 gives the

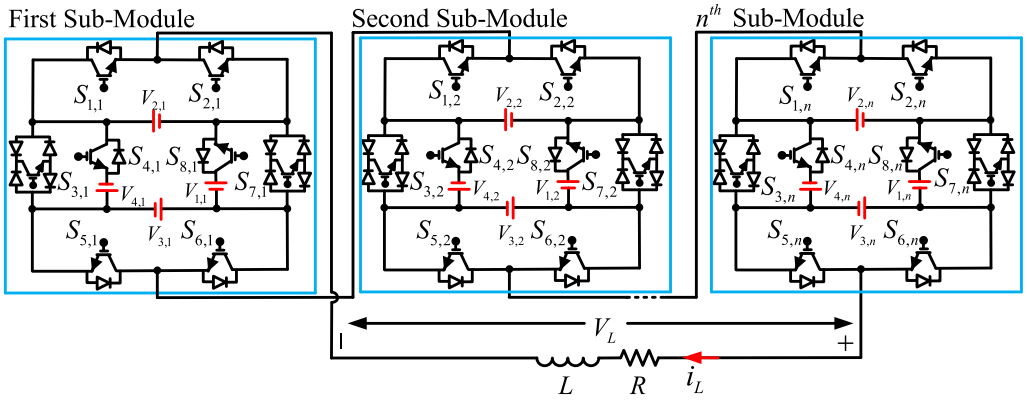

FIGURE 2. Power circuit of single-phase proposed cascaded topology.

TABLE 3. Magnitudes of DC Supplies for the Proposed Cascaded Topology.

Methods	Magnitudes of DC Supplies for j $= 1, 2, \cdots, n$	$\mathbf{V}_{omax}$	$\mathbf{N}_L$	$\mathbf{V}_{block}$
$\mathbf{M}_{1Cas}$ ($\mathbf{M}_1$)	$V_{1j} = V_{2j} = V_{3j} = V_{4j} = V_{dc}$	$3nV_{dc}$	$6n+1$	$3(N_L-1)$
$\mathbf{M}_{2Cas}$	$V_{1j} = V_{4j} = V_{dc}, V_{2j} = 2V_{dc}, V_{3j} = 4V_{dc}$	$[(15n-2)/2]V_{dc}$	$15n-1$	$3(N_L-1)$
$\mathbf{M}_{3Cas}$	$V_{1j} = V_{2j} = V_{3j} = V_{4j} = 7^{j-1}V_{dc}$	$[(7^n-1)/2]V_{dc}$	7^n	$3(N_L-1)$
$\mathbf{M}_{4Cas}$	$V_{1j} = V_{3j} = V_{4j} = 9^{j-1}V_{dc}, V_{2j} = 2(9^{j-1})V_{dc}$	$[(9^n-1)/2]V_{dc}$	9^n	$3(N_L-1)$
$\mathbf{M}_{5Cas}$	$V_{1j} = V_{4j} = 11^{j-1}V_{dc}, V_{2j} = V_{3j} = 2(11^{j-1})V_{dc}$	$[(11^n-1)/2]V_{dc}$	11^n	$3(N_L-1)$
$\mathbf{M}_{6Cas}$	$V_{1j} = V_{4j} = 13^{j-1}V_{dc}, V_{2j} = 2(13^{j-1})V_{dc}, V_{3j} = 3(13^{j-1})V_{dc}$	$[(13^n-1)/2]V_{dc}$	13^n	$3(N_L-1)$
$\mathbf{M}_{7Cas}$ ($\mathbf{M}_2$)	$V_{1j} = V_{4j} = 15^{j-1}V_{dc}, V_{2j} = 2(15^{j-1})V_{dc}, V_{3j} = 4(15^{j-1})V_{dc}$	$[(15^n-1)/2]V_{dc}$	15^n	$3(N_L-1)$

TABLE 4. All Required Parameters of Presented Multilevel Inverters for Comparison Study Correspond to DC Power Supplies Magnitude.

Topologies	Methods	$\mathbf{N}_{IGBT}$	$\mathbf{N}_{Switch}$	$\mathbf{N}_{Diode}$	$\mathbf{N}_{DC}$	$\mathbf{N}_{Variety}$	TBV(p.u)
NPC	R1	$2(N_L-1)$	$2(N_L-1)$	$3N_L-1$	$(N_L-1)/2$	1	$2(N_L-1)$
FC	R2	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	N_L-2	1	$2(N_L-1)$
CHB	R3	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	1	$2(N_L-1)$
	R4	$4[\log_2^{(N_L+1)}-1]$	$4[\log_2^{(N_L+1)}-1]$	$4[\log_2^{(N_L+1)}-1]$	$[\log_2^{(N_L+1)}]-1$	$[\log_2^{(N_L+1)}]-1$	$2(N_L-1)$
	R5	$4\log_3^{N_L}$	$4\log_3^{N_L}$	$4\log_3^{N_L}$	$\log_3^{N_L}$	$\log_3^{N_L}$	$2(N_L-1)$
(BUMLI)	R6	$6[(N_L-3)/5]+3$	$6[(N_L-3)/5]+3$	$6[(N_L-3)/5]+3$	$[(N_L-3)/2]+3$	1	$(7N_L-2)/2$
[8]	R7	$5[\log_2^{(N_L+5)}]-9$	$5[\log_2^{(N_L+5)}]-9$	$5[\log_2^{(N_L+5)}]-9$	$3[\log_2^{(N_L+5)}]-8$	$[\log_2^{(N_L+5)}]-2$	$(10N_L-9)/3$
(ST-Type)	R8	$12[(N_L-1)/8]$	$11[(N_L-1)/8]$	$12[(N_L-1)/8]$	$(N_L-1)/2$	2	$5(N_L-1)/2$
[12]	R9	$12\log_{17}^{N_L}$	$11\log_{17}^{N_L}$	$12\log_{17}^{N_L}$	$4\log_{17}^{N_L}$	$2\log_{17}^{N_L}$	$5(N_L-1)/2$
(K-Type)	R10	$14[(N_L+6)/8]$	$11[(N_L+6)/4]$	$14[(N_L+6)/4]$	$(N_L+6)/4$	2	$4(N_L+6)$
[13]	R11	$14[(N_L+10)/12]$	$11[(N_L+10)/6]$	$14[(N_L+10)/6]$	$(N_L+10)/6$	$(N_L+10)/6$	$16[(N_L+10)/6]$
(EMLC)	R12	$10[(N_L-1)/8]$	$8[(N_L-1)/8]$	$10[(N_L-1)/8]$	$(N_L-1)/2$	1	$9[(N_L-1)/4]$
[14]	R13	$10\log_{17}^{N_L}$	$8\log_{17}^{N_L}$	$10\log_{17}^{N_L}$	$4\log_{17}^{N_L}$	$2\log_{17}^{N_L}$	$9[(N_L-1)/4]$
(BUMLC)	R14	$10[(N_L-1)/8]$	$10[(N_L-1)/8]$	$10[(N_L-1)/8]$	$(N_L-1)/2$	1	$9[(N_L-1)/4]$
[15], [16]	R15	$10\log_{17}^{N_L}$	$10\log_{17}^{N_L}$	$10\log_{17}^{N_L}$	$4\log_{17}^{N_L}$	$2\log_{17}^{N_L}$	$9[(N_L-1)/4]$
Proposed	**M1**	$8[(N_L-1)/6]$	$8[(N_L-1)/6]$	$14[(N_L-1)/6]$	$4[(N_L-1)/6]$	1	$3(N_L-1)$
	M2	$8\log_{15}^{N_L}$	$8\log_{15}^{N_L}$	$8\log_{15}^{N_L}$	$4\log_{15}^{N_L}$	$3\log_{15}^{N_L}$	$3(N_L-1)$

proposed arrangements for the magnitudes of DC supplies. In this Table the recommended quantities of DC supplies arrange from the minimum number to the maximum number of voltage levels, which the suggested cascaded topology can create. For example, if two asymmetric sub-module topologies are connected as cascades, the total number of levels is 29-level (M_{2Cas}) which means 14 positive levels, 14 negative levels, and zero levels. In the seventh proposed method (M_{7Cas}), each series sub-module topology makes different 15 voltage levels, which means the first module creates 15-level and the second module produces 15-level with different magnitude. Consequently, this arrangement can make 15^{j-1} voltage levels.

The proposed sub-module topology, CHB, and presented MLI topologies in, [12]–[16], requires several independent DC power supplies in the input. There are different methods for supplying the input DC sources of the proposed topology, some of which are illustrated in Fig. 3. Two regulation

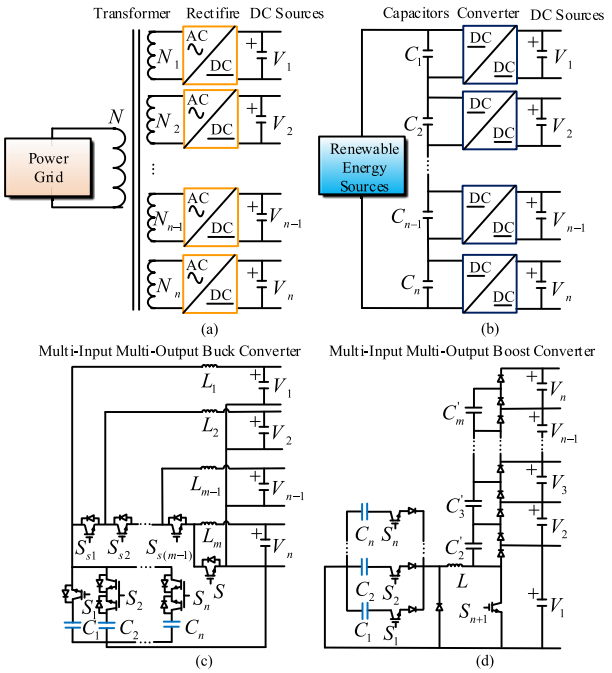

FIGURE 3. DC-link regulation systems; (a) multi-tap transormer; (b) DC/DC converters; (c) multi-input multi-output buck converter; (d) multi-input multi-output boost converter.

DC-link systems have been presented for the first time in [25], [26] to generate distinct DC voltage source magnitudes. It is worth mentioning, the improved regulated DC-link Fig. 3(a) was resented in [30] and was suggested for a medium voltage DC link. The presented first system (Fig. 3(a)) comprises an AC voltage source which can be a local power grid, a multi-tap transformer and a diode-bridge rectifier circuit along with DC capacitors that are usually used for motor drive applications. The second system (Fig. 3(b)) uses several independent DC/DC converters which are suitable for renewable energy applications such as wind, solar, fuel cell, etc.

The third and fourth systems (Figs. 3(c) and 3(d)) have been presented in [28], [29] which are multi-input and multi-output buck and boost converters which are also suitable for renewable energy applications. Hence, we recommend these systems (depending on the application) to regulate the input DC-link of the proposed topology. It should be noted that the objective of this article is to present a new sub-module topology for the multilevel inverter configurations, not a method to supply the DC-link voltage in the multilevel inverters.

IV. COMPARISON OUTCOMES

To demonstrate the proposed topologies' strengths and weaknesses, a comprehensive study was conducted among the proposed topologies, CHB, and other published MLIs [8] and [12]–[16]. The comparative study was performed in terms of the number of IGBTs, switches, discrete diodes, DC power supplies, capacitors, on-state switches, the variety of DC power supplies, and the magnitude of TBV to endorse the new capabilities of the proposed topologies in competition with other MLIs. Table 4 summarizes all parameters of proposed cascaded MLIs and other cascaded MLIs that are used for the comparison. The number of required IGBTs in each MLI for both symmetric and asymmetric DC sources to make the various numbers of voltage levels are represented in Fig. 4(a). As one can see in Fig. 4(a), the proposed topologies (M1 and M2) diminish the number of IGBTs compared to other MLIs to produce the same voltage levels. The number of required power switches (gate drivers) in each topology for both modes of symmetric and asymmetric to create different number levels are exhibited in Fig. 4(b). According to the figure, it is apparent that the proposed topologies use fewer power switches to create the maximum number of levels. The comparison of the number of power diodes versus the number of levels for all MLI topologies is shown in Fig. 4(c). As can be seen from this figure, the proposed topology requires a lower number of diodes than other topologies. Fig. 4(d) exhibits the required number of DC power supplies to generate different voltage levels in all presented MLI topologies. Concerning this figure, in the asymmetric mode, after CHB (R4, R5), and reported MLIs [14]–[16], the proposed topology (M2) requires a minimum number of DC power supplies to create the same voltage levels as other MLIs. The minimum value of the DC voltage source in the symmetric mode belongs to the presented MLI in [13].

One of the factors that impact the cost of cascaded multilevel inverters is the variety of DC power supplies. This factor has been introduced in [8] for the first time. After that, it has been used in other publications for comparison. $N_{variety}$ is the variety of DC power supplies or the number of different voltage magnitudes of the used DC power supplies in cascaded multilevel inverters. Fig. 4(e) indicates the variety of DC power supply values for all MLI topologies versus different voltage levels. In the symmetric mode, all MLI topologies have the same value of 1.0 except [12], [13], which has a high value of 2.0. In the asymmetric case, [17] (R6) has a low value, and the proposed topology (M2) and [12], [14], [15], [16] have almost the same value and CHB (R4, R5) and [12] possess a maximum value than other MLI topologies.

Fig. 4(f) presents the variation of the maximum total blocking voltage versus the different levels in all topologies. According to this figure, in the symmetric and asymmetric modes, the proposed topology has a reduced (TBV) value and it has a low value close to four recent presented topologies [12] and [14]–[16].

Further, to the above comparison, the proposed asymmetric sub-module topology is compared with other MLIs in aspects of required component counts to make fifteen voltage levels. Noted, some MLIs cannot generate exactly 15-level, they can generate 13 and 17 levels that are close to 15-level. As depicted in Table 5, the proposed asymmetric inverter requires a lower number of switching devices and gate drivers than other MLIs.

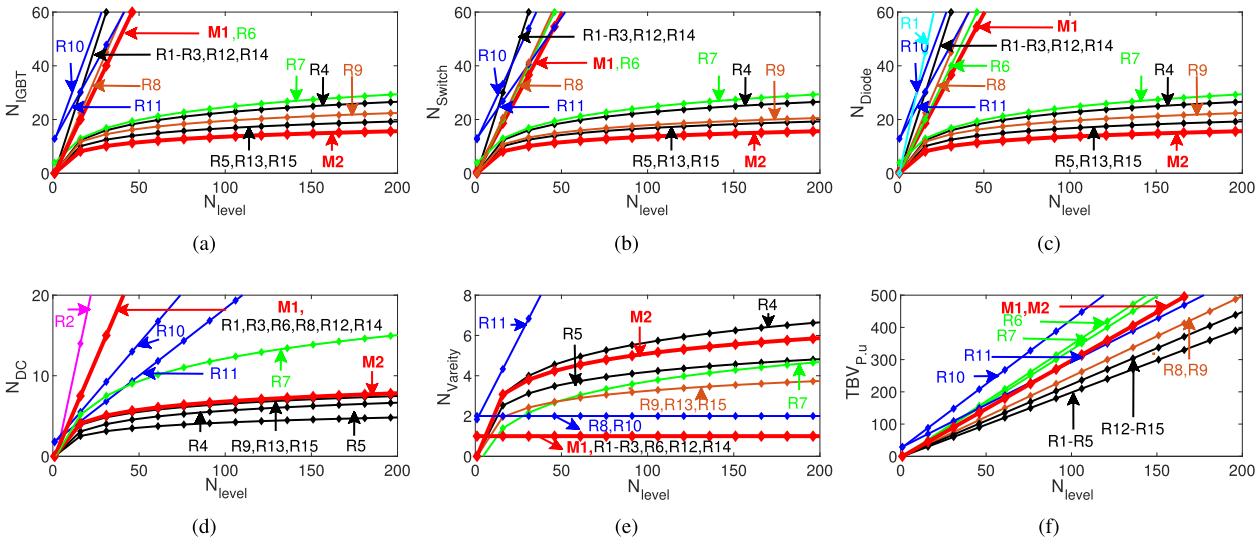

FIGURE 4. Comparison studies for both asymmetric and symmetric cascaded topologies; (a) variation of N_{level} against N_{IGBT}; (b) variation of N_{level} against N_{Switch}; (c) variation of N_{level} against N_{Diode}; (d) variation of N_{level} against N_{DC}; (e) variation of N_{level} against $N_{Variety}$; (f) variation of N_{level} against $TBV_{P.u}$.

TABLE 5. The Number of Required Components of Proposed Asymmetric 15-level Sub-Module Topology and Other Multilevel Inverter Topologies.

Topologies	N_L	N_{IGBT}	N_{driver}	N_{Diode}	N_{DC}	N_{cap}	N_{On}	TBV(p.u)
2019 [13]	13	14	11	14	2	2	5	34
2019 [15]	13	10	10	10	4	-	4	26
2015 [8]	15	16	16	16	7	-	9	44
2020 [21]	15	16	16	16	7	-	9	44
CHB[R4]	15	12	12	12	3	-	6	28
2019 [18]	15	10	9	10	7	-	5	36
2017 [14]	15	10	10	10	4	-	4	36
2019 [17]	15	10	9	10	3	-	5	34
2020 [20]	15	9	9	12	3	-	4	31
Proposed	**15**	**8**	**8**	**14**	**4**	**-**	**3**	**42**
2018 [12]	17	12	9	12	4	-	5	40
2019 [16]	17	10	10	10	4	-	4	36

V. POWER LOSSES CALCULATIONS AND COMPARISON

The power losses depend on switching losses and conduction losses [10], [12], [13]. The switching losses are dissipated power during switching turn-on and turn-off of the power. Losses are calculated for the switch and the anti-parallel diode, which is highly proportional to the switching frequency (f_s). Turn-on and turn-off power losses for each switch $P_{s,on,n}$, $P_{s,off,n}$, can be obtained as follows:

$$\begin{aligned} P_{s,on,n} &= \int_0^{t_{on}} v(t)i(t)dt \\ &= \int_0^{t_{on}} \left[\frac{I(t-t_{on}) - v_{block,n}t}{t_{on}}\right] dt \\ &= \frac{1}{6} \times I \times t_{on} \times V_{block,n} \end{aligned} \tag{11}$$

$$P_{s,off,n} = \frac{1}{6} \times I \times t_{off} \times V_{block,n} \tag{12}$$

Here, $V_{block,n}$, I, t_{on}, t_{off} are the voltage of IGBT in the off-state and on-state, the flowing current by the IGBT before turning-off and in case of turn-on after turning-on, on-state and off-state of IGBT, respectively. The sum of the switching losses ($P_{L,s,n}$) for each power switch is computed as follows:

$$P_{L,s,n} = f_s(P_{s,on,n} + P_{s,off,n}) \tag{13}$$

Here, f_s is the switching frequency of power switches. Assuming $t_{on} = t_{off}$ in eqs. (11)-(13) can be written as:

$$P_{L,s,n} = \frac{2 \times I \times t_{on}}{6} \times f_s \times V_{block,n} \tag{14}$$

By considering $\frac{2 \times I \times t_{on}}{6} = c$ as a constant, (14) can be written as:

$$P_{L,s,n} = c \times f_s \times V_{block,n} \tag{15}$$

By replacing eqs. (2)-(7) in eq. (15), the switching losses for 15-level asymmetric sub-module topology $P_{L,s,asymmetric}$ can be calculated as:

$$\begin{aligned} P_{L,s,asymmetric} = c \times \big(&f_s(V_1 + 4V_2 + 4V_3 + V_4) \\ &+2f_o(V_1 + V_2 + V_3 + V_4)\big) \end{aligned} \tag{16}$$

Here, f_o is the fundamental frequency. By considering $V_1 = V_4 = V_{dc}$, $V_2 = 2V_{dc}$, $V_3 = 4V_{dc}$ to generate 15-level, (16) can be written as:

$$\begin{aligned} P_{L,s,asymmetric} &= c \times V_{dc} \times (26f_s + 16f_o) \\ &= 26 \times c \times V_{dc} \times (f_s + \frac{16}{26}f_o) \end{aligned} \tag{17}$$

For the reason that $f_s \gg \frac{16}{26}f_o$, (17) can be written as:

$$P_{L,s,asymmetric} = 26 \times c \times V_{dc} \times f_s \tag{18}$$

Similarly, by using eq. (15) the switching losses for a 15-level CHB converter is $(56 \times c \times V_{dc} \times f_s)$. Therefore,

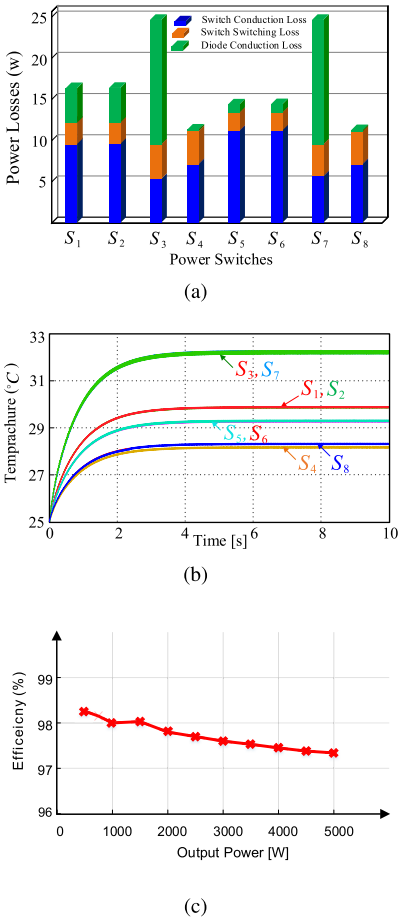

FIGURE 5. Power loss study of proposed 15-level MLI topology; (a) switching and conduction losses of power switches and diodes; (b) temperature of the switches; (c) efficiency.

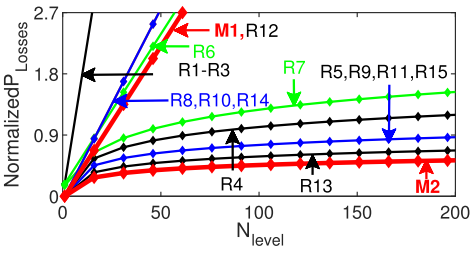

FIGURE 6. Normalized power losses against N_{level}.

the switching losses of the proposed sub-module topology are much lower than for the CHB converter.

The conduction losses of multilevel inverters depend on the number of switches in which they are in an on-state mode in the current path at every time instance [12]–[14]. Therefore, the conduction losses are obtained by calculating the number of active devices in multilevel inverter topologies. For the proposed sub-module topology, the maximum number of on-state IGBT based on the switching table (see Table 1) is three.

The power loss of the proposed 15-level topology is seen in the PLECS environment. For this study, the IGBT IKFW40N65ES5 is chosen. The simulation results are

TABLE 6. Power Loss comparison of the proposed 15-level converter by using standard and advanced PWM technique at output power 5[Kw].

Methods	MI	f_s	Power Loss [W]		
			P_{Cond}	P_{Sw}	P_{Loss}
S-PWM [31]	1.0	2	43	90	133
	0.9	2	67	99	166
	0.8	2	78	112	190
THTD-PWM [33]	1.0	2	28	79	107
	0.9	2	64	86	150
	0.8	2	69	96	165
MTHD-PWM [34]	1.0	2	21	69	90
	0.9	2	50	82	132
	0.8	2	62	99	161

obtained at 5[kW] output power. The input DC sources are assumed to be $V_1 = V_4 = 70$[V], $V_2 = 140$[V], $V_3 = 280$[V] and the inverter is interfaced with a pure resistance load of 23[Ω]. A high frequency modulation technique with a switching frequency of 2[kHz] is applied to the proposed topology which is discussed in section VI. The power losses and temperature of each switch are illustrated in Figs. 5(a) and 5(b). The starting temperature is set to 25[°C]. The switches (S_3, S_7) lose the most power and, as a result, have a higher temperature. The switch (S_1, S_2) thereafter loses much more power. As shown in Fig. 5(c), the suggested 15-level MLI has a total loss of 133[W] and an efficiency of 97.34% for a 5[kW] output power. Fig. 6 displays the variation in the number of levels against normalized power losses. As shown in the figure, the proposed cascaded topology significantly reduces power losses in both operation modes when compared to other MLI topologies.

Recently, several PWM techniques have been presented for power converters in the literature, such as standard Sinusoidal PWM (S-PWM) and Space Vector PWM (SV-PWM), and advanced PWM methods such as Modified Total Harmonics Distortion PWM (MTHD-PWM), and Trapezoidal Total Harmonics Distortion PWM (TTHD-PWM), etc. [31]-[34]. The advanced PWM approaches present several advantages over the standard ones, such as low switching and conduction loss, which improve the efficacy of the converters. Hence, the power loss analysis of the proposed topology is presented by two aforementioned advanced PWM methods. Therefore, these PWM techniques are applied to the proposed 15-level converter to show their advantage over the proposed topology.

The power loss simulation for the presented PWM methods and standard SPWM is performed in the PLECS environment. A comparison is made between the advanced PWM techniques and the standard ones. Table 6 illustrates the power losses of the proposed converter which is mutilated by standard S-PWM, MTHD-PWM, and THTD-PWM. The power losses are calculated for different modulation indexes (0.8, 0.9, and 1.0) at a fixed switching frequency of 2[Khz]. As can see from this table, the conduction (P_{Con}) and switching losses (P_{Sw}) of the standard SPWM are higher than the presented advanced PWM methods for the proposed topology. At modulation index 1.0, the lowest power loss is for MTHD-PWM and then THTD-PWM.

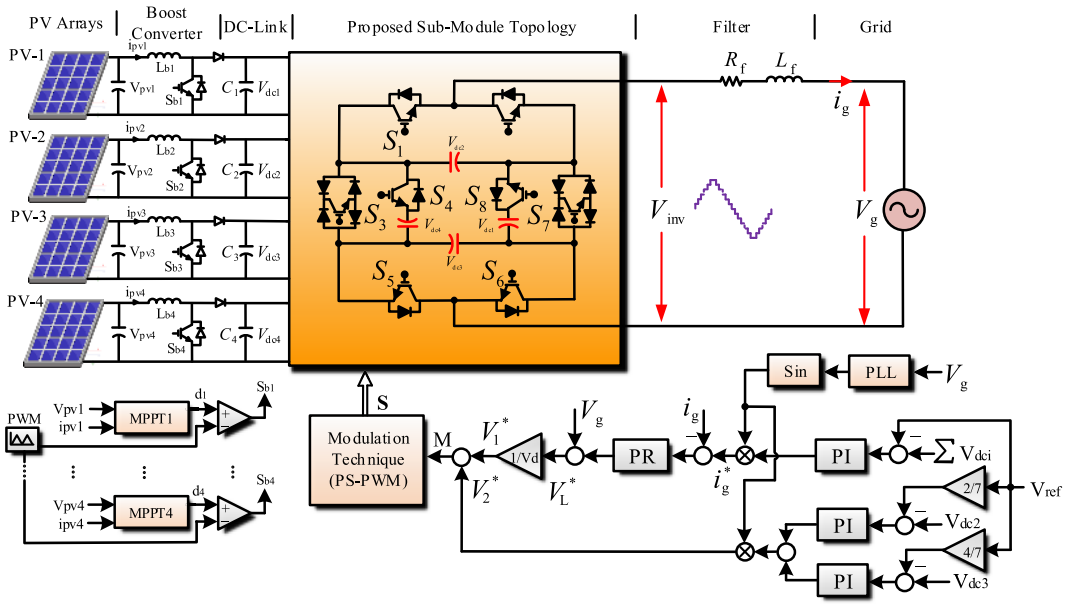

FIGURE 7. Proposed Control scheme for grid-connected PV application of the proposed topology.

VI. APPLICATION AND POWER SWITCHES SELECTION EXAMPLE

A. GRID-CONNECTED PV APPLICATION OF THE PROPOSED TOPOLOGY

The proposed topology is a general topology, the same as other topologies of multilevel inverters that can be applied to renewable energy sources (PV and Wind), EVs, FACTS, etc. As an example, the proposed topology can be applied to grid-connected PV applications due to requiring fewer power switches and drivers, which makes the system more efficient. Fig. 7 shows the application of the proposed topology in the grid-connected PV system. To regulate the grid current in a sinusoidal shape, an effective control technique is adopted which provides a near unity power factor with the grid voltage. To do this, the individual DC link voltages should be kept equal to their DC-link references (V_{ref}), which are assumed to be in the ratio of 1:2:4 in variable irradiation conditions. Therefore, two independent voltage controllers are employed to keep track of the total DC-link voltage and the individual DC-link voltages. As can be seen from Fig. 7, the asymmetric input dc sources of the proposed inverter are replaced by PV panels with different powers. The voltage of PVs is boosted by four separate DC-DC converters with independent maximum power point tracking (MPPT) algorithms at the desired magnitudes.

1) TOTAL DC-LINK VOLTAGE CONTROL

To inject a maximum current into the grid with a fixed nominal voltage by the proposed inverter, the output voltage of the inverter is controlled by a close-loop control, as shown in Fig. 7. The total DC-link voltage is controlled by comparing the DC-link voltage reference (V_{ref}) with the measured capacitor voltage ($\sum V_{dci}$). It is worth nothing that the total DC-link reference voltage can be obtained from the sum of the PV voltages (d_i) and a constant coefficient which depends on the grid voltage magnitude. Then, by tuning a Proportional-Integral (PI) controller, the maximum current is generated that is essential for grid-connected PV inverters. To generate a sinusoidal reference current and track the grid frequency, a standard phase-locked loop (PLL) control is used, as shown in Fig. 7.

2) GRID CURRENT CONTROL

A Proportional Resonance (PR) current control method is utilized to control the grid current. The reference current is made by multiplying the output of PLL (i_g^*), then it is compared with the measured grid current (i_g). The output of the PR controller maximizes the current and sums it with the grid voltage to generate a proper reference signal under grid voltage variations. Finally, since the magnitude (V_L^*) is inappropriate to apply to the proposed inverter, it is scaled down to produce the part of the reference voltage (V_1^*) of the proposed asymmetric inverter.

3) INDIVIDUAL DC-LINK VOLTAGE CONTROL

In order to produce 15-level with the proposed inverter, the ratio of DC-link voltages is kept at a binary algorithm (1:2:4) under the environmental variations of PV panels. The overall DC-link voltage controller is controlled at the total DC link voltage of the inverter equal to $7V_{dc}$. To maintain the other DC-link voltages (V_{dc2}, V_{dc3}), which should have amplitudes equal to $2V_{dc}$ and $4V_{dc}$ two individual voltage controllers are added to the control system, as shown in Fig. 7. By using these three independent (PI) controllers, the DC-link voltages can

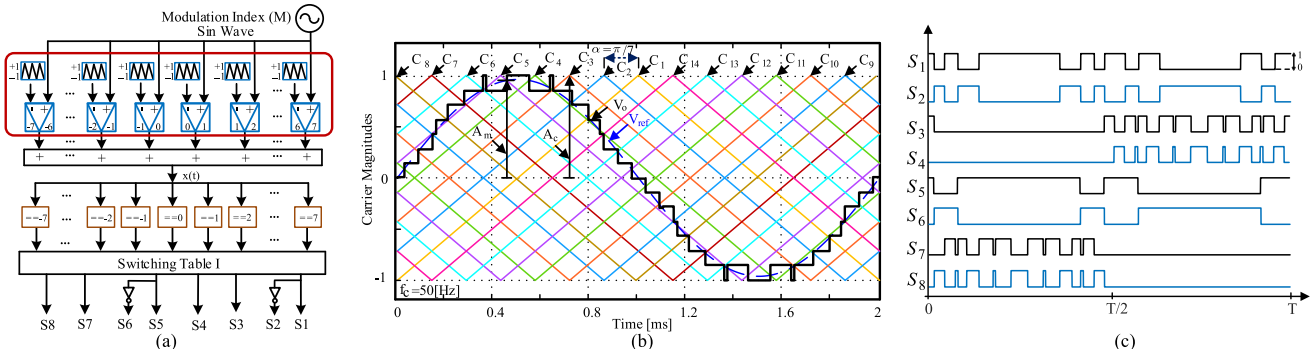

FIGURE 8. Proposed PS-PWM modulation technique for the proposed 15-level topology; (a) modulation block diagram; (b) reference voltage, output waveform, carriers; (c) generated switching pulses of proposed topology based on PS-PWM.

be balanced and fixed in their references. The output of these three PI controllers provides the proper modulation index. The switching pulses of the proposed inverter are produced by the proposed PWM technique which is presented in the following.

4) PROPOSED PHASE-SHIFT CARRIER BASE PWM MODULATION TECHNIQUE

A Phase-Shift Carrier base Sinusoidal PWM (PSC-SPWM) modulation technique is proposed to generate switching pulses for the proposed grid-connected 15-level multilevel inverter. Fig. 8(a) shows the block diagram of the proposed PSC-PWM modulation method. To produce a 15-level, fourteen high-frequency triangular carriers with the same magnitude of -1 to $+1$ but with different phases are defined and compared with the modulation index (M) that has the frequency of grid voltage. As discussed above, the modulation index (M) is generated by the presented control system in Fig. 7. The amplitude of reference voltage (A_m) is controlled by the modulation index which is shown in Fig. 8(b). The amplitude of modulation for the proposed 15-level MLI can be obtained from the formula $M_a = \frac{A_m}{A_c}$, where A_c is the maximum value of carrier. The phase shift of triangular carriers can be obtained as $\alpha = \pi/7$. Therefore, the seven triangular carrier that are used for generating positive levels have phases of $0, \alpha, 2\alpha, \ldots, 6\alpha$, and the seven triangular carrier that are used for producing negative levels have phases $\pi, (\pi + \alpha), (\pi + 2\alpha), \ldots, (\pi + 6\alpha)$. The triangular carriers are compared with the specified numbers, which are related to the number of levels. In the comparator blocks, if the modulation index (reference signal) is greater than the carrier signal, the output of the comparator will be "c", otherwise it will be "c-1". The comparator output will be "-(c-1)" if the reference signal is larger than the negative carrier signal, otherwise it will be "-c." The obtained signals are added together to produce the x(t) signal displayed in Fig. 8(a). Finally, based on the switching states of the proposed topology (Table 1), all gate pulses are created to activate the power switches, as shown in Fig. 8(c).

TABLE 7. IGBTs Voltages of 15-level Sub-Module Topology and 225-level Cascaded Topology.

15-level			225-level		
$V_{switches}$	V_{block}	$V_{nominal}$	$V_{switches}$	V_{block}	$V_{nominal}$
V_{S_1}	536.5V	1200V	$V_{S_{1,1}} = V_{S_{2,1}}$	33.52V	250V
V_{S_2}	536.5V	1200V	$V_{S_{3,1}} = V_{S_{7,1}}$	117.32V	250V
V_{S_3}	1878V	3300V	$V_{S_{4,1}} = V_{S_{8,1}}$	134.08V	250V
V_{S_4}	2146.28V	3300V	$V_{S_{5,1}} = V_{S_{6,1}}$	67.04V	250V
V_{S_5}	1073.14V	1700V	$V_{S_{1,2}} = V_{S_{2,2}}$	502.8V	1200V
V_{S_6}	1073.14V	1700V	$V_{S_{3,2}} = V_{S_{7,2}}$	1470.05V	2500V
V_{S_7}	1878V	3300V	$V_{S_{4,2}} = V_{S_{8,2}}$	2011.02V	3300V
V_{S_8}	2146.28V	3300V	$V_{S_{5,2}} = V_{S_{6,2}}$	1005.6V	1700V

B. CALCULATION OF POWER SWITCHES FOR MEDIUM-VOLTAGE APPLICATIONS

The selection of power switches in the proposed topology is related to the voltage rating of each switch. The maximum operating voltage (3-phase line–line RMS voltage) of the proposed topology is obtained by $\sqrt{1.5}V_{IGBT,scv}/\gamma$, where $V_{IGBT,scv}$ is the highest standard commercial voltage of IGBT and γ is a factor to ensure the safe operation of the IGBT that is typically assumed as $\gamma = 1.7$. Therefore, by the determination of the maximum IGBT voltage, the operation voltage of the proposed topology is obtained. By assuming that the maximum IGBT voltage in medium voltage applications is 3.3[KV] the operation voltage of the 3-phase line-to-line RMS voltage will be 2.3[KV]. For the single-phase system, the operation phase voltage RMS will be 1328[V]. The consideration of the proposed topologies is a 15-level sub-module inverter (Table 2, M_{5sub}), and a 225-level cascaded topology consists of two series of sub-module inverters (Table 3, M_{7Cas}). Therefore, for such an RMS voltage 1328[V] or maximum voltage of 1878[V], the DC power supply magnitudes for the 15-level sub-module inverter are: $V_1 = V_4 = 268.28$[V], $V_2 = 536.56$[V], $V_3 = 1073.12$[V] and for 225-level cascaded topology are: for the first sub-module $V_{1,1} = V_{4,1} = 16.76$[V], $V_{2,1} = 33.52$[V], $V_{3,1} = 67.04$[V] and for the second sub-module $V_{1,2} = V_{4,2} = 251.4$[V], $V_{2,2} = 502.8$[V], $V_{3,2} = 1005.6$[V].

TABLE 8. IGBTs and driver circuits price comparison among the proposed 15-level sub-module topology and recent 15-level MLIs for medium-voltage applications.

IGBTs and Driver Circuits Type	Voltage and Current Rating	Unit Price	[14]		[17]		[18]		[21],[8]		[20]		**Proposed**	
			No.	Price	No.	Price	No.	Price	No.	Price	No.	Price	No.	Price
CM400DU-12NFH	600V, 400A	$153	2	$306	4	$612	2	$306	6	$918	4	$612	-	-
CM400HA-24A	1200V, 400A	$197	2	$394	-	-	1	$197	4	$788	-	-	2	$394
CM400DU-34KA	1700V, 400A	$516	2	$1,032	2	$1,032	-	-	2	$1,032	1	$516	2	$1,032
CM400DY-50H	2500V, 400A	$550	-	-	-	-	2	$1,100	-	-	-	-	-	-
CM400DY-66H	3300V, 400A	$773	4	$3,092	4	$3,092	4	$3,092	4	$3,092	4	$3,092	4	$3,092
SKYPER-32PRO2	Up to 1700V	$92.71	3	$278.13	3	$278.13	3	$278.13	6	$556.26	3	$278.13	2	$185.42
1SC0450V2A0-65	Up to 6500V	$267.62	2	$535.24	2	$535.24	2	$535.24	2	$535.24	2	$535.24	1	$535.24
Total Price			$5,637.37		$5,549.37		$5,508.37		$6,921.5		$5,033.3		**$5,238.66**	

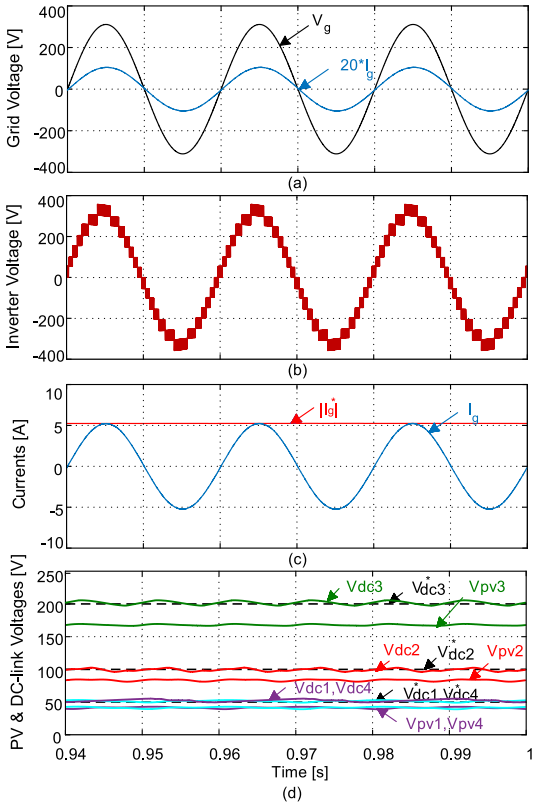

FIGURE 9. Steady state simulation study; (a) grid voltage and grid current; (b) inverter voltage; (c) grid current and reference current; (d) PV voltages, DC-link voltages and reference DC-link voltages.

Table 7 illustrates the commercial IGBT voltage rating for the proposed 15-level sub-module inverter and 225-level cascaded topology. According to Table 7, the maximum standing voltage is related to four switches (S_3, S_4, S_7, S_8) for the proposed 15-level inverter and two power switches ($S_{4,2}$, $S_{8,2}$) for the proposed cascaded topology. As can be seen, the rating of power switches is mitigated in the proposed cascaded topology, which makes it suitable for medium-voltage applications. The price of the proposed single-phase 15-level sub-module inverter, and recent 15-level [8], [14], [17], [18], [21] are compared in Table 8. The selected IGBT types are industrial IGBTs for medium-voltage applications with a nominal current of 400[A] manufactured by MITSUBISHI company.

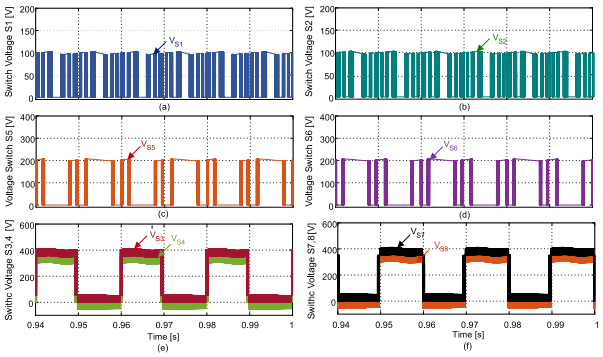

FIGURE 10. Voltage stress of switches; (a) V_{S1}; (b) V_{S2}; (c) V_{S5}; (d) V_{S6}; (e) V_{S3}, V_{S4}; (f) V_{S7}, V_{S8}.

The cost of IGBTs (single pack) and gate driver circuits (Semikron, dual pack) are in USD, as an example [27]. As can be seen from the table, comparing the number of elements and the cost, it is clear that the proposed topology requires eight power switches and eight drivers, whereas other topologies require more than nine power switches and drivers, resulting in a lower cost of the proposed inverter when compared to other recently presented MLIs except [20].

VII. SIMULATION RESULTS OF THE PROPOSED INVERTER FOR GRID-CONNECTED PV APPLICATION

The simulation results of the proposed 15-level topology are conducted in MATLAB/Simulink software in a single-phase grid-connected PV system. The proposed topology is controlled based on the suggested control scheme, which is presented in section VI.

The PV sources are connected to the proposed topology through four independent DC-DC boost converters which are controlled by the P&O MPPT algorithm. The detail of single-phase PV panels, boost converters and output filter and grid parameters, are listed in Table 9. Fig. 9 shows the steady-state simulation results of the grid voltage (V_g), inverter voltage (V_{inv}), reference and grid currents (i_g^*, i_g), and PV ($V_{pv,i}$), DC-link ($V_{DC,i}$) and DC-link reference ($V_{DC,i}^*$) voltages. In this case, the irradiance and temperature of PV sources are set at 1000 [W/m^2] and 25[°C]. As can be seen from this

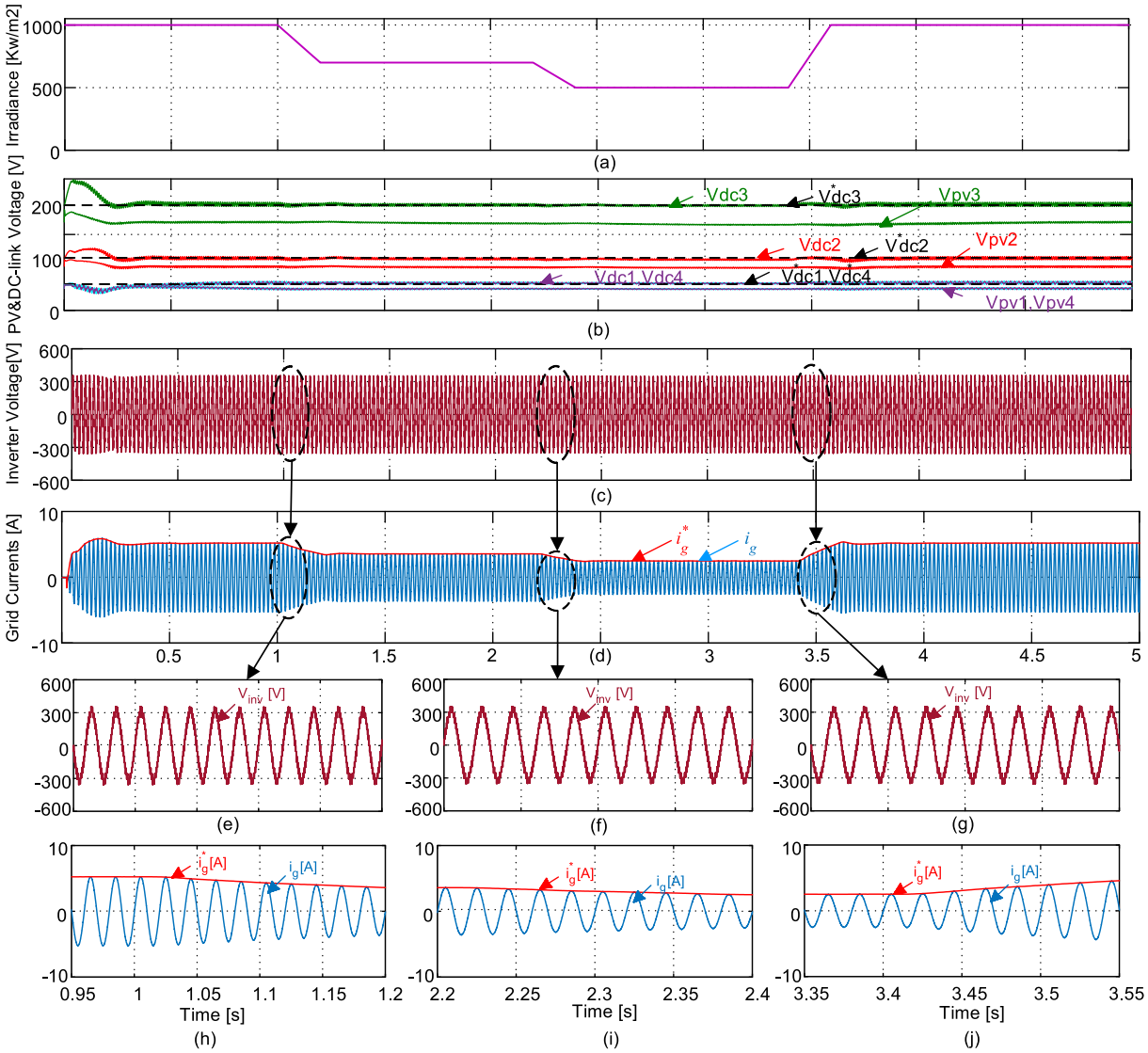

FIGURE 11. Simulation study for irradiance variations; (a) PV irradiance; (b) PV voltages, DC-link voltages and reference DC-link voltage; (c) inverter voltage; (d) grid current and reference current; (e) zoomed inverter voltage at decreasing irradiance from 1000 to 700[Kw/m^2]; (f) zoomed inverter voltage at decreasing irradiance from 700 to 500[Kw/m^2]; (g) zoomed inverter voltage at increasing irradiance from 500 to 1000[Kw/m^2]; (h) zoomed grid current at time 1[s]; (i) zoomed grid current at time 2.2[s]; (j) zoomed grid current at time 3.4[s].

figure, the grid voltage is in phase with the grid current and all 15 voltage levels are produced by the inverter. It also shows that the grid current tracks its reference properly. The DC-link voltages track the references in an asymmetric algorithm, which confirms the accuracy of the proposed control scheme. The steady-state simulation results of the stress voltage of all eight power switches are shown in Fig. 10. These figures confirm the presented eqs. (2)-(7). The highest stress voltage is for power switches (S_3, S_7) which endure 400[V].

The proposed 15-level inverter is simulated and tested for different environmental conditions of PV sources. The results are shown in Fig. 11. As can be seen from Fig. 11(a), in the first the irradiance and temperatures of all four PV panels are set to 1000[W/m^2] and 25 [°C]. At t=1[s], the irradiance of all PV panels reduces to 700[W/m^2], then at t=2.2[s] it reduces to 500 [W/m^2], then finally, back to 1000[W/m^2] at t=3.4[s]. The PV, DC-link, and reference voltages are shown in Fig. 11(b) which shows that the PV panels always work at their maximum voltage points ($V_{PV1} = V_{PV4} = 42[V]$, $V_{PV2} = 84[V]$, $V_{PV3} = 168[V]$), and all DC-link voltages track their references ($V_{DC1} = V_{DC4} = 50[V]$, $V_{DC3} = 100[V]$, $V_{DC4} = 200[V]$) during the irradiance changes. As a result, the inverter generates a 15-level with a constant voltage of 350[V] during the input variations, as shown in Fig. 11(c). The grid current waveform and its reference are indicated in Fig. 11(d). As observed from this figure, the grid current has a pure sinusoidal waveform and its amplitude varies with solar irradiance variations. Figs. 11(e) to 11(j) show the zoomed view of the inverter voltage and grid current at the different irradiance variation times. From these figures, it can be observed that a constant voltage is produced by the proposed inverter during irradiance

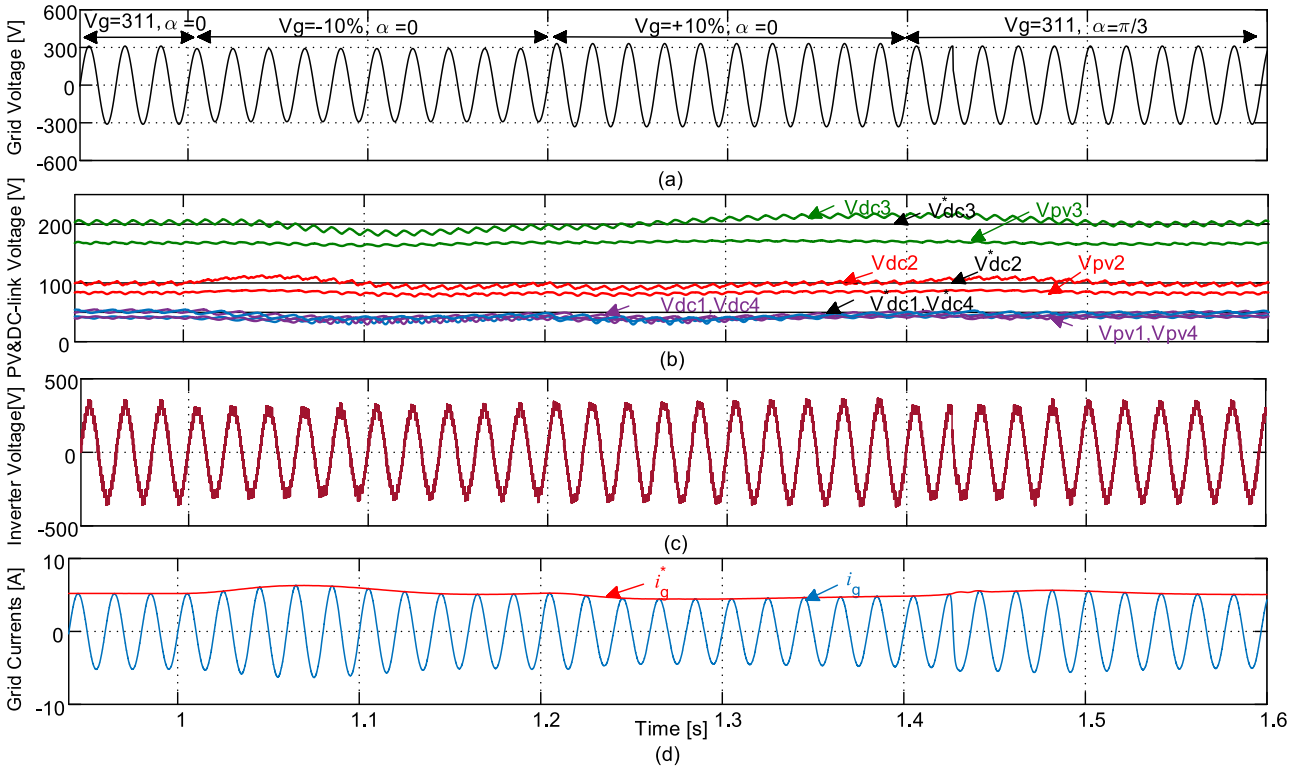

FIGURE 12. Simulation study for grid voltage variations; (a) grid voltage; (b) PV, DC-link and reference voltages; (c) inverter voltage; (d) grid and reference currents.

TABLE 9. Simulation Study Parameters for Grid-Connected PV Application.

	Parameter	Value
PV Sources	Total PV power (P_{pv})	1.6[KW]
	Maximum power (PV-1,PV-4)	200[W]
	Total cells ($N_{s1,s4} \times N_{p1,p4}$)	42×1
	Maximum power (PV-2)	400[W]
	Total cells ($N_{s2} \times N_{p2}$)	(42×2)×1
	Maximum power (PV-3)	800[W]
	Total cells ($N_{s3} \times N_{p3}$)	(42×4)×1
DC-DC converter	Boost inductors (L_b)	6.8[mH]
	Boost converter switching frequency (f_{sb})	10[KHz]
Capacitors	Input capacitors ($C_{in,i}$)	250[μF]
	DC-link capacitors (C_i)	5000[μF]
Inverter	DC-link Voltage ($V_{dc1} = V_{dc4} = V_{dc}$)	50[V]
	DC-link Voltage ($V_{dc2} = 2V_{dc}$)	100[V]
	DC-link Voltage ($V_{dc3} = 4V_{dc}$)	200[V]
	Inverter output voltage (V_{inv})	350[V]
	Inverter switching frequency (f_{sw})	2[KHz]
Grid	Grid voltage (V_g (rms))	311[V]
	Grid frequency (f_o)	50[Hz]
	Output filter (R,L)	1[mΩ],4[mH]

changes, and the magnitude of grid current changes when solar irradiance varies. These figures confirm the correctness of operation of the proposed inverter and control system.

In addition to the input variations, the response of the inverter to the output variations (V_g) is also conducted. The simulation results for grid voltage variations are shown in Fig. 12. The response of the system is evaluated by step changes in amplitude and phase of the grid. Fig. 12(a) shows the grid voltage variation between ±10% and also its phase changes from 0 to $+\pi/3$. It can be seen from Fig. 12 that, when the grid voltage amplitude varies, the inverter voltage changes for a short time and then returns to the constant value, but the inverter voltage increases and decreases slightly due to the difference between the voltage of the inverter and the grid. Besides, when the phase of grid voltage changes, the inverter voltage remains constant and the grid current remains in phase with the grid voltage.

VIII. EXPERIMENTAL VALIDATIONS

The simulation and experimental results for three topologies, symmetric 7-level, an asymmetric 15-level sub-module topology, and a 29-level cascaded topology are presented to validate the performance of the proposal. IGBTs are used as switching devices in the topology prototype. The list of components is used for experimental set-up is shown in Table 10. To control switching pulses of the proposed topology, the presented Fundamental Frequency Modulation (FFM) technique in [10] is applied to control of the proposed topologies because it is simple and easy to implement at a high number of levels. Additionally it uses low-frequency switching that causes low power losses. This modulation technique uses a sinusoidal stepped waveform with a fundamental frequency as illustrated in Fig. 13. In this technique, by considering the desired total number of levels N_L in the proposed topologies,

TABLE 10. Electrical Parameters of the Proposed Sub-Module 15-Level Converter.

Parameters	Value
DC supply type	Symmetric and asymmetric laboratory DC power supplies
DC supply ratio 7L	$V_1 = V_2 = V_3 = V_4 = 15$[V]
DC supply ratios 15L	$V_1 = V_4 = 15$[V], $V_2 = 30$[V], $V_3 = 60$[V]
DC supply ratios 29L	$V_{1,1} = V_{1,2} = V_{4,1} = V_{4,2} = 15$[V], $V_{2,1} = V_{2,2} = 30$[V], $V_{3,1} = V_{3,2} = 60$[V]
IGBT	FGH80N60FDTU, 600[V], 40[A]
FPGA Basys 2	Spartan 3E-100 CP132
R-L values	60[Ω], 40[mH]

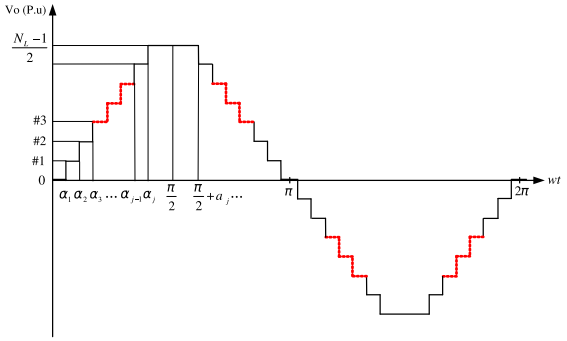

FIGURE 13. Proposed PS-PWM modulation technique of the proposed 15-level MLI topoogy.

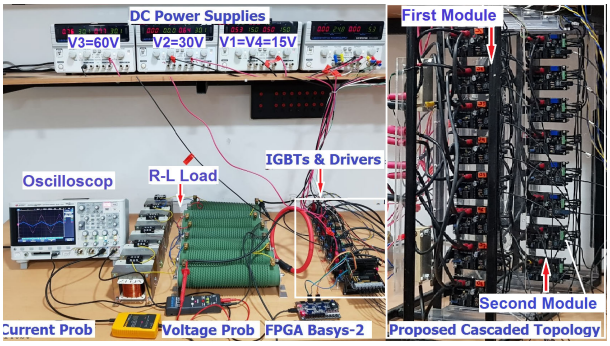

FIGURE 14. The prototype picture of the proposed sub-module and cascaded multilevel inverters.

the switching angles are calculated for $0 < \alpha_j < \pi/2$ as follows:

$$\alpha_j = sin^{-1}(\frac{j-0.5}{N_L}) \quad forj = 1, 2, \ldots, \frac{N_L - 1}{2} \qquad (19)$$

Then, the switching angles generate the switching pulses of the proposed multilevel inverter which are determined separately based on the switching states in Table 1. The step timing is chosen based on the output frequency and is calculated offline.

The field-programmable gate array (FPGA) is used to generate pulses, to implement the presented fundamental frequency modulation technique for the proposed topologies. The 7-level, 15-level and 29-level switching states are programmed by Verilog-language in Xiling software.

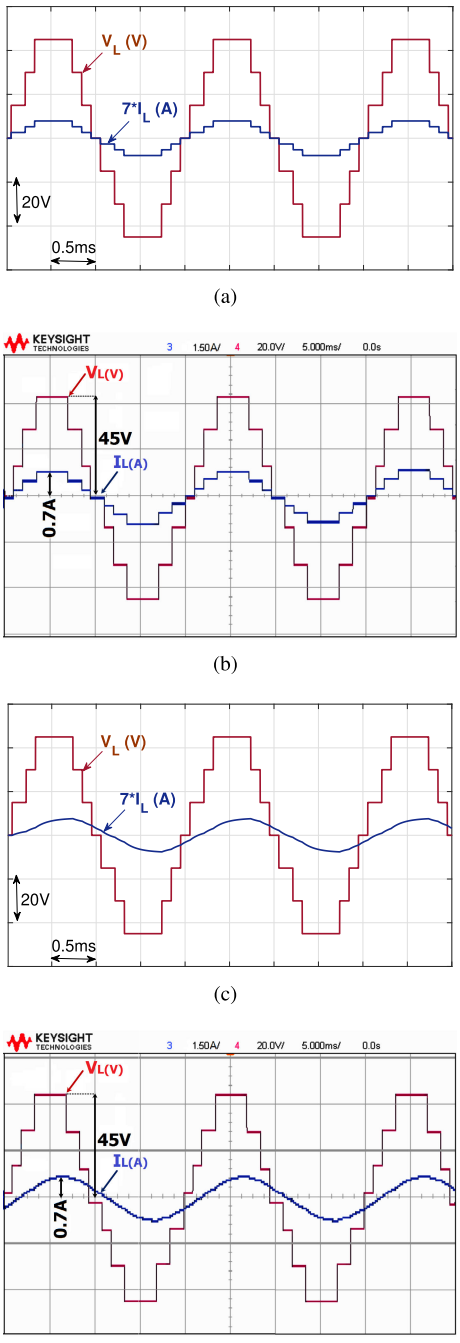

FIGURE 15. Simulation and experimental results of symmetric 7-level proposed sub-module inverter; (a) simulation results of the output waveforms of proposed 7-level inverter with R-load; (b) experimental results of the output waveforms of the proposed 7-level inverter with R-load; (c) simulation results with R-L load; (d) experimental results with R-L load.

Then, the switching states transfer to Basys 2 hardware. $2[\mu s]$ dead-time is considered to avoid a short circuit. Finally, the switching pulses move to IGBTs by optic-wires for the proposed topology. FGH80N60FDTU IGBT power switches are used to switch DC power supplies

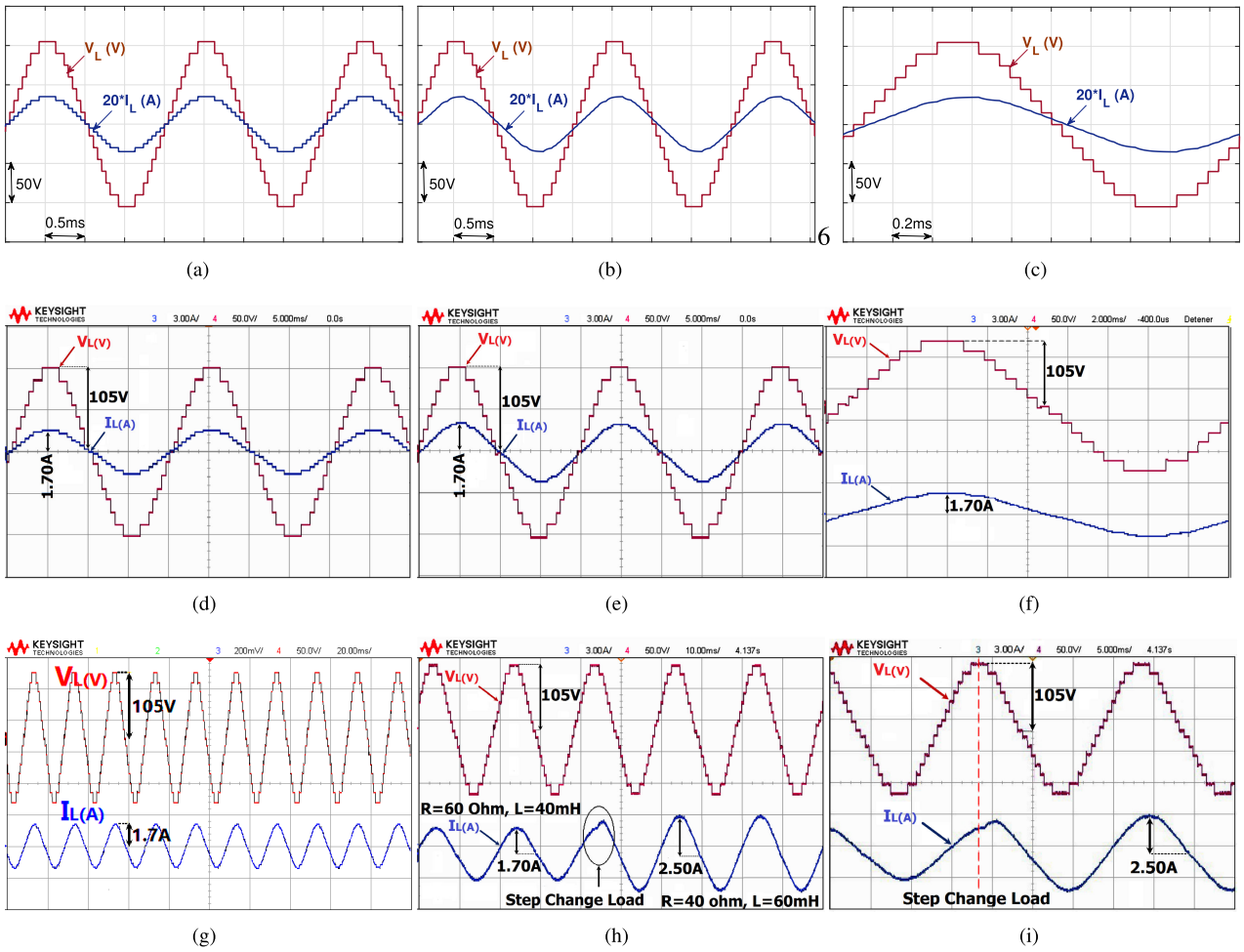

FIGURE 16. Simulation and experimental results of an asymmetric 15-level proposed sub-module inverter; (a) simulation results of the output waveforms with R-load; (b) simulation results with RL-load (c) zoomed view of the output waveforms in 2ms; (d) experimental results of the output waveforms with R-load; (e) experimental results with R-L load (f) zoom view of (f) in 2ms; (g) experimental output waveforms with R-L load; (h) experimental results of the load voltage and current waveforms with a step change load; (i) step change load zoom of the output and current waveforms.

and generate the desired output voltage to 60[Ω], 40[mH] AC load.

A. SEVEN-LEVEL SYMMETRIC EVALUATION

Fig. 14 is the prototype picture of the proposed sub-module inverter with eight power switches and four equal DC source magnitudes. The simulation and experimental results of the symmetric 7-level sub-module inverter are shown in Fig. 15. The magnitudes of all DC power supplies are set at 15[V]. The output voltage and current waveforms of the proposed 7-level sub-module topology in both simulation and experimental results are presented in Figs. 15(a) and 15(b) with a pure resistance load 60[Ω] and presented in Figs. 15(c) and 15(d) for an R-L load 60[Ω], 40[mH]. These figures prove the ability of the proposed topology to supply a sinusoidal current to an R-L load that has a sinusoidal wave. The THD percentage of the load voltage and current for the simulation results of the 7-level sub-module inverter are 12.56% and 6.35%, and the experimental results are 13.14% and 6.92%, respectively.

B. FIFTEEN-LEVEL ASYMMETRIC EVALUATION

In asymmetric sub-module topology, four DC power supply magnitudes are set by a binary algorithm (1:2:4). The quantity of DC supplies required to create 15-level in the experimental study corresponds to M_{5sub} (see Table 2) and is given in Table 10. The simulation and experimental results of the 15-level sub-module topology are shown in Fig. 16. In this case, similar to the symmetric mode, the proposed inverter is evaluated in two states: a pure resistance load and a resistance-inductive load. Figs. 16(a) and 16(d) show the simulation and experimental results of the load voltage and current waveforms of the proposed 15-level inverter for a pure resistance 60[Ω], and Figs. 16(b) and 16(e) and Figs. 16(c) and 16(f)

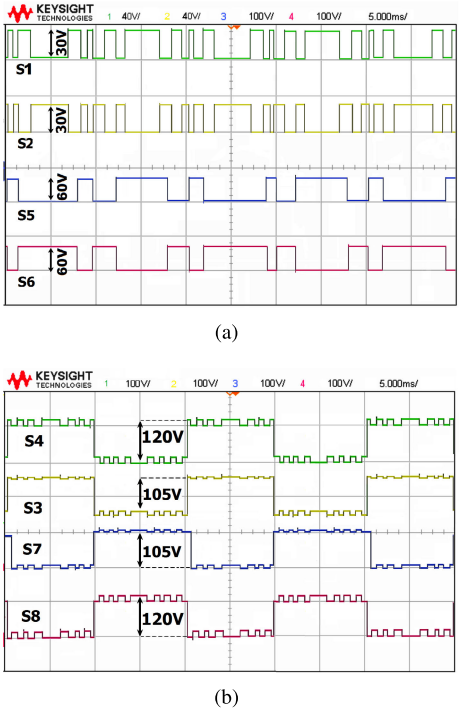

FIGURE 17. Experimental results blocking voltages on power switches and diodes of proposed 15-level sub-module inverter; (a) blocking voltages of power switches S_1, S_2, S_5, S_6; (b) blocking voltages of power switches S_3, S_4, S_7, S_8.

indicate the same for a resistance-inductive load 60[Ω], 40[mH],respectively. From these figures, it is evident that the proposed inverter has a good agreement with the proposed DC power supply methods to generate 15-level and can operate in different loads. The peak output voltage and current for a 15-level sub-module inverter are equal to 105[V], 1.73[A] for the simulation study, and nearly 105[V], 1.7[A] for the experimental study. The THD percentage of the load voltage and current for the simulation results of the 15-level sub-module inverter are 5.79% and 3.4%, and the experimental results are 6.12% and 3.91%, respectively.

The dynamic response of the proposed 15-level inverter is tested with a sudden load change, which is a typical test for single-phase multilevel inverters. The experimental results of dynamic response are presented in Fig. 16(h) and 16(i). The value of the load changes from a 60[Ω], 40[mH] to 40[Ω], 60[mH]. It is clear that the proposed topology remains in steady operation, and each output level remains unchanged. The experimental results of the blocking voltage of all used power switches are illustrated in Fig. 17 to approve eqs. (2) to (7). Figs. 17(a) and 17(b) show the low blocking voltages on power switches S_1, S_2 with a magnitude of 30[V], the medium blocking voltage is on power switches S_5, S_6 with the value of 60[V] and the high blocking voltage is on the four power switches S_3, S_7 and S_4, S_8 with magnitudes of 105[V] and 120[V], respectively.

In order to calculate the efficiency (η) of proposed topology, the input power (P_{in}) and output power (P_{out}) are

TABLE 11. Efficiency of the Proposed 15-level Sub-Module Inverter.

V_{in} [V]	P_{in} [W]	P_{loss} [W]	P_{out} [W]	R_L [Ω], L_L [H]	η%
$V_1 = 15$	$P_{V1} = 21.35$	3.86	173.4	60, 0.04	97.82
$V_2 = 30$	$P_{V2} = 40.2$				
$V_3 = 60$	$P_{V3} = 93.6$				
$V_4 = 15$	$P_{V3} = 22.1$				

measured $\eta = \frac{P_{out}}{P_{in}}$. Table 11 shows the measured input and output power of the proposed 15-level topology. As can be seen in Table 11, the input DC power is obtained by the summing of four used DC sources (177.25W) to create fifteen levels of proposed topology. The output power is measured by current, and voltage probes (173.4W) and the power loss is 3.86W. Hence, the efficiency of the proposed topology is 97.82%.

C. TWENTY-NINE-LEVEL CASCADED TOPOLOGY

The experiment results of the proposed cascaded topology have been conducted—the proposed cascaded topology is comprised of two proposed asymmetric sub-module topologies. The proposed asymmetric inverter with two series sub-module inverters can make a maximum 225-level based on the proposed method (M_{7Cas}), as shown in Table 3, but herein to prove the performance of cascaded configuration 29-level is considered. The values of DC supplies are chosen to correspond to proposed methods (M_{2Cas}) that are presented in Table 3. The first and second sub-module inverters separately generate 15-level at different timed so the total output voltage is the sum of these voltages equal to 29-level. The output voltage of each sub-module topology (V_{o1}) and (V_{o2}), load voltage (V_L), and load current (I_L) waveform of the 29-level cascaded topology are indicated in Fig. 18(a). A zoomed view of Fig. 18(a) is shown in Figs. 18(b) and 18(c). The first and second sub-module topologies generate 15-level with a peak of near 105[V], so the peak of the load voltage of cascaded topology is near 210[V] with a peak current of 3.4[A]. The THD percentage of the load voltage and load current of 29-level cascaded topology are 1.83% and 0.87%, respectively. The low value of THD requires a high power quality to deliver the load.

IX. DISCUSSION

The performance of the proposed sub-module topology was validated through simulation and experimental analysis for both symmetric and asymmetric sources under resistance and resistance-inductance loads and in a grid-tied PV system. Corresponding to the presented performance analysis, the proposed topologies are able to generate all levels based on presented theoretical concepts and can also work in both operation modes as well as having good performance with a pure sinusoidal current waveform. Evaluation of the reliability of MLIs to apply in a real application is an essential function of their design. In this paper, the reliability of the proposed

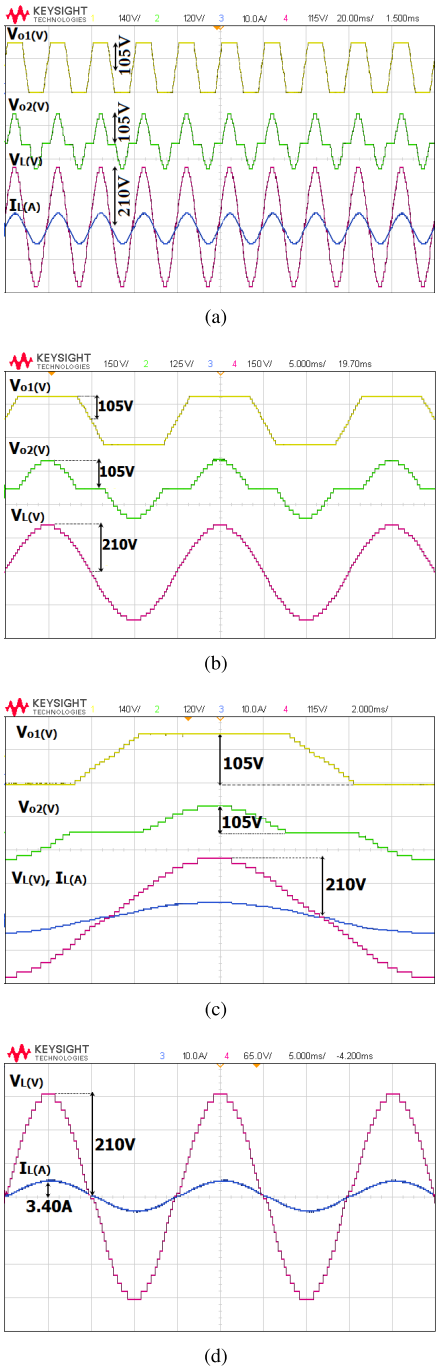

FIGURE 18. Experimental results of proposed 29-level cascaded topology; (a) output voltage of first sub-module topology V_{o1}, output voltage of second sub-module topology V_{o2} and load voltage and current waveforms V_L, I_L in 20ms; (b) zoom of output voltages in 5ms; (c) output voltages of first and second sub-module topologies, load voltage and current waveforms in 2ms; (d) load voltage and load current waveforms in 5ms.

topology is discussed in terms of control complexity and the capability of creating a large number of levels.

A. CONTROL COMPLEXITY

Classical topologies NPC, FC, as well as the presented topologies of [13] and [22]–[24] require several sensors (voltage/current), costly controller, signal processing circuits, and sophisticated control algorithm, to deal with the voltage balance of capacitors. These will introduce complexity and reduce reliability. Conversely, the proposed topology does not require any capacitor to balance the capacitor voltages. Indeed, it does not need any sensors or complicated control, which enhances the reliability of the proposed MLI than other MLIs that use capacitors in their circuits.

X. CONCLUSION

In this article, a reduced sub-module topology was proposed for cascaded multilevel power inverters with reduced switching devices to be applied to renewable energy sources. The presented sub-module topology generates seven voltage levels in symmetric sources and fifteen voltage levels in asymmetric sources with eight switching devices. A cascaded configuration with several DC source arrangements was investigated to minimize the number of switching devices, the number of gate drivers, and the cost of the inverter. The comparison outcomes indicate that the required switching devices for fifteen levels in the proposed sub-module topology have been reduced by thirty-three percent in contrast to the CHB multilevel inverter. The cost of the proposed fifteen-level sub-module topology was reduced compared to other recent multilevel inverters for medium voltage applications. In addition, in order to show flexibility and performance of the proposed topology in grid-tied PV applications, a close-loop control system was proposed in which the proposed inverter was modulated with high-frequency PSC-PWM. The obtained results from simulations and experimental validation have demonstrated that the proposed sub-module topology and its cascaded connection are able to operate in both symmetric and asymmetric sources with a reduced number of switching devices and also have a good response in grid-tied PV systems.

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