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4-Channel, 100 Gbps Inductorless Optical Receiver Analog Front-End in CMOS for Optical Interconnect

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ABSTRACT In this paper, a 4-channel, 100 Gbps inductorless optical receiver analog front-end fabricated in a 55 nm bulk-CMOS technology is presented. Active feedback technique is widely adopted to improve the performance of the optical receiver without the area-occupied inductors. To alleviate the voltage headroom stress of the local feedback loop in traditional regulated cascode transimpedance amplifier, the common gate amplifier is inserted before the traditional common source feedback stage. And the cross-couple active feedback stage provides a negative signal path to extend the bandwidth of the local feedback loop. Multi-stage limiting amplifier with active negative and positive feedback stages are employed to extend bandwidth and acquire high gain simultaneously. The optical receiver was realized as 4-element arrays occupying the area of 800 μm $\times$ 1800 μm, whereas the core area of each channel is just 275 μm $\times$ 650 μm. The measured 3-dB bandwidth reaches 22.8 GHz, sufficient for 25-Gbps operation. For an input voltage of 2.5 $mV_{p\text{-}p}$, the optical receiver achieves a BER $= 10^{-12}$ at 25-Gbps PRBS7, and 310 mV differential output voltage is delivered. From the supply voltage of 1.2 V, the test chip consumes the power of 226 mW and exhibits the power efficiency of 2.3 mW/Gb/s, when 25-Gbps PRBS31 is supplied.

INDEX TERMS Active feedback, cross-coupled feedback, limiting amplifier, negative and positive feedback, optical receiver, transimpedance amplifier.

I. INTRODUCTION

In recent years, a boom of data traffic has emerged from pervasiveness of multimedia consumer applications in daily life, and high-density and energy-efficient data interconnects are required to accommodate the explosive transfer volume of data center [1]–[6]. Several Ethernet standards have been developed to address this need and specify 100+ Gb/s links capable of spanning distances from meters to kilometers [7]–[9]. Compared to the conventional electrical cables, the fiber-based optical interconnects yield better results in terms of channel bandwidth, energy loss, and crosstalk, have been a vital solution to accomplish 100+ Gb/s links [3], [5], [7], [10], [11].

As the key element of optical interconnect system, optical receiver analog front-end (Rx_AFE) is just located between the photo detector (PD) and the clock and data recovery (CDR) circuit [12]. Generally, the large area PD is needed for high responsibility, which inevitably introduces a large capacitance at the input of Rx_AFE and limits the bandwidth [13]. On the other hand, the weak photocurrent produced by PD is converted and amplified into logic-lever voltage signal for post-processing, thereby the sufficient transimpedance gain is necessary in design of high-speed Rx_AFE. Besides, the weak photocurrent also put forward the demand for the high sensitivity of Rx_AFE. In summary, it is a formidable challenge to balance the gain, bandwidth, and noise in the design of a low-cost, high-speed, and energy-efficient Rx_AFE.

Compared with the III-V compound processes frequently used to meet the above-mentioned requirements, Rx_AFE in a mature and reliable CMOS technology has been preferred in terms of power efficiency, manufacture cost and integration as the feature size of CMOS scaled down [11], [14], [15]. However, the scaled-down supply voltage, the comparably lower cut-off frequency and the smaller transconductance

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of active devices in CMOS technology make it hard to achieve the prospective effect through various bandwidth extension techniques. For example, the regulated cascode (RGC) configuration TIA is frequently used to isolate the big capacitance of PD due to the lower equivalent input impedance [16]–[18]. But the gain bandwidth product (GBP) of the local feedback stage is limited by the scaled-down supply voltage [12], [19], then the roll-off feedback gain will lead to inductive input impedance in low-frequency domain and hence decreasing the bandwidth of RGC TIA. In addition, in the design of the limiting amplifier (LA), the characteristic frequency and the smaller transconductance make it necessary to adopt the multi-stage configuration for the expected GBP [20]. But the cascade of several low-gain main amplifiers will lead to a dramatic drop in bandwidth and a linear increase in power consumption. Moreover, the excess circuit area occupied by the inductive peaking technique is prohibitively large, especially when cascaded gain stages are employed, leading to a higher cost for the circuit implementation. Fortunately, active negative and positive feedback technique, multi-peak bandwidth enhancement technique, source degeneration and so on are proved valid in boosting the performance in the low-cost, high-speed, and energy-efficient Rx_AFE [21]–[25].

In this paper, a 4-channel 100 Gbps Rx_AFE mainly consisted of a CG TIA with the local active feedback stage and an active negative and positive feedback LA is presented. To increase GBP of the local feedback stage in RGC TIA with the finite supply voltage, an additional common-gate (CG) amplifier is inserted before the traditional CS feedback stage, then the equivalent input impedance will decrease, and the bandwidth can be improved efficiently. At the same time, active feedback technique is used inside the local feedback stage to speed up the feedback signal and avoid inductive input impedance in low-frequency domain. Multi-stage configuration LA are adopted in this design to attain the expected voltage gain. Active negative and positive feedback technique is used to extend the deteriorated bandwidth by splitting and shifting the coincided poles. The proposed Rx_AFE exhibits a 3-dB bandwidth of 22.8 GHz and a transimpedance gain of 76 dBΩ, while a power of 226 mW is consumed from the supply voltage of 1.2 V. This paper is organized as follows: Section-2 describes the architecture of the proposed Rx-AFE, and the function of each portion is analyzed in brief. Section-3 analyzes the common-gate (CG) transimpedance amplifier with local active feedback stage and the active negative and positive feedback limiting amplifier, and various bandwidth extension techniques are adopted to optimize the performance of the Rx-TIA. Section-4 presents the measurement results while the discussion the conclusions and are drawn in section-5.

II. ARCHITECTURE OF THE PROPOSED Rx_AFE

The architecture of the proposed 4-channel Rx_AFE is shown in Fig. 1, and a CG TIA with active local feedback, an active negative and positive feedback LA, a DCOC (DC Offset Cancellation circuit) and a 50-Ω terminal output buffer are included in each channel.

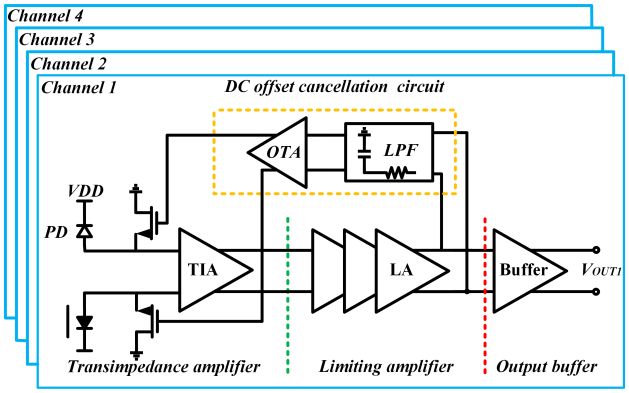

FIGURE 1. The architecture of the proposed 4-channel Rx_AFE.

The modulated optical signal is detected and converted into faint photocurrent by PD. Then the photocurrent will be converted into a voltage signal by TIA. The pseudo-differential TIA is employed to decrease common mode noise and improve stability. Multi-stage LA with active feedback is adopted to attain the expected bandwidth and voltage gain. The DCOC is consisted of a transconductance amplifier and a low pass filer (LPF), which is used to cancel the DC offset caused by manufacturing mismatch [26]. As the interface of the Rx-AFE, the double f_T output buffer is used to drive the load capacitance and provide a large output swing for measurements and practical applications [27].

III. CIRCUIT DESIGN

A. CG TIA WITH LOCAL CROSS-COUPLED ACTIVE FEEDBACK

To isolate the effect of PD's capacitance, RGC TIAs have been widely used for the fiber-optical Rx-AFE due to their relatively simple circuit topology and low input impedance [16]–[18]. The classic RGC TIA consisted of a common-gate (CG) main amplifier and a common-source (CS) local feedback amplifier is shown in Fig. 2. The input signal is inverted and amplified to the gate of M_1 by the CS local feedback amplifier. Thus, the effective transconductance of M_1 is increased and the equivalent input impedance is reduced. However, the CS local feedback gain of RGC TIA is constrained by the cascade of the gate-source voltage of M_1 and M_2 (V_{GS1} and V_{GS2}). According to the schematic of RGC TIA, the CS local feedback gain A_F can be expressed by

$$A_F = g_{m2}R_{D2} = \frac{2I_{D2}}{V_{GS2} - V_{TH}} \frac{(V_{DD} - V_{GS1} - V_{GS2})}{I_{D2}} \quad (1)$$

where the bias current of the CS local feedback amplifier is represented by I_{D2}, and V_{TH} is the threshold voltage of M_2. As indicated by the formulation (1), the only way to increase the A_F is reducing the value of V_{GS2}. To maintain constant V_{GS1}, the size of M_2 should be increased simultaneously.

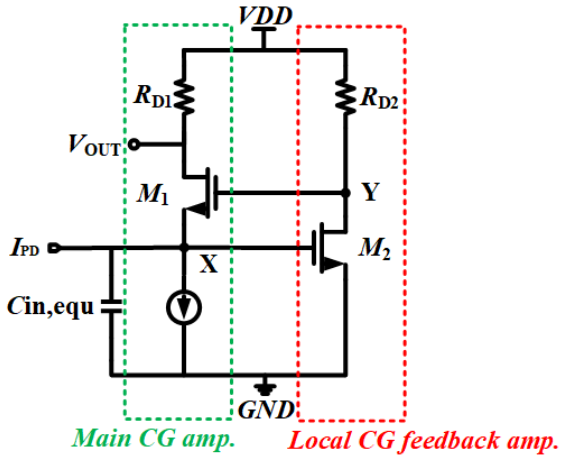

FIGURE 2. The topology of the classic RGC TIA.

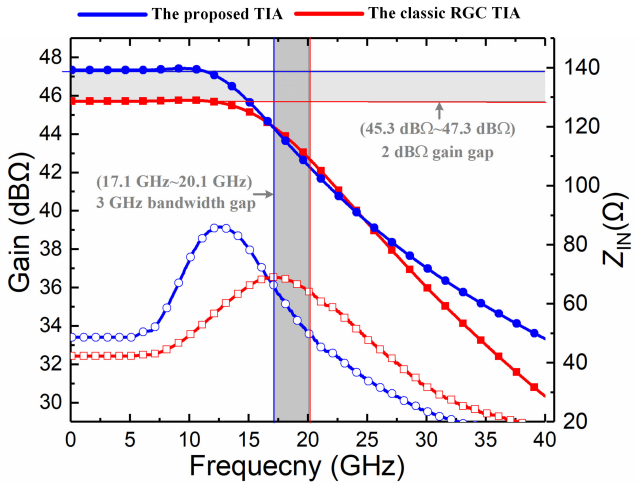

FIGURE 3. The simulated equivalent input impedance Z_{IN} and amplitude-frequency curves of the proposed TIA and RGC TIA.

However, the large M_2 will seriously deteriorate the pole frequency of the input node due to Miller capacitance. In addition, the value of V_{GS2} is also limited by the threshold voltage (V_{TH}).

To increase GBP of the local feedback with the finite supply voltage, a CG TIA with local cross-coupled active feedback is proposed and shown in Fig. 3. A CG amplifier is inserted before the traditional CS amplifier to relieve the voltage headroom and increase the feedback gain. Meanwhile, the Miller capacitance caused by the CS amplifier will be eliminated. However, the additional CG amplifier will lead to the bandwidth drop of the CGCS (Common-gate and common-source) local feedback stage due to the two coincident poles. The 3-dB bandwidth ($\omega_{3\text{-dB,CGCS}}$) of the CGCS local feedback stage can be calculated to be $0.64\omega_0$ according to the following transfer function expressed by

$$A_{\text{CGCS}}(s) = -\frac{A^2}{(1+s/\omega_0)^2} \tag{2}$$

with

$$A = g_{m3}R_{L3} = g_{m5}R_{L5} \tag{3}$$
$$\omega_0 = 1/R_{D3}C_{L3} = 1/R_{D5}C_{L5} \tag{4}$$

where g_{mx} represents the transconductance of M_X, and the load capacitance of each stage is C_{LX}. Generally, the dominant pole is located at the input node due to the big PD capacitance. However, when an additional CG amplifier is cascaded, $\omega_{3\text{-dB,CGCS}}$ will be close to the pole frequency of input node, which will lead to inductive input impedance. To increase the bandwidth of the CGCS local feedback stage, the cross-coupled active feedback stage is added inside the local feedback loop to improve the feedback-signal speed. The transfer function of the CGCS local cross-coupled active feedback stage is given by

$$A_{\text{AF-CGCS}}(s) = -\frac{A^2}{(1+s/\omega_0)^2 + A\cdot A_{\text{AF}}} \tag{5}$$

with

$$A_{\text{AF}} = g_{m\text{F}}R_{D3} \tag{6}$$

where $g_{m\text{F}}$ represents the transconductance of M_F. Due to the cross-coupled active feedback stage, the bandwidth of the CGCS local feedback amplifier can be extended efficiently. By setting $A_{\text{AF}} = A/4$, the bandwidth and gain the CGCS local cross-coupled active feedback stage are both larger than those of the CS feedback stage in RGC TIA. Thus, the simulated equivalent input impedance Z_{IN} of the proposed TIA shown in Fig. 3 is smaller at low frequency, and the peaking of Z_{IN} caused by the roll-off feedback gain appears later compared with RGC TIA.

The load impedance of each single stage (including the CG main stage and the CG and CS feedback stages) are represented by Z_{D1}, Z_{D3} and Z_{D5} separately. Then the transimpedance gain of the proposed CG TIA with local cross-coupled active feedback can be calculated from the half small signal model shown in Fig. 5:

$$Z_{\text{TIA}}(s) = \frac{-g_{m1}Z_{D1}(1+A_{\text{AF-CGCS}}(s))}{C_{\text{in,equ}}s + g_{m1}(1+A_{\text{AF-CGCS}}(s)) + g_{m3}} \tag{7}$$

with

$$A_{\text{AF-CGCS}}(s) = \frac{g_{m3}g_{m5}Z_{D3}Z_{D5}}{1+g_{m5}g_{m\text{F}}Z_{D3}Z_{D5}} \tag{8}$$

where $C_{\text{in,equ}}$ represents the equivalent input capacitance including PAD capacitance and the parasitic capacitances of M_1 and M_3. When $g_{m1}(1+|A_{\text{AF}}|) \ggg_{m3}$, the low-frequency transimpedance gain Z_{TIA} is approximately R_{D1}. And the denominator of the formulation (3) clearly indicates that the transconductance of M_1 is enlarged by the gain of the local feedback. By introducing an additional CG amplifier before the traditional CS feedback stage, the proposed TIA further increases the local feedback gain and reduces the equivalent input impedance with the finite supply voltage. Meanwhile, the active feedback technique is applied

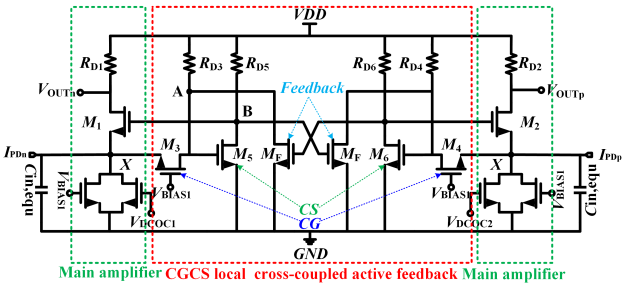

FIGURE 4. The topology of the proposed CG TIA with local cross-coupled active feedback.

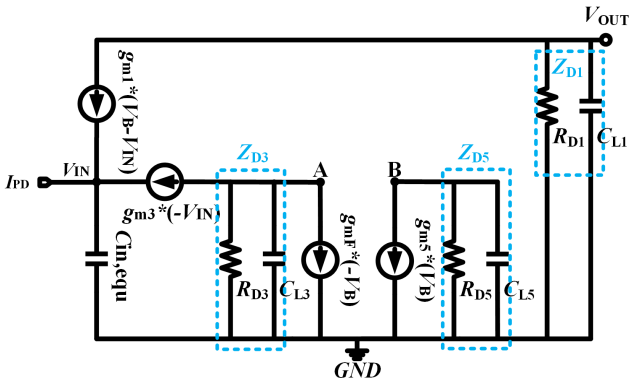

FIGURE 5. The half small signal model of the proposed CG TIA with local cross-coupled active feedback.

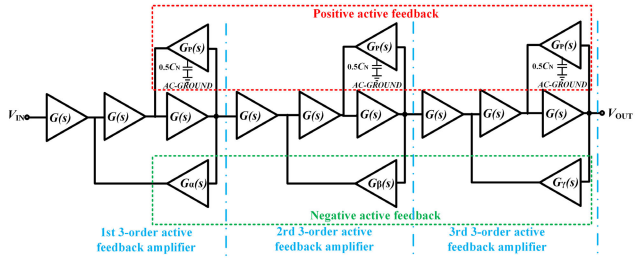

FIGURE 6. The architecture of the proposed active negative and positive feed-back LA.

to speed up the feedback signal to avoid inductive input impedance. As the simulation results of the transimpedance gain in Fig. 3 demonstrates, compared with the traditional RGC TIA, the proposed TIA has a broader bandwidth while exhibiting excellent gain flatness within the entire frequency bandwidth, because of the larger GBP of the CGCS local cross-coupled active feedback stage.

To evaluate the noise performance of the proposed TIA, the channel thermal noise of the active devices and the thermal noise of the resistor are considered. According to the half small signal model shown in Fig. 5, the noise voltage spectral density at output node can be given by

$$\begin{aligned}\overline{V_{\text{in,TIA}}^2} = &(R_{\text{D1}}\hat{I}_{\text{RD1}})^2 + (R_{\text{D3}}\hat{I}_{\text{D3}}A_{\text{OUT-A}})^2 \\ &+ (R_{\text{D5}}\hat{I}_{\text{D5}}A_{\text{OUT-B}})^2 + (R_{\text{D1}}\hat{I}_{\text{M1}})^2 \\ &+ (R_{\text{D3}}\hat{I}_{\text{M3}}A_{\text{OUT-A}})^2 + (R_{\text{D5}}\hat{I}_{\text{M5}}A_{\text{OUT-B}})^2 \end{aligned} \tag{9}$$

where the parameters $A_{\text{OUT-A}}$ and $A_{\text{OUT-B}}$ stand for the voltage gain from the output node to the node A and B separately. The noise voltage spectral density of the resistors and transistors can be calculated according to the van der Ziel model, then total input-referred noise current spectral density can be approximated by

$$\begin{aligned}\overline{I_{\text{in,TIA}}^2} \approx &\frac{4kT}{R_{\text{D1}}} + 4kT\Gamma g_{\text{m1}} \\ &+ (\frac{4kT}{R_{\text{D3}}} + 4kT\Gamma g_{\text{m3}})(g_{\text{m1}}g_{\text{m5}}R_{\text{D5}})^2 \\ &+ (\frac{4kT}{R_{\text{D3}}} + 4kT\Gamma g_{\text{m5}})(g_{\text{m1}})^2 \end{aligned} \tag{10}$$

where k is Boltzmann's constant, T is the absolute temperature, and Γ is the excess noise factor of short channel transistor. Obviously, the extra noise is introduced by the additional CG amplifier and increased with the local feedback gain. Therefore, the output resistance R_{D1} should be increased appropriately to alleviate the effect of the local feedback stage.

B. ACTIVE NEGATIVE AND POSITIVE FEEDBACK LIMITING AMPLIFIER

Due to the comparably lower transconductance of transistors in CMOS technology, multi-stage configuration is often adopted to achieve the required voltage gain in the design of LA. But the sharp roll-off amplitude-frequency response of LA will cause the decreasing bandwidth. Active feedback technique can separate the coincide poles into the complex conjugate poles to increase the bandwidth, such as 3rd-order active feedback LA. However, when the 3-order active feedback stages with the same structure (CS amplifier) and parameters are cascaded, the complex conjugate poles will overlap, which would lead to attenuation (when the damping factor of pairs of conjugate poles with $\xi > 1/\sqrt{2}$) or the gain peaking (when the damping factor of pairs of conjugate poles with $\xi < 1/1/\sqrt{2}$).

To avoid the above-mentioned phenomenon, the complemented active negative feedback technique and active positive feedback technique are proposed and adopted in this paper. The architecture of the proposed active negative and positive feedback limiting amplifier is shown in Fig. 6, where the CS amplifier is used as the main stage, and three complementary negative feedback stages with different low-frequency gain (α, β, γ) are separately introduced between main stages to cause the differentiation of the complex conjugate poles. In addition, the position of the conjugate poles is adjusted by introducing the active positive feedback stage between the main stages to eliminate gain ripple.

To determine the feedback gain of each negative feedback stage, the active positive feedback stages are neglected. Then the complementary active negative feedback LA can be equivalently transformed into the 3rd-order interleaving active negative feedback LA presented in [21]. To simplify

the analysis, the gain of the main stage and the feedback stage are approximated by the single-pole stages expressed as

$$G(s) = \frac{A}{(1+s/\omega_0)}, \quad G_\alpha(s) = \frac{\alpha}{(1+s/\omega_0)} \tag{11}$$

$$G_\beta(s) = \frac{\beta}{(1+s/\omega_0)}, \quad G_\gamma(s) = \frac{\gamma}{(1+s/\omega_n)} \tag{12}$$

with

$$\omega_0 = 1/R_D C_L, \quad A = g_m R_D \tag{13}$$

$$\alpha = g_{m\alpha} R_D, \quad \beta = g_{m\beta} R_D, \ \gamma = g_{m\gamma} R_D \tag{14}$$

where R_D and C_L are respectively the resistive and capacitive loads of the main stage, and the low-frequency gain of the main stage are represented by A. In addition, the transconductance of the main stages is expressed g_m, and the transconductances of three different negative feedback stages are expressed as $g_{m\alpha}$, $g_{m\beta}$ and $g_{m\gamma}$ respectively. According to Mason formulation, the transfer function of the complemented active negative feedback LA can be given by

$$H_a(s) = \frac{A^9}{(1+\frac{s}{\omega_0})^9 + 5A^2\lambda(1+\frac{s}{\omega_0})^6 + 6A^4\lambda^2(1+\frac{s}{\omega_0})^3 + A^6\lambda^3} \tag{15}$$

with

$$\alpha \cdot \beta \cdot \gamma = \lambda^3, \alpha + \beta + \gamma = 5\lambda, \alpha\beta + \alpha\gamma + \beta\gamma = 6\lambda^2 \tag{16}$$

where λ is the low-frequency feedback gain of the 3rd-order interleaving active negative feedback LA. As the feedback gain λ varies, the different amplitude-frequency responses are plotted in Fig. 7. To attain better bandwidth, the value of λ is set 0.3 corresponding to the different negative feedback gains ($\alpha = 0.974$, $\beta = 0.466$, $\gamma = 0.059$). In such a case, the amplitude-frequency response exhibits a 3-dB bandwidth of $1.7\omega_0$, a voltage gain of 39.4 dBΩ, but a gain peaking up to 3 dB.

From the above analysis, it is observed that the complementary active feedback circuit can extend the bandwidth deteriorated by the cascade of main stages because of the pole splitting effect. However, to attain the larger bandwidth, the value of λ is a little higher, which leads to 3-dB gain peaking inevitably. By introducing active positive feedback amplifier in each 3rd-order active stage, the negative capacitance generated can adjust the position of the complex conjugate poles, and the severe gain peaking can be overcome efficiently.

The schematic and the small signal model of main stage with active positive feedback are shown in Fig. 8(a) and 8(b) respectively (To facilitate the calculation, the correlative CS stages are included to calculate the transfer function of the active positive feedback stage). The analysis of the small signal model provides the transfer function of main stage with

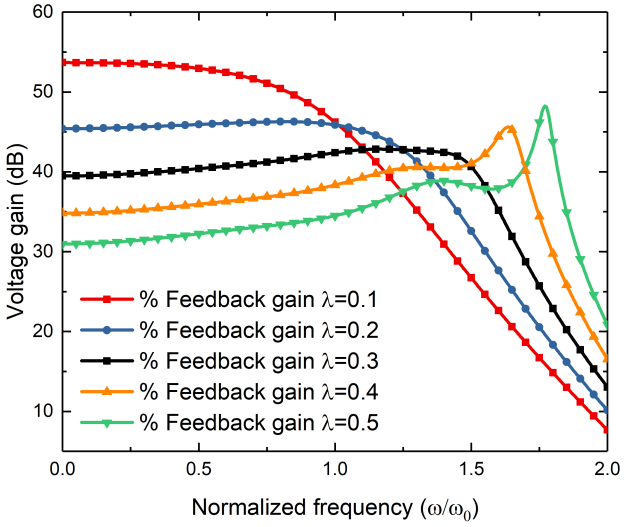

FIGURE 7. The amplitude-frequency response of the complementary active negative feedback LA with different value of λ.

active positive feedback stage as

$$G_{APF}(s) = \frac{V_{AB}}{V_{IN}} = \frac{-g_m R_D}{1 + sR_D(C_L - \frac{g_m R_D g_{m1} C_N}{g_{m1}+C_N})} \approx \frac{-g_m R_D}{1 + sR_D(C_L - g_{m1} R_D C_N)} = \frac{-A}{1+\frac{s}{\theta\omega_0}} \tag{17}$$

with

$$\theta = C_L/(C_L - AC_N) \tag{18}$$

when

$$\omega \ll g_{m1}/C_N \tag{19}$$

where the transconductance of M_1 is expressed by g_{m1}, and C_N is the source degradation capacitance in active feedback stage. It is clearly that the negative capacitance is added in parallel with the load of the CS amplifier. Then pole frequency of the second main stage in each 3rd-order active negative feedback stage can be increased. By substituting (17) into (15), the transfer function of the active negative and positive feedback LA is given by

$$H_b(s) = \frac{A^9}{(1+\frac{s}{\omega_0})^6(1+\frac{s}{\theta\omega_0})^3 + 5A^3\lambda(1+\frac{s}{\omega_0})^4(1+\frac{s}{\theta\omega_0})^2 + 6A^6\lambda^2(1+\frac{s}{\omega_0})^2(1+\frac{s}{\theta\omega_0}) + A^6\lambda^3} \tag{20}$$

Based on the transfer function in (20), the simulated amplitude-frequency response and pole map with different values of θ are depicted in Fig. 9. When θ is set 2.5, corresponding to $C_P = C_N/4$, the amplitude-frequency response of the active negative and positive feedback LA is depicted by blue. Compared with the amplitude-frequency response (derived from the formulation (15) or formulation (20) with θ =1) depicted by the red curve, the poles position of the active negative and positive feedback LA all move to the

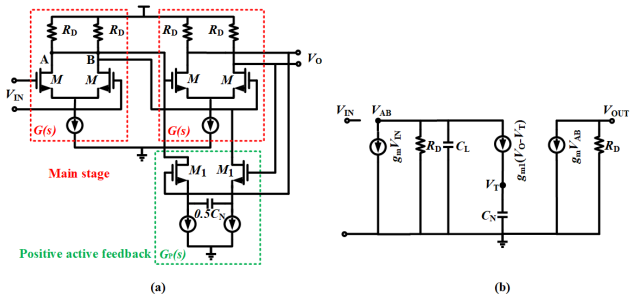

FIGURE 8. The schematic and the small signal model of the main stage with active positive feedback.

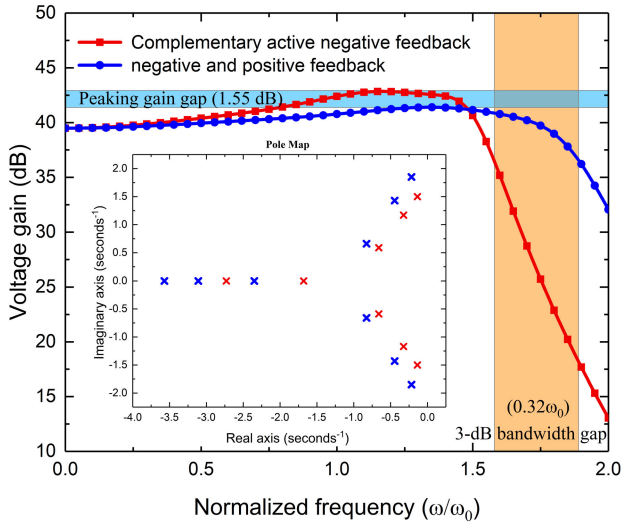

FIGURE 9. The simulated amplitude-frequency response and pole map of the active negative and positive feedback LA with the different value of θ.

higher-frequency position as shown in the pole map because of the negative capacitance. Then the 3-dB bandwidth of the active negative and positive feedback LA reaches up to $1.98\omega_0$ without the gain losses. Furthermore, the excess gain peaking near the roll-off frequency is effectively suppressed to be just 1.45 dB, exhibiting excellent gain flatness within the entire frequency bandwidth.

IV. MEASUREMENTS

The die micrograph of the proposed 4-channel 100 Gbps Rx-AFE and the layout details of each channel are shown in Fig. 10. The layout of each channel is surrounded by deep well guard rings, so that the coupling noise of supply and substrate from adjacent channels can be suppressed by the reversed pn junction. Implemented in a 55nm CMOS technology, the whole chip including pads occupies an area of 800 μm $\times$ 1800 μm, whereas the core area of each channel is only 275 μm $\times$ 650 μm. In addition, the test chip consumes a power of 226 mW from 1.2 V supply voltage, exhibiting a power efficiency of 2.3 mW/Gb/s.

To characterize the small-signal performance of the proposed Rx-AFE, the S-parameter of each channel was measured with the network analyzer separately. The S-parameter curves of channel 1 are demonstrated in Fig. 11. As could be seen from the S-parameter curves, 3-dB bandwidth of the proposed Rx-AFE reaches 22.8 GHz, while maintaining an output return losses S22 better than -12 dB and an input return losses S11 better than -15 dB. As the same time, the differential trans-impedance gain at middle frequency can be calculated to be 76 dBΩ based the S-parameter measured. It is noted that differential gain is 6 dBΩ higher than single-ended gain directly computed by S-parameter characteristic impedance.

The frequency response of the crosstalk between adjacent channels (channels 1 and 2) is shown in Fig. 12. The measured crosstalk between the channels is less than -22 dB within the entire 3-dB bandwidth range.

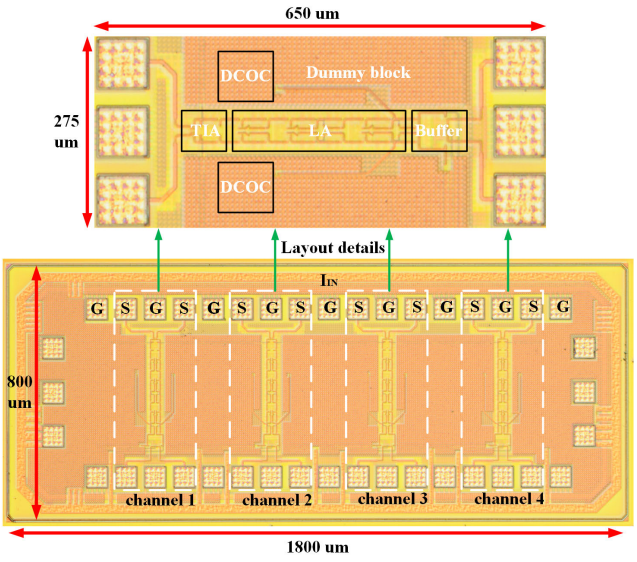

FIGURE 10. The die micrograph of the proposed 4-channel Rx-AFE and the lay-out details of each channel.

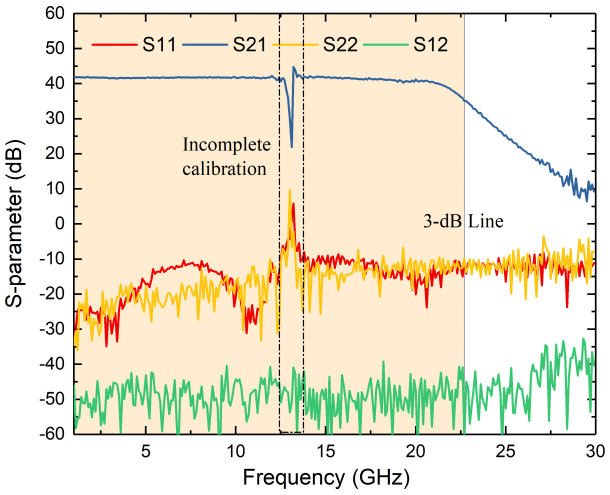

FIGURE 11. The measured S-parameter curves.

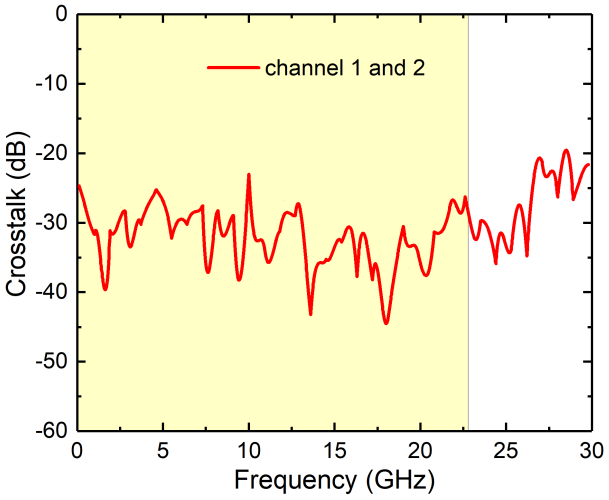

FIGURE 12. The measured crosstalk between adjacent channels.

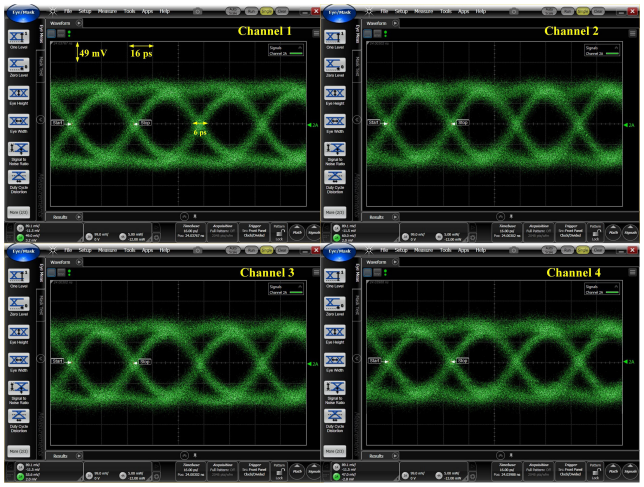

FIGURE 13. The 25-Gbps eye diagrams of four channels.

To evaluate the transient-response specifications, 2^{31}-1 pseudo-random bit sequence (PRBS31) of 25 Gbps was generated by the pattern generator and then attenuated by the cascade of two attenuations. The attenuated signal was transmitted to the circuit through the GSGSG probe. The single-end eye diagrams of four channels with 2.5-$mV_{p\text{-}p}$ input swing are shown in Fig. 13. Obviously, the single-end voltage swing of four eye diagrams is about 155 $mV_{p\text{-}p}$ and the horizontal jitter is about 6 ps.

Then the single-end transimpedance gain of the circuit can be calculated to be approximately 70 dBΩ based on 50-Ω characteristic impedance, which is consistent with the results estimated by the measured S-parameter. The 25-Gbps eye diagrams with the input swing of 3.5 $mV_{p\text{-}p}$ and 5 $mV_{p\text{-}p}$ are shown in Fig. 14 separately. When the peak-to-peak value of the input signal reaches 5 $mV_{p\text{-}p}$, the maximum single-end output swing (215 $mV_{p\text{-}p}$) can be acquired.

For 25 Gbps PRBS7 data pattern, the electrical sensitivity was measured to be 2.5 $mV_{p\text{-}p}$ (1.25 $mV_{r.m.s}$) for a BER

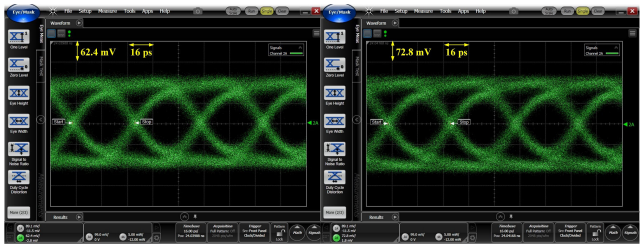

FIGURE 14. The 25-Gbps eye diagrams with the input swing of 3.5 $mV_{p\text{-}p}$ and 5 $mV_{p\text{-}p}$.

TABLE 1. Comparison between the proposed design and state-of-the-art works.

Metric	[3]	[7]	[16]	This work
Bandwidth (GHz)	21	22.8	23.2	22.8
Data rate (Gbps)	100	100	100	100
Transimpedance gain (dBΩ)	72.5	69.8	74.3	76
Power consumption (mW)	276	296	304	226
Power Efficient (mW/Gb/s)	2.7	3	3	2.3
Electrical sensitivity (mV)	5	9	6	2.5
Chip area/channel (mm^2)	/	0.4	0.2	0.18
Technology (nm)	65	65	65	55

of 10^{-12}. The input referred RMS noise current $I_{\text{in,TIA}}$ of the circuit could be estimated by the electrical sensitivity according to the following relationship:

$$I_{\text{in,TIA}} = \frac{I_{\text{in,min}}}{Q} \tag{21}$$

where Q denotes the value of the "Q-function" to maintain a certain BER (Q = 7.4 for BER = 10^{-12}), and $I_{\text{in,min}}$ represents the minimum RMS input current calculated to be 33.8 $\mu A_{\text{r.m.s}}$ by 50 Ω input impedance [28]. The average input noise current spectral density $\overline{I_{in,TIA}}$ can be estimated to be 22.3 pA/$\sqrt{\text{Hz}}$ by

$$\overline{I_{\text{in, TIA}}} \approx \frac{I_{\text{in, TIA, tot}}}{\sqrt{BW}} \tag{22}$$

where BW represents the 3-dB bandwidth of the circuit.

V. DISCUSSION AND CONCLUSION

Table 1 outlines the performance of this work and other state-of-the-art Rx-AFEs. Due to the adoption of the inductorless bandwidth extension techniques, the proposed 100 Gbps Rx-AFE has demonstrated a comparable bandwidth and a better sensitivity with a less core area consumption when compared with the other respectable state-of-the-arts.

A 4-channel, 100 Gbps inductorless optical receiver analog front-end is implemented in a 55 nm bulk-CMOS technology. A CG TIA with cross-coupled active feedback is proposed to decrease the equivalent input impedance by increasing the local feedback gain in the entire frequency bandwidth. And multi-stage LA with active negative and positive feedback can attain the expected transimpedance gain and bandwidth because of the pole splitting effect. In addition, a direct offset cancellation circuit is adopted to ensure the stability of the

Rx-AFE, and a double f_T buffer is used as the interface of the circuit. The whole chip including pads occupies an area of 800 μm × 1800 μm. The measurements indicate that the 3-dB bandwidth of the circuit reach 22.8 GHz, the sensibility is 2.5 mV for a BER of 10^{-12} at 25-Gbps PRBS7 operation, and the power efficiency is just 2.3 mW/Gb/s. The proposed Rx-AFE provides a promising potential for low-cost, low-power, and high-performance solution for 100-GbE systems.

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