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Breaking the Limits in Ternary Logic: An Ultra-Efficient Auto-Backup/Restore Nonvolatile Ternary Flip-Flop Using Negative Capacitance CNTFET Technology

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ABSTRACT Despite the advantages of ternary logic, it has suffered from excessive transistor count and limited noise margin. This work proposes an ultra-efficient nonvolatile ternary flip-flop (FF) based on negative capacitance carbon nanotube field-effect transistors (NC-CNTFETs). By harnessing the negative differential resistance effect in NC-CNTFETs, the proposed design is similar to a conventional volatile binary FF regarding the number of transistors and control signals. During a scheduled power gating or a sudden power outage, the proposed ternary FF benefits from an auto-backup/auto-restore capability without employing any additional transistors, nonvolatile devices, or control signals. This leads to zero device overhead, which is a breakthrough in designing nonvolatile memory circuits. On the other hand, the back-to-back slave latch's hysteretic behavior provides an extraordinary static noise margin that transcends the noise margin of both conventional ternary and binary latches. The simulation results indicate that eliminating additional backup and restore circuitries provides 43% improvements in transistor count, 59% improvements in power saving and 98% improvements in energy-saving than state-of-the-art binary and ternary FFs. Moreover, the proposed design presents a 1.5 times higher static noise margin than the conventional binary and ternary FFs. Our proposed approach opens new doors in realizing ultra-efficient nonvolatile ternary circuits and systems in neuromorphic applications using ferroelectric-based transistors.

INDEX TERMS Ternary flip-flop, nonvolatile, auto-backup, auto-restore, noise margin, NC-CNTFET.

I. INTRODUCTION

The earth is replete with tremendous energy resources that can answer any requirement. However, we utilize them much faster than their production. Energy conservation in every field plays a pivotal role in improving human life. The simplest way to mitigate electrical energy dissipation is to turn off the electrical devices when they are not in use. However, they may continue to draw power, and the only way to truly power down is to unplug the devices. However, when keeping the circuit's current information is crucial, the power supply cannot simply be unplugged. Therefore, nonvolatile components can be employed as a versatile solution to cope with this problem [1].

By Utilizing various memory elements such as magnetic tunnel junctions, floating gate devices, ReRAMs, and memristors, chip designers and manufacturers have tried to present high-performance and energy-efficient nonvolatile circuits [2], [3]. However, the energy dissipation and area overhead of nonvolatile circuits are not ignorable. Many authors have focused on designing efficient nonvolatile memory circuits. Most of them necessitate extra peripheral backup

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and restore circuitries, resulting in a noticeable increment in transistors count and energy dissipation [4]–[6].

On the other hand, implementing backup and restore structures becomes more complicated for nonvolatile circuits with more than the binary logical state. They require complex wiring, additional clock, and control signals, which cause area, energy, and delay overhead [7]–[11].

Ferroelectric field-effect transistors (FeFETs) have recently been introduced as encouraging candidates to overcome the inherent limitations in conventional silicon-based technologies [12], [13]. FeFETs presents two intriguing features: steep-slope and hysteresis operation modes. It has recently been demonstrated that the benefit of steep-slope operation mode is faded in the nanoscale transistors with a high density of states channel materials such as carbon nanotubes, molybdenum disulfide, and graphene nanoribbons. FeFETs with nonvolatile behavior and rich polarization switching dynamics are the focal point of ultra-efficient neuromorphic applications such as spiking neural networks [14] and chaotic oscillators [15]. Using the hysteretic feature of FeFETs is a promising alternative for constructing new generations of nonvolatile neuromorphic systems. Therefore, the hysteresis feature remains the primary advantage of the FeFETs [16].

Conventional complementary metal-oxide-semiconductor (CMOS) transistors are challenging for ultra-scaling purposes due to the emerging catastrophic short channel effects (SCEs) [17]. Considering the various candidates, carbon nanotube FET (CNTFET) with superior mobility, long mean free path, fascinating current delivery capability, ballistic transport regime operation, suppressed short channel effects, and the ease of integration with CMOS fabrication process has been emerged as one of the most feasible next commercial technologies [18]. The threshold voltage of CNTFETs can be harnessed through the chirality concept and flat-band voltage, making them appealing for multi-valued logic (MVL), especially ternary arithmetic circuits and systems [19]–[21].

Despite several achievements of ternary logic, such as offering significant advantages to reduce the number of interconnects, the complexity of operations, and increasing data density, ternary logic circuits are engaged with two substantial problems: (1) high transistor count, and (2) low noise margin [21]–[24]. The excessive number of transistors in conventional ternary logic circuits raises a significant energy dissipation and enlarges the chip area. On the other hand, the ternary arithmetic circuits' limited noise margin hampers further downscaling in terms of the supply voltage and the total footprint [25].

It has recently been demonstrated that by employing the negative differential resistance (NDR) effect in the negative capacitance CNTFETs (NC-CNTFETs), ternary logic gates can be realized with structures similar to their binary counterparts [26]. Despite significant energy saving and compression, these ternary logic gates require different flat-band voltages for correct operation.

By virtue of the outstanding electronic properties of NC-CNTFETs, in this work, we propose an innovative design strategy to demonstrate a low-voltage ternary nonvolatile flip-flop (TNVFF). By utilizing the NDR effect in NC-CNTFETs, both master and slave ternary latches of the proposed TNVFF have a similar transistor count to the conventional volatile binary latches. During the power gating or a sudden power outage, the proposed TNVFF has been designed in a particular way that does not need any peripheral circuitry for backup and restore operations. As a result, the proposed design exploits fewer transistors and shows significant energy saving than all previous NVFFs in binary and ternary fashions. The main contributions of this work are summarized as follows:

- Equal transistor count (16 transistors) of the proposed TNVFF to the volatile binary FF
- Auto-backup and auto-restore capabilities during power gating and even sudden power outage without using any additional transistors and control signals
- Elimination of the need for extra wiring of control signals and their related circuits for backup and restore operations
- No energy and latency overheads during backup and restore operations as a critical issue in all of the previous related binary and ternary NVFFs
- The achieved static noise margin (SNM=224mV) is higher than the conventional ternary (SNM=112mV) and even binary (SNM=208mV) volatile FFs due to the superior noise margin of the hysteretic ternary latches
- The capability of operation in low supply voltages due to the superior noise margins, a far-fetched goal for the other conventional ternary NVFFs

Following this introductory section, an overview of the fundamental platform and the research's basic theory is provided in Section II. Section III presents the proposed design methodology of the proposed TNVFF. Comprehensive simulations are carried out in Section IV. Finally, the main results are highlighted in Section V.

II. PLATFORM AND BASIC THEORY

During the last few years, negative capacitance FETs with outstanding electronic properties have gained considerable attention as a potential candidate beyond conventional CMOS technology [12], [13], [27]. A negative capacitance transistor's functionality depends on two fundamental factors: (1) the utilized ferroelectric material, and (2) the baseline transistor.

Negative capacitance can be realized by perovskite-based or doped HfO_2-based ferroelectrics. The conventional perovskite-based ferroelectrics are dealing with ferroelectricity sustainability problems for thicknesses below 50nm [28]. On the contrary, doped HfO_2 ferroelectric materials present robust 10-30$\mu C/cm^2$ remnant polarization within a range of 5nm-30nm thickness [29]. It was experimentally proven in the literature that the Si dopant shows stable remnant polarization in HfO_2 ferroelectrics under different thicknesses [30], [31]. Various nanoscale transistors can be served as the baseline devices to realize a negative capacitance FET.

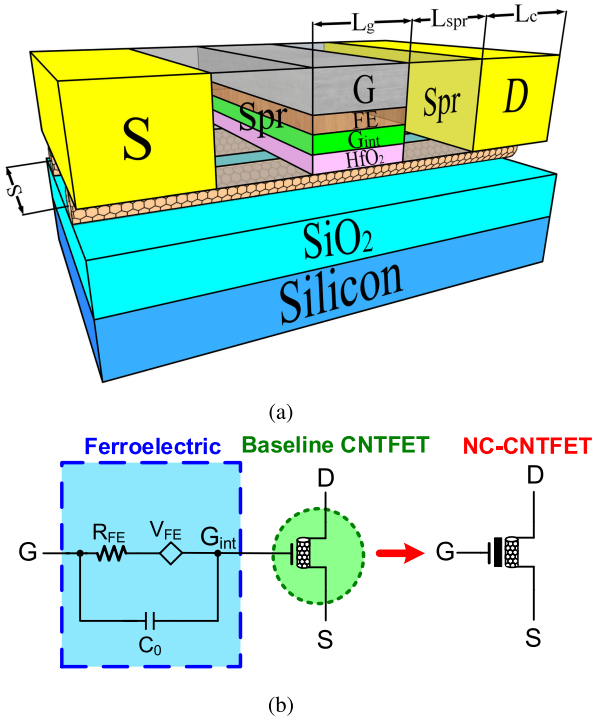

FIGURE 1. (a) The 3D representation (b) the equivalent circuit of a NC-CNTFET. R_{FE} and C_0 denote the parasitic RC components of the ferroelectric.

Carbon nanotube FETs with high carrier mobility, excellent I_{ON}/I_{OFF} ratio, and superlative immunity to the SCEs are known as the future commercial technology beyond silicon-based transistors [18].

The 3D illustration and the equivalent circuit of the modelled NC-CNTFET are shown in Fig. 1. It is worth noting that a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure has been considered due to the better I_{ON}/I_{OFF} current ratio for ultra-scaled dimensions [12]. In a NC-CNTFET, parallel semiconducting carbon nanotubes are placed over an insulator such as SiO_2 to establish the channel region. A high-k dielectric material such as hafnium oxide (HfO_2) is then utilized to restrain the gate leakage current and provide better gate electrostatic characteristics. After forming a thin metal intermediate layer, a Si-doped HfO_2 ferroelectric, an appropriate choice for nonvolatile memory applications, is aligned on top of the gate dielectric to construct the negative capacitance. Subsequently, a thin metal layer such as palladium or tantalum is deposited to accomplish the external gate contact. It is worthwhile to mention that a spacer region is used to restrict the carriers' ambipolar conduction between source and drain contacts [18], [32].

In this work, the Stanford virtual-source Verilog-A compact model has been utilized for the baseline CNTFET considering nonidealities such as band-to-band and direct source-to-drain tunneling leakage currents [33]. This compact model is calibrated with an experimentally reported CNTFET device with 1.2nm CNT diameter [34].

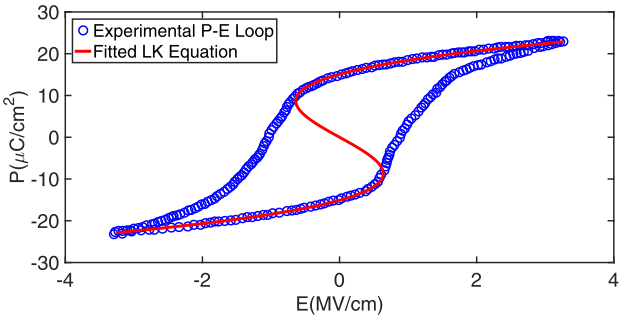

FIGURE 2. A comparison between the fitted LK equation and the experimental P-E loop of a 10nm fabricated Si-doped HfO_2 ferroelectric presented in [31].

The time-dependent Landau-Khalatnikov (LK) equation is utilized to include the negative capacitance behavior of the ferroelectric as follows [35]:

$$E = \alpha P + \beta P^3 + \gamma P^5 \tag{1}$$

where α, β, and γ are the ferroelectric static constant parameters, and E and P are the electric field and polarization, respectively.

Considering $E = V_{FE}/t_{FE}$ and $Q_{FE} = A_{FE}P$, the voltage drop (V_{FE}) across the ferroelectric can be related to the ferroelectric thickness as:

$$V_{FE} = \rho R_{FE}\frac{dQ_{FE}}{dt} + \frac{t_{FE}}{A_{FE}}\left(2\alpha Q_{FE} + \frac{4\beta Q_{FE}^3}{A_{FE}^2} + \frac{6\gamma Q_{FE}^5}{A_{FE}^4}\right) \tag{2}$$

where t_{FE} and A_{FE} are the ferroelectric thickness and area respectively, Q_{FE} is the ferroelectric charge density, and ρ is the kinetic parameter to include the ferroelectric's dynamic behavior. More descriptions regarding the ferroelectric parameters are described in detail in [35], [36].

The LK equation of the modelled NC-CNTFET has been adjusted with a fabricated 10nm Si-doped HfO_2 ferroelectric suitable for nonvolatile memory applications to portray a realistic picture of the proposed TNVFF [31].

A comparison between the fitted LK equation of the modelled NC-CNTFET and the experimentally reported Si-doped HfO_2 ferroelectric is indicated in Fig. 2. The developed NC-CNTFET model's vital parameters used to implement the proposed TNVFF are tabulated in Table 1.

The utilized Si-doped HfO_2 ferroelectric had experimentally shown a $13\mu C/cm^2$ remnant polarization and 0.85MV/cm coercive field [31].

Fig. 3 shows the NC-CNTFET current delivery considering various ferroelectric thicknesses. It can be observed that increasing the ferroelectric thickness improves the device on-current, and simultaneously, reduces the leakage current thanks to the negative capacitance feature that amplifies the internal gate electric field. On the other hand, operating in the ballistic transport regime with the long mean free path and superior carrier mobility of carbon nanotube transistors are fundamental features that enhance the current delivery.

TABLE 1. Some of the vital parameters of the modelled NC-CNTFET technology.

Device Parameter	Value
Physical gate length (L_g)	14nm
Physical gate width (W_g)	20nm
Physical gate height (H_g)	15nm
Oxide thickness (t_{ox})	4nm
Ferroelectric thickness (t_{FE})	10nm
Source/drain contact length (L_c)	14nm
Carbon nanotube diameter (D_{CNT})	1.2nm
Source/drain spacer region length (L_{spr})	5nm
CNT center-to-center inner pitch (S)	8nm
Source/drain Fermi level (E_{FSD})	0.258eV
Gate dielectric constant (K_{ox})	16
Substrate dielectric constant (K_{sub})	3.9
Channel material dielectric constant (K_{ch})	1
Ferroelectric constant parameter (α)	$-5.5 \times 10^8 m/F$
Ferroelectric constant parameter (β)	$1.21 \times 10^{10} m^5/F/C^2$
Ferroelectric constant parameter (γ)	$0 m^9/F/C^4$
kinetic coefficient (ρ)	$0.025\,(\Omega/m)$
Ferroelectric coercive field (E_c)	$0.85 MV/cm$
Ferroelectric remnant polarization (P_r)	$13 \mu C/cm^2$
Model temperature	25^oC

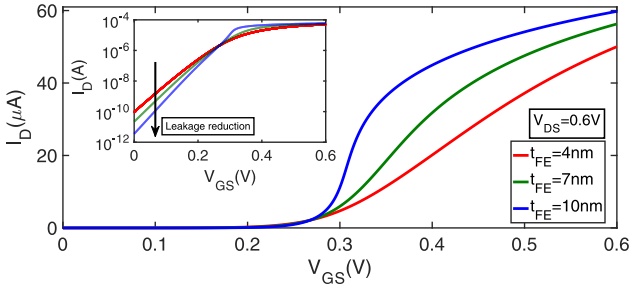

FIGURE 3. The NC-CNTFETs' current delivery capability.

For the 10nm ferroelectric thickness (based on a fabricated ferroelectric capacitor [31]), the NC-CNTFET shows 60μA oon-current and the extremely low leakage current of 3.5pA (see the inset plot in Fig. 3). Accordingly, by presenting a superb $I_{ON}/I_{OFF} = 1.7 \times 10^7$ ratio and extreme low internal capacitance of NC-CNTFETs, these transistors are potential candidates for demonstrating ultra-efficient and high-performance digital circuits and systems.

The output characteristics ($I_D - V_{DS}$) of the modelled NC-CNTFET is depicted in Fig. 4a. Since our primary focus is to exploit the nonvolatile feature, the steep-slope switching performance analysis has been omitted. After interpreting the results, it can be observed that for lower V_{GS} values, increasing the ferroelectric thickness causes a negative slope in the NC-CNTFET current. This phenomenon, known as the NDR effect, is the basis of the ferroelectric FETs nonvolatile memory applications [26].

The transfer ($I_D - V_{GS}$) characteristics of the modelled NC-CNTFET is shown in Fig. 4b. It can be observed that the positive increment of V_{GS} beyond the critical gate-to-source voltage, V_{GSC}, (which is smaller than the coercive voltage) would positively polarize the NC-CNTFET. At this condition,

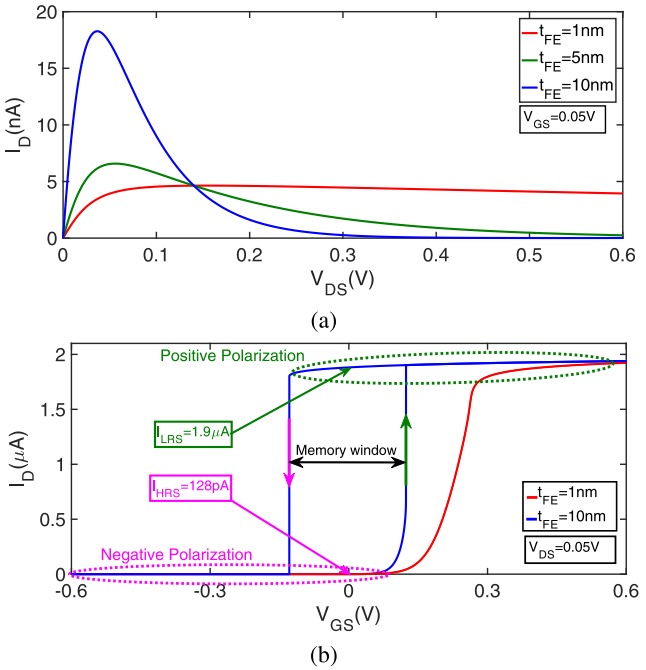

FIGURE 4. (a) The output and (b) the transfer characteristics of the modelled NC-CNTFET under different ferroelectric thickness.

the NC-CNTFET presents a low-resistance state (LRS) with a considerable on-current. Correspondingly, a V_{GS} lower than $-V_{GSC}$ would negatively polarize the ferroelectric layer in the NC-CNTFET gate-stack and leads to a low-to-high resistance state (HRS). The positively and negatively polarized NC-CNTFET can retain its condition even for $V_{GS} = 0V$. These two stable states at $V_{GS} = 0V$ with a significant current ratio of $I_{LRS}/I_{HRS} > 10^4$ makes the modelled NC-CNTFET highly desirable for nonvolatile memory applications. It is noteworthy that a wider hysteresis loop can be achieved at the cost of increasing the ferroelectric thickness. Since the negative capacitance behavior of the ferroelectric layer is completely matched with the experimental results [31] (see Fig. 2), we have considered 10nm constant ferroelectric thickness.

III. PROPOSED DESIGNS

In this section, by employing the magnificent electrical properties of the NC-CNTFET, we demonstrate a low-voltage TNVFF. First, we demonstrate a Schmitt trigger-based, two transistors standard ternary inverter (STI) with an enhanced noise margin beyond the conventional ternary and even binary inverters. Then, we harnessed the proposed Schmitt trigger-based STI to propose an ultra-efficient TNVFF with auto-backup and auto-restore properties.

A. DEMONSTRATION OF THE HYSTERETIC STI GATE

During the past few years, carbon nanotube FETs had paved the way for presenting ternary logic circuits. However, these circuits suffer from high transistor count and feeble noise margin [21], [22]. Recently, by employing the NDR effect

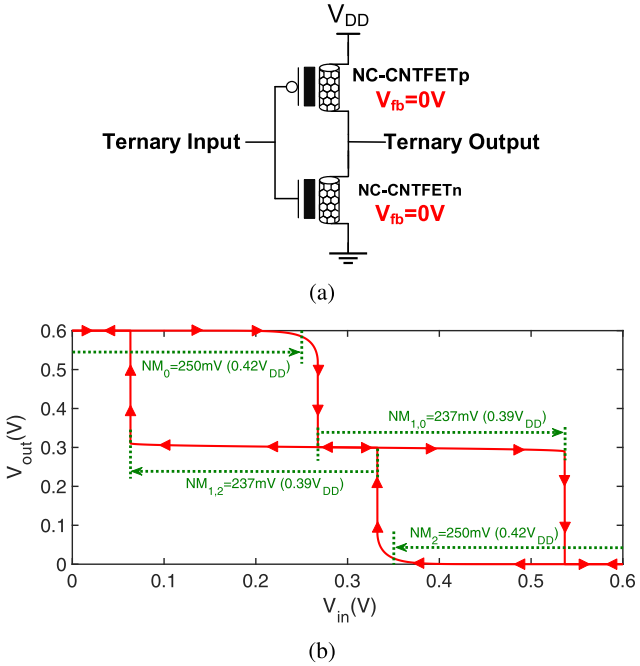

FIGURE 5. (a) The circuit illustration and (b) the VTC of the proposed NC-CNTFET-based STI gate.

observed in NC-CNTFETs, an STI gate with a similar transistor count to its conventional binary counterpart has been presented in [26]. However, the physical device engineering, such as different flat-band voltages was essential to acquire a voltage transfer characteristic (VTC) similar to the conventional STI gates.

The circuit illustration and the related VTC of the Schmitt trigger-based STI gate are given in Fig. 5. The demonstrated Schmitt trigger-based STI gate operates with 0V flat-band voltage and does not need various flat-band voltages, which is highly suitable for practical implementations based on commercial technologies. Choosing appropriate values for the ferroelectric thickness generates the NDR in both n-type and p-type NC-CNTFETs. As a result, the VTC of the STI gate shows ternary behavior. In the demonstrated VTC and according to the observed hysteretic behavior of the modelled NC-CNTFET (see Fig. 4b and Table. 1), when the input voltage raises to V_{DD}, the on-resistance of NC-CNTFETp (NC-CNTFETn) would decreases (increases). Therefore, the proposed VTC shifts to the right (see Fig. 5b). Similarly, when V_{in} reduces from V_{DD} to 0V, the on-resistance of NC-CNTFETn (NC-CNTFETp) decreases (increases). In this situation, the VTC of the STI gate shifts to the left side (see Fig. 5b). Based on this unique behavior, a Schmitt trigger-based STI gate is demonstrated by utilizing only two transistors (similar to a conventional binary inverter). This extraordinary feature of this 2-transistors NC-CNTFET-based STI was not demonstrated in [26].

We have performed a quantitative comparison between the noise margin of the 2-transistors NC-CNTFET-based Schmitt trigger STI (237mV, 39% of V_{DD}), the conventional

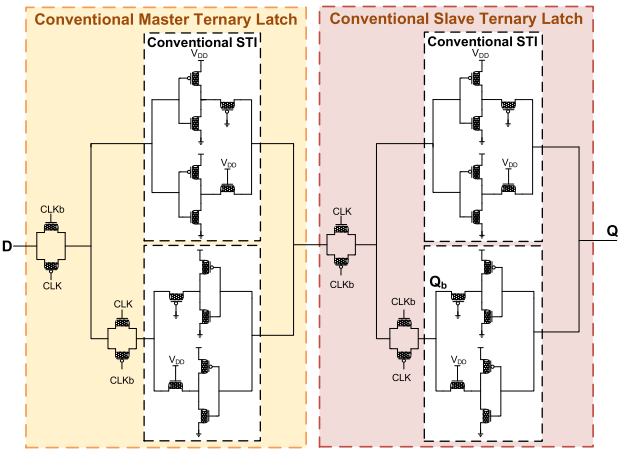

FIGURE 6. A conventional ternary volatile flip flop in CNTFET technology.

6-transistors (6T) STI [37] (129mV), and the conventional 2-transistors binary inverter (208mV). The conventional 6T STI and binary inverter gates have efficiently been designed and optimized based on the baseline CNTFET technology to have a fair meaningful comparison. Notably, the CNTFETs of the conventional 6T STI require different flat-band voltages for the correct operation [37], which is an innate shortcoming. According to the results from Fig. 5b and the resulted noise margin, the demonstrated STI gate is a striking achievement due to removing noise margin restrictions as the longstanding historical barrier of the ternary logic gates without imposing any additional transistors. Owing to the Schmitt trigger behavior of the VTC, the demonstrated STI indicates 237mV noise margin, surpassing the ideal noise margin limitation of the STI gate (V_{DD}/4=150mV). Astoundingly, the resulted noise margin of the proposed 2T STI (237mV) is even higher than a conventional binary inverter (208mV) based on the baseline CNTFET technology. It is essential to point out that the binary Schmitt triggers can present a higher noise margin than the conventional binary inverters. However, this costs four more transistors and spending significant power and area budgets.

B. PROPOSED AUTO-BACKUP AND AUTO-RESTORE TNVFF

Flip-flops (FFs) are among the most frequently used elements in integrated circuits, including registers, counters, data synchronizers, and frequency dividers. Unlike volatile circuits, nonvolatile circuits can retain the stored information during a scheduled power gating or even sudden power outage. Therefore, nonvolatile memory elements require extra backup and restore circuitries, operational phases, and control signals for data retention. Consequently, these additional circuits inevitably lead to higher power consumption, more design complexity, extra wirings, and occupying the chip area.

A conventional volatile ternary flip flop (FF) is shown in Fig. 6. In this structure, conventional 6T STI gates are utilized in both master and slave ternary latches. The conventional ternary FF suffers from two major issues: (1) unable to operate as a nonvolatile memory cell during a power outage,

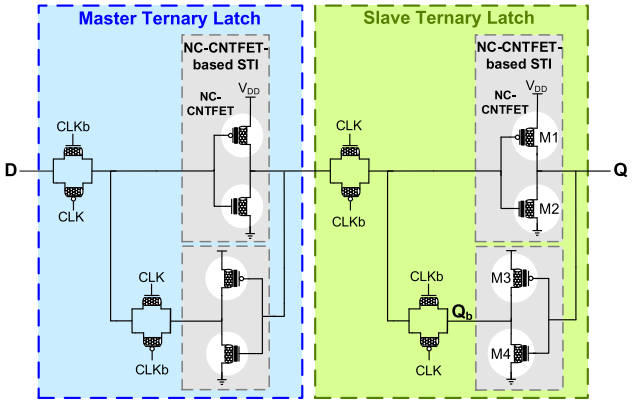

FIGURE 7. The proposed auto backup/auto restore NC-CNTFET-based TNVFF.

and (2) a high number of transistors and, thereby, energy dissipation [37].

The proposed auto-backup/auto-restore TNVFF utilizing the NC-CNTFET technology is illustrated in Fig. 7. The NC-CNTFET-based Schmitt trigger STI is the fundamental core to establish the master and slave ternary latches. Moreover, the transmission gates are implemented through the conventional n-type and p-type baseline CNTFETs. The transistor count and structure of the proposed TNVFF are similar to a conventional volatile binary data flip-flop (DFF). However, the proposed design can preserve the stored data in Q and Q_b nodes without any additional backup and restore circuitries and control signals.

When the input clock signal is low (high), the master and slave latches are in the transparent (hold) and hold (transparent) states, respectively. Consequently, a feedback loop, including two back-to-back ternary STIs in the ternary latches, is generated in the hold state. Accordingly, during the normal operation phase (when the power supply (V_{DD}) is activated), the back-to-back NC-CNTFET-based STIs holds the corresponding 0V, $V_{DD}/2$, or V_{DD} voltage levels. In this phase, the proposed FF sequences a ternary data on each positive clock edge like a conventional ternary FF.

To authenticate the auto-nonvolatility, the performance analysis of the proposed TNVFF during the backup and restore operation modes for ternary inputs is shown in Figs. 8-9.

1) BACKUP OPERATION

When the power supply intentionally (power gating) or suddenly (power outage) unplugged, for Q = "2", and Q_b = "0", the M1 and M4 NC-CNTFETs are positively polarized and present a low drain-to-source resistance (LRS). This condition will negatively polarize the M2 and M3 NC-CNTFETs and leads to a higher magnitude drain-to-source resistance (HRS) (see Fig. 8a). For Q = "0" and Q_b = "2" states (Fig. 8b), the M2 and M3 NC-CNTFETs are positively polarized and show LRS. Meanwhile, the M1 and M4 are negatively polarized and indicate HRS. When Q and Q_b are "1", both pullup and pulldown transistors in the back-to-back

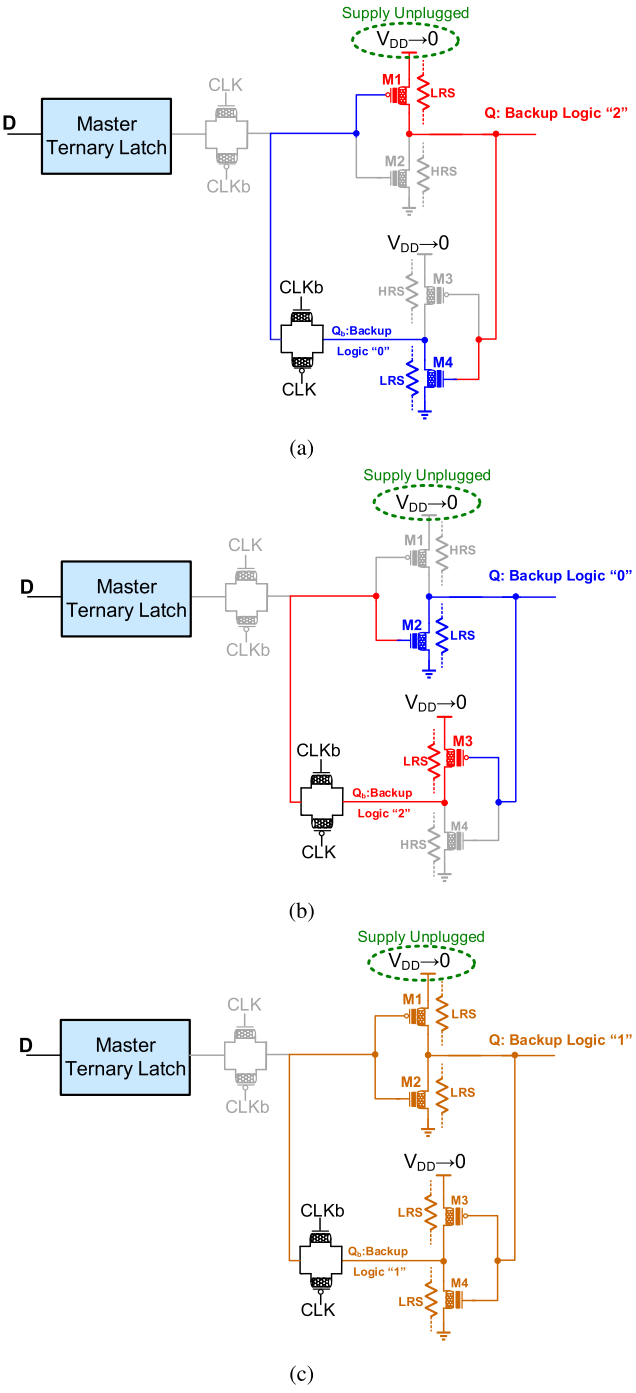

FIGURE 8. The operation of the proposed TNVFF for getting backup from (a) "2", (b) "0", and (c) "1" logic states.

STI latch are positively polarized and show equal LRS's (see Fig. 8c). After the polarization switching is fulfilled, eliminating power supply will not influence the stored polarization states.

2) RESTORE OPERATION

After the power supply is retrieved (Fig. 9), the difference between the drain-to-source resistance of the NC-CNTFETs

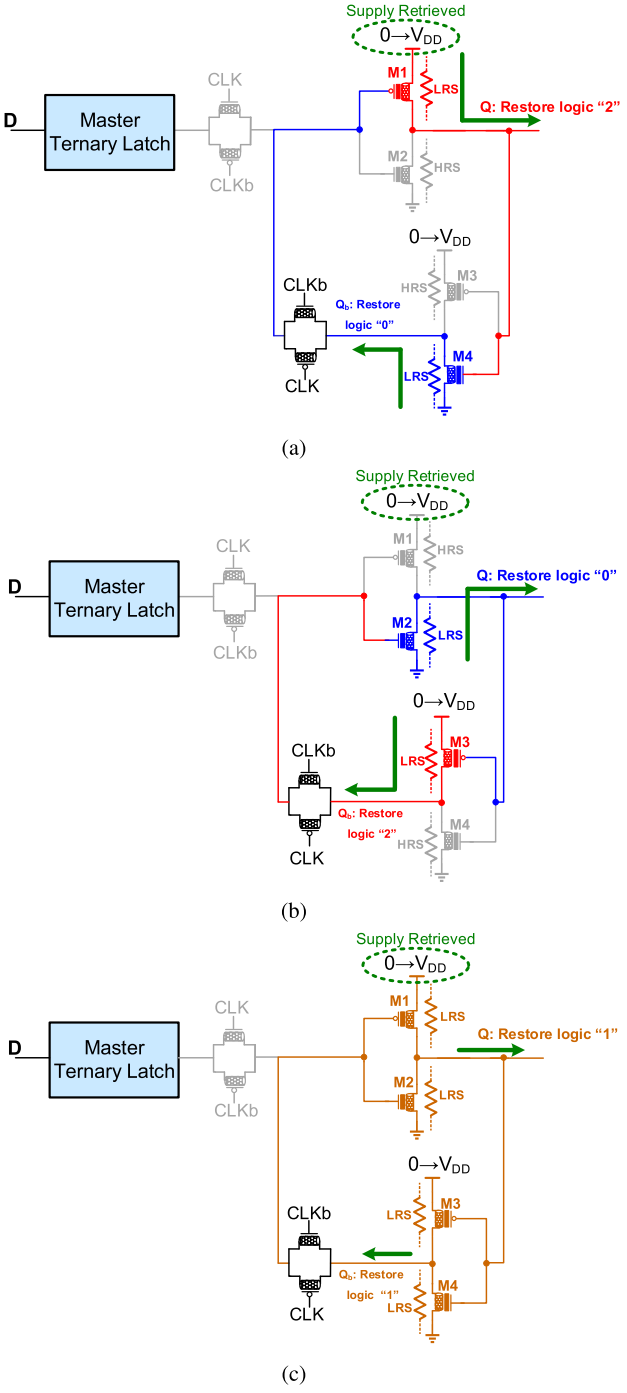

FIGURE 9. The restore phase of the proposed TNVFF to recover (a) "2", (b) "0", and (c) "1" logic states.

will recover the logic values stored in the nodes Q and Q_b. When M1 is in the LRS and M2 is in the HRS state, the difference between the pullup and pulldown resistances imposes the logic value "2" to the node Q. At the same time, the difference between the drain-to-source resistance of the M3 (HRS) and M4 (LRS) transistors will restore the logic value "0" at the Q_b node (see Fig. 9a). Thereupon, the back-to-back STI slave latch fully settles the voltages of the nodes Q and Q_b to V_{DD} and 0V, respectively. For recovering Q = "0" and

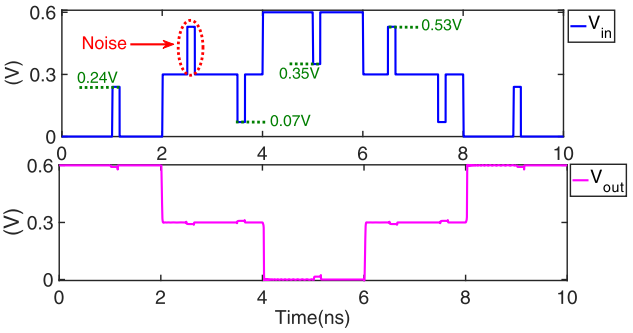

FIGURE 10. The transient response of the proposed NC-CNTFET-based TNVFF.

Q_b = "2" (Fig. 9b), the M1 and M4 are in the HRS, and M2 and M3 are in the LRS states. Accordingly, the back-to-back STIs in the slave latch completely recovers the logic states of the out nodes. When both pullup and pulldown transistors are equally in the LRS state (Fig. 9c), the logic "1" is delivered to the Q and Q_b nodes. Then, the feedback structure of the slave latch restores the voltages at these nodes to $V_{DD}/2$.

It is worth mentioning that the data is backed up automatically on each of the latches, which is in the hold state (master or slave) according to the discussed mechanism. Therefore, regardless of the clock level at which the power supply is disconnected, the data will be adequately restored as soon as the power supply is connected.

IV. PERFORMANCE EVALUATION

In this section, we examine the performance functionality of the proposed TNVFF through comprehensive simulations. The Synopsis HSPICE tool has been utilized for circuit simulation.

A. ANALYSIS OF THE FUNCTIONALITY OF THE PROPOSED DESIGN

Fig. 10 shows the transient response of the NC-CNTFET-based Schmitt trigger STI gate fed with a noisy input signal. It can be observed that if the input signal strongly affected by high-amplitude and durable noises, the proposed 2T STI performance would not be violated thanks to the superior noise margin characteristic. On the contrary, the conventional 6T STI malfunctions under this noisy input due to the limited noise margin. In this regard, the NC-CNTFET-based Schmitt trigger lay the foundations for designing low-voltage, high-performance, and ultra-compact ternary memory elements with a similar number of transistors to a conventional binary inverter.

The transient response of the proposed TNVFF is shown in Fig. 11. A 500MHz clock frequency is applied to the proposed TNVFF during the active mode. Moreover, the rise times and fall times for activating and deactivating the supply voltage (V_{DD}) are taken to be 30ps each. According to the polarization switching of the output nodes, it can be observed that the proposed design has successfully performed auto-backup and auto-restore operations during power active and sleep modes. Based on the analyses and the simulation results, it can be

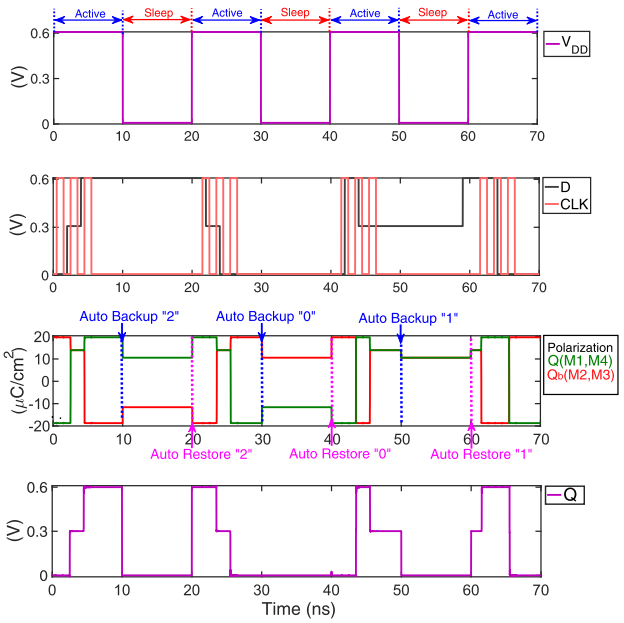

FIGURE 11. The transient response of the proposed TNVFF.

concluded that the proposed TNVFF can automatically perform backup and restore operations without any additional peripheral circuitries, control signals, and latency. Another advantage of the proposed design is to operate as a ternary nonvolatile FF with an identical transistor count and general structure with a conventional binary volatile FF.

In designing memory elements such as flip-flops, the static noise margin (SNM) is the most critical parameter that ensures data retention under experiencing extraneous signals. The latch SNM for each logic is defined as the length of the largest square side, which can be inscribed within its corresponding lobe in the butterfly curve of the back-to-back latch [22]. The minimum noise margin obtained for all logics is reported as the noise margin of the latch. To benchmark the data retention ability, we have performed a comparison between the SNMs of the proposed TNVFF (SNM=224mV) and the conventional ternary (SNM=112mV) and binary (SNM=208mV) DFFs. The Schmitt trigger behavior of the proposed TNVFF surpasses the fundamental noise margin limitation of the ternary DFF ($V_{DD}/4$=150mV). Moreover, the proposed ternary NVFF shows a higher SNM even compared to the conventional volatile binary DFF with a similar transistor count, which breaks the limits in ternary logic.

B. ASSESSING THE IMPACTS OF PROCESS AND SUPPLY VOLTAGE VARIATIONS

In advanced nanoscale technologies, physical parameters and supply voltage variations can critically influence the device and circuit performance characteristics. To capture the impact of physical parameters variations, 1000 runs of Monte Carlo simulations have been conducted considering Gaussian distribution and 10% variations for the baseline CNTFET physical parameters and 5% variations for the ferroelectric thickness at the $\pm 3\sigma$ level [38], [39].

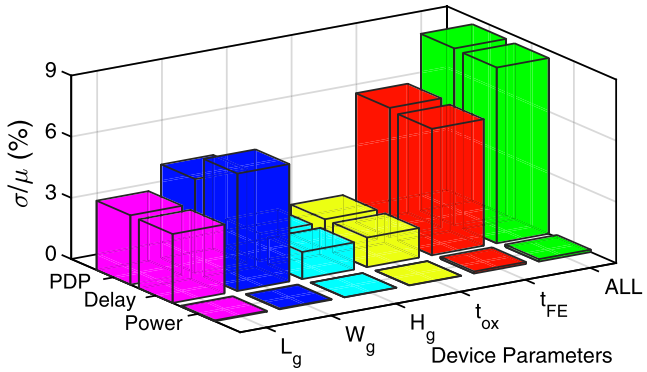

FIGURE 12. The impact of process variations on the clock-to-Q delay, power, and PDP of the proposed TNVFF.

TABLE 2. Performance comparison of the proposed TNVFF under different ferroelectric annealing temperatures (V_{DD}=0.6V).

Performance metrics	Annealing temperature 650 °C	800 °C
Clock-to-Q delay (t_{CQ})	34 ps	39 ps
Average power	3.67 μW	3.80 μW
PDP (Average power×t_{CQ})	125 aJ	148 aJ
Static noise margin	147 mV	224 mV

According to the Monte Carlo simulation results portrayed in Fig. 12, the coefficient of variation (σ/μ) of the power-delay product (PDP) of the proposed TNVFF is lower than 9%. Therefore, the proposed TNVFF is completely functional and operates robustly under major physical parameters fluctuations.

Annealing temperature can significantly affect the P-V hysteresis loop, which should be taken into consideration, especially in ferroelectric-based nonvolatile memory circuits. Table 2 illustrates a comparison between the performance metrics of the proposed TNVFF under 650 °C and 800 °C annealing temperatures. It is worth mentioning that the results have been obtained based on the 10nm Si-doped HfO_2 ferroelectric capacitors fabricated with 650 °C and 800 °C annealing temperatures [31]. Reducing the annealing temperature from 800 °C to 650 °C decreases the remnant polarization from 13μC/cm^2 to 8μC/cm^2. Although it leads to a relatively lower power-delay product (125aJ vs. 148aJ), it considerably reduces the SNM of the TNVFF (147mV vs. 224mV). However, it is worth mentioning that the SNM of the proposed TNVFF for the 650 °C annealing temperature is still higher than that of a conventional ternary DFF (147mV vs. 112mV) and is comparable to the ideal noise margin in ternary logic (150mV).

In digital integrated circuits, the supply voltage fluctuations may lead to performance degradation and functional failure. Accordingly, it is necessary to assess the impact of power supply variations on the overall performance of the designed circuits. A 10% supply voltage variation is usually expected in digital integrated circuits [40]. However, in a more conservative scenario, we have considered ±20% supply voltage variations in our design.

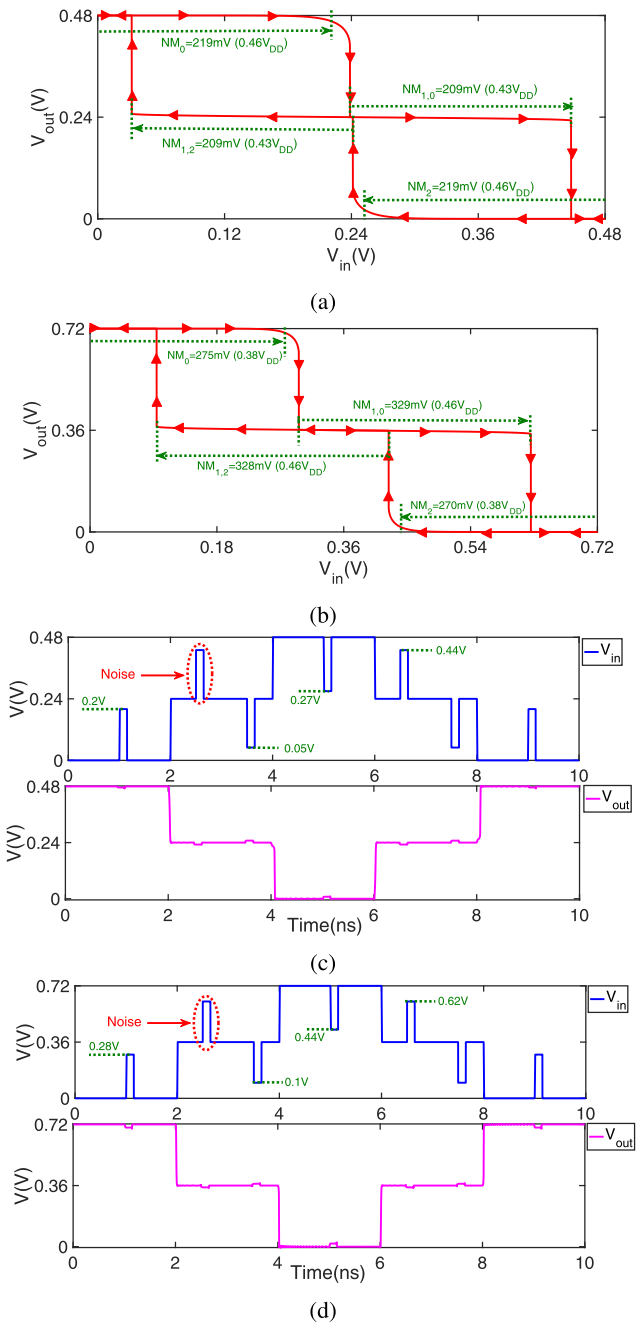

FIGURE 13. **The impact of power supply variations on the VTC of the NC-CNTFET-based hysteretic STI gate.**

Fig. 13 portrays the impact of the supply voltage fluctuations on the VTC and transient response of the NC-CNTFET-based hysteretic STI gate used in the proposed TNVFF. According to the results, ±20% variations in the supply voltage change the noise margin from 237 mV (see Fig. 5b) to 209 mV (Fig. 13a) and 275 mV (Fig. 13b). Moreover, as indicated in Figs. 13c and 13d, the NC-CNTFET-based hysteretic STI gate operates correctly with no functional failure under noisy conditions in the presence of major supply voltage fluctuations.

C. CIRCUIT-LEVEL PERFORMANCE COMPARISON

A comparative analysis between the proposed TNVFF and some state-of-art binary and ternary TNVFFs is depicted in Table 3. The proposed TNVFF demonstrate a reasonable clock-to-Q fan-out-of-four (FO4) delay (30ps) due to the small inherent capacitors and the high current delivery of NC-CNTFETs. However, it is higher than the delays of the TNVFFs presented in [37] and [45]. The restore time and energy dissipation of the proposed TNVFF are measured between the power supply's activation (when its amplitude reaches to $0.5V_{DD}$) and the moment that the voltage of the node Q reaches to $V_{DD}/4$ for logic "1" and $V_{DD}/2$ for logic "2" and "0", respectively. It is worth mentioning that there is no backup energy dissipation in the proposed design as the Schmitt trigger-based slave ternary latch automatically performs backup operation during the power gating or even sudden power outage.

The restore energy has been calculated as the multiplication of the power consumption during the restore period and the restore time. According to the results given in Table. 3, the proposed TNVFF presents a short restore time (7.5ps) and a significantly low restore energy (68.7aJ). The superior reductions in the restore time and restore energy are mainly due to the elimination of the peripheral restore circuit and its corresponding control signals and the small parasitic capacitors of the CNTFET device.

In addition to the low supply voltage (0.6V), elimination of the backup and restore peripheral circuits and their related control signals, and the low number of devices, which reduce the dynamic power dissipation, the proposed TNVFF has a reasonable average static power consumption. It is worth mentioning that when the power supply is gated, the proposed TNVFF dissipates no static power regardless of its last logic state. Moreover, the proposed TNVFF has a reasonable average static power consumption considering all of the existing operational and sleep cycles.

The main achievements of the proposed design can be summarized based on the results given in Table 3 as follows:

- In the ternary NVFFs, further reducing the supply voltage is not practical due to the limited noise margin [37], [45]. With the ability to reduce the supply voltage to less than 0.5V, the proposed TNVFF has overcome this limitation of the ternary logic.
- Considerably higher noise margin (SNM=224mV) than the other more complex ternary NVTFFs and even its binary volatile counterpart (SNM=208mV) with a similar number of transistors, a far-fetched goal for the other NVFFs.
- The well-designed structure of the proposed TNVFF provides 39% total average improvement in device count compared to the other counterparts.
- The proposed TNVFF does not need any peripheral circuitry and control signals (opposing extra control circuits and wirings to the system) to perform backup and restore operations.
- The proposed design presents zero device overhead.

TABLE 3. A performance comparison between the proposed TNVFF and some of the recent state-of-the-art works.

	[41]	[42]	[43]	[44]	[37]	[37]	[45]	This work
Power Supply (V_{DD})	0.5V	0.8V	0.8V	0.7V	0.9V	0.9V	0.8V	**0.6V**
Transistor count and NV elements	23T	20T	19T	19T	41T+2MTJ	41T+2MTJ	44T+2MTJ	**16T**
Need Peripheral backup/restore circuitry?	YES	YES	YES	YES	YES	YES	YES	**NO**
Clock-to-Q delay	>50ps	>40ps	>50ps	59.82ps	29ps	20ps	12ps	**39ps**
Power consumption	>50μW	>10μW	>100μW	39.45μW	12μW	4.4μW	4.9μW	**3.8μW**
Device overhead	7 extra FETs	4 extra FETs	3 extra FETs	3 extra FETs	25 extra FETs+2MTJ	25 extra FETs+2MTJ	28 extra FETs+2MTJ	**NO**
Backup delay	1.4ns	1ns	-	N/A	3ns	2.8ns	1.49ns	**-**
Backup energy	7fJ	1.3fJ	-	N/A	95.1fJ	33.7fJ	11.5fJ	**-**
Restore delay	75ps	56ps	~10ps	28ps	13.2ps	12.4ps	51ps	**7.5ps**
Restore energy	9fJ	1.1fJ	~fJ	1.90fJ	14.1fJ	4.3fJ	365aJ	**68.7aJ**
Supporting sudden power outage	NO	YES	YES	YES	NO	NO	YES	**YES**
Output logic level	Binary	Binary	Binary	Binary	Ternary	Ternary	Ternary	**Ternary**
NV element	FeFET	FeFET	FeFET	FeFET	MTJ	MTJ	MTJ	**FeFET**
Technology	10nm FinFET	10nm FinFET	10nm FinFET	10nm FinFET	7nm FinFET	10nm CNTFET	10nm CNTFET	**10nm CNTFET**

- The proposed TNVFF shows significant power-saving (64% average improvement).
- Zero backup energy dissipation because of eliminating additional transistors and control signals for the backup process.
- The proposed design's automatic restore capability ensures extraordinary restore energy saving (higher than 98% on average improvement) than the previous state-of-the-art NVFFs.
- Support the sudden power supply outage, which is not considered in the designs presented in [37], [41].

The comparison results envision that the proposed NC-CNTFET-based TNVFF opens up a new era in designing ultra-compact and high-performance nonvolatile neuromorphic circuits and systems.

V. CONCLUSION

By employing the NDR effect and hysteretic behavior of the NC-CNTFETs, this work proposed a novel design strategy for demonstrating an ultra-efficient high noise margin TNVFF. The structure of the proposed ternary nonvolatile design is similar to a conventional volatile binary FF. The primary advantage of the proposed TNVFF is the auto-backup and auto-restore capability during power gating or power outage without imposing any extra transistors, memory devices, and control signals. On the other hand, the Schmitt trigger nature of the ternary latches provides an excellently high noise margin, surpassing conventional binary and ternary FFs. After performing comprehensive simulations and analysis, we have indicated that the proposed design can tolerate high-amplitude and durable noises due to the breathtaking noise margin characteristic. The proposed TNVFF operates robustly under experiencing significant process variations and presents outstanding improvements in terms of transistor count (39%), power (64%), and energy dissipation (98%) thanks to the eliminating peripheral backup and restore circuitries, additional wiring, and control signals. Our investigations establish a new paradigm for designing ultra-efficient MVL nonvolatile memory circuits beyond conventional binary counterparts for neuromorphic applications.

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